MP8128

1A, LNB Voltage Regulator with I²C Interface and DiSEqC 2.x Function

DESCRIPTION

The MP8128 is a highly integrated voltage regulator designed to provide efficient, low-noise power and interface signals to a satellite receiver's low noise block downconverter (LNB) at the antenna port. The device provides a 22kHz tone signal and a standard I²C interface for satellite receivers. It is compatible with both DiSEqC 1.x and DiSEqC 2.x.

The MP8128 integrates a boost regulator followed by a tracking linear regulator. The boost regulator provides a power source that exceeds the final output voltage by 1.1V, while the tracking linear regulator provides low noise power and protects the output against overloads or shorts.

The device provides a number of features including voltage selection, over-current protection (OCP), and 22kHz tone signal control. The MP8128 offers a simple solution with a low component count and high efficiency.

The MP8128 is available in QFN-20 (3mmx3mm) package.

FEATURES

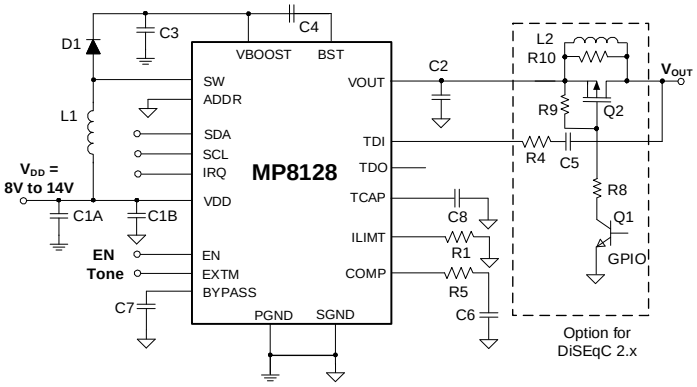
- DiSEqC 1.x and DiSEqC 2.x Compatible
- Integrated I²C Interface
- 8V to 14V Input Voltage
- 40V V_{OUT} Rating
- Up to 1A Configurable Current Limit
- Low-Noise LDO Output
- 440kHz Switching Frequency
- Selectable Internal or External 22kHz Signal Source
- Selectable Output Voltage
- OCP, SCP, and OVP
- Over-Temperature Protection (OTP)
- Available in QFN-20 (3mmx3mm) Package

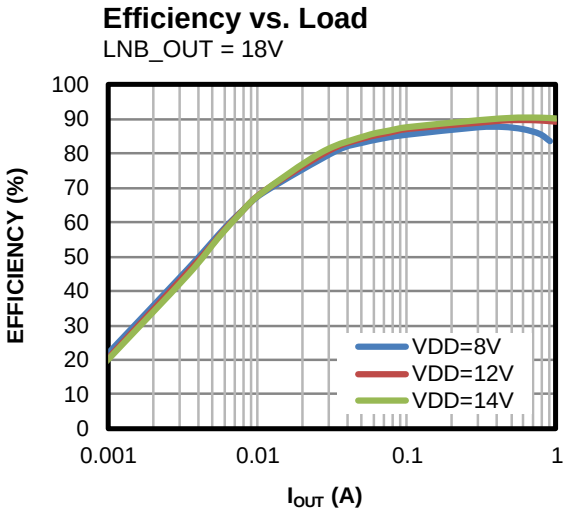
MPL Optimized Performance with MPS Inductor MPL-AL6060 Series

APPLICATIONS

- LNB Power Supplies and Control for Satellite Set Top Boxes
- TV Satellite Receivers
- PC Card Satellite Receivers

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8128GQ	QFN-20 (3mmx3mm)	*See Below*	1
EVKT-MP8128	Evaluation kit		

* For Tape & Reel, add suffix –Z (e.g. MP8128GQ–Z).

TOP MARKING

AXBY

LLL

AXB: Product code of MP8128GQ
Y: Year code
LLL: Lot number

EVALUATION KIT EVKT-MP8128

EVKT-MP8128 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV8128-Q-00A	MP8128 evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I²C communication interface, one USB cable, and one ribbon cable	1

Order directly from MonolithicPower.com or our distributors.

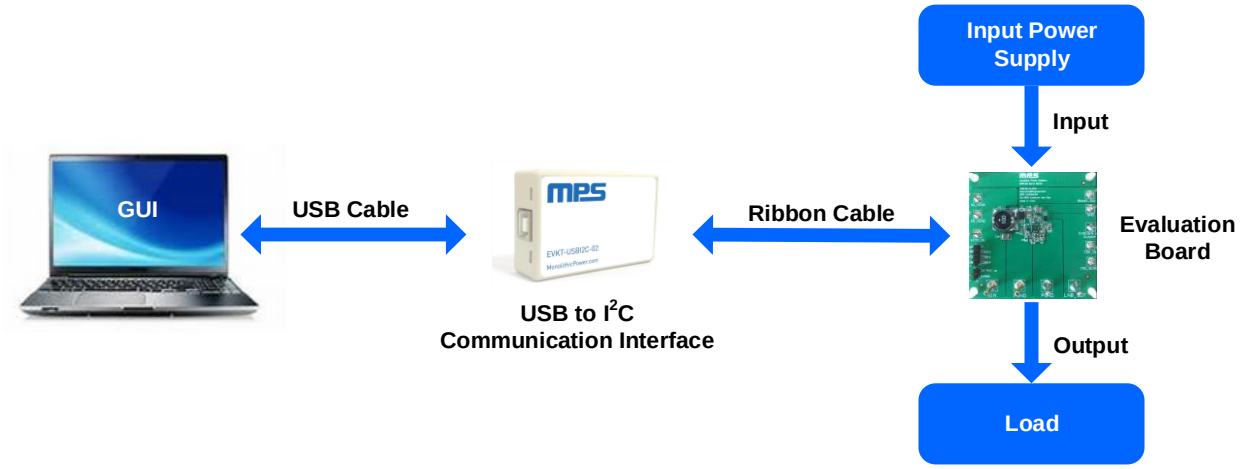
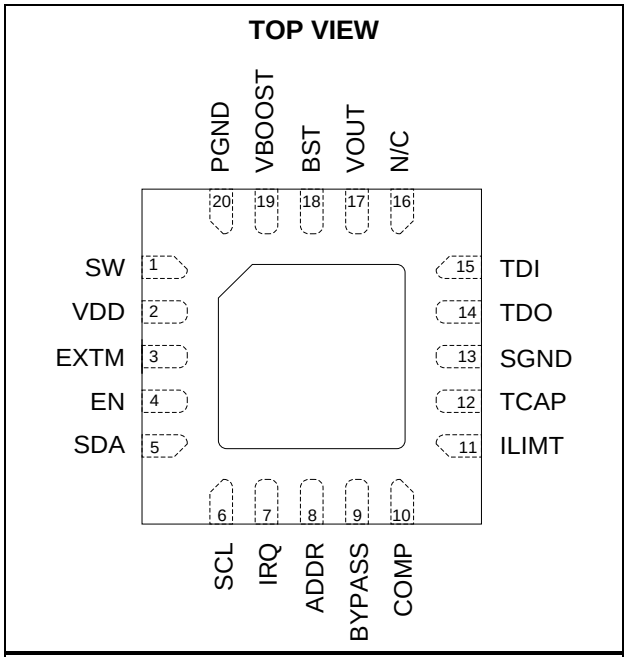


Figure 1: EVKT-MP8128 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-20 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	SW	**Power switch output.** SW is the drain of the internal MOSFET switch for the boost stage. Connect the power inductor and output rectifier to SW.
2	VDD	**Input power supply.**
3	EXTM	**External modulation input for 22kHz tone signal.** There are two functions for the EXTM pin, described in greater detail below: • If the TEN bit = 1 and the TCTRL bit = 0: A high voltage on the EXTM pin can enable the internal 22kHz tone signal generator. A low voltage on the EXTM pin disables the internal 22kHz tone generator. • If the TEN bit = 1 and TCTRL bit = 1: 22kHz signals is introduced from EXTM pin externally.
4	EN	**Regulator on/off control input.** Apply a high voltage on EN to turn the regulator on; apply a low voltage on EN to turn the regulator off. For automatic start-up, connect EN to the input source using a resistor divider. Do not float EN.
5	SDA	**I²C-compatible data input/output.**
6	SCL	**I²C-compatible clock input.**
7	IRQ	**Interrupt request pin.** If an over-current (OC) or over-voltage (OV) fault occurs, the IRQ pin pulls low. IRQ is an open-drain output.
8	ADDR	**I²C addresses setting pin.** Connect a resistor to the ADDR pin to select different I²C addresses. For more details, see the I²C Interface section on page 24.
9	BYPASS	**Power bias for the internal circuit.** Connect a 0.22μF bypass capacitor to the BYPASS pin.
10	COMP	**Compensation pin for the boost regulator.**
11	ILIMT	**LNB output current limit setting pin.** Connect a resistor from ILIMT to GND to configure the current limit. Do not float the ILIMT pin
12	TCAP	**Soft start pin.** Connect a capacitor from TCAP to ground to set a rising time for the output voltage. The TCAP voltage is the feedback reference voltage, and the capacitor should be placed far away from the noise source.
13	SGND	**Signal ground.**
14	TDO	**Tone detection output.** TDO pulls low when a tone signal is detected on TDI. Open-drain output.
15	TDI	**Tone decoder input.** Connect TDI to the LNB_OUT for the 22kHz tone detection function. TDI must be AC coupled to the DiSEqC 2.x bus line of VOUT. It is recommended to connect a 10nF capacitor and a 100Ω resistor between the output and the TDI pin.
16	N/C	**No connection.**
17	VOUT	**LDO output voltage.**
18	BST	**Internal LDO driver supply.**
19	VBOOST	**Internal LDO power input.**
20	PGND	**Power ground for boost converter.**
	Exposed Pad	Connect the exposed pad to PGND to improve thermal performance. Place thermal vias on the PCB to enhance power dissipation.

ABSOLUTE MAXIMUM RATINGS (1)

VDD .....-0.3V to +20V
VOUT, SW, VBOOST .....-0.3V to +40V
BST .....V_{BOOST} + 6.5V
TDI .....-0.6V to +6.5V (2)
EN..... -0.3V to +6.5V (3)
EN pin clamps current..... 0.1mA (3)
All other pins .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (4) (6)
.....3.57W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (5)

Supply voltage (V_{DD}) .....8V to 14V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-20 (3mmx3mm)			
EV8128-Q-00A (6)	35	4	°C/W
JESD51-7 (7)	60	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The TDI voltage rating is 6.5V, but there is one internal clamp circuit clamping the input voltage when V_{OUT} ramps up quickly. It is recommended to connect a 10nF capacitor and a 100Ω resistor between VOUT and the TDI pin.
3) The EN voltage rating is 6.5V, but there is one internal clamp circuit. To clamp the pull-up current, ensure that the input current to EN pin is below 0.1mA.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on EV8218-Q-00A, 2-layer 63mmx63mm PCB.
7) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12V, V_{EN} = 3.3V, T_J = -40°C to +125°C [8], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
General Parameter						
Input voltage range	V_{DD}		8	12	14	V
Shutdown current	I_{SD1}	EN pin = 0V			10	μA
	I_{SD2}	V_{LINE} = 111		0.25	0.65	mA
Input supply current [9]	I_{DD}	V_{SEL} = 11, V_{LINE} = 010, Load = 0A, TEN = 0, V_{OUT}= 18.6V, no tone		5.5		mA
		V_{SEL} = 11, V_{LINE} = 010, Load = 0A, TEN = 1, TCTRL = 0, EXTM = high, V_{OUT} = 18.6V, tone from inner		14.5		mA
I²C under-voltage lockout threshold	V_{I2C_UVLO}	V_{BYPASS} rising		4.3		V
I²C under-voltage lockout hysteresis				0.48		V
Power stage under-voltage lockout threshold	V_{DD_UVLO}	V_{DD} rising	6.8	7.15	7.6	V
Power stage under-voltage lockout hysteresis				380		mV
Voltage on the BYPASS pin	V_{BYP}	I_{BYP} = 0mA to 10mA	4.5	5	5.5	V
Over-temperature shutdown threshold [9]	T_{SD}			150		°C
Over-temperature shutdown hysteresis [9]	T_{SDHYS}			20		°C
Boost Regulator						
Boost switch on resistance	$R_{DS(ON)}$	I_{SW} = 500mA		200		mΩ
Boost MOSFET current limit		V_{OUT} = 18V, ISEL bit = 0	4	6	7.5	A
		V_{OUT} = 18V, ISEL bit = 1	2	2.8	3.6	A
Boost frequency	f_{SW}		390	440	480	kHz
Linear Regulator						
Dropout voltage	V_{DROP}	V_{BOOST} - V_{OUT}, LDM bit = 0, no tone, I_{OUT} = 50mA		1.1		V
Output voltage accuracy	V_{OUT}	V_{OUT} = 18V, load = 0mA to 100mA	-2		+2	%
Output line regulation		8V ≤ V_{DD} ≤ 14V, V_{OUT} = 18V, I_{OUT} = 500mA		7		mV
Output load regulation [9]		0mA ≤ I_{OUT} ≤ 1A, V_{OUT} = 13V		8		mV
		0mA ≤ I_{OUT} ≤ 1A, V_{OUT} = 18V		14		mV
Output current limit	I_{LIMIT}	R_{LIMIT} = 6.98kΩ	1.17	1.3	1.43	A
		R_{LIMIT} = 14kΩ		650		mA
		R_{LIMIT} = 19.1kΩ		475		mA
Dynamic overload protection off time [9]	t_{OFF}	Time for an attempted restart		1.8		s

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD} = 12V, V_{EN} = 3.3V, T_J = -40°C to +125°C [8], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Dynamic overload protection on time [9]	t_{ON}	Time to onset of shutdown		50		ms
TCAP pin current	I_{CAP}		4.2	6.2	8.2	µA
LDO output sink current	I_{SINK}	VSEL bits = 01, VLINE bits = 000, TCTRL bit =0, EXTM pin = high, clamp V_{OUT} to 14V		54		mA
		VSEL bits = 01, VLINE bits = 000, TCTRL bit = 0, EXTM pin = low, clamp V_{OUT} to 14V		14		mA
LDO output sink current time-out	$I_{SINK-TIMER}$	VSEL bits = 01, VLINE bits = 000, TCTRL bit = 0, clamp V_{OUT} to 14V, EXTM pin = high/low		10		ms
LDO output sink current after time-out	$I_{SINK-TO}$	VSEL bits = 01, VLINE bits = 000, clamp V_{OUT} to 14V, after the STO bit is set to 1		2		mA
Output backward leakage current [10]	I_{BKLK}	VLINE bits = 111, V_{OUT} is clamped to 21V		0.7	1.3	mA
Power Good						
Power not good upper trip threshold		With respect to V_{OUT} setting, PNG set to 1,V_{OUT} = 18V	105	115	125	%
		With respect to V_{OUT} setting, PNG reset to 0, V_{OUT} = 18V	102	110	118	%
Power not good upper hysteresis				5		%
Power not good lower trip threshold		With respect to V_{OUT} setting, PNG set to 1, V_{OUT} = 18V	78	85	92	%
		With respect to V_{OUT} setting, PNG reset to 0, V_{OUT} = 18V	83	90	97	%
Power not good lower hysteresis		With respect to V_{OUT} setting		5		%
Tone Signal						
Internal tone frequency	f_{TONE}	TEN bit = 1, TCTRL bit = 0, EXTM pin = high	20	22	24	kHz
External tone source frequency range [11]	f_{EXTM}	TEN bit = TCTRL bit = 1	20	22	24	kHz
Peak-to-peak amplitude	V_{PP}	I_{OUT} = 0A, C_{OUT} = 0.1µF	0.5	0.66	0.85	V
		I_{OUT} = 0A to 1A, C_{OUT} = 0.1µF [9]		0.66		
Duty cycle	D_{TONE}	R_{LOAD} = 1kΩ, C_{OUT} = 0.1µF	40	50	60	%
Rising and falling time		R_{LOAD} = 1kΩ, C_{OUT} = 0.1µF	5	10	15	µs
TONE Detector						
Detect frequency range	f_{DETIN}	0.4Vpp sine wave	17	22	27	kHz
Detector input tone amplitude	V_{DETIN}	22kHz sine wave	0.2		1.0	V
TDI input impedance	Z_{DETIN}			50		kΩ

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD} = 12V, V_{EN} = 3.3V, T_J = -40°C to +125°C [8], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Logic Signal						
Input logic low voltage	V_{LI}	EN, EXTM			0.8	V
Input logic high voltage	V_{HI}	EN, EXTM	2			V
Logic input pin current		EN, EXTM connect to 5V or 0V	-10		+10	μA
Output logic low voltage	V_{LO}	TDO, sink current = 3mA			0.4	V
Output logic high leakage		TDO output high, connect to 5V			1	μA
I²C Interface						
SDA, SCL input logic low voltage	V_{IL}				0.4	V
SDA, SCL input logic high voltage	V_{IH}		1.2			V
SDA, SCL input current		Connect to 5V or 0V	-1		+1	μA
SDA, IRQ output logic low voltage		Sink current = 2mA			0.4	V
SDA, IRQ output logic high leakage		SDA, IRQ output high, connect to 5V			1	μA
SCL maximum clock frequency	$f_{MAX-CLK}$			400		kHz
I²C Address Setting						
ADDR pin detection current			45	50	55	μA
ADDR voltage for address 0001000		It is recommend to connect ADDR to GND	0		0.6	V
ADDR voltage for address 0001001		It is recommend to connect ADDR to GND through a 27kΩ resistor	1		1.6	V
ADDR voltage for address 0001010		It is recommend to connect ADDR to GND through a 47kΩ resistor	2		2.6	V
ADDR voltage for address 0001011		It is recommended to float the ADDR pin	3.05		5	V

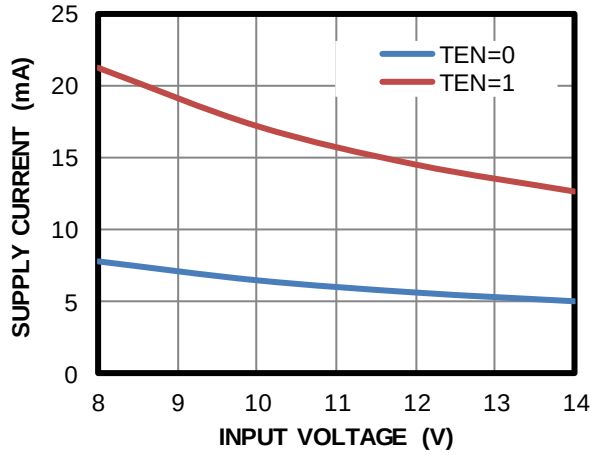
Notes:

8) Not tested in production. Guaranteed by over-temperature correlation.
9) Guaranteed by characterization. Not tested in production.
10) Can withstand the back voltage for an indefinite period of time. When the fault condition is removed, the device returns to normal operation.
11) This range guarantees the EXTM function.

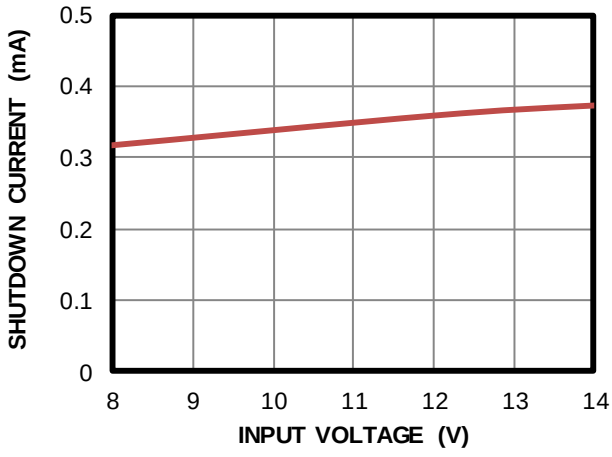
TYPICAL CHARACTERISTICS

V_{DD} = 12V, LNB_OUT = 18V, L = 10µH, T_A = 25°C, unless otherwise noted.

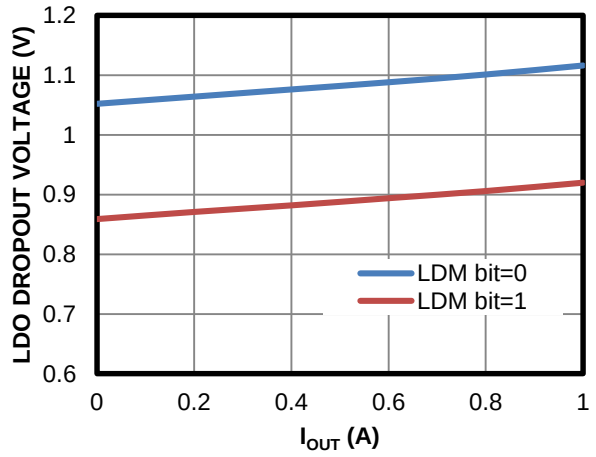
Supply Current vs. Input Voltage



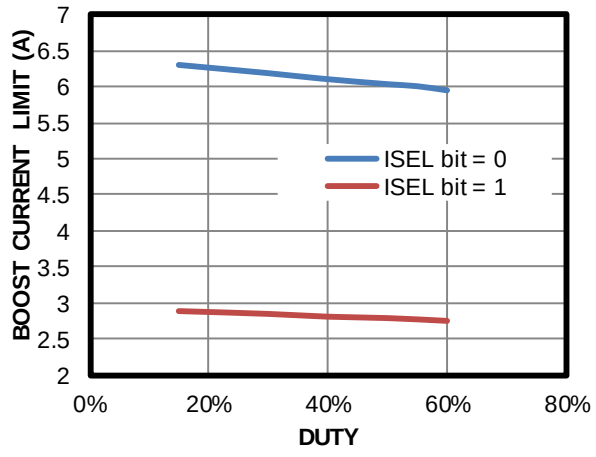
I²C Shutdown Current vs. Input Voltage



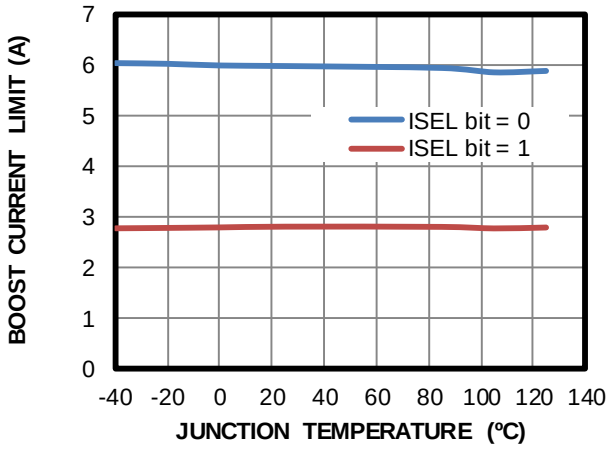
LDO Dropout Voltage vs. I_{OUT}



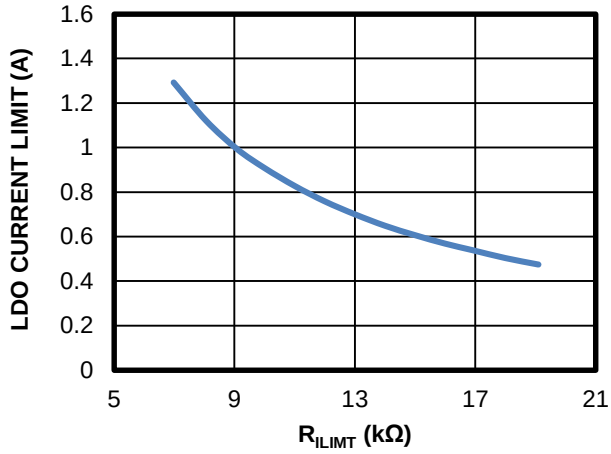
Boost Current Limit vs. Duty



Boost Current Limit vs. Temperature



LDO Current Limit vs. R_{ILIMT}

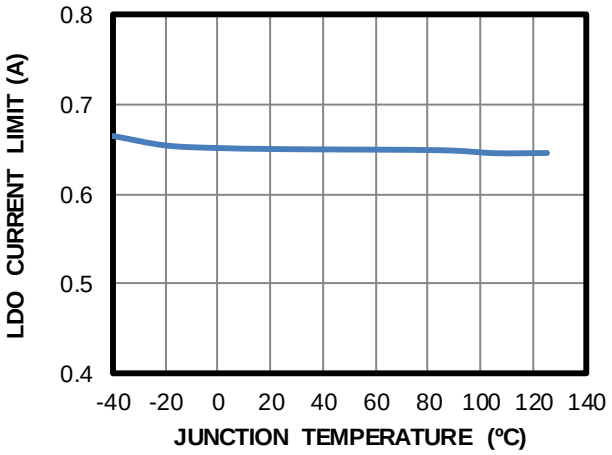


TYPICAL CHARACTERISTICS *(continued)*

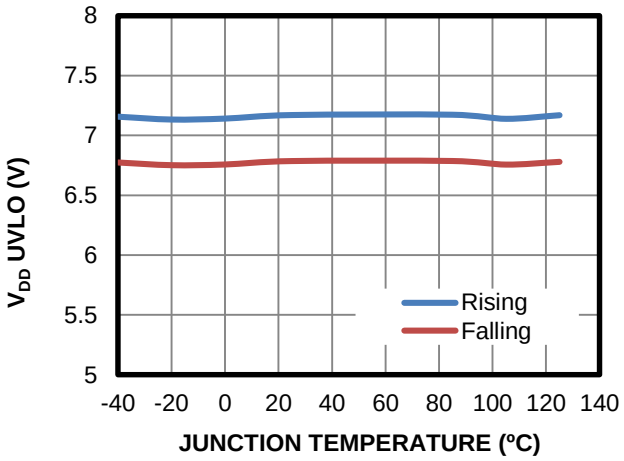
V_{DD} = 12V, LNB_OUT = 18V, L=10µH, T_A = 25°C, unless otherwise noted.

LDO Current Limit vs. Temperature

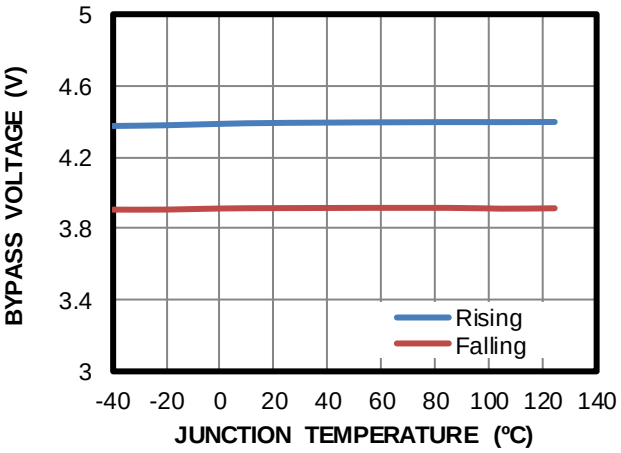
R_{ILIMT} = 14kΩ



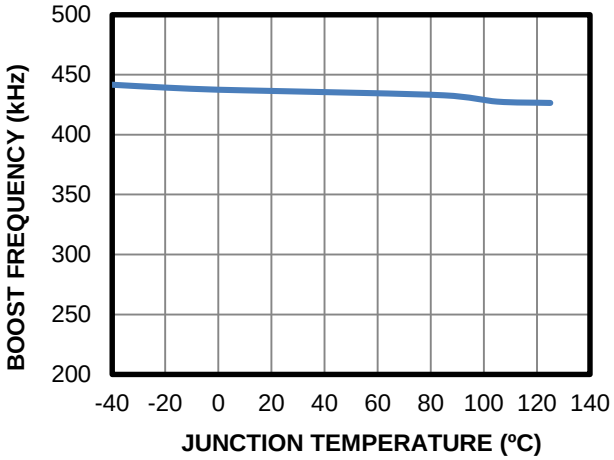
VDD UVLO vs. Junction Temperature



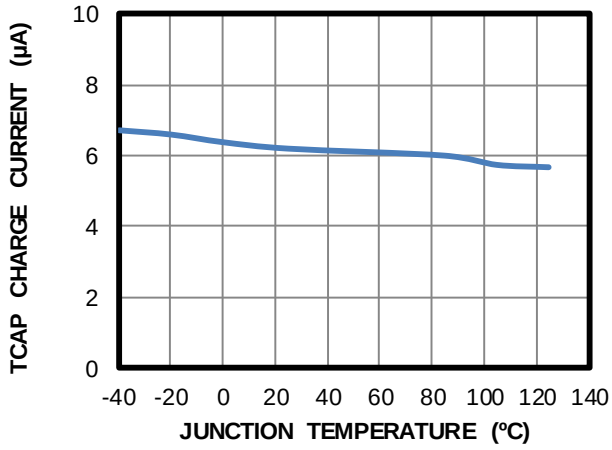
I²C UVLO vs. Junction Temperature



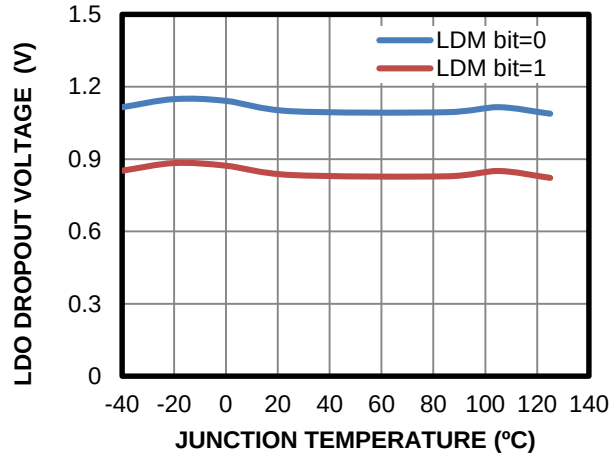
Boost Frequency vs. Temperature



TCAP Charge Current vs. Temperature



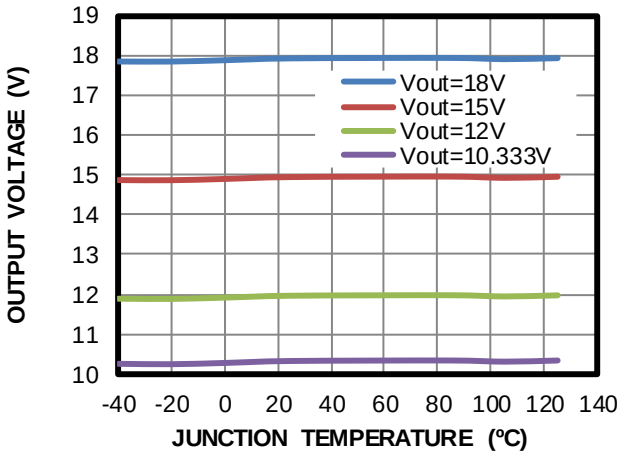
LDO Dropout Voltage vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

V_{DD} = 12V, LNB_OUT = 18V, L = 10µH, T_A = 25°C, unless otherwise noted.

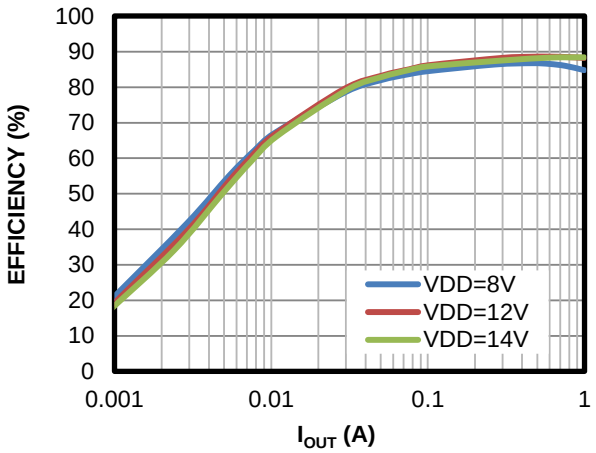
Output Voltage vs. Temperature



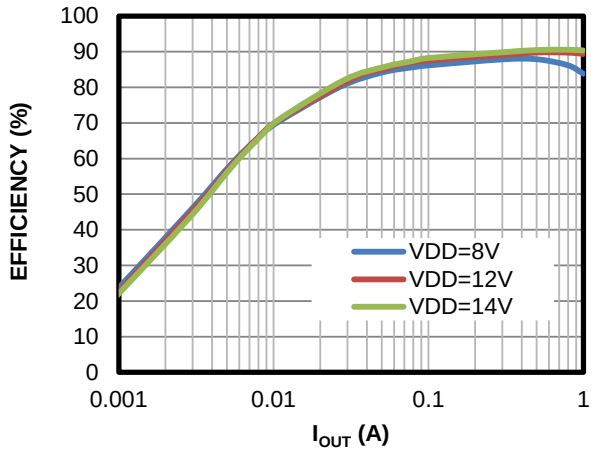
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section on page 29. V_{DD} = 12V, LNB_OUT = 18V, L = 10µH, T_A = 25°C, unless otherwise noted.

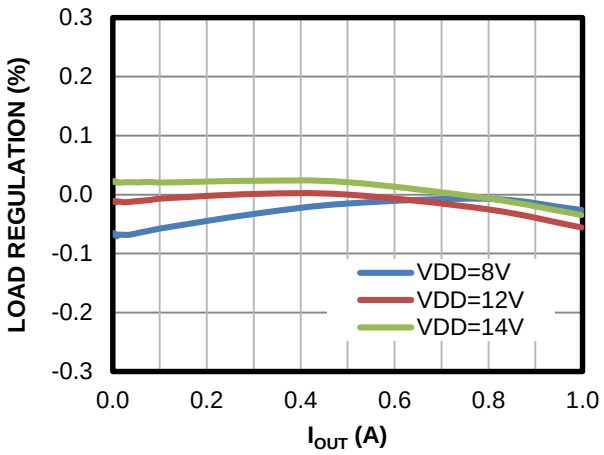
Efficiency
LNB_OUT = 13V



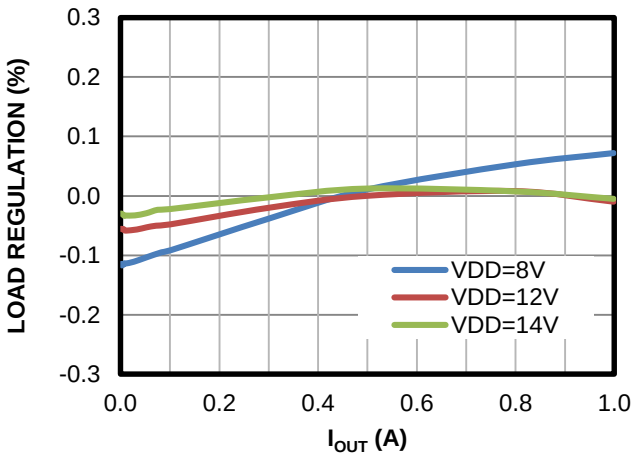
Efficiency
LNB_OUT = 18V



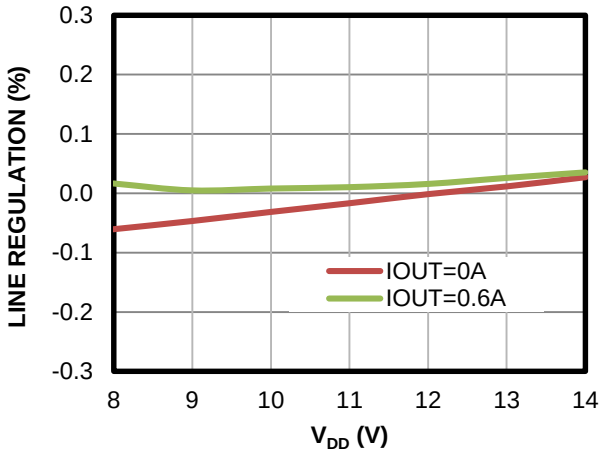
Load Regulation
LNB_OUT = 13V



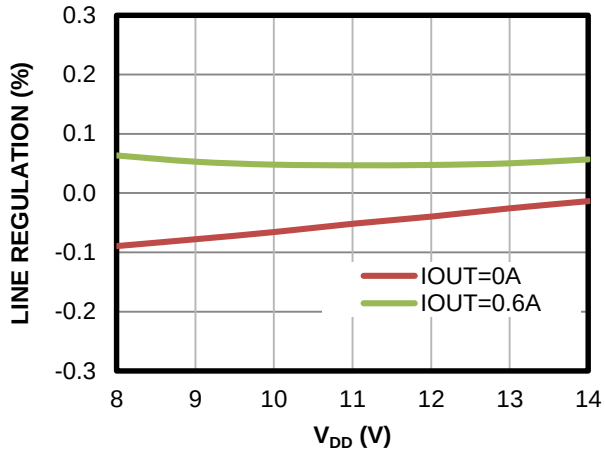
Load Regulation
LNB_OUT = 18V



Line Regulation
LNB_OUT = 13V



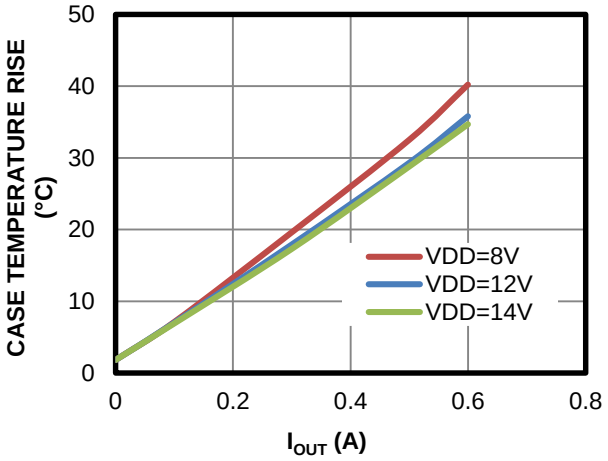
Line Regulation
LNB_OUT = 18V



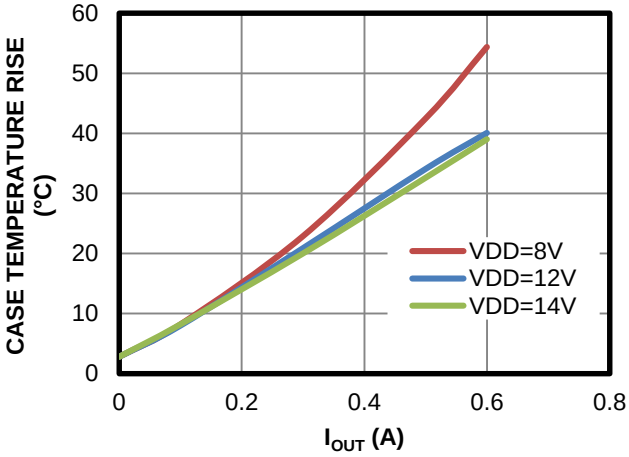
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 29. V_{DD} = 12V, LNB_OUT = 18V, L = 10µH, T_A = 25°C, unless otherwise noted.

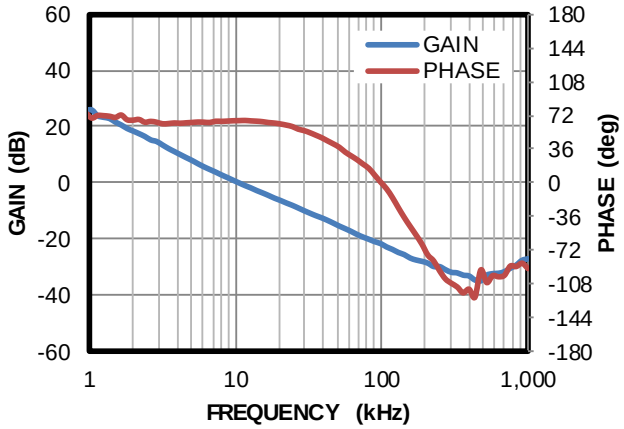
Case Temperature Rise
LNB_OUT = 13V



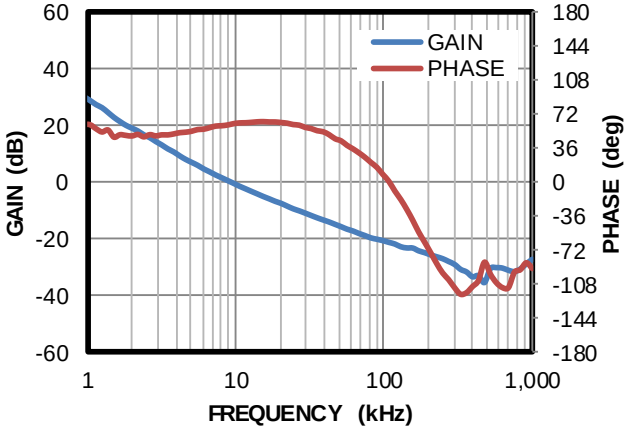
Case Temperature Rise
LNB_OUT = 18V



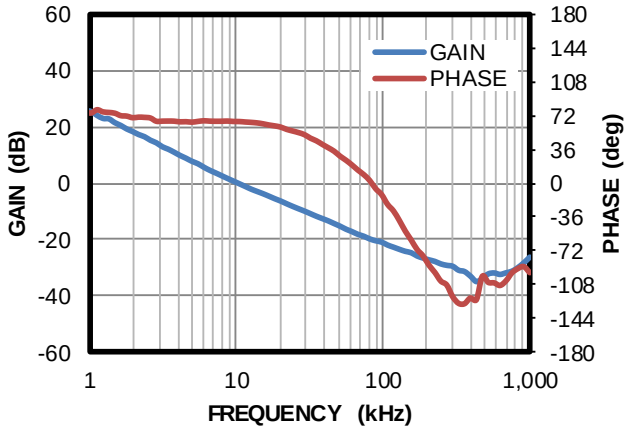
Boost Bode Plot
LNB_OUT = 13V, boost load = 0.6A



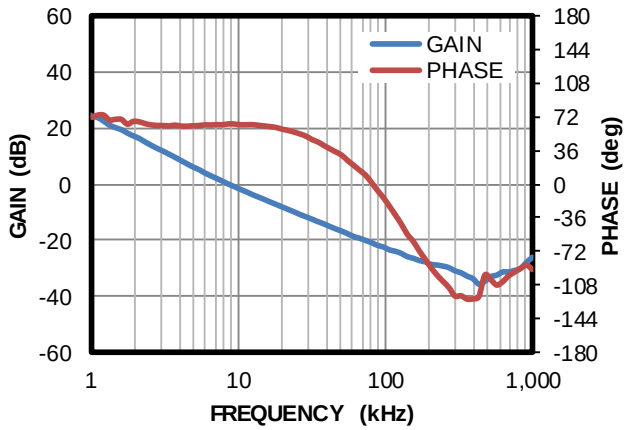
Boost Bode Plot
LNB_OUT = 18V, boost load = 0.6A



Boost Bode Plot
LNB_OUT = 13V, boost load = 1A



Boost Bode Plot
LNB_OUT = 18V, boost load = 1A

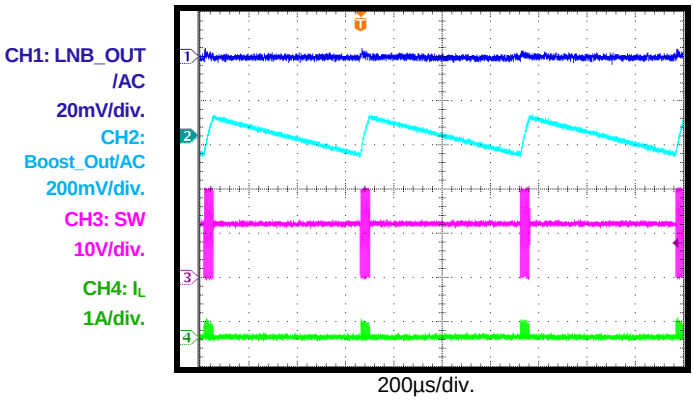


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 29. V_{DD} = 12V, LNB_OUT = 18V, L = 10µH, T_A = 25°C, unless otherwise noted.

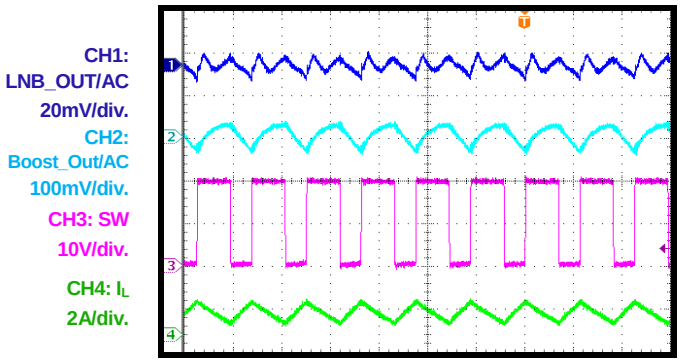
Steady State

I_{OUT} = 0A



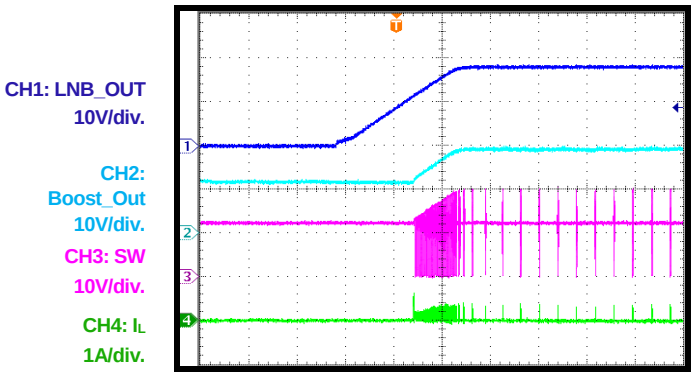
Steady State

I_{OUT} = 0.6A



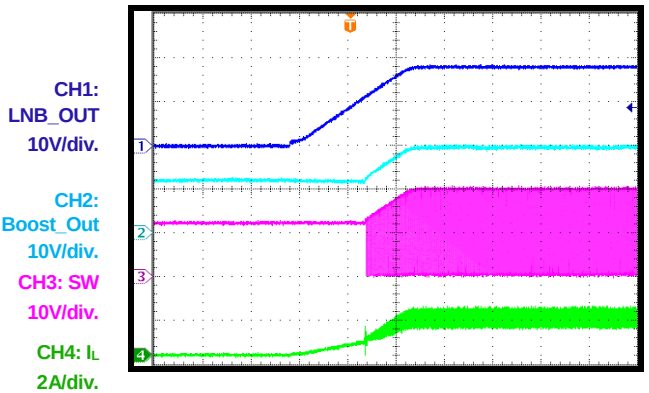
Start-Up via the I²C

I_{OUT} = 0A, set the VLINE bit to 000



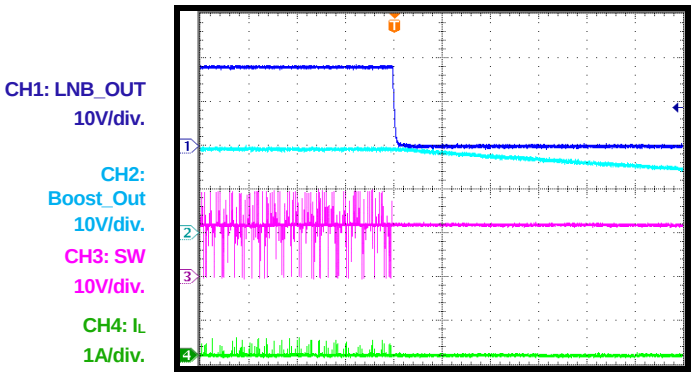
Start-Up via the I²C

I_{OUT} = 1A, set the VLINE bit to 000



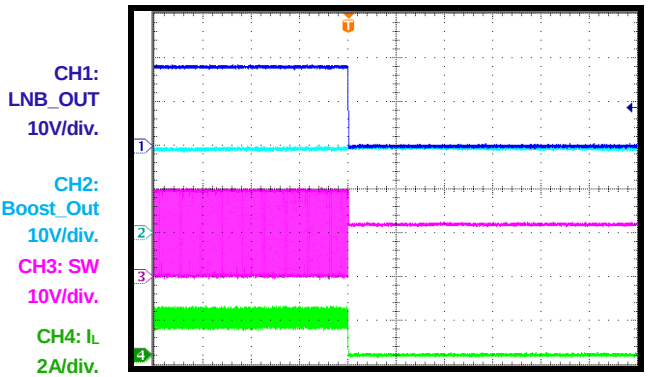
Shutdown via the I²C

I_{OUT} = 0A, set the VLINE bit to 111



Shutdown via the I²C

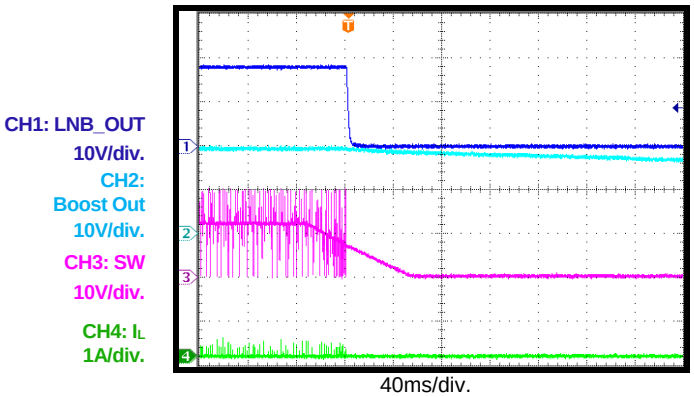
I_{OUT} = 1A, set the VLINE bit to 111



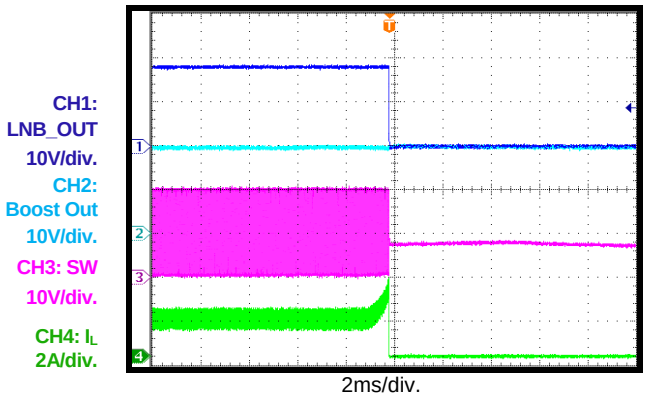
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 29. V_{DD} = 12V, LNB_OUT = 18V, L = 10µH, T_A = 25°C, unless otherwise noted.

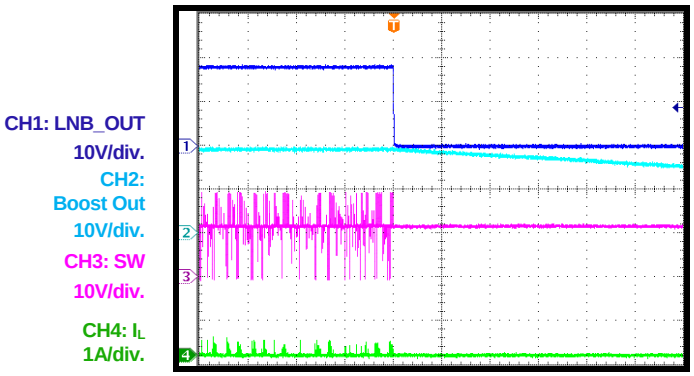
VDD Off
I_{OUT} = 0A



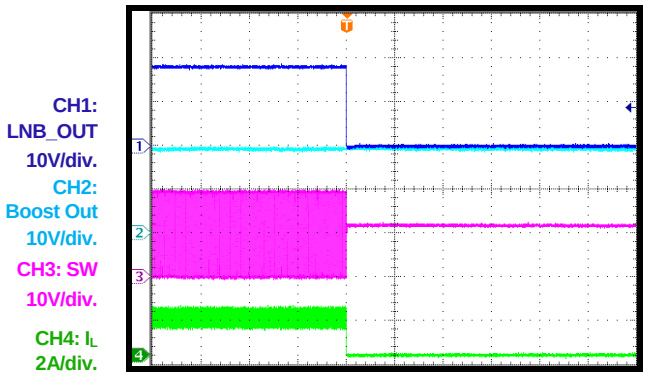
VDD Off
I_{OUT} = 1A



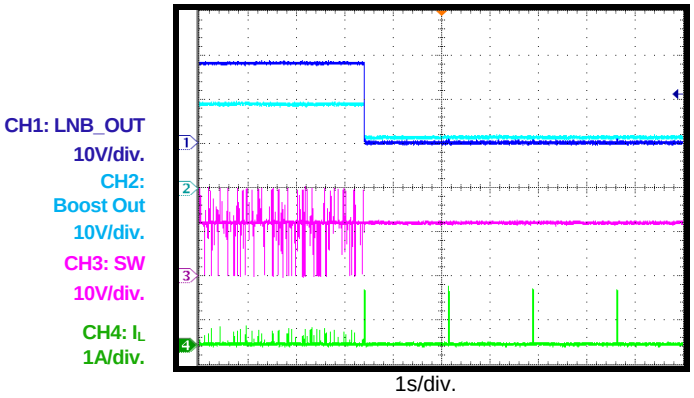
EN Off
I_{OUT} = 0A



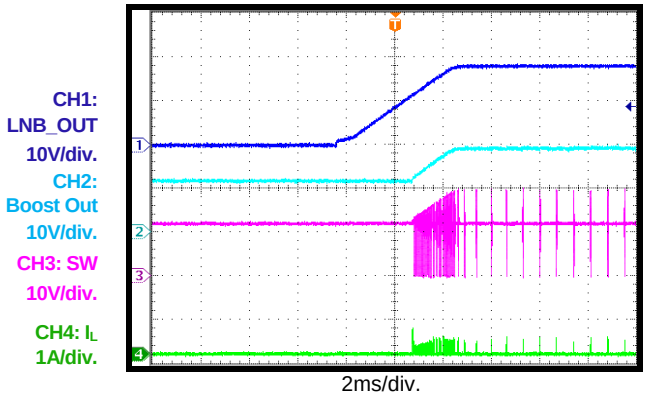
EN Off
I_{OUT} = 1A



SCP Entry
OCR bit = 0, DCL bit = 1, I_{OUT} = 0A



SCP Recovery
OCR bit = 0, DCL bit = 1, I_{OUT} = 0A

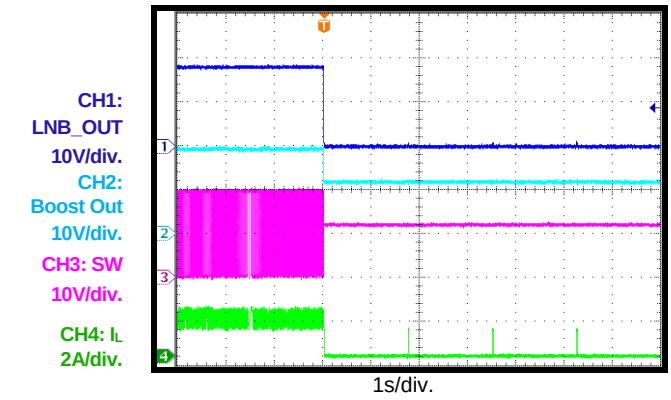


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 29. V_{DD} = 12V, LNB_OUT = 18V, L = 10µH, T_A = 25°C, unless otherwise noted.

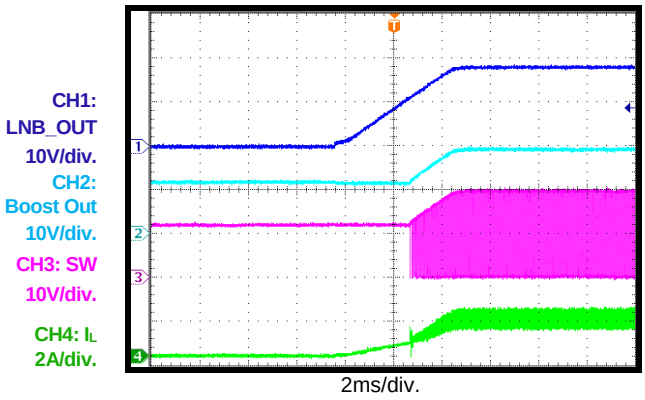
SCP Entry

OCR bit = 0, DCL bit = 1, I_{OUT} = 1A



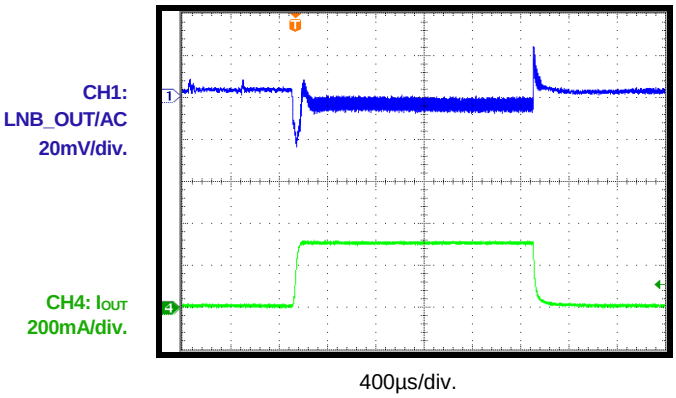
SCP Recover

OCR bit = 0, DCL bit = 1, I_{OUT} = 1A



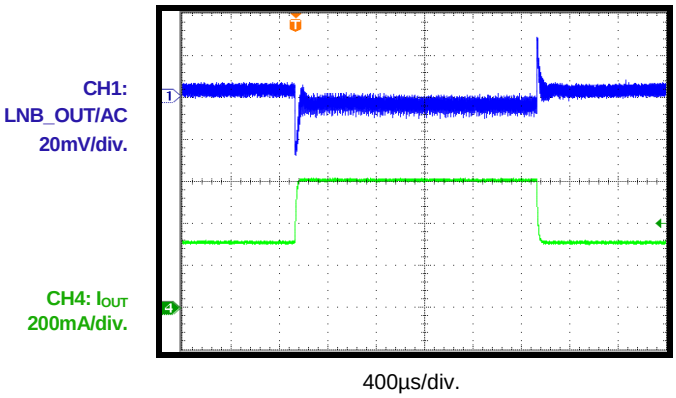
Load Transient

I_{OUT} = 0A to 0.3A



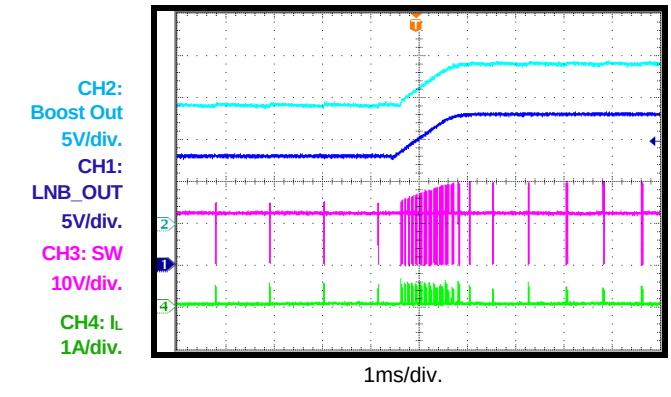
Load Transient

I_{OUT} = 0.3A to 0.6A



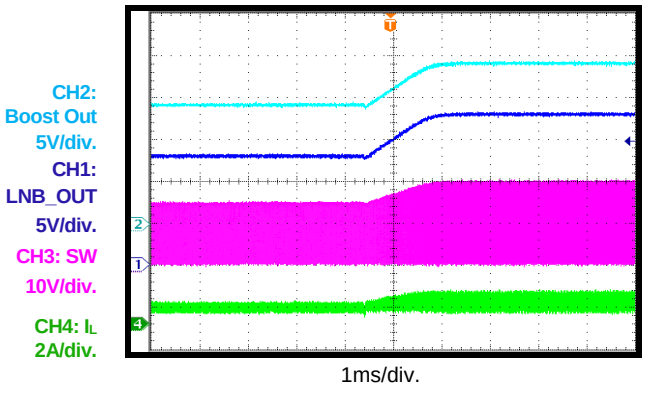
13V to 18V Switching

I_{OUT} = 0A



13V to 18V Switching

I_{OUT} = 0.6A

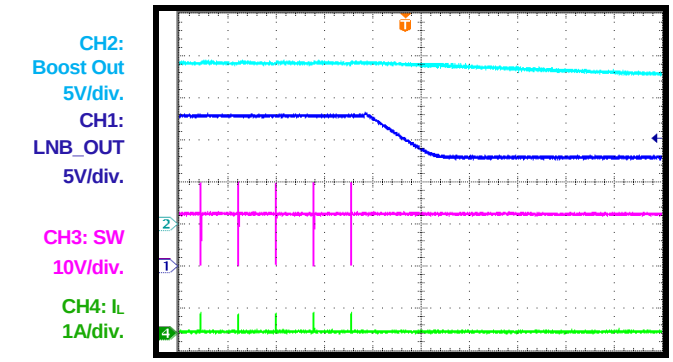


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 29. V_{DD} = 12V, LNB_OUT = 18V, L = 10µH, T_A = 25°C, unless otherwise noted.

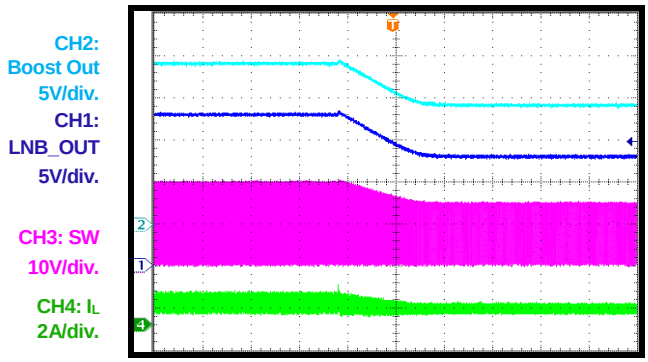
18V to 13V Switching

I_{OUT} = 0A



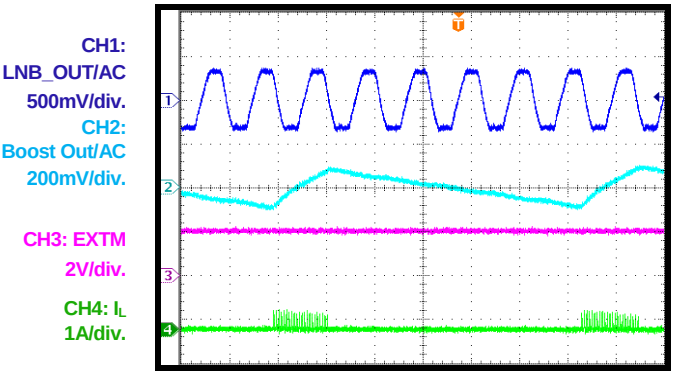
18V to 13V Switching

I_{OUT} = 0.6A



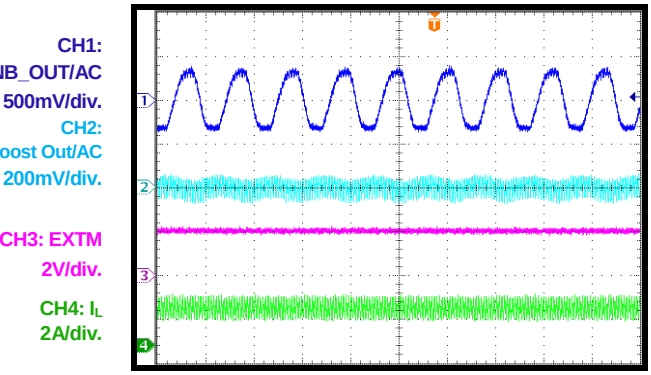
Tone Signal Steady State

EXTM = 2V, TCTRL bit = 0, I_{OUT} = 0A



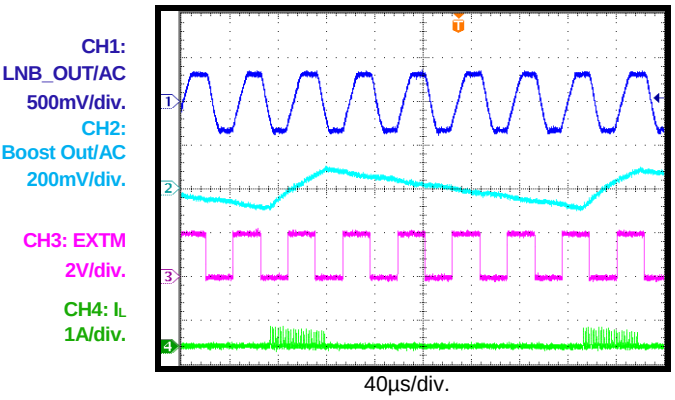
Tone Signal Steady State

EXTM = 2V, TCTRL bit = 0, I_{OUT} = 1A



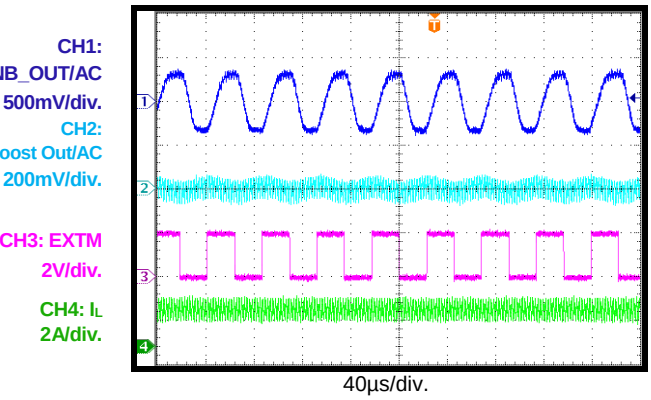
Tone Signal Steady State

EXTM = 22kHz square, TCTRL bit = 1,
I_{OUT} = 0A



Tone Signal Steady State

EXTM = 22kHz square, TCTRL bit = 1,
I_{OUT} = 1A

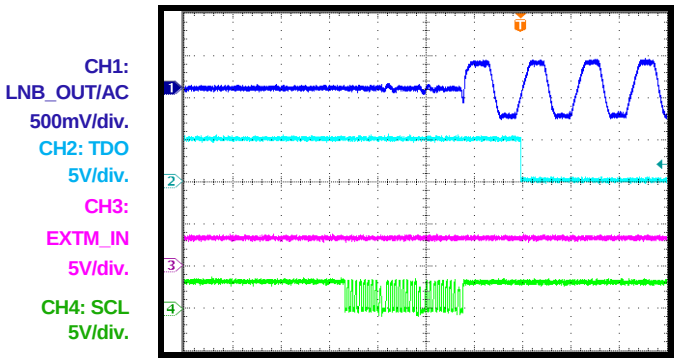


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 29. V_{DD} = 12V, LNB_OUT = 18V, L = 10µH, T_A = 25°C, unless otherwise noted.

Tone Entry

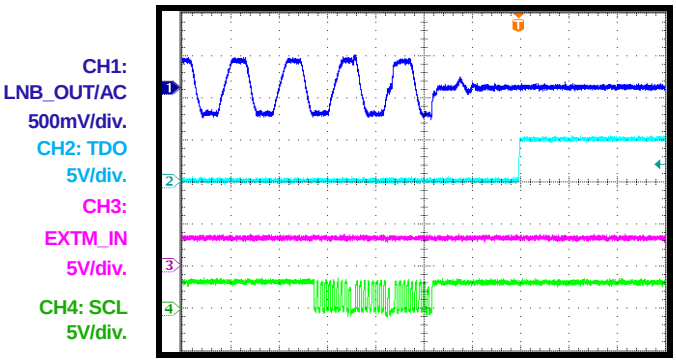
EXTM = 3.3V, TCTRL bit = 0, I_{OUT} = 0A,
TEN = 0 to 1



40µs/div.

Tone Exit

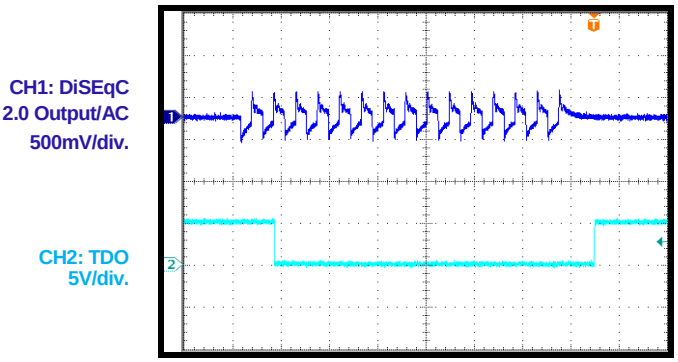
EXTM = 3.3V, TCTRL bit = 0, I_{OUT} = 0A,
TEN = 1 to 0



40µs/div.

Detect Tone Signal from Load

DiSEqC 2.0 output load = one pulse
(0mA to 40mA), f = 22kHz, duty = 50%)



100µs/div.

FUNCTIONAL BLOCK DIAGRAM

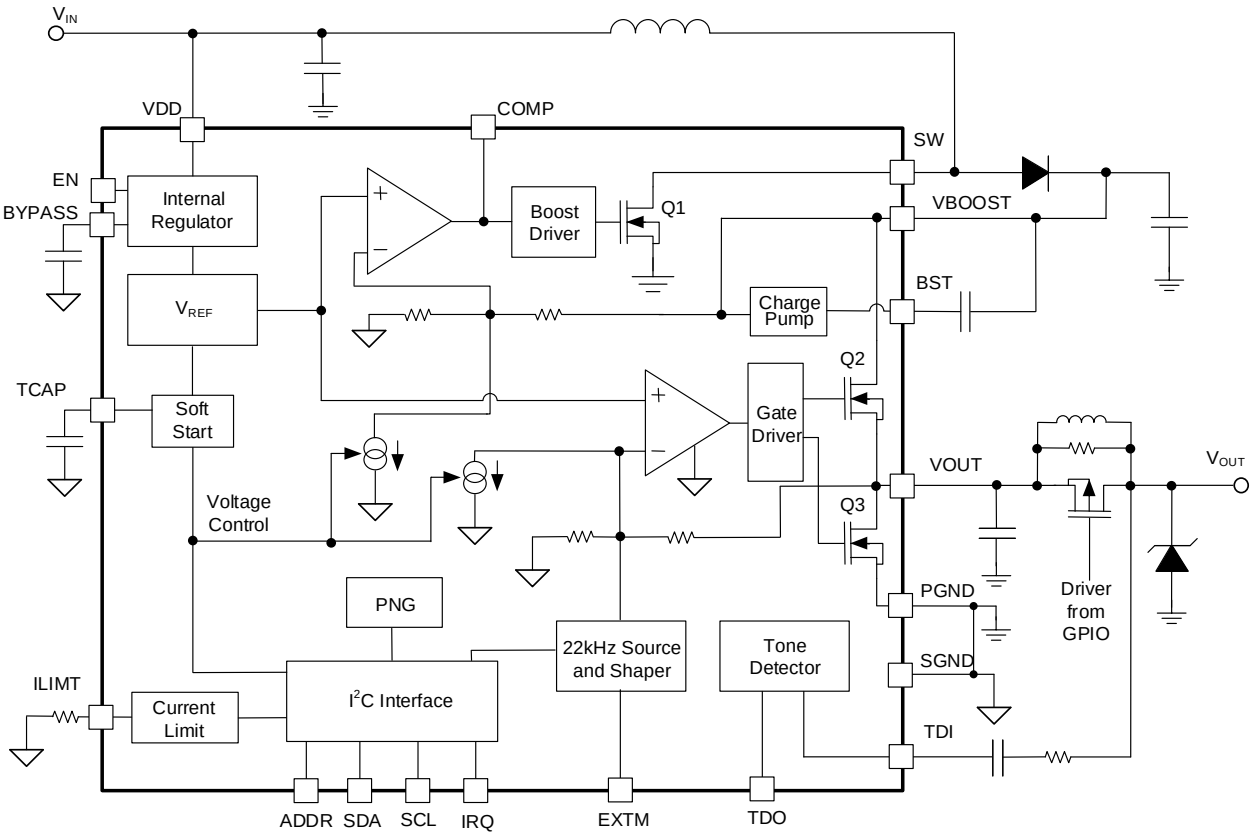


Figure 2: Functional Block Diagram

OPERATION

The MP8128 is a single-output voltage regulator that provides both a supply voltage and a control signal from satellite set top box modules to the low noise block downconverter (LNB) of the antenna port. The device is compatible with both DiSEqC 1.x and DiSEqC 2.x.

The MP8128 has an integrated boost converter that works from an 8V to 14V supply source. The converter generates a voltage to enable the linear post regulator to work at a minimum dissipated power.

Input Under-Voltage Lockout (UVLO)

The BYPASS voltage is powered by V_{DD} when input power is applied. The I²C interface starts working when the BYPASS voltage exceeds V_{I2C_UVLO}, but the power output cannot be enabled until V_{DD} rises to V_{DD_UVLO}.

When the BYPASS voltage exceeds V_{I2C_UVLO}, an under-voltage lockout (UVLO) fault occurs, and the IRQ pin pulls low to indicate the power stage's input UVLO interruption. One read cycle can reset the IRQ pin (even if V_{DD} is below V_{DD_UVLO}), but the UVLO bit can only be reset by reading a cycle after V_{DD} exceeds V_{DD_UVLO}. Then the V_{LINE} bits can be written to enable the output voltage.

If the V_{DD} voltage drops to V_{DD_UVLO}, the MP8128 stops switching and a UVLO fault occurs again. To remove the UVLO fault, there must be a new reading cycle after V_{DD} rises to V_{DD_UVLO}. Then the output can be enabled again.

Boost Converter/Linear Regulator

The boost converter is a fixed-frequency, non-synchronous voltage regulator with peak current mode control. The MP8128 provides a high 440kHz operating frequency, and the external COMP pin provides a flexible compensation design for any type of output capacitor.

To reduce power dissipation, the boost converter operates in a pulse-skip mode at light loads. The boost converter's output voltage tracks the requested LNB output voltage to allow the linear regulator to work with a minimum dropout voltage. If the LDM bit is set to 0, the LDO dropout voltage is about 1.1V. If the LDM bit is set to 1, the LDO dropout voltage is about 0.9V. During tone transmission, the LDM bit must set to 0 to guarantee sufficient voltage headroom. The LDM bit can be set to 1 if no tone transmission is required.

Output Voltage Control

To simplify the design for different polarization directions and line drop voltage compensation, the MP8128 output voltage can be easily configured via 5 bits (The V_{SEL} and V_{LINE} bits) in the internal registers of the I²C interface. Refer to the REG00 section on page 26 for V_{OUT} selection.

Output Slew Rate Control

The MP8128 TCAP pin supports a flexible soft start (SS) function to reduce the inrush current during start-up. The SS time is determined by the internal charge current on the capacitor connected to TCAP.

During V_{OUT} transient (e.g. 13V to 18V), the output voltage rising and falling times are also controlled by the soft-start circuit. The 22kHz tone rise is not controlled by the SS time.

Output Discharge Function Shutdown

When the V_{LINE} bits are set to 111, the MP8128 output voltage is disabled. Generally, there is a 0.7mA leakage current from VOUT to GND, so the output capacitor can be discharged even without a load current.

Boost Over-Voltage Protection (OVP)

The MP8128 features an over-voltage protection (OVP) circuit on SW. If VBOOST is disconnected on the board, the boost converter's output voltage cannot feed back to the boost control circuit, and the boost output voltage runs away. A typical 30V OVP circuit on SW shuts down the MP8128 to prevent damage to the IC once the over-voltage condition is detected. A 100ns blanking time is added to the detection circuit to avoid mistriggering OVP due to the SW voltage spike. Once the device initiates OVP, the MP8128 can be restarted by resetting the V_{LINE} bits or cycling the device's power.

If OVP occurs, the OVP event is recorded in the OVP register, and one interrupt signal is generated on the IRQ pin. The register resets after the output voltage has been disabled then re-enabled, or if the device restarts.

Current Limit

The LDO output current is limited, and the limit threshold can be configured via an external resistor connected to the ILIMT pin. The current limit can be calculated with Equation (1):

$$I_{LIMIT}\ (mA) = 9040 / R_{ILMIT}\ (k\Omega) \quad (1)$$

If the ILIMT pin is an open circuit, the current limit is about 0A. If the ILIMT pin is shorted to GND due to a fault condition, the current limit is clamped at about 1.5A.

The MP8128 provides two types of overload protection: dynamic or static protection.

If an overload condition is detected in dynamic protection mode, the output current is regulated at the current limit level for 50ms. If the overload is still detected after this period, the output shuts down for 1.8s before resuming operation. If an overload occurs, the window is registered and lasts for 50μs. If another overload is detected within this 50μs window, a new 50μs window begins. This detection mode ensures that OCP hiccup mode occurs in the event of a high oscillatory load current.

If the OCR bit is set to 0 in dynamic protection mode, the MP8128 can automatically recover after the overload condition is removed. If the OCR bit is set to 1, the output cannot recover until the V_{LINE} bits have been rewritten. See the Over-Current Protection (OCP) Logic section on page 23 for more details.

If an overload condition is detected in static mode, the output current is permanently limited at the current limit level until over-temperature protection (OTP) is triggered.

It is recommended to set the current limit in dynamic mode to avoid unnecessary power loss and excessively high temperatures on the IC.

Tone Generation

To make the design flexible, the MP8128 can introduce a 22kHz tone signal from an internal or external source (set by the TCTRL bit). Figure 3 shows the typical waveform.

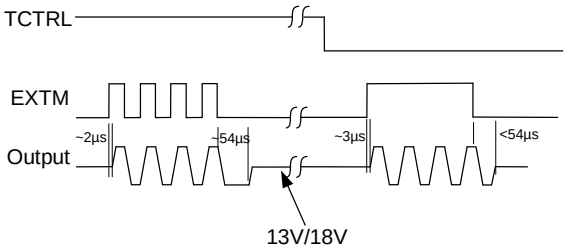


Figure 3: Tone Signal on the Output

The tone can be generated in three ways, described below:

1. TEN = 1 and TCTRL = 1: Apply an external 22kHz signal on EXTM to generate a tone on V_{OUT}.
2. TEN = 1 and TCTRL = 0: Apply a high or low voltage on EXTM. The output tone follows the EXTM signal envelope
3. Control the through TEN bit: When the EXTM voltage is high and TCTRL = 0, write the TEN bit from 0 to 1 to enable output tone generation.

Under light-load or no-load conditions, the tone signal on V_{OUT} is considered to have a good shape (no distortion) due to the MP8128's internal pull-down current capability.

Tone Decoding

To comply with DiSEqC 2.x bidirectional interface control, the MP8128 can detect the specified frequency and amplitude range signal on the TDI pin through a 10nF capacitor and a 100Ω resistor from VOUT. The TDO pin is an open-drain output that is pulled low when a tone signal is applied on the TDI pin. Generally, the TDO signal is sent one cycle (1T) after the TDI signal (see Figure 4).

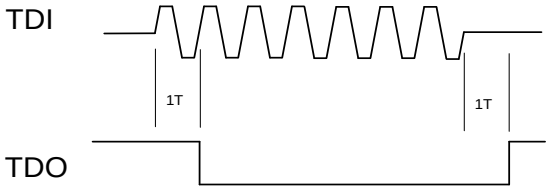


Figure 4: Tone Signal Detection

If the detected signal from TDI is out of specification, the MP8128 rejects the error signal to avoid mis-triggering TDO. The typical

rejection frequency is below 14kHz and above 30kHz. If the signal is below 100mV or above 1.1V, the signal is rejected by TDI detection.

The DiSEqC 2.x hardware specification requires one RL filter to receive the signal. To avoid the RL filter affection during tone transmissions, one gate driver signal from the host controller is required to drive the external P-channel MOSFET on and bypass the RL filter.

LDO Pull-Down Current and Protection

The VOUT pin sinks current when the output voltage exceeds the set voltage. This means that the voltage transient from high to low (or a 22kHz tone signal) is functional even if there is no load current on the output. To prevent power loss and thermal issues caused by the sink current when the output is biased to a higher voltage, an on timer (typically 10ms) is enabled when the sink current triggers the sink current limit. After 10ms, the LDO sink current limit is reduced to 2mA and the STO bit is set to 1. If the LDO sink current drops below the 2mA limit, the STO bit is reset, as well as the 10ms timer and sink current limit. There is 20µs de-glitch time for sink current protection recovery.

The LDO has different sink current capabilities depending on whether a tone is available.

Thermal Protection

If the junction temperature exceeds 150°C, the part shuts down and triggers an interrupt signal. Once the junction temperature drops to about 130°C, the part can recover automatically or after being re-enabled, as determined by the TSDM bit.

Fault Interrupt Operation

If over-temperature protection (OTP), over-voltage protection (OVP), under-voltage lockout (UVLO), or over-current protection (OCP) occurs, the open drain IRQ pin is pulled low to indicate the protection event. This can be used as an interrupt signal for the controller. The other status registers from PNG and STO do not trigger an IRQ request, and continuously update according to the system signal. The IRQ signal is reset to high with any I²C read cycle (even the fault bit is not cleared).

Under-Voltage Lockout (UVLO) Bit Logic

When BYPASS voltage exceeds V_{I2C_UVLO} during start-up, the I²C interface and register work. The UVLO bit is set to 1 by default, and the IRQ pin is pulled low. One read cycle can reset the IRQ signal to high, but the UVLO bit can only be reset to 0 once the input voltage exceeds 7.15V (V_{DD_UVLO}). One additional I²C read cycle is required to clear the UVLO bit after VDD rises above V_{DD_UVLO}, even though the IRQ pin is reset by one read cycle before VDD rises above V_{DD_UVLO}. The converter's output voltage can be enabled after the UVLO bit is cleared.

If the input power falls below the V_{DD_UVLO} falling threshold after the MP8128 is enabled, the UVLO bit is set to 1, and the V_{LINE} bits reset to 111. At the same time, the IRQ pin pulls low to generate an interrupt request. After the power recovers, the power stage can be re-enabled with one read cycle and one write operation to the V_{LINE} bits. The V_{LINE} bits cannot be written before the UVLO bit is cleared.

Over-Voltage Protection (OVP) Logic

If the SW pin triggers over-voltage protection (OVP), the OVP bit is set to 1 and the V_{LINE} bits are set to 111. At the same time, the IRQ pin is pulled low to signal an interrupt. After OVP, the MP8128 latches off. The OVP bit and IRQ pin can be reset by one read cycle, but the V_{LINE} bits stay at 111 unless one new value is written to the V_{LINE} bits. The V_{LINE} bits cannot be written before the OVP bit is cleared.

Over-Current Protection (OCP) Logic

If an over-current (OC) condition occurs in dynamic protection mode, V_{OUT} is shut down and the OCP bit is set to 1 after 50ms. At the same time, IRQ pulls low. After a 1.8s interval timer, the MP8128 restarts with a 50ms timer if OCR bit is set to 0. If V_{OUT} can recover within this 50ms, normal operation resumes. After OCP recovery, the OCP bit can be set to 0 by one I²C read cycle. In dynamic OCP, the V_{LINE} bits stay at their original value for recovery (see Figure 5).

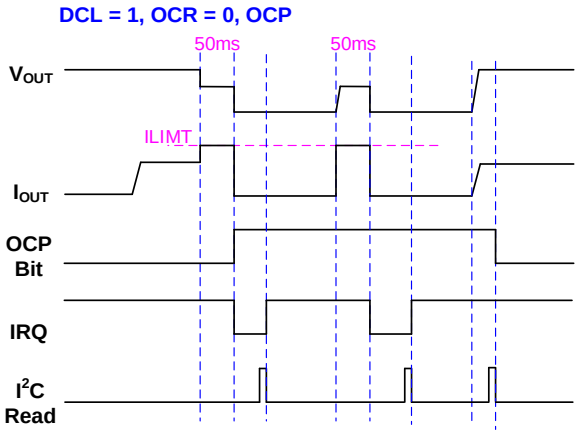


Figure 5: Dynamic OCP with Automatic Recovery

Dynamic OCP with automatic recovery follows the steps listed below:

1. The IRQ pin and OCP bit are set after 50ms.
2. The IRQ pin resets after one I²C read cycle, but the OCP bit cannot be reset by an I²C read cycle until the over-current condition is removed.
3. V_{OUT} recovers after the over-current condition is removed.

If the OCR bit is set to 1, the MP8128 cannot recover after the 50ms OCP detection time. In this scenario, all V_{LINE} bits are set to 111 once OCP is triggered. An I²C read cycle can reset OCP and IRQ, but the V_{LINE} bits must be rewritten for the MP8128 to recover (see Figure 6).

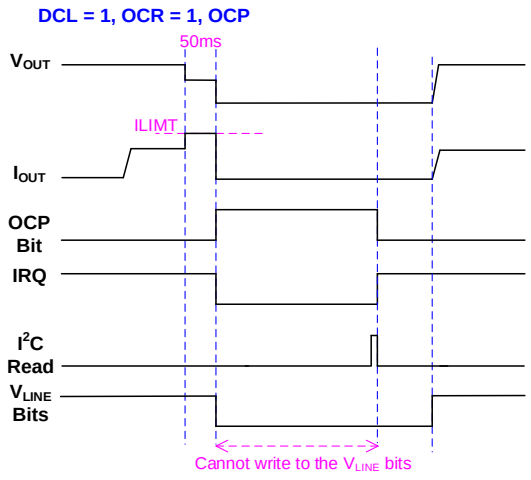


Figure 6: Dynamic OCP Without Automatic Recovery

Dynamic OCP without automatic recovery follows the steps listed below:

1. The IRQ pin and OCP bit are set after 50ms.
2. The IRQ pin and the OCP bit reset after one I²C read cycle.
3. V_{OUT} recovers after rewriting the V_{LINE} bits. The V_{LINE} bits cannot be written until the OCP bit is reset.

If OCP occurs in static protection mode, the OCP bit is set to 1 once the current limit is reached. The IRQ pin pulls low after OCP occurs, then pulls high after one I²C read cycle (see Figure 7).

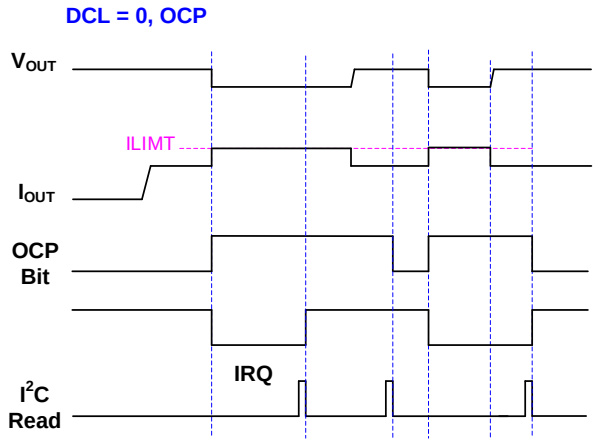


Figure 7: Static OCP

Static OCP follows the steps listed below:

1. The IRQ pin and OCP bit are set after the current limit is reached
2. The IRQ pin resets after one I²C read cycle, but the OCP bit cannot be reset by an I²C read cycle until the over-current condition is removed.
3. V_{OUT} recovers after the over-current condition is removed.

Over-Temperature Protection (OTP) Logic

If over-temperature protection (OTP) occurs, the MP8128 shuts down. Then the OTP bit is set to 1, and IRQ pulls low. After the temperature drops to the OTP recovery threshold, the MP8128 recovers according to the TSDM bit.

If the TSDM bit is set to 1, the MP8128 automatically sets the V_{LINE} bits to 111 to disable the LNB output. If the temperature drops, the OTP bit and IRQ pin recover after one reading cycle. The LNB output cannot recover until the V_{LINE} bits have been rewritten (see Figure 8).

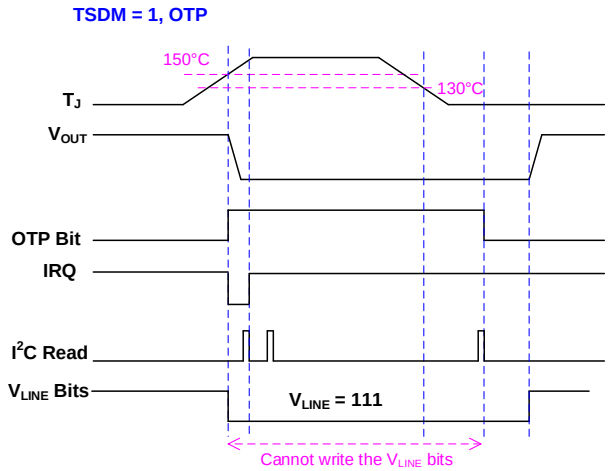


Figure 8: OTP (Latch-Off Mode)

Latch-off mode follows the steps below:

1. The IRQ pin and OTP bit are set once the device reaches 150°C.
2. The IRQ pin resets after one I²C read cycle, but the OTP bit cannot be reset by an I²C read cycle until the over-temperature condition is removed.
3. The V_{LINE} bits are automatically set to 111. These bits cannot be written until the over-temperature condition is removed.
4. After the over-temperature condition is removed, write to the V_{LINE} bits to restart the MP8128.

If TSDM = 0, the V_{LINE} bits stay at the same setting that they had before thermal shutdown. The LNB output can automatically recover once the over-temperature condition is removed (see Figure 9).

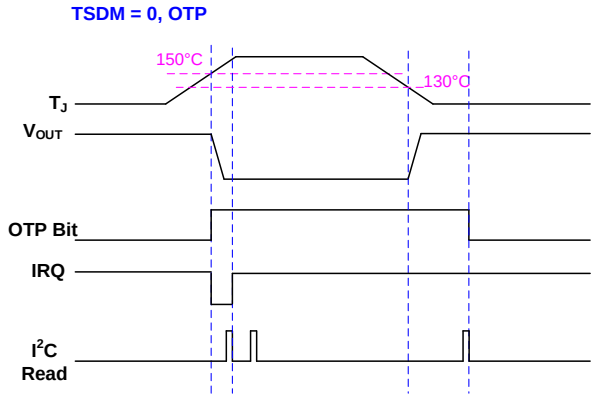


Figure 9: OTP (Non Latch-Off Mode)

Non latch-off mode follows the steps below:

1. The IRQ pin and OTP bit are set once the device reaches 150°C.
2. The IRQ pin resets after one I²C read cycle, but the OTP bit cannot be reset by an I²C read cycle until the over-temperature condition is removed.
3. After the over-temperature condition is removed, V_{OUT} recovers automatically.

Enable Control through the I²C

The MP8128's I²C interface starts to work after input power is applied. The MP8128 output voltage is disabled by default when the V_{LINE} bits are set to 111. Change V_{LINE} to enable the output power. When the V_{LINE} bits are set to 111, all power stage circuits are disabled.

I²C Interface

The MP8128 features with one I²C interface that allows transfers up to 400kbps. This interface can be used to configure internal functions and read the working statuses. See the Register Map on page 26 for the I²C control functions. The device address is configured from 0001000 to 0001011. The device does not support general call addresses.

Table 1 lists the recommended I²C slave addresses based on the ADDR resistor.

Table 1: Recommended I²C Slave Address Selection by the ADDR Resistor

ADDR Resistor	I²C Slave Address	
	Binary	Hex
0Ω	000 1000	08
27kΩ	000 1001	09
47kΩ	000 1010	0A
Float	000 1011	0B

I²C Data Transfer

Every byte put on the SDA line must be 8 bits long. Each byte has to be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable (low) during the high period of this clock pulse.

Figure 10 shows the data transfer format. After the start (S) condition, a slave address is sent. This address is 7 bits long followed by an eighth bit, which is a data direction bit (R/W). A 0 indicates a transmission (write), while a 1 indicates a request for data (read). A data transfer is always terminated by a stop (P) condition generated by the master. However, if a master must continue to communicate on the bus, it can generate a repeated start (Sr) condition and address another slave without first generating a stop condition (see Figure 10).

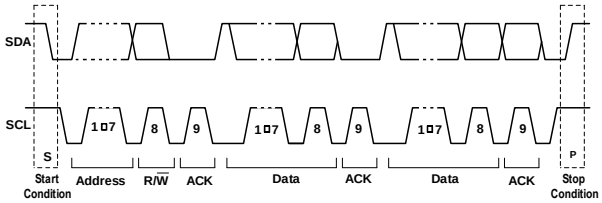


Figure 10: Complete Data Transfer

The MP8128 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification requirements. It requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. The MP8128 acknowledges each byte it has received by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP8128. The MP8128 performs an update on the falling edge of the LSB byte.

Figure 11 shows an example of an I²C write command. Figure 12 shows an example of an I²C write command.

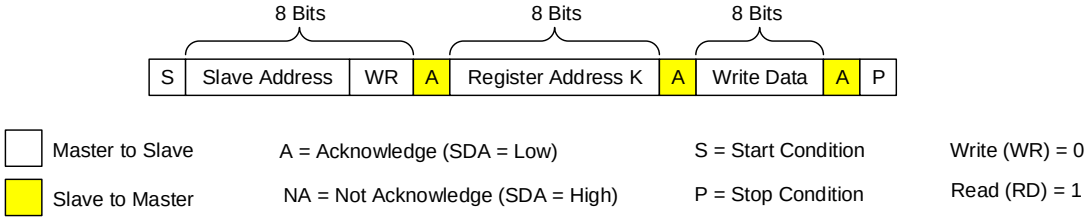


Figure 11: I²C Write Example

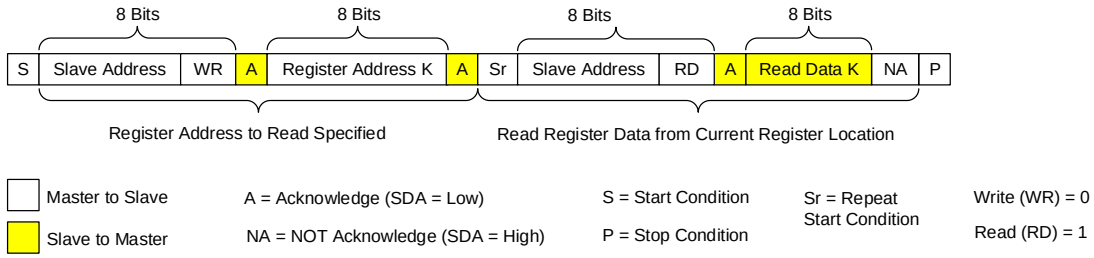


Figure 12: I²C Read Example

I²C REGISTER MAP

Add	R/W	Name	D7	D6	D5	D4	D3	D2	D1	D0
00	R/W	CTRL1	-	-	-	V_{SEL}		V_{LINE}		
01	R/W	CTRL2	-	TSDM	ISEL	TEN	LDM	OCR	DCL	TCTRL
02	R	STATUS	-	TDET	OVP	OTP	UVLO	STO	PNG	OCP
03	R	ID	-	-	-	-	VENDOR_ID		FAB	

Register Default Values

Add	R/W	Name	D7	D6	D5	D4	D3	D2	D1	D0
00	R/W	CTRL1	-	-	-	0	1	1	1	1
01	R/W	CTRL2	-	0	0	0	0	0	1	0
02	R	STATUS	-	0	0	0	1	0	1	0
03	R	ID	-	-	-	-	0	0	0	0

REGISTER DESCRIPTION

REG00: CTRL1

Bits	Name	Description
D[4:3]	V_{SEL}	Selects the VOUT voltage. 00: 10.333V 01: 12.667V 10: 15V 11: 18V
D[2:0]	V_{LINE}	Sets the V_{OUT} line drop compensation, which is added to V_{OUT} by V_{SEL}. 000: 0V compensation 001: 0.333V compensation 010: 0.667V compensation 011: 1.000V compensation 100: 1.333V compensation 101: 1.667V compensation 110: 2.000V compensation 111: Disable power output (this is default setting after start-up)

REG01: CTRL2

Bits	Name	Description
D6	TSDM	Sets the thermal shutdown recovery mode. 0: The V_{LINE} bits keep same value after over-temperature protection (OTP). If OTP recovers, MP8128 will automatically restart 1: V_{LINE} bits are set to 111 after OTP. If OTP recovers, V_{OUT} stays at 0V until the V_{LINE} bits are rewritten
D5	ISEL	Selects the boost inductor current limit. 0: The boost switching current limit is about 6A 1: The boost switching current limit is about 2.8A

D4	TEN	Controls the tone for signal transmitting. 0: The 22kHz tone is disabled 1: The 22kHz tone is enabled. The tone output is controlled by the EXTM pin and the TCTRL bit
D3	LDM	Controls the LDO low voltage drop mode, 0: The LDO voltage drop is about 1.1V. This bit must be 0 for tone transmission 1: The LDO voltage drop is about 0.9V
D2	OCR	Sets the dynamic OCP recovery. 0: V_{OUT} recovers with a 1.8s off time. 1: After 50ms of OCP, V_{OUT} does not recover until the V_{LINE} bits are rewritten
D1	DCL	Sets the over-current control mode. 0: Dynamic output current limit control is disabled 1: Dynamic output current limit control is enabled
D0	TCTRL	Controls the 22kHz tone signal source when TEN = 1. 0: The tone is internally generated according to the EXTM pin's voltage 1: The tone is controlled by an external 22kHz source on the EXTM pin

REG02: STATUS

Bits	Name	Description
D6	TDET	1: A 22kHz tone is detected on the TDI pin 0: No 22kHz tone signal is detected on the TDI pin
D5	OVP	1: A boost triggers over-voltage latch-off protection 0: A boost does not trigger over-voltage latch-off protection
D4	OTP	1: The junction temperature has reached 150°C, and the power stage has shut down due to over-temperature protection (OTP) 0: No OTP has occurred
D3	UVLO	1: The VDD voltage is below the V_{DD_UVLO} falling threshold 0: The VDD voltage exceeds the V_{DD_UVLO} rising threshold, and the under-voltage lockout (UVLO) falling event is cleared by an I²C read cycle
D2	STO	1: If the LDO output sinks the maximum current for longer than 10ms, STO is to 1 to indicate a sink. This may occur when an external voltage is added on LDO output. STO recovers after the sink current drops to 2mA 0: No over-current sink event has occurred
D1	PNG	1: The VOUT voltage is out of specification 0: The VOUT voltage is within specification See the Electrical Characteristics section on page 7 for PNG specifications.
D0	OCP	1: The LDO over-current limit has been triggered 0: No over-current condition has occurred

REG03: ID

Bits	Name	Description
D[3:2]	VENDOR_ID	Vendor ID.
D[1:0]	FAB	Fab location.

APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor (C1) maintains the DC input voltage. Low-ESR ceramic capacitors with 10µF X7R dielectrics are recommended. The input voltage ripple can be estimated with Equation (2):

$$\Delta V_{IN} = \frac{V_{IN}}{8 \times f_{SW}^2 \times L \times C_1} \times (1 - \frac{V_{IN}}{V_{BOOST}}) \quad (2)$$

Where f_{SW} is the boost switching frequency, L is the boost inductor value and V_{BOOST} is the boost converter output voltage.

Selecting the Boost Output Capacitor

The boost converter has a discontinuous output current, and requires an output capacitor (C3) to supply the AC current to the load. Use low-ESR capacitors for the best performance. The boost output voltage ripple can be estimated with Equation (3):

$$\Delta V_{BOOST} = \frac{V_{BOOST}}{f_{SW} \times R_L \times C_3} \times (1 - \frac{V_{IN}}{V_{VBOOST}}) \quad (3)$$

Where R_L is the value of the load resistor.

Ceramic capacitors with X7R dielectrics are highly recommended because of their low ESR and small temperature coefficient. Typically, two 10µF X7R ceramic capacitors are recommended. Place one capacitor close to the boost switching loop, then place the second capacitor close to the LDO input pin.

Tantalum or low-ESR electrolytic capacitors are sufficient for the boost output. In this scenario, place two smaller-sized ceramic capacitors (0.1µF or higher value) close to both the boost switching loop output and the LDO input pin. When using electrolytic capacitors, a high ESR can result in a higher voltage ripple on the boost output. If this occurs, an additional filter may be require to minimize the ripple.

Selecting the Boost Converter Inductor

MPL **Optimized Performance with MPS Inductor MPL-AL Series**

The inductor must transfer the energy between the input source and the boost converter's output capacitors. A larger-value inductor results in less ripple current but results in a lower peak inductor current, which reduces the stress on the power MOSFET. However, a larger-value inductor has a larger physical size, higher series resistance, and lower saturation current.

For most designs, the inductance value can be calculated with Equation (4):

$$L = \frac{V_{IN} \times (V_{BOOST} - V_{IN})}{f_{SW} \times V_{BOOST} \times \Delta I_L} \quad (4)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% to 50% of the maximum inductor peak current. Generally, a 10µH inductor is recommended. Ensure that the inductor does not saturate under the worst-case load transient condition. The inductor should have a low DCR (series resistance of the inductor current without saturating windings) to reduce the resistive power loss.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AL	4.7µH to 15µH	MPS
MPL-AL6060-100	10µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information

Selecting the Boost Converter Rectifier Diode

The high switching frequency demands high-speed rectifiers. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. Typically, a 2A or 3A Schottky diode is recommended for the boost converter for high efficiency, and the diode voltage rating should exceed the output voltage (or require a higher rating based on other protections, such as surge protection).

Selecting the LDO Output Capacitor and Diode

To transport the 22kHz tone signal, a 0.1μF output capacitor is recommended for the LDO regulator. A capacitance that is too high may affect the 22kHz signal shape, while a low capacitance may lead to LDO instability.

For over-current or short-circuit conditions on the far end of the bus line (cable), the MP8128 shuts down if a protection is triggered, and the VOUT voltage may become negative due to the long cable. One low voltage drop Schottky diode (e.g. 1N5819 or DFLS140) should be placed between the VOUT and GND pins to clamp the negative voltage.

Selecting the Soft-Start Capacitor

With the required output voltage rising time (t_{RISE}), the value of the TCAP capacitor (C_{TCAP}) can be calculated with Equation (5):

$$C_{TCAP} = \frac{(13.5 \times I_{CAP} \times t_{RISE})}{V_{OUT}} \quad (5)$$

Where I_{CAP} is charging current (typically 6.2μA).

The TCAP soft-start capacitor also controls the voltage transient slew rate.

TCAP is the feedback reference voltage of boost and LDO output, so one smaller-sized capacitor is required to decouple the TCAP pin. Generally, a 22nF is recommended to control soft start and decouple the reference voltage.

Setting the Boost Converter Compensation Circuits

The output of the transconductance error amplifier (COMP) is used to compensate the regulation control system. R5 and C6 are placed in series to compensate the feedback loop gain and phase. Generally, it is recommended for R5 to equal 6.8kΩ, and for C6 to equal 4.7nF if using a ceramic output capacitor (see Figure 14 on page 31).

If an electrolytic capacitor is used to replace the ceramic capacitor, it is recommended to place one small capacitor from COMP to GND. This forms a pole with R5 to compensate the zero formed by the electrolytic capacitor's ESR.

Selecting the BYPASS Capacitor

The MP8128 integrates the V_{CC} power in the internal circuit bias (typically 5V). The internal regulator requires one 0.22μF ceramic bypass capacitor. The V_{CC} power supplies the internal control circuit. Do not connect an external load to the V_{CC} power.

Selecting the BST Capacitor

The MP8128 integrates one charge pump to power the N-channel MOSFET for the LDO regulator. One external bootstrap capacitor is required to bypass the charge pump power. Generally, it is recommended to place a 0.1μF ceramic capacitor between the BST and VBOOST pins.

Design Example

Table 3 lists a design example following the recommended application guidelines.

Table 3: Design Example

Parameter	Symbol	Value	Units
Input voltage	V_{DD}	8 to 14	V
LNB output voltage (12)	LNB_OUT	10.33 to 20	V
LNB output current	I_{OUT}	0 to 1	A

Figure 14 on page 31 shows the detailed application schematic. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section on page 12. For more device applications, refer to the related evaluation board datasheet.

Note:

12) Use the I²C interface to set the LNB output voltage

PCB Layout Guidelines

Efficient PCB layout is critical for high-frequency switching power supplies. A poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. For the best results, refer to Figure 13 and follow the guidelines below:

1. Keep the boost output loop (the MP8128's SW pin, D1, C3B, and the MP8128's PGND pin) as small as possible.
2. Place the LDO input capacitor (C3A) and the output capacitor (C2) as close as possible to the VBOOST and VOUT pins.
3. Connect the LDO output capacitor and the other signal ground to SGND.
4. Connect the boost output ground to PGND and then connect SGND to PGND with a single point.
5. Keep all high-frequency AC current power traces (VBOOST, SW, and PGND) as short and wide as possible.
6. Keep the TCAP voltage trace far away from any noise sources, such as the SW node.
7. Place a small decoupling capacitor as close as possible to VDD to reduce the input voltage ripple.
8. Place the bypass capacitor as close as possible to the BYPASS pin.
9. Keep the BST voltage path as short as possible.
10. Use a wide copper trace for GND to improve thermal performance. Place vias on GND and the copper around (and under) the MP8128 to further improve thermal performance.

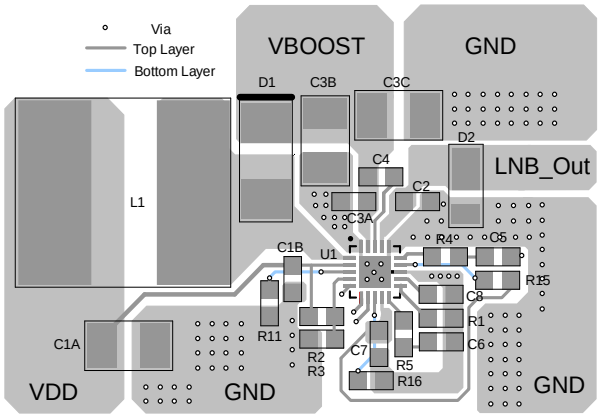


Figure 13: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

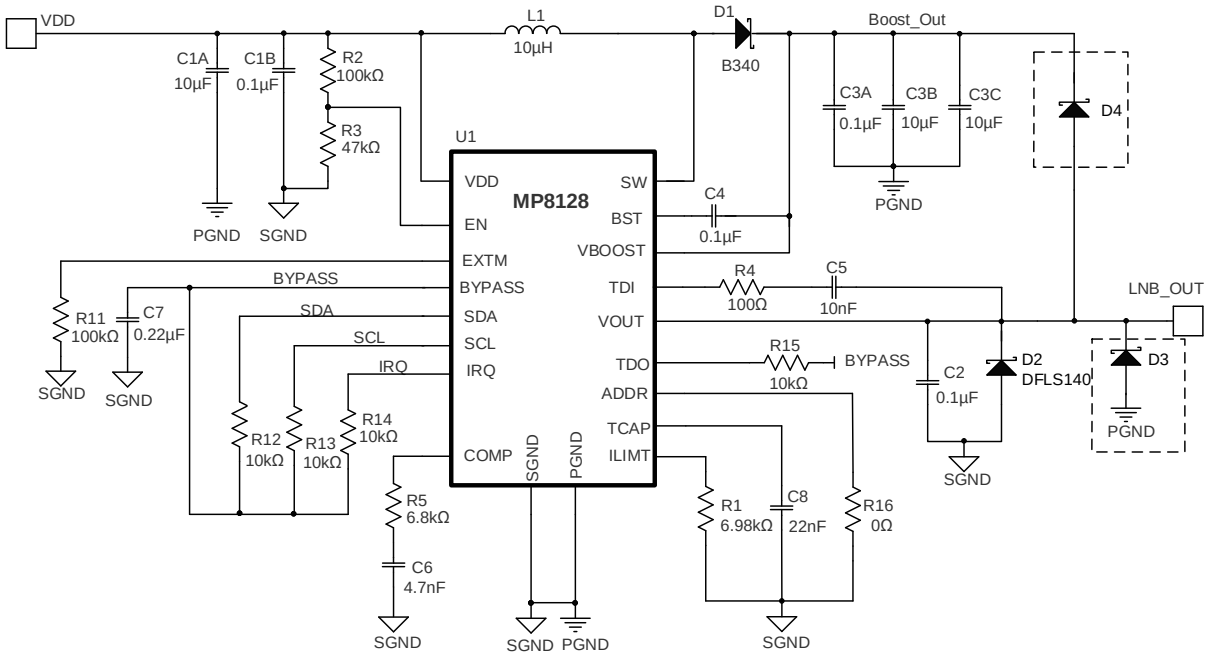


Figure 14: Typical DiSEqC 1.0 Application Circuit (13)

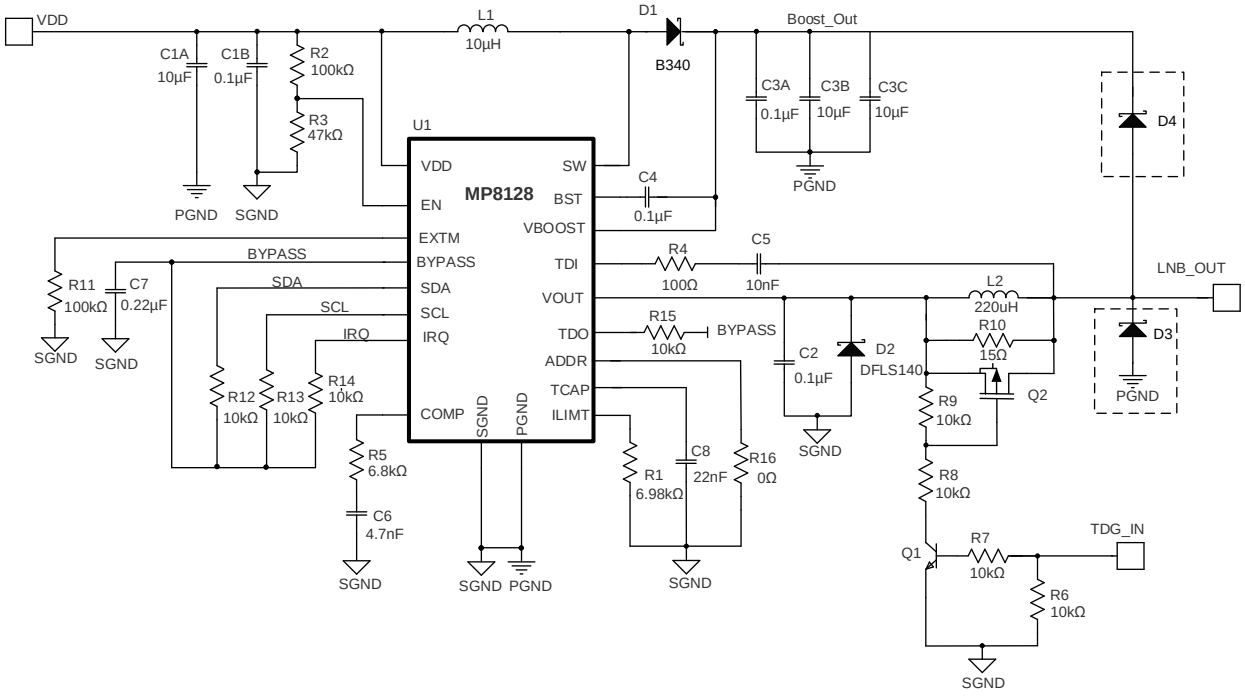


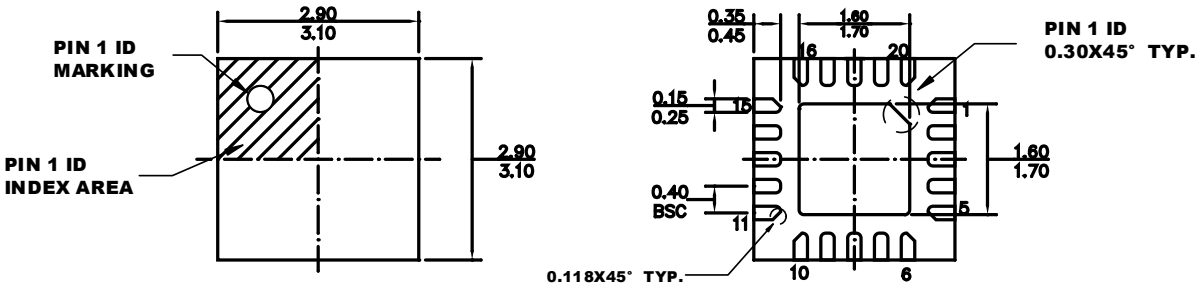
Figure 15: Typical DiSEqC 2.0 Application Circuit (13)

Note:

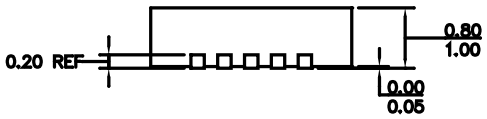
13) D3 is TVS diode, D4 is Schottky diode. D3 and D4 are optional for surge tests. If no surge test is required, D3 and D4 can be removed.

PACKAGE INFORMATION

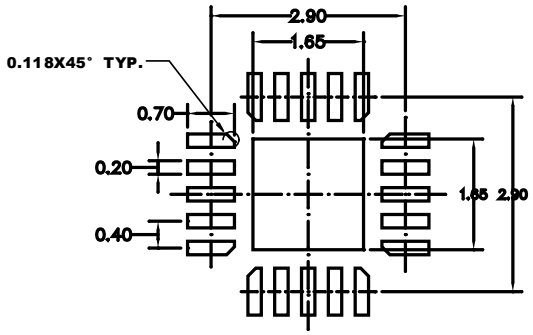
QFN-20 (3mmx3mm)



TOP VIEW **BOTTOM VIEW**



SIDE VIEW

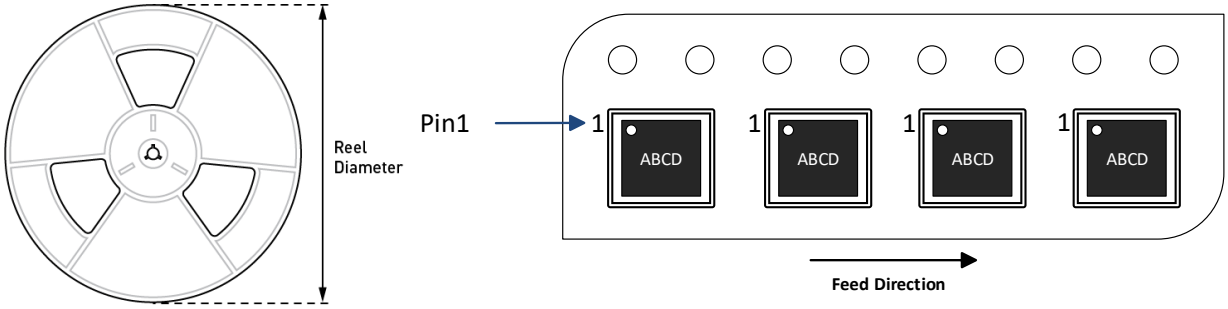


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8128GQ–Z	QFN-20 (3mmx3mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/26/2021	Initial Release	-