

DESCRIPTION

The MP8130 is a rail-to-rail output, high voltage operational amplifier in a TSOT-23 package. This amplifier provides 200KHz bandwidth while consuming an incredibly low 10 μ A of supply current. The MP8130 can operate over a single supply range of 2.7V to 36V. It is available in tiny TSOT23-5 packages.

FEATURES

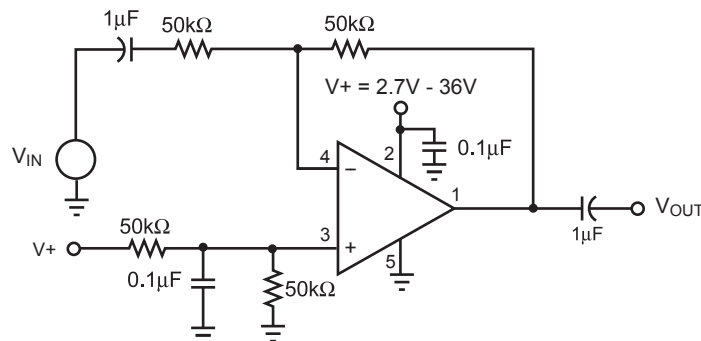
- Single Supply Operation: 2.7V to 36V
- TSOT23-5 Package
- 200KHz –3dB Bandwidth
- 10 μ A Supply Current
- Rail-to-Rail Output
- Unity-Gain Stable
- Input Common Mode to Ground
- Drives Up to 1000pF of Capacitive Loads
- Available in a TSOT23-5 Package

APPLICATIONS

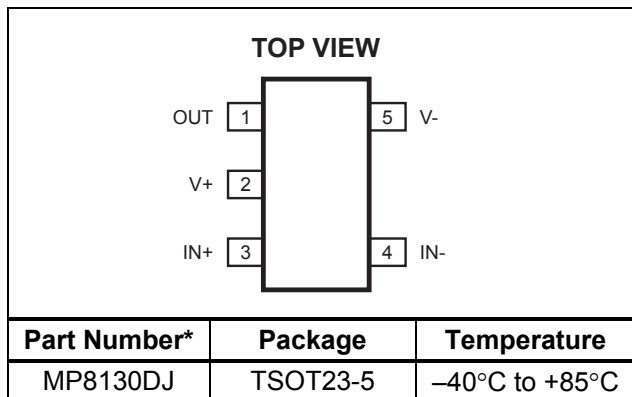
- Precision Micropower Amplifiers
- Micropower Signal Processing
- Test Equipment

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TYPICAL APPLICATION



PACKAGE REFERENCE



* For Tape & Reel, add suffix -Z (eg. MP8130DJ-Z)
 For RoHS compliant packaging, add suffix -LF (eg. MP8130DJ-LF-Z)

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply Voltage (V+ to V-) +40.0V
 Differential Input Voltage (V_{IN+} - V_{IN-}) +6.0V
 Input Voltage
 V_{IN+} = V_{IN-} (V-) - 0.3V, (V+) + 0.3V

Recommended Operating Conditions ⁽²⁾

Supply Voltage +2.7V to +36V
 Operating Temperature -40°C to +85°C

Thermal Resistance ⁽³⁾

θ_{JA} θ_{JC}
 TSOT23-5 220 110.. °C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The device is not guaranteed to function outside of its operating conditions.
- 3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V₊ = +20V, V₋ = 0V, V_{CM} = V₊/2, R_L = 50kΩ, T_A = +25°C, unless otherwise noted.

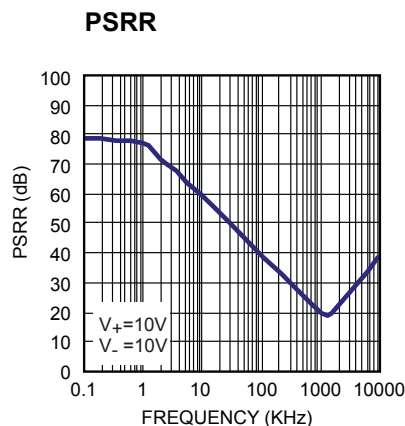
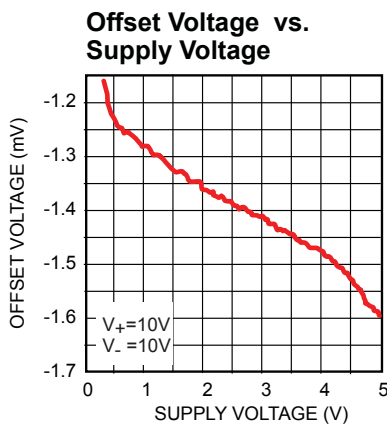
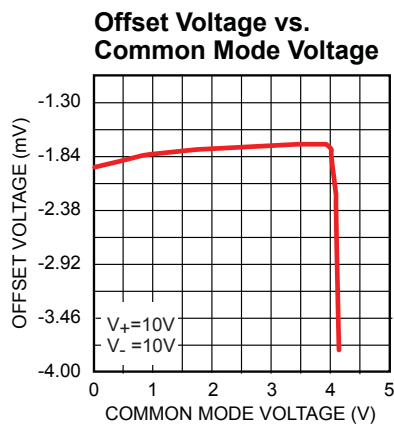
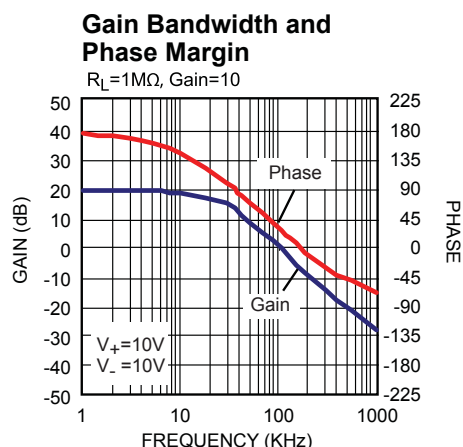
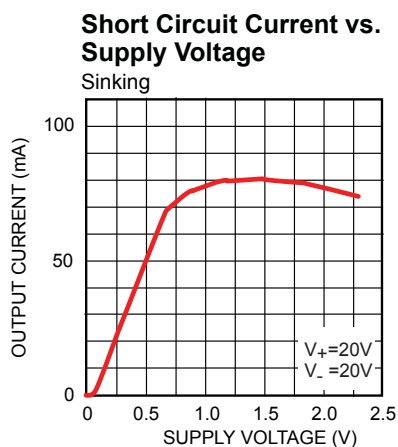
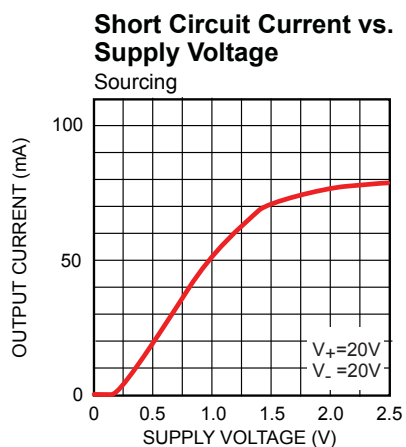
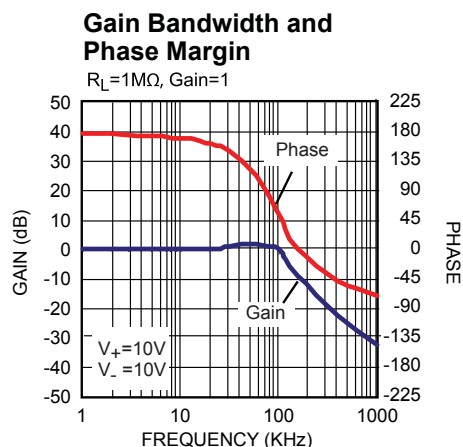
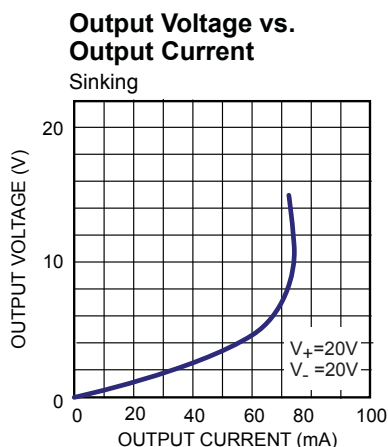
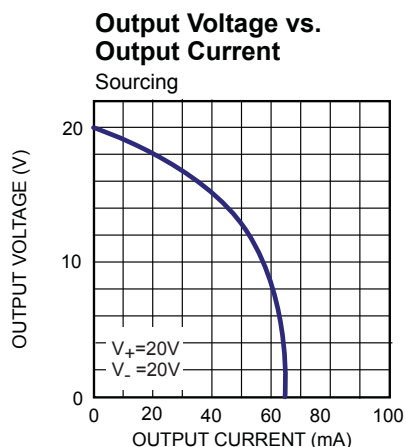
Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Offset Voltage	V _{OS}		-5	1	+5	mV
Input Offset Voltage Temp Coefficient				15		μV/°C
Input Bias Current ⁽⁴⁾	I _B			2		pA
Input Offset Current ⁽⁴⁾	I _{OS}			0.2		pA
Input Voltage Range	V _{CM}	CMRR > 60dB (V ₊ = 36V)	0		36	V
Common-Mode Rejection Ratio	CMRR	0 < V _{CM} < 36.0V (V ₊ = 36V)	80	82		dB
Power Supply Rejection Ratio	PSRR	Supply Voltage change of 2.7V/ 36V		80		dB
Large Signal Voltage Gain	A _{VOL}	R _L = 100kΩ, V _{OUT} = 5.0 Peak to Peak	60	88		dB
Maximum Output Voltage Swing	V _{OUT}	R _L = 100k		(V ₊) - 50mV		V
Minimum Output Voltage Swing	V _{OUT}	R _L = 100k		(V ₋) + 50mV		V
Gain-Bandwidth Product ⁽⁴⁾	GBW	R _L = 1MΩ, C _L = 2pF, V _{OUT} = 0V		100		KHz
-3dB Bandwidth ⁽⁴⁾	BW	A _V = 1, C _L = 2pF, R _L = 1MΩ		200		KHz
Slew Rate ⁽⁴⁾	SR	A _V = 1, C _L = 2pF, R _L = 1MΩ		0.1		V/μs
Short Circuit Current	I _{SC}	Source	-20			mA
		Sink	20			mA
Supply Current	I _{sup}	No Load		10	15	μA

Note:

4) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

C1= C3 =0.1 μ F, C2=C4=10 μ F, R_L = 1M Ω (Reference Figure 3)

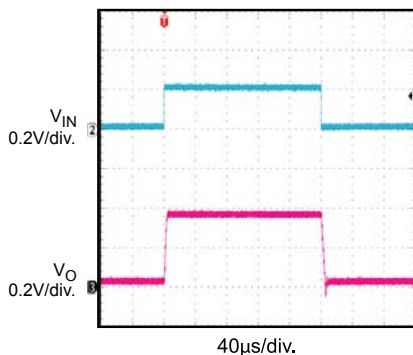


TYPICAL PERFORMANCE CHARACTERISTICS

C1= C3 =0.1μF, C2=C4=10μF, R_L = 1MΩ (Reference Figure 3)

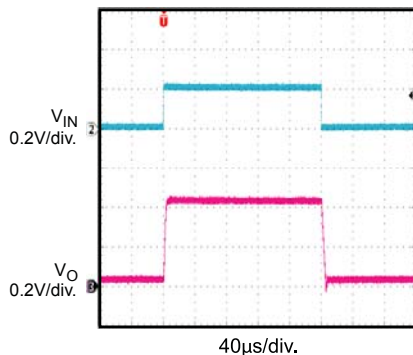
Small Signal Pulse Response

A_V = 2, V₊ = V₋ = 10V, R_L = 1MΩ



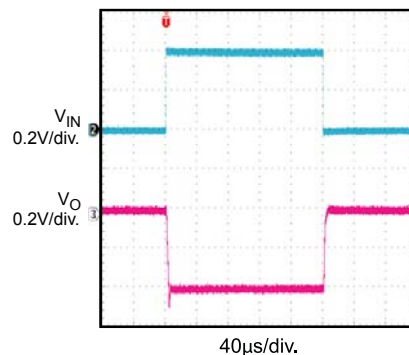
Small Signal Pulse Response

A_V = 2, V₊ = V₋ = 15V, R_L = 1MΩ



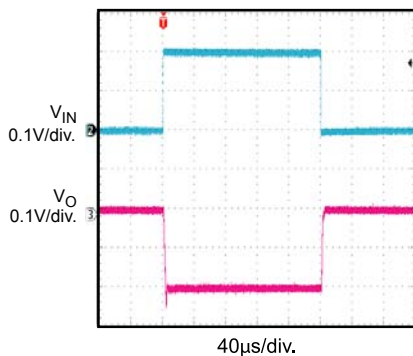
Small Signal Pulse Response

A_V = -1, V₊ = V₋ = 5V, R_L = 1MΩ



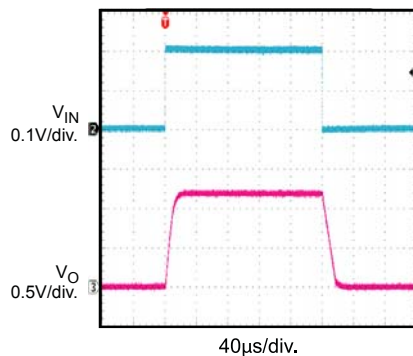
Small Signal Pulse Response

A_V = -1, V₊ = V₋ = 12V, R_L = 1MΩ



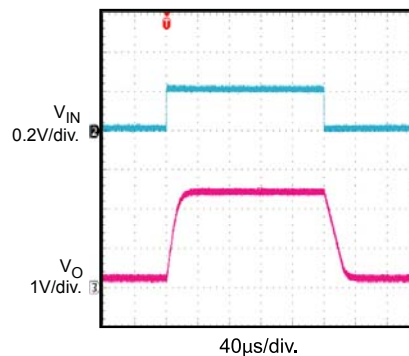
Small Signal Pulse Response

A_V = 6, V₊ = V₋ = 5V, R_L = 1MΩ



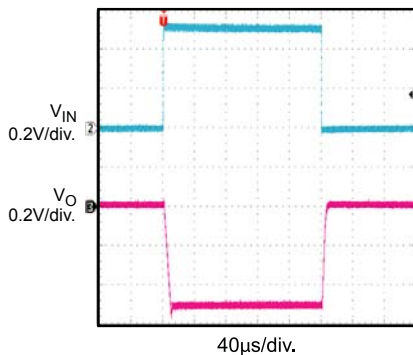
Small Signal Pulse Response

A_V = 6, V₊ = V₋ = 15V, R_L = 1MΩ



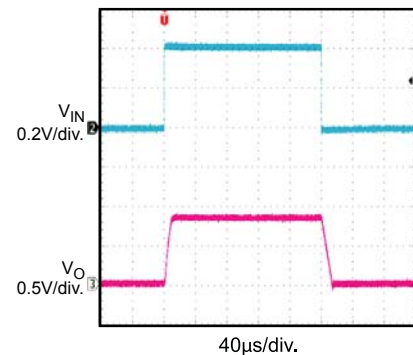
Small Signal Pulse Response

A_V = -1, V₊ = V₋ = 2.5V, R_L = 1MΩ



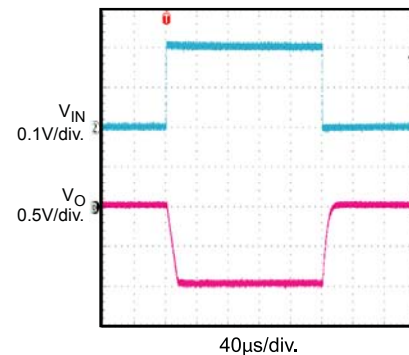
Small Signal Pulse Response

A_V = 2, V₊ = V₋ = 2.5V, R_L = 1MΩ



Small Signal Pulse Response

A_V = -5, V₊ = V₋ = 12V, R_L = 1MΩ

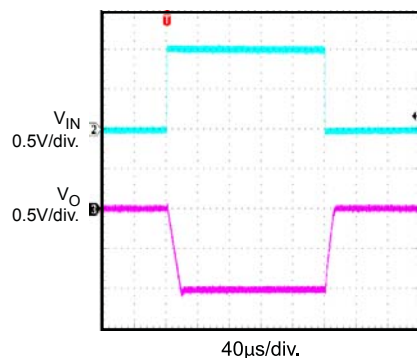


TYPICAL PERFORMANCE CHARACTERISTICS

$C1 = C3 = 0.1\mu\text{F}$, $C2 = C4 = 10\mu\text{F}$, $R_L = 1\text{M}\Omega$ (Reference Figure 3)

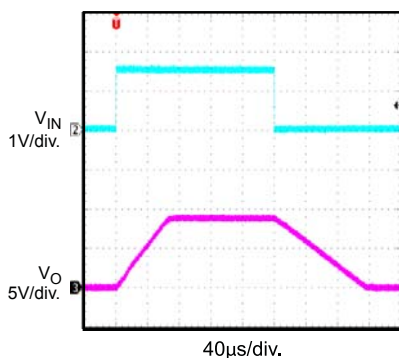
Large Signal Pulse Response

$A_V = -1$, $V_+ = V_- = 2.5\text{V}$, $R_L = 1\text{M}\Omega$



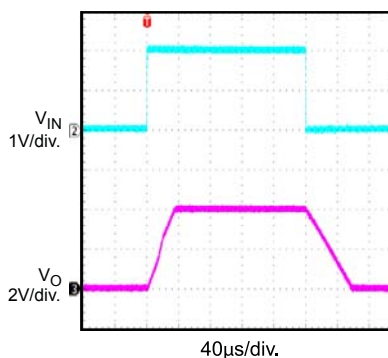
Large Signal Pulse Response

$A_V = 6$, $V_+ = V_- = 12\text{V}$, $R_L = 1\text{M}\Omega$



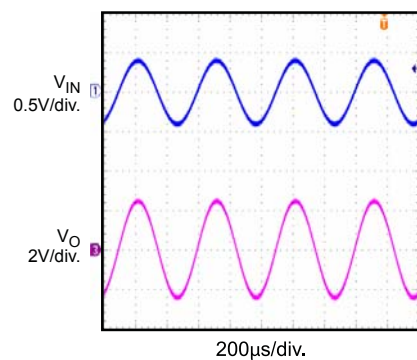
Large Signal Pulse Response

$A_V = 2$, $V_+ = V_- = 5\text{V}$, $R_L = 1\text{M}\Omega$



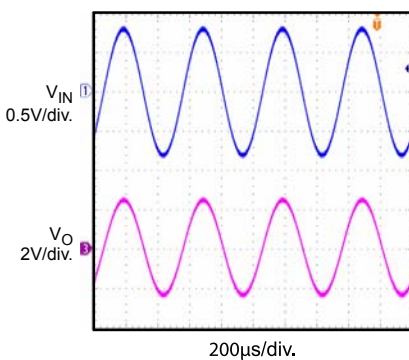
Rail to Rail Output Operation

$A_V = 6$, $V_+ = V_- = 2.5\text{V}$, $R_L = 1\text{M}\Omega$



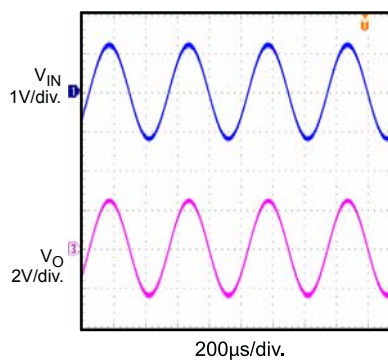
Rail to Rail Output Operation

$A_V = 3$, $V_+ = V_- = 2.5\text{V}$, $R_L = 1\text{M}\Omega$



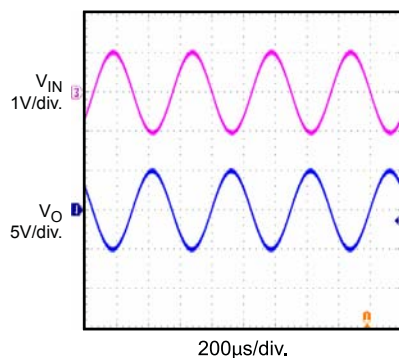
Rail to Rail Output Operation

$A_V = 2$, $V_+ = V_- = 2.5\text{V}$, $R_L = 1\text{M}\Omega$



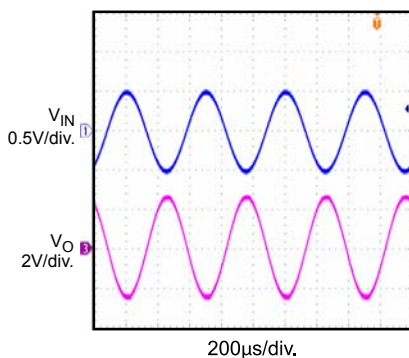
Rail to Rail Output Operation

$A_V = -5$, $V_+ = V_- = 5\text{V}$, $R_L = 1\text{M}\Omega$



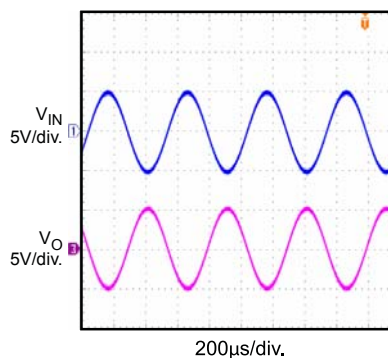
Rail to Rail Output Operation

$A_V = -5$, $V_+ = V_- = 2.5\text{V}$, $R_L = 1\text{M}\Omega$



Rail to Rail Output Operation

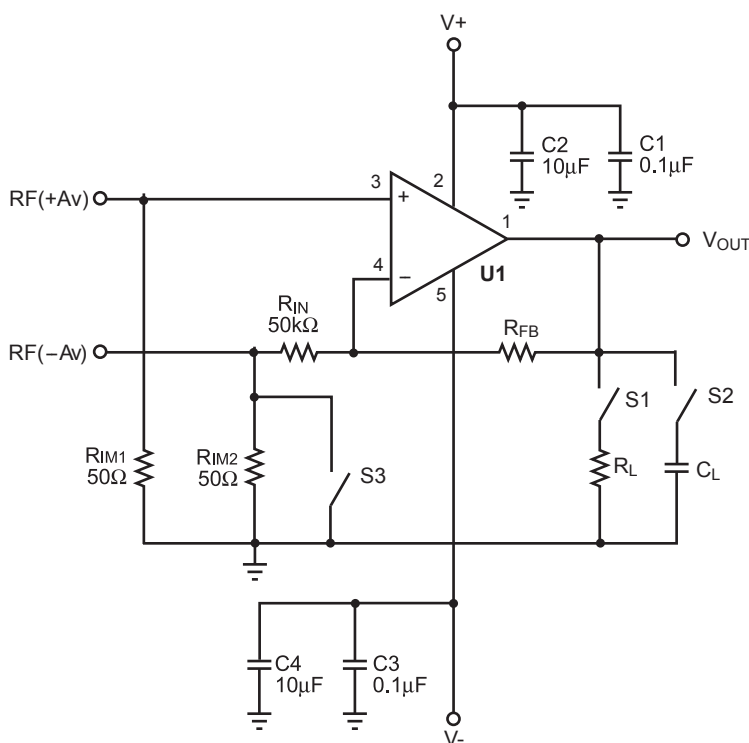
$A_V = -1$, $V_+ = V_- = 5\text{V}$, $R_L = 1\text{M}\Omega$



PIN FUNCTIONS

Pin #	Name	Description
1	OUT	Output.
2	V+	Supply Voltage.
3	IN+	Non-Inverting Input.
4	IN-	Inverting Input.
5	V-	Ground or Supply Return Pin.

TEST CIRCUITS



Notes: Close S3 for positive gain. Input signal to RF(+Av) connector.
 The gain $A_v = 1 + R_{FB}/R_{IN}$.
 For unity gain, remove R_{IN} and short R_{FB} .
 Open S3 for negative gain. Input signal to RF(-Av) connector.
 The gain $A_v = -R_{FB}/R_{IN}$.
 S1 and S2 are switches for possible resistor and capacitor load connections.

Figure 1—AC Test Circuit

TEST CIRCUITS *(continued)*

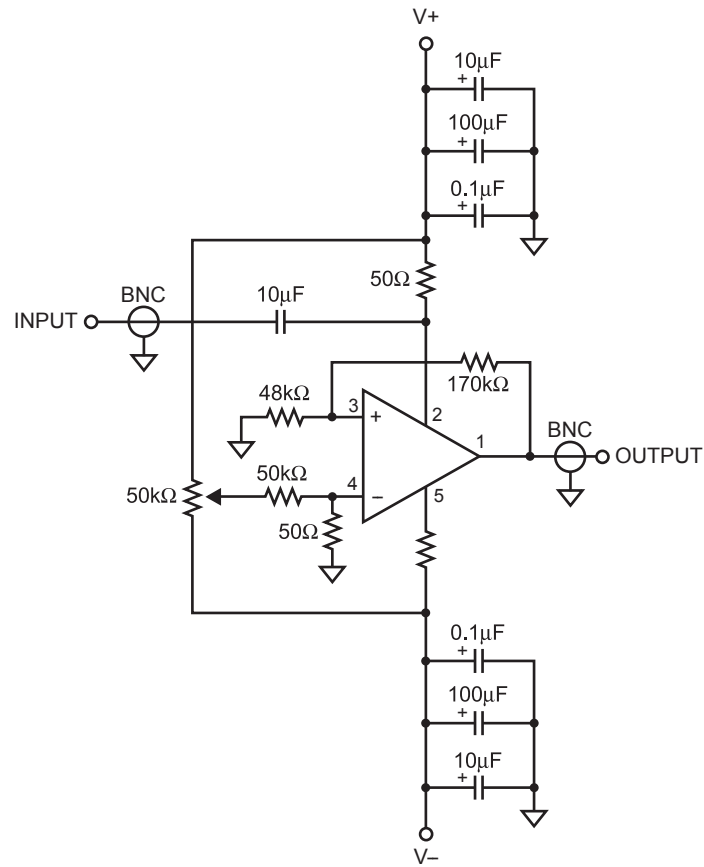


Figure 2—Positive Power Supply Rejection Ratio Measurement

APPLICATION INFORMATION

Power Supply Bypassing

Regular supply bypassing techniques are recommended. A $10\mu\text{F}$ capacitor in parallel with a $0.1\mu\text{F}$ capacitor on both the positive and negative supplies is ideal. For the best performance, all bypassing capacitors should be located as close to the op amp as possible and all capacitors should be low ESL (Equivalent Series Inductance) and low ESR

(Equivalent Series Resistance). Surface mount ceramic capacitors are ideal.

For large input signals, the op amp needs two clamp diodes to the input side. (See Figure 3 Large Input Signal Schematic).

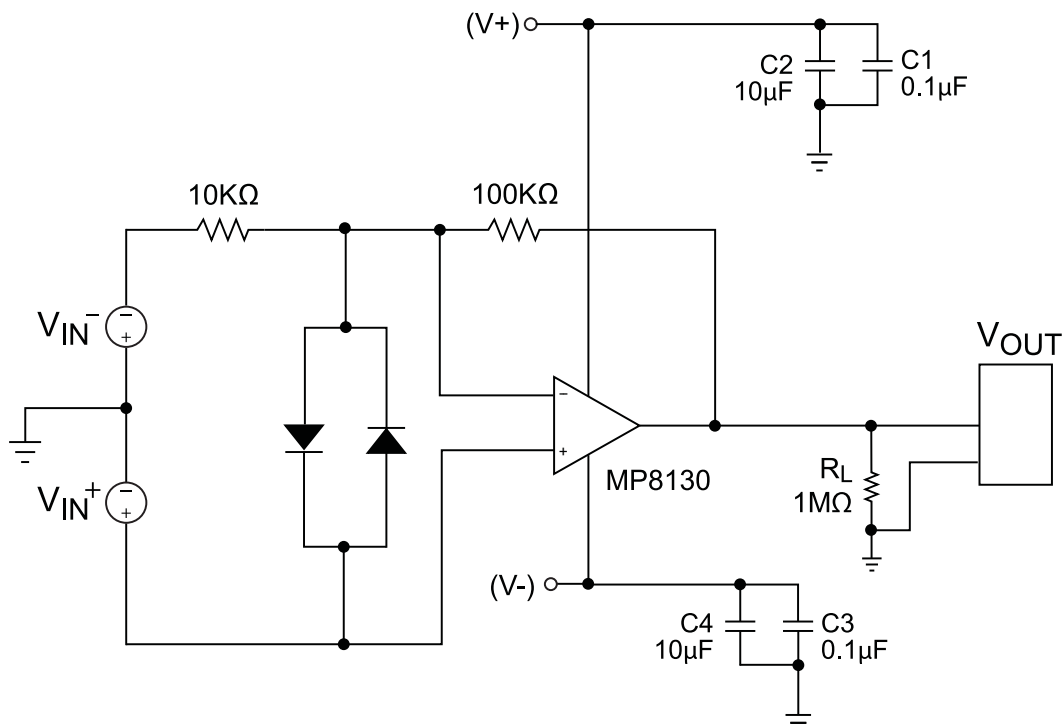
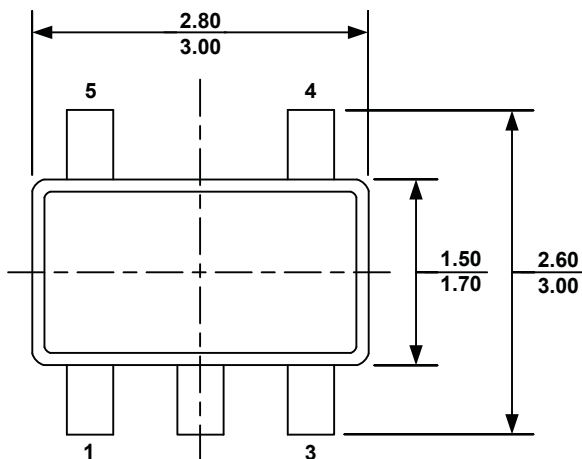


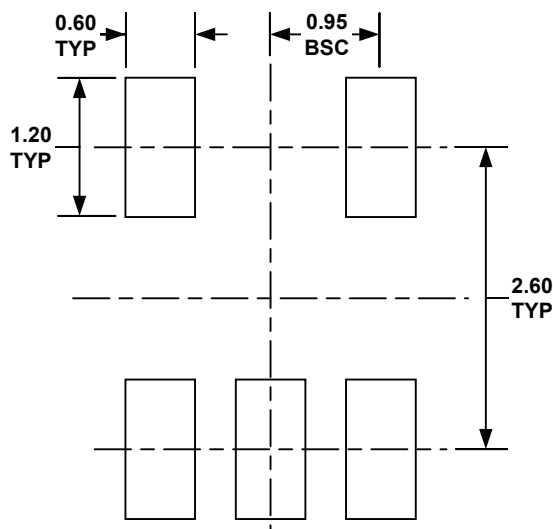
Figure 3—Large Input Signal Schematic

PACKAGE INFORMATION

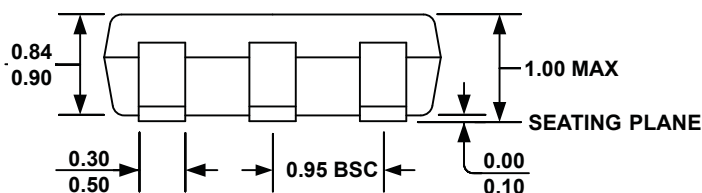
TSOT23-5



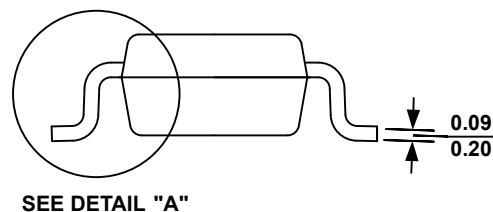
TOP VIEW



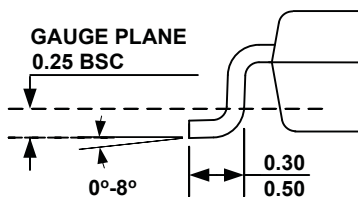
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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