MP8854

2.85V - 18V, 4A, High-Efficiency, Wide-Input, Synchronous, Step-Down Converter with Integrated Telemetry via I²C Interface

DESCRIPTION

The MP8854 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with an I²C control interface. The MP8854 offers a fully integrated solution that achieves 4A of continuous output current with excellent load and line regulation over a wide input voltage supply range.

The output voltage level can be controlled on-the-fly through an I²C serial interface. The reference voltage range can be adjusted from 0.6V to 1.108V in 4mV steps. The voltage slew rate, frequency, current limit, hiccup/latch-off protection, enable, and power-save mode (PSM) are also selectable through the I²C interface.

Constant-on-time (COT) control operation provides fast transient response. An open-drain power good (PG) pin indicates that the output voltage is in the nominal range. Full protection features include over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

The MP8854 is available in a QFN-14 (3mmx4mm) package.

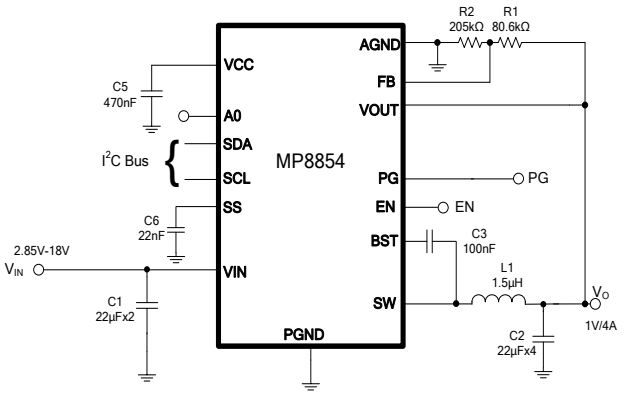
FEATURES

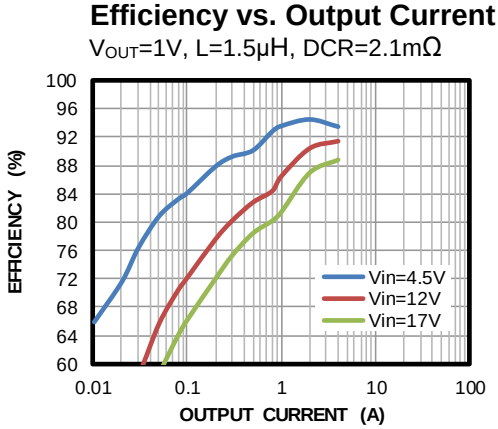
- Wide 2.85V to 18V Operating Input Range
- 4A Continuous Output Current
- 1% Internal Reference Accuracy
- I²C Programmable Reference Range from 0.6V to 1.108V in 4mV Steps with Slew Rate Control
- 5% Accuracy Output Voltage and Output Current Monitoring via I²C
- Selectable PFM/PWM Mode, Adjustable Frequency and Current Limit through I²C
- Four Different Selectable I²C Addresses
- External Soft Start (SS)
- Open-Drain Power Good (PG) Indication
- Output Over-Voltage Protection (OVP)
- Hiccup/Latch-Off Over-Current Protection (OCP)
- VOUT Adjustable up to 5.5V using FB pin
- Available in a QFN-14 (3mmx4mm) Package

APPLICATIONS

- Solid-State Drives (SSD)
- Flat-Panel Televisions and Monitors
- Digital Set-Top Boxes
- Distributed Power Systems
- Networking/Servers

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number	Package	Top Marking
MP8854GL*	QFN-14 (3mmx4mm)	*See Below*
EVKT-MP8854	Evaluation Kit	

* For Tape & Reel, add suffix –Z (e.g. MP8854GL–Z)

TOP MARKING

MPYW
8854
LLL

MP: MPS prefix
Y: Year code
W: Week code
8854: First four digits of the part number
LLL: Lot number

EVALUATION KIT EVKT-MP8854

EVKT-MP8854 Kit contents: (Items can be ordered separately).

#	Part Number	Item	Quantity
1	EV8854-L-00A	MP8854GL evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I2C communication interface device, one USB Cable, and one Ribbon Cable	1

Order direct from MonolithicPower.com or our distributors

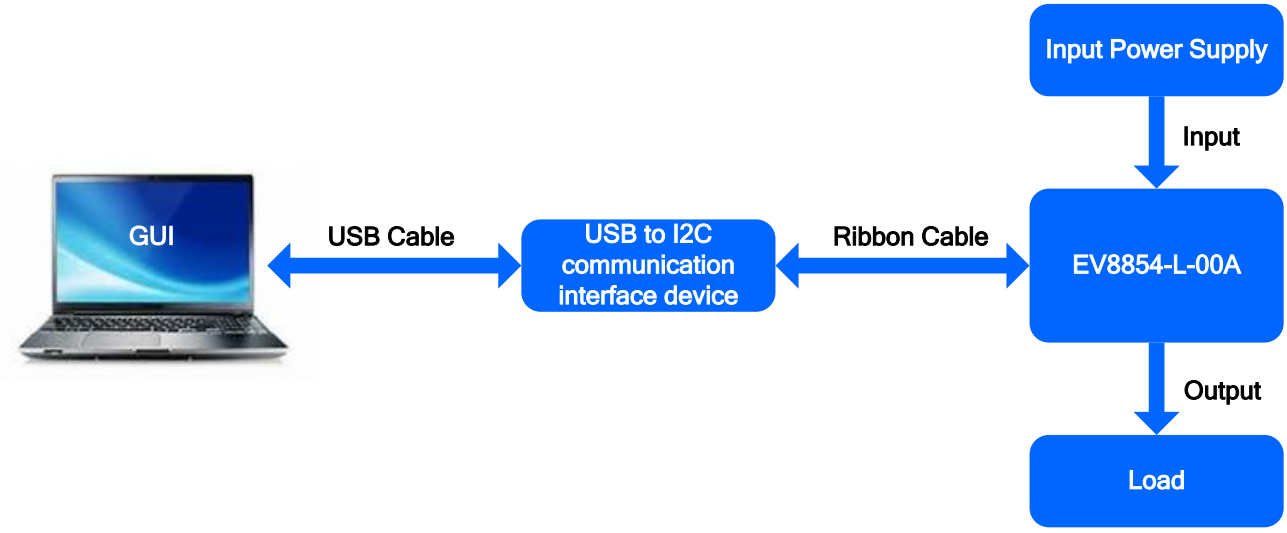
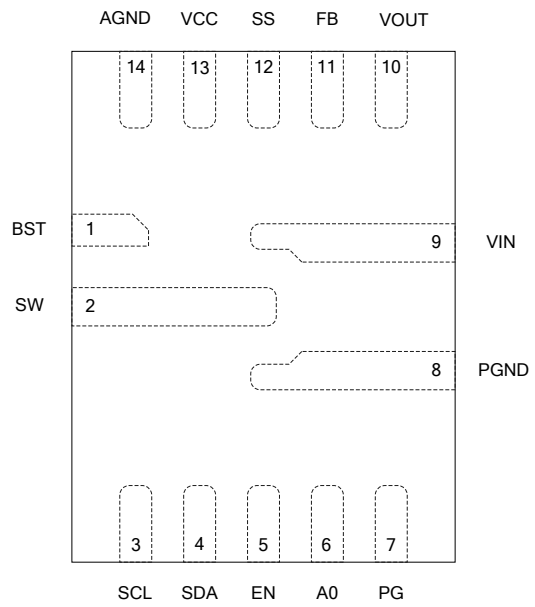


Figure 1. EVKT-MP8854 Evaluation Kit Setup

PACKAGE REFERENCE

TOP VIEW



QFN-14 (3mmx4mm)

PIN FUNCTIONS

QFN-14 Pin#	Name	Description
1	BST	**Bootstrap.** A capacitor is required between SW and BST to form a floating supply across the high-side switch driver.
2	SW	**Switch output.** Connect SW using a wide PCB trace.
3	SCL	**I²C serial clock.**
4	SDA	**I²C serial data.**
5	EN	**Enable.** Set EN high to enable the MP8854. EN has a 1.5MΩ internal pull-down resistor to GND. EN is a high-voltage pin, so it can be connected to VIN directly for automatic start-up.
6	A0	**I²C address set-up.** Connect a resistor divider from VCC to A0 to set different I²C addresses.
7	PG	**Power good indication.** PG is an open-drain structure. PG is de-asserted if the output voltage is out of the regulation window.
8	PGND	**System power ground.** PGND is the reference ground of the regulated output voltage and requires special consideration during PCB layout. Connect PGND to the ground plane with copper traces and vias.
9	VIN	**Supply voltage.** The MP8854 operates from a 2.85V to 18V input rail. Decouple the input rail with a ceramic capacitor. Connect VIN using a wide PCB trace.
10	VOUT	**Output voltage sense.** Connect VOUT to the positive terminal of the load.
11	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage.
12	SS	**Soft start set-up.** Connect a capacitor from SS to ground to set the soft-start time.
13	VCC	**Internal LDO regulator output.** Decouple VCC with a 0.47µF capacitor.
14	AGND	**Signal ground.** If AGND is not connected to PGND internally, ensure that AGND is connected to PGND in the PCB layout.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to 19V
V_{SW} .....-0.6V (-7V for <10ns) to VIN + 0.7V (25V for <25ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} 18V
V_{OUT} 7V
All other pins .....-0.3V to 4V
Continuous power dissipation (T_A = +25°C) (2)
QFN-14 (3mmx4mm) 2.5W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.85V to 18V
Output voltage (V_{OUT}) .....0.6V to 5.5V
Operating junction temp. (T_J) -40°C to+125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-14 (3mmx4mm)			
EV8854-L-00A(4)	22	4	°C/W
JESD51-7(5)	130	60	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV8854-L-00A, 4 Layer PCB, 85mm x 85mm.
5) The value of θJA given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

VIN = 12V, T_J = -40°C to +125°C (5), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		2.1	4	μA
Supply current (quiescent)	I_q	No switching, FB = 105% V_{REF}, PFM mode		420	600	μA
HS switch on resistance	$HS_{RDS(ON)}$	V_{BST} - $_{SW}$ = 3.3V		50		mΩ
LS switch on resistance	$LS_{RDS(ON)}$	VCC = 3.3V		20		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V, T_J = +25°C			1	μA
Low-side valley current limit	I_{LIMIT_L}	Adjustable by I^2C	5.5			A
Low-side negative current limit	I_{LIMIT_LN}	In forced PWM mode or OVP state		-3		A
Low-side ZCD threshold	I_{ZCD}	T_J = +25°C		200		mA
Switching frequency	f_{SW1}	VIN = 12V, V_{OUT} = 1V	400	500	600	kHz
	f_{SW2}	VIN = 12V, V_{OUT} = 5V	400	500	600	kHz
Minimum off time (6)	T_{OFF_MIN}			185		ns
Minimum on time (6)	T_{ON_MIN}	VOUT = 0.6V		50		ns
Reference voltage	V_{ref}	T_J = 25°C	-1%	720	+1%	mV
		-40°C < T_J < 125°C (5)	-1.5%	720	+1.5%	
FB current	I_{FB}	V_{FB} = 740mV		10	50	nA
A0 voltage threshold 1	V_{ADD_1}	Set I^2C address 61H			0.24	VCC
A0 voltage threshold 2	V_{ADD_2}	Set I^2C address 63H	0.28		0.49	VCC
A0 voltage threshold 3	V_{ADD_3}	Set I^2C address 65H	0.53		0.72	VCC
A0 voltage threshold 4	V_{ADD_4}	Set I^2C address 67H	0.77			VCC
A0 to GND pull-down resistor	R_{A0_PD}			2		MΩ
EN rising threshold	V_{EN_RISING}		1.1	1.2	1.3	V
EN threshold hysteresis	V_{EN_HYS}			110		mV
EN to GND pull-down resistor	R_{EN}			1.5		MΩ
VIN under-voltage lockout threshold rising	$INUV_{Vth\_r}$		2.45	2.65	2.85	V
VIN under-voltage lockout threshold falling	$INUV_{Vth\_f}$			2.5	2.7	V
Power good UV threshold rising	PGVth-Hi	Good	0.86	0.9	0.94	VOUT
Power good UV threshold falling	PGVth-Lo	Fault	0.81	0.85	0.89	VOUT
Power good OV threshold rising	PGVth-Hi	Fault	1.11	1.15	1.19	VOUT
Power good OV threshold falling	PGVth-Lo	Good	1.01	1.05	1.09	VOUT
Power good deglitch time	PGTd	I^2C programmable		30		μs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V

ELECTRICAL CHARACTERISTICS *(continued)*

VIN = 12V, T_J = -40°C to +125°C (5), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
OVP rising threshold	V_{OVP_Rise}	FB	121%	125%	129%	V_{REF}
OVP falling threshold	$V_{OVP\_Falling}$	FB	106%	110%	114%	V_{REF}
OVP delay	T_{OVP}			3.7		µs
Output pin absolute OV	V_{OVP2}		6	6.5	7	V
UVP threshold	$V_{FB\_UV\_th}$	Hiccup entry	55%	60%	65%	V_{REF}
UVP delay (6)	T_{UVP}			10		µs
Soft-start current	I_{SS}		5	7	9	µA
VCC voltage	V_{CC}			3.5		V
VCC load regulation	V_{CC_reg}	I_{CC} = 20mA			3	%
Thermal shutdown (6)	T_{TSD}			160		°C
Thermal hysteresis (6)	T_{TSD_HYS}			20		°C

NOTES:

5) Not tested in production and guaranteed by over-temperature correlation.

6) Guaranteed by design and characterization test.

I/O LEVEL CHARACTERISTICS

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Low-level input voltage	V_{IL}		-0.5	$0.3V_{CC}$	-0.5	$0.3V_{CC}$	V
High-level input voltage	V_{IH}		$0.7V_{CC}$	V_{CC} + 0.5	$0.7V_{CC}$	V_{CC} + 0.5	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	V_{CC} > 2V	$0.05V_{CC}$	-	$0.05V_{CC}$	-	V
		V_{CC} < 2V	$0.1V_{CC}$	-	$0.1V_{CC}$	-	
Low-level output voltage (open drain) at 3mA sink current	V_{OL}	V_{CC} > 2V	0	0.4	0	0.4	V
		V_{CC} < 2V	0	$0.2V_{CC}$	0	$0.2V_{CC}$	
Low-level output current	I_{OL}		-	3	-	3	mA
Transfer gate on resistance for currents between SDA and SCAH, or SCL and SCLH	R_{onL}	VOL level, IOL = 3mA	-	50	-	50	Ω
Transfer gate on resistance between SDA and SCAH, or SCL and SCLH	R_{onH}	Both signals (SDA and SDAH, or SCL and SCLH) at V_{CC} level	50	-	50	-	kΩ
Pull-up current of the SCLH current source	I_{cs}	SCLH output levels between 0.3Vcc and $0.7V_{CC}$	2	6	2	6	mA
Rise time of the SCLH or SCL signal	T_{rCL}	Output rise time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80			ns
Fall time of the SCLH or SCL signal	T_{fCL}	Output fall time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80	20	250	ns
Rise time of SDAH signal	T_{rDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
Fall time of SDAH signal	T_{fDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	10	0	50	ns
Input current each I/O pin	I_i	Input voltage between $0.1V_{CC}$ and $0.9V_{CC}$	-	10	-10	+10	µA
Capacitance for each I/O pin	C_i		-	10	-	10	pF

I²C PORT SIGNAL CHARACTERISTICS

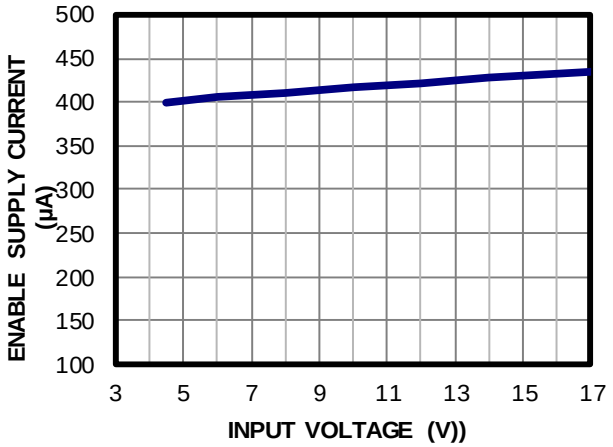
Parameter	Symbol	Condition	Cb = 100pF		Cb = 400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start condition	$T_{SU;STA}$		160	-	600	-	ns
Hold time (repeated) start condition	$T_{HD;STA}$		160	-	600	-	ns
Low period of the SCL clock	T_{LOW}		160	-	1300	-	ns
High period of the SCL clock	T_{HIGH}		60	-	600	-	ns
Data set-up time	$T_{SU:DAT}$		10	-	100	-	ns
Data hold time	$T_{HD;DAT}$		0	70	0	-	ns
Rise time of SCLH signal	T_{rCL}		10	40	20*0.1Cb	300	ns
Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	T_{fCL1}		10	80	20*0.1Cb	300	ns
Fall time of SCLH signal	T_{fCL}		10	40	20*0.1Cb	300	ns
Rise time of SDAH signal	T_{fDA}		10	80	20*0.1Cb	300	ns
Fall time of SDAH signal	T_{fDA}		10	80	20*0.1Cb	300	ns
Set-up time for stop condition	$T_{SU;STO}$		160	-	600	-	ns
Bus free time between a stop and start condition	T_{BUF}		160	-	1300	-	ns
Data valid time	$T_{VD;DAT}$		-	16	-	90	ns
Data valid acknowledge time	$T_{VD;ACK}$		-	160	-	900	ns
Capacitive load for each bus line	C_b	SDAH and SCLH line	-	100	-	400	pF
		SDAH + SDA line and SCLH + SCL line	-	400	-	400	pF
Noise margin at the low level	C_i	For each connected device	-	$0.1V_{CC}$	$0.1V_{CC}$	-	V
Noise margin at the high level	V_{nH}	For each connected device	-	$0.2V_{CC}$	$0.2V_{CC}$	-	V

NOTE:
V_{CC} is the I²C bus voltage, in the 1.8V to 3.6V range, and used for 1.8V, 2.5V, and 3.3V bus voltages.

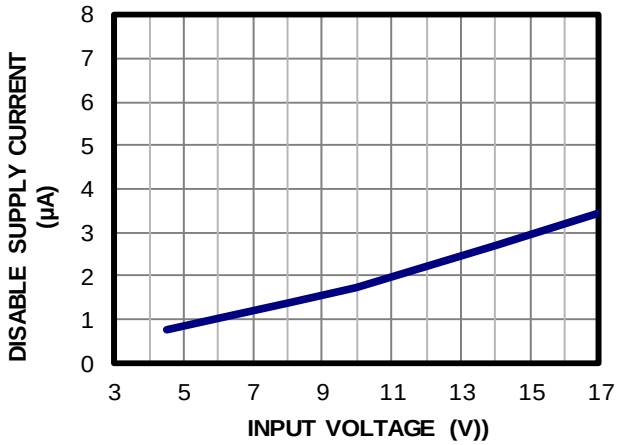
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board.
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

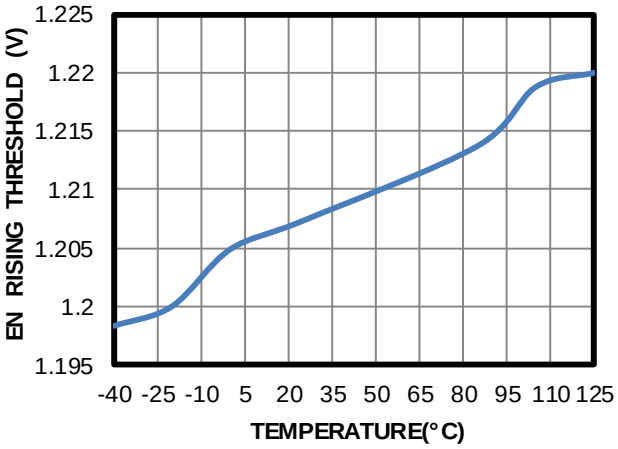
Enabled Supply Current vs. Input Voltage



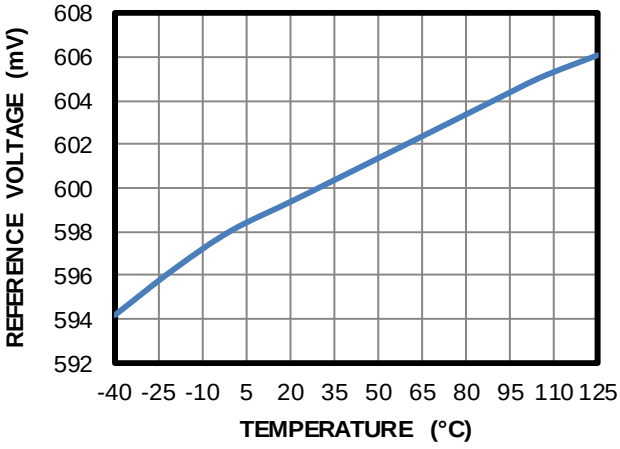
Disabled Supply Current vs. Input Voltage



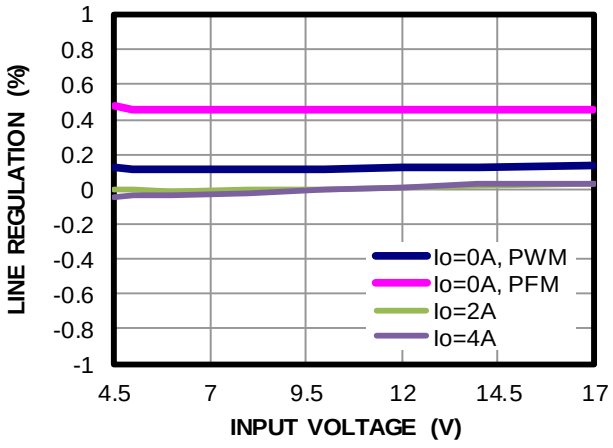
EN Rising Threshold vs. Temperature



Reference Voltage vs. Temperature

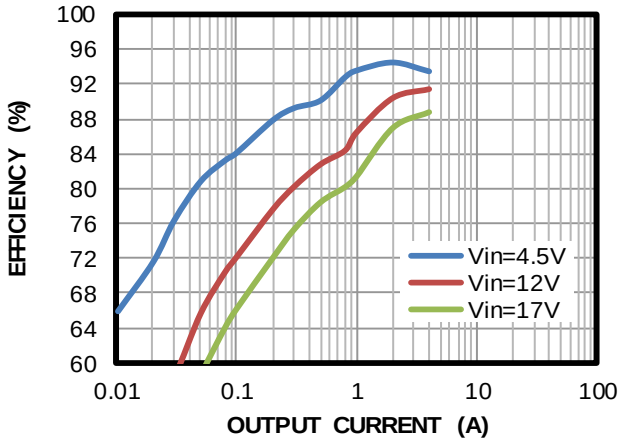


Line Regulation vs. Input Voltage



Efficiency vs. Output Current

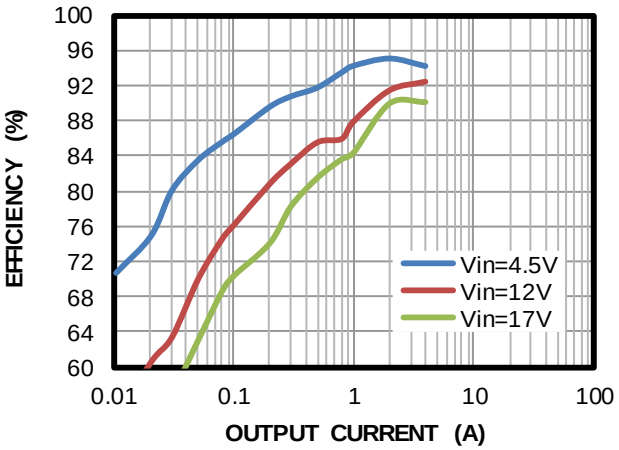
V_{OUT}=1V, L=1.5µH, DCR=2.1mΩ



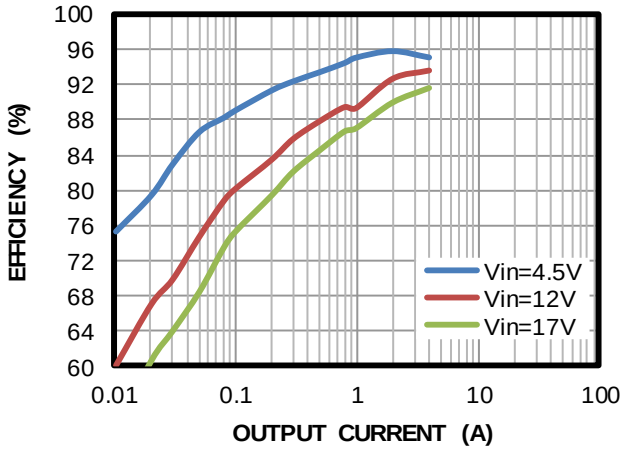
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

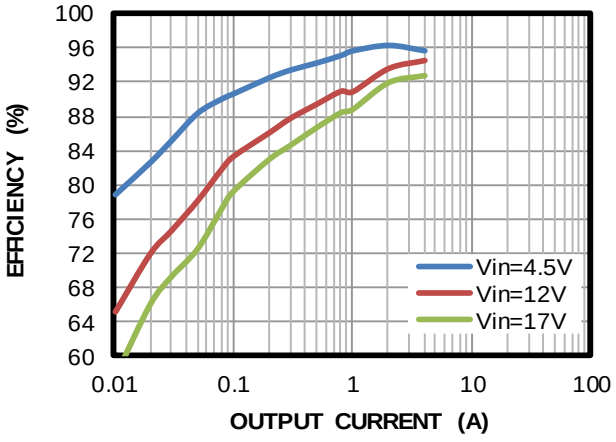
Efficiency vs. Output Current
V_{OUT}=1.2V, L=1.5µH, DCR=2.1mΩ



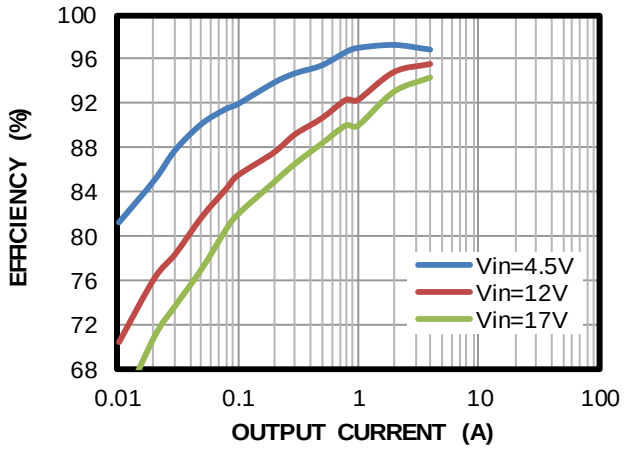
Efficiency vs. Output Current
V_{OUT}=1.5V, L=1.5µH, DCR=2.1mΩ



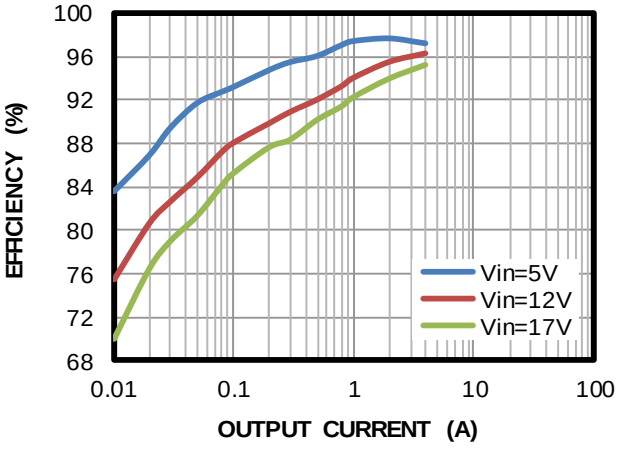
Efficiency vs. Output Current
V_{OUT}=1.8V, L=1.5µH, DCR=2.1mΩ



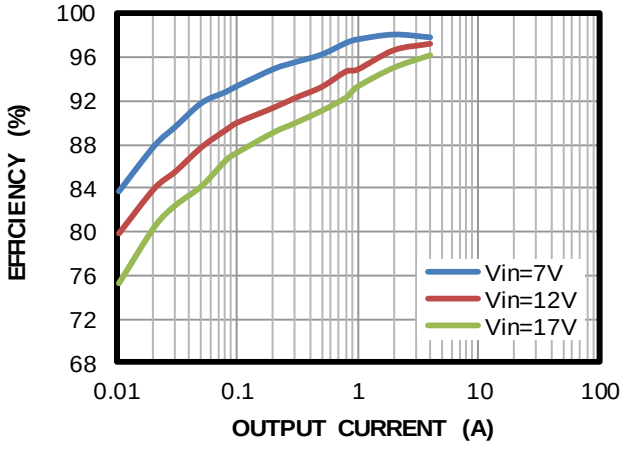
Efficiency vs. Output Current
V_{OUT}=2.5V, L=2.2µH, DCR=3mΩ



Efficiency vs. Output Current
V_{OUT}=3.3V, L=2.2µH, DCR=3mΩ



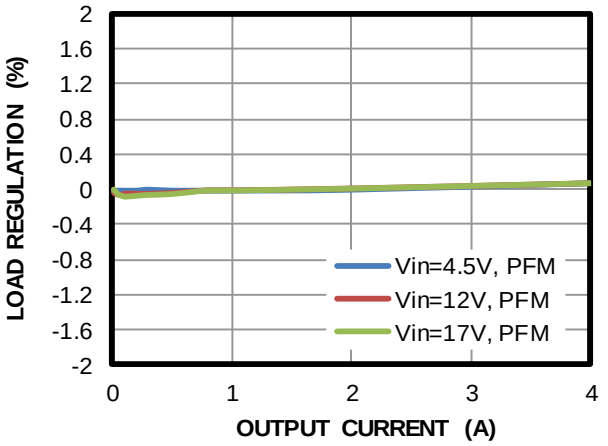
Efficiency vs. Output Current
V_{OUT}=5V, L=3.3µH, DCR=4..4mΩ



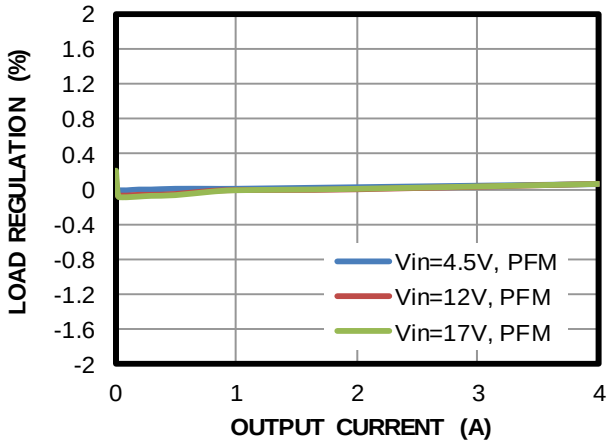
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

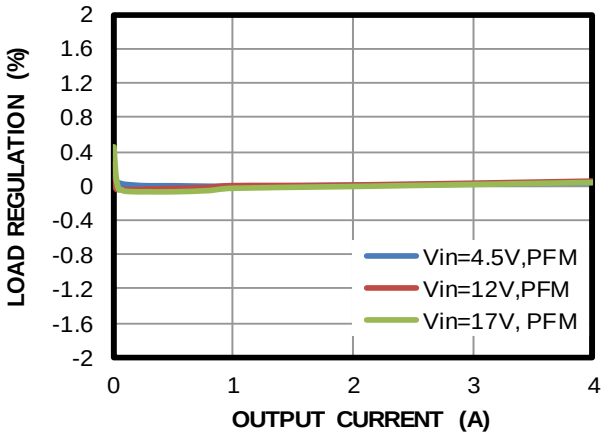
Load Regulation vs. Output Current
V_{OUT}=1V, PFM Mode



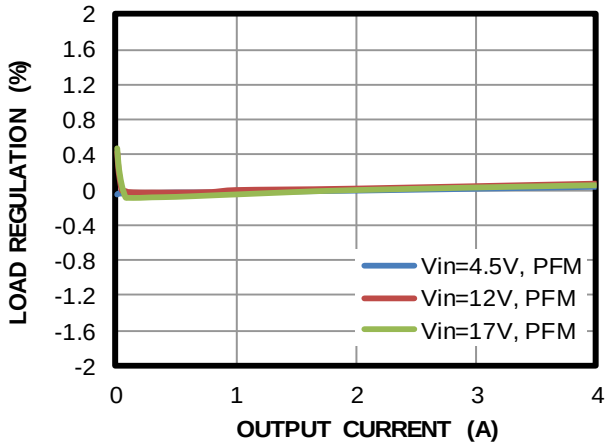
Load Regulation vs. Output Current
V_{OUT}=1.2V, PFM Mode



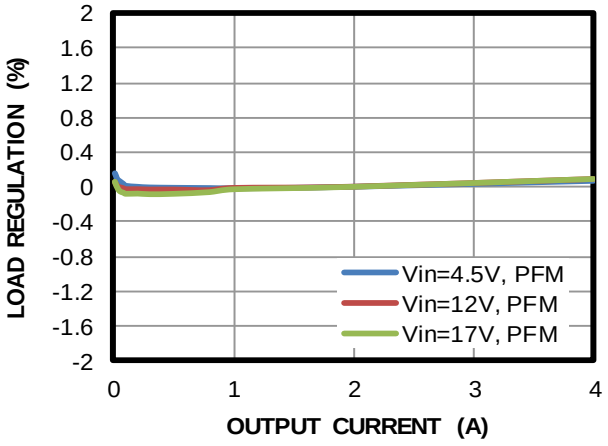
Load Regulation vs. Output Current
V_{OUT}=1.5V, PFM Mode



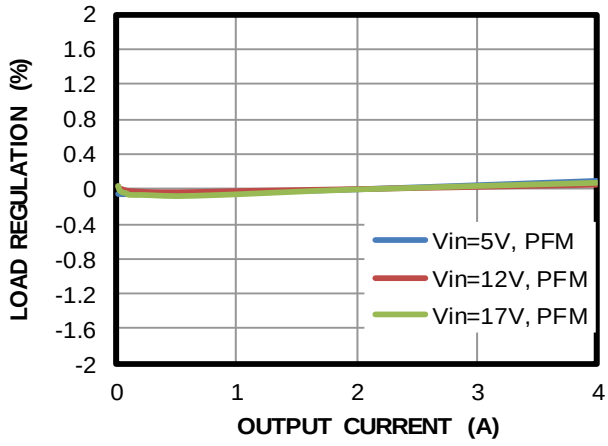
Load Regulation vs. Output Current
V_{OUT}=1.8V, PFM Mode



Load Regulation vs. Output Current
V_{OUT}=2.5V, PFM Mode



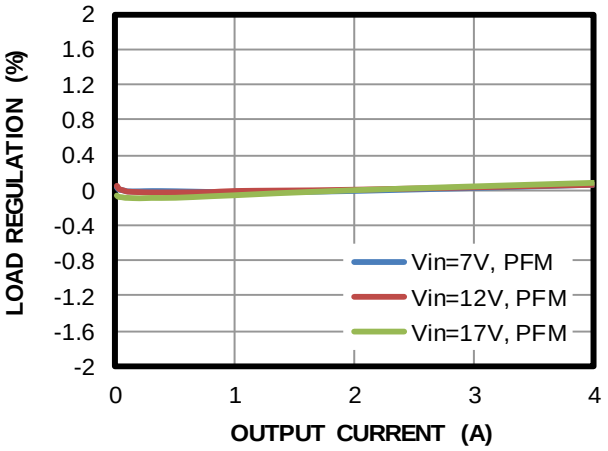
Load Regulation vs. Output Current
V_{OUT}=3.3V, PFM Mode



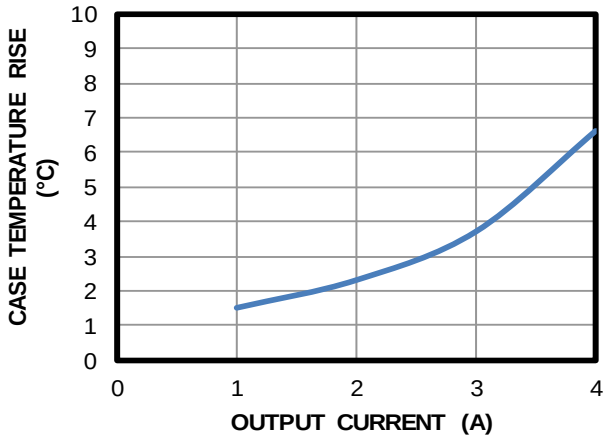
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.
VIN = 12V, VOUT = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

Load Regulation vs. Output Current
V_{OUT}=5V, PFM Mode



Case Temperature Rise vs. Output Current

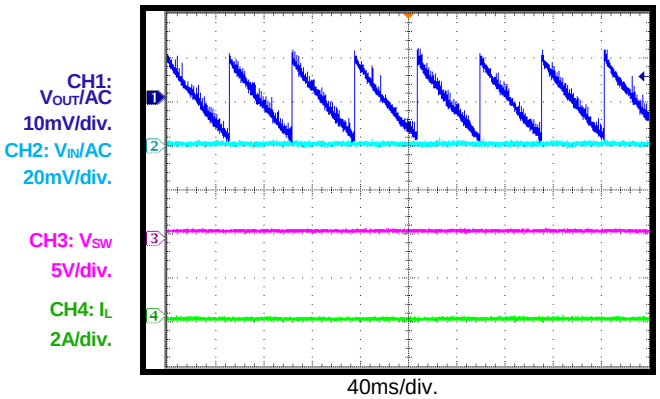


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.
VIN = 12V, VOUT = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

Input/Output Ripple

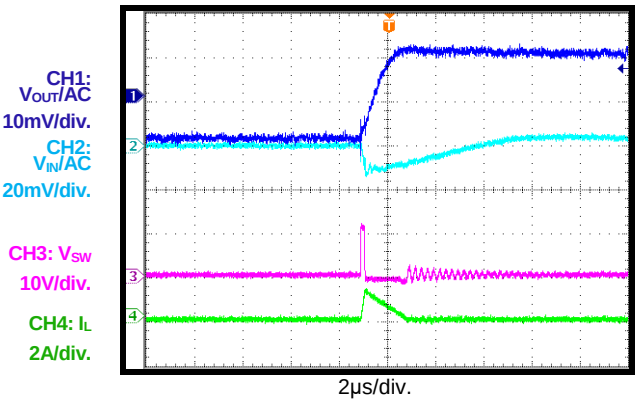
I_{OUT}=0A



40ms/div.

Input/Output Ripple

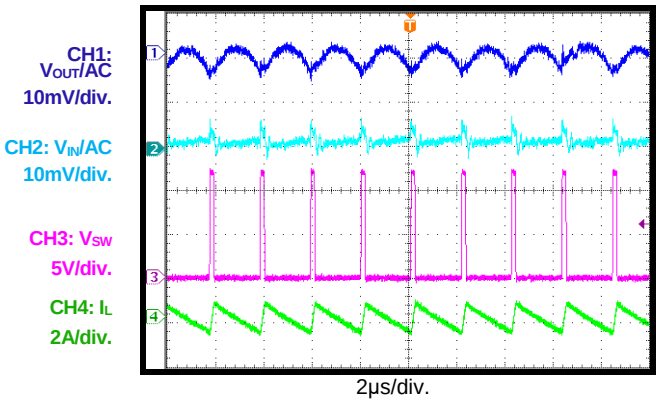
I_{OUT}=0A



2µs/div.

Input/Output Ripple

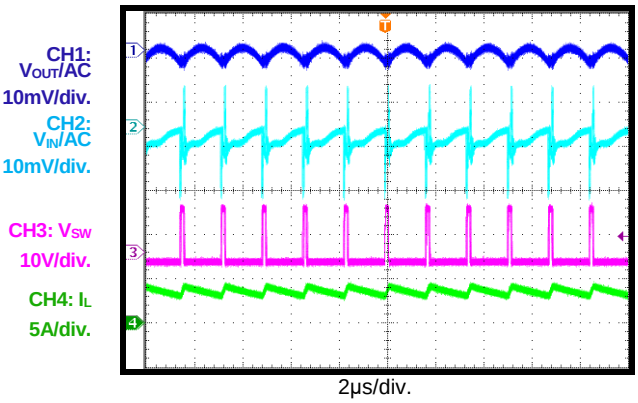
I_{OUT}=0A, Force PWM



2µs/div.

Input/Output Ripple

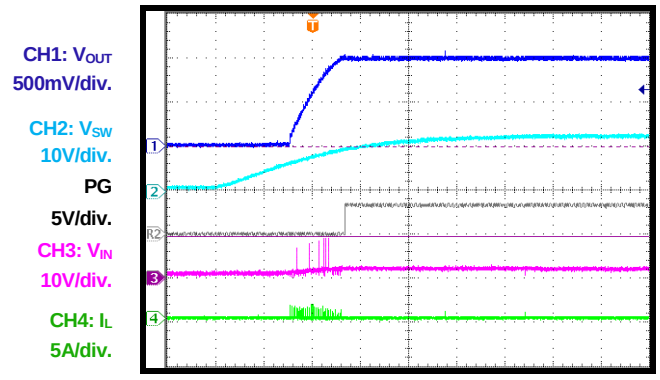
I_{OUT}=4A



2µs/div.

Start-Up through Input Voltage

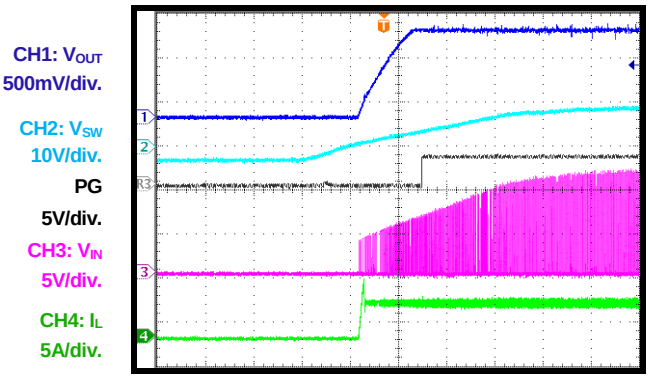
I_{OUT}=0A



2ms/div.

Start-Up through Input Voltage

I_{OUT}=4A



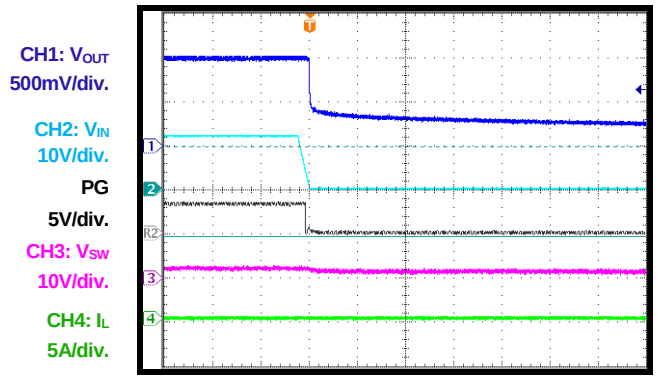
2ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.
VIN = 12V, VOUT = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

Shutdown through Input Voltage

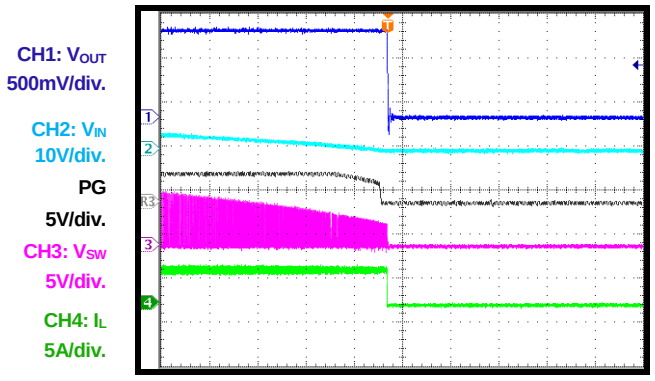
I_{OUT}=0A



400ms/div.

Shutdown through Input Voltage

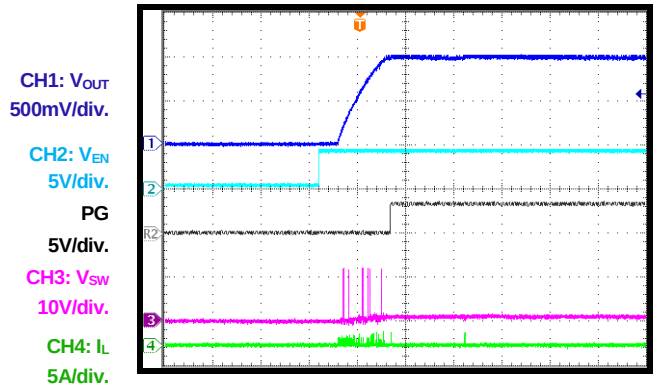
I_{OUT}=4A



1ms/div.

Start-Up through EN

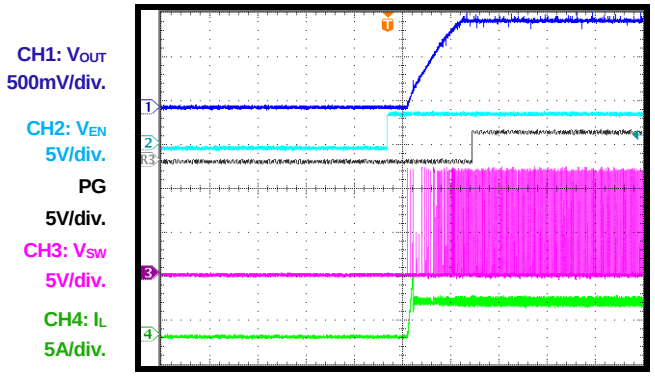
I_{OUT}=0A



2ms/div.

Start-Up through EN

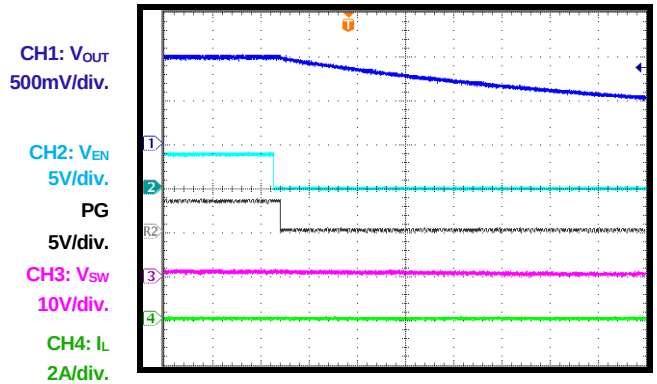
I_{OUT}=4A



2ms/div.

Shutdown through EN

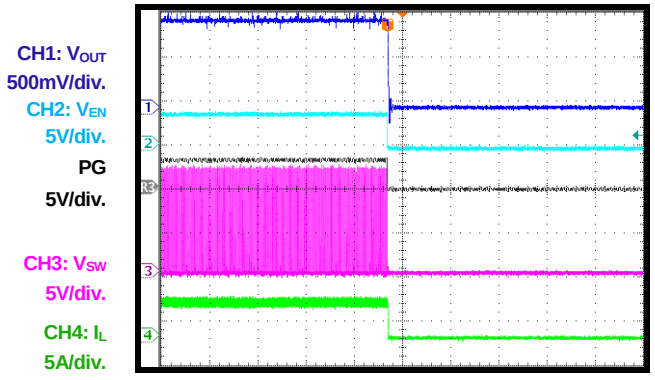
I_{OUT}=0A



1s/div.

Shutdown through EN

I_{OUT}=4A



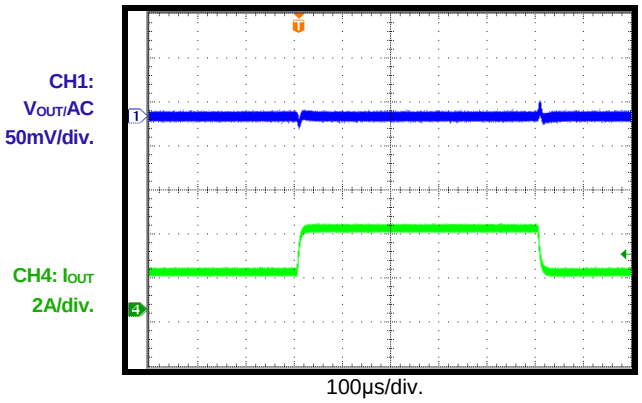
1ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

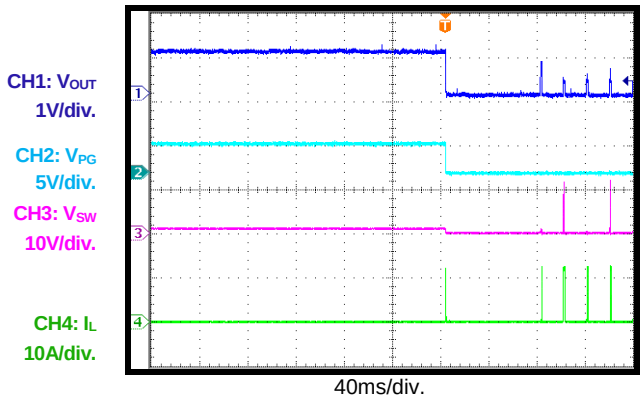
Performance waveforms are tested on the evaluation board.
VIN = 12V, VOUT = 1V, L = 1.5µH, F_S = 500kHz, auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

Load Transient

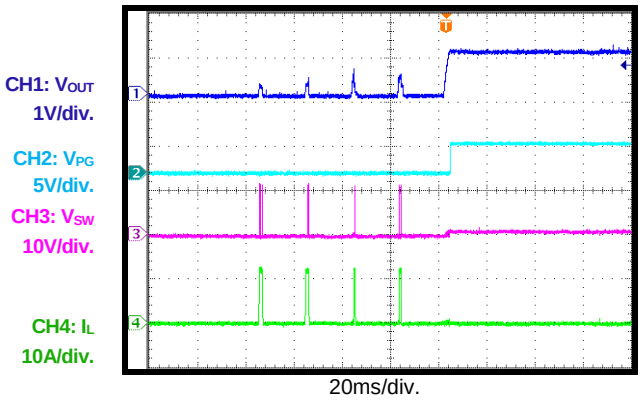
I_{OUT}=2A-4A



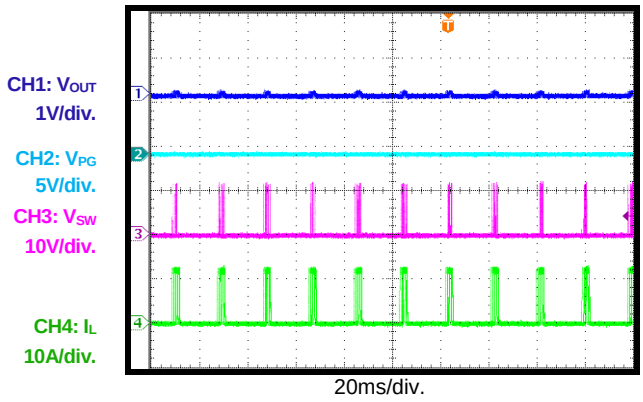
Short-Circuit Protection Entry



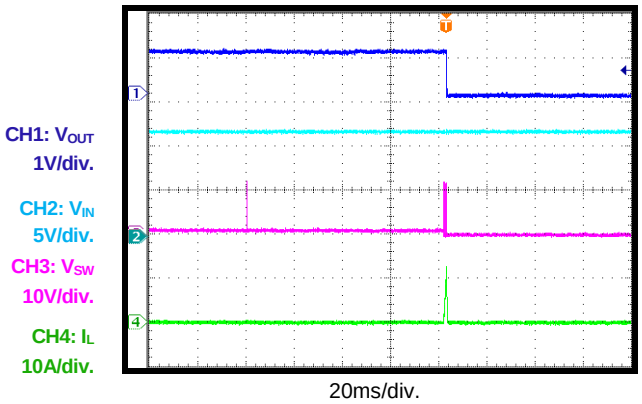
Short-Circuit Protection Recovery



Short-Circuit Protection Steady State



Latch Off



BLOCK DIAGRAM

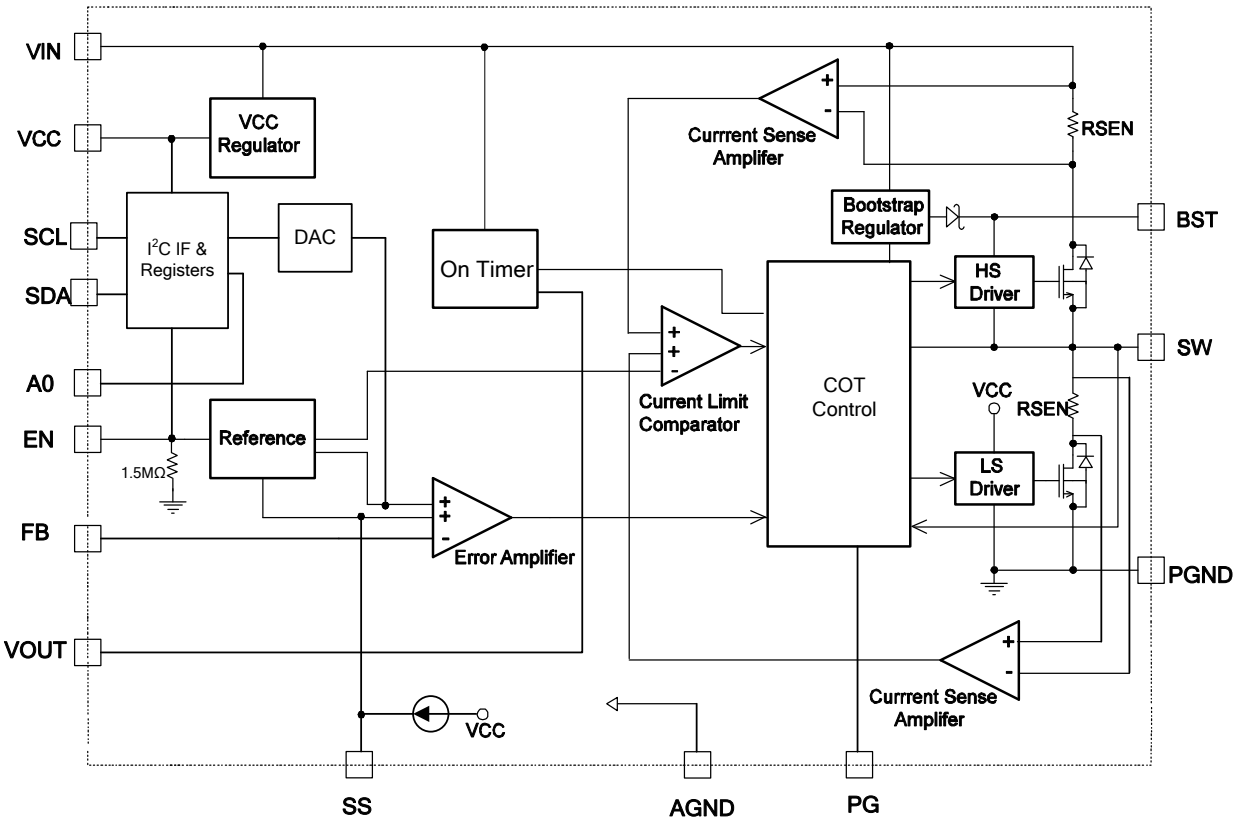


Figure 2: Functional Block Diagram

OPERATION

Pulse-Width Modulation (PWM) Operation

The MP8854 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. The MP8854 uses constant-on-time (COT) control to provide fast transient response and ease loop stabilization. Figure 3 shows the simplified ramp compensation block.

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage (V_{Ramp}) is lower than the error amplifier output voltage (V_{EAO}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET enters the off state. By cycling the HS-FET on and off, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss.

Shoot-through occurs when both the HS-FET and LS-FET are turned on at the same time, causing a dead short between the input and GND and reducing efficiency dramatically. The MP8854 prevents shoot-through by generating a dead time (DT) internally between the HS-FET off and LS-FET on period and the LS-FET off and HS-FET on period. The MP8854 enters either heavy-load operation or light-load operation depending on the amplitude of the output current.

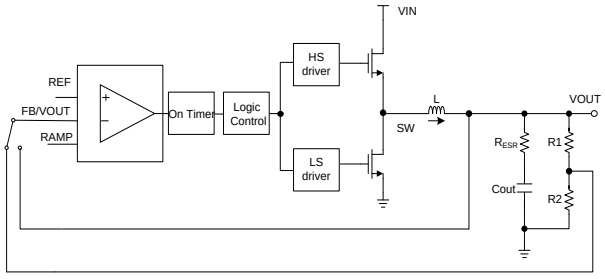


Figure 3: Simplified Compensation Block

Switching Frequency

The MP8854 uses constant-on-time (COT) control, so there is no dedicated oscillator in the IC. The input voltage is fed into the one-shot on-timer through the internal frequency resistor. The duty ratio is VOUT/VIN, and the switching frequency is fairly constant over the input voltage range. The MP8854's switching frequency can be adjusted by setting the two bits D[5:4] in register 02 through the I^2C communication. When the output voltage setting is low and the input voltage is high, the switching on-time may be limited by the internal minimum on-time limit, and the switching frequency decreases. Table 1 shows the maximum switching frequency vs. the output voltage when VIN = 12V and VIN = 5V.

Table 1: Maximum Frequency Selection vs. Output Voltage

	Maximum Frequency Selection	
Vo (V)	VIN = 12V	VIN = 5V
5	1.25MHz	/
3.3	1.25MHz	1.25MHz
2.5	1.25MHz	1.25MHz
1.8	1.25MHz	1.25MHz
1.5	1.25MHz	1.25MHz
1.2	1MHz	1.25MHz
1	750kHz	1.25MHz
0.9	750kHz	1.25MHz
0.6	500kHz	1.25MHz

Forced PWM Operation

When the MP8854 works in forced pulse-width modulation (PWM) mode, the MP8854 enters continuous conduction mode (CCM), where the HS-FET and LS-FET repeat the on/off operation, even if the inductor current is zero or a negative value. The switching frequency (F_{SW}) is fairly constant. Figure 4 shows the timing diagram during this operation.

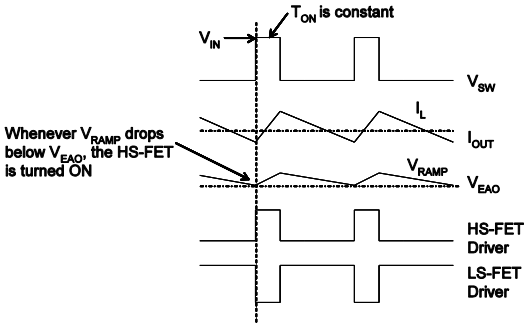


Figure 4: Forced PWM Operation

Light-Load Operation

When the MP8854 works in auto-PWM or auto-pulse-frequency modulation (PFM) mode in light-load operation, the MP8854 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops

almost to zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (Hi-Z) (see Figure 5). The output capacitors discharge slowly to GND through R1 and R2. This operation improves device efficiency greatly when the output current is low.

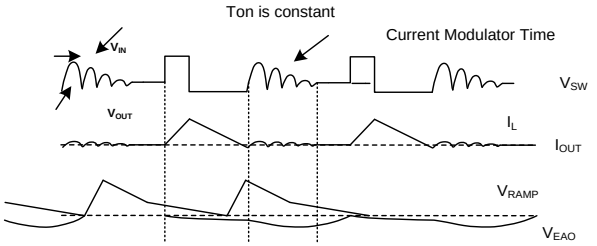


Figure 5: Light-Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does during a heavy-load condition. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the current modulator regulation time period becomes shorter, the HS-FET turns on more frequently, and the switching frequency increases. The output current reaches critical levels when the current modulator time is zero and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The MP8854 reverts to PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

The MP8854 can operate in PFM mode under light load to improve efficiency (low-power mode). The MP8854 can also operate in forced PWM mode at any load condition. The mode is selectable through the I²C control. To enable low-power mode, set the Mode bit to 0. To disable low-power mode, set the Mode bit to 1, and the converter works in forced PWM mode. The Mode bit is set to 0 (PFM) by default.

Operating without an External Ramp

The traditional constant-on-time (COT) control scheme is intrinsically unstable if the output capacitor's ESR is not large enough to be an effective current-sense resistor. Ceramic capacitors cannot be used as output capacitors, typically. The MP8854 has built-in, internal ramp compensation to ensure that the system is stable, even without the help of the output capacitor's ESR. The pure ceramic capacitor solution can reduce the output ripple, total BOM cost, and board area significantly.

VCC Regulator

A 3.5V internal regulator powers most of the internal circuitries. A 470nF decoupling capacitor is needed to stabilize the regulator and reduce ripple. This regulator takes the VIN input and operates in the full VIN range. After EN is pulled high and VIN is greater than 3.5V, the output of the regulator is in full regulation. When VIN is lower than 3.5V, the output voltage decreases and follows the input voltage. A 0.47µF ceramic capacitor is required for decoupling.

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage against the internal 0.6V reference (REF) and outputs a PWM signal. The reference voltage can be programmed from 0.6V to 1.108V via the I²C. The optimized internal ramp compensation minimizes the external component count and simplifies the control loop design.

Enable (EN)

EN is a digital control pin that turns the regulator, including the I²C block, on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. An internal 1.5MΩ resistor is connected from EN to ground. EN can operate with an 18V input voltage, which allows EN to be directly connected to VIN for automatic start-up. When the external EN is high, set the EN bit to 0 in register 01 to stop the HS-FET and LS-FET from switching. The MP8854 resumes switching by setting the EN bit to 1.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8854 UVLO comparator monitors the input voltage, VIN, and output voltage of the VCC regulator. The MP8854 is active when the voltages exceed the UVLO rising threshold.

Soft Start (SS) and Pre-Bias Start-Up

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V to VCC. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference.

The approximate typical soft-start time can be calculated with Equation (2):

$$t_{ss}(ms) = \frac{V_{ref}(V) \times C_{ss}(nF)}{7\mu A} \quad (2)$$

Where V_{ref} is the reference voltage.

If the output of the MP8854 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor exceeds the sensed output voltage at FB.

The MP8854 also provides a selectable soft-stop function, which defines the output discharge behavior after EN shutdown. By default, the output is not controlled after an EN shutdown. If setting the Soft Stop control bit D[3] to 1 in register 02 via the I²C, the output is discharged linearly to zero in a quarter of the soft-start time.

Over-Current Protection (OCP)

The MP8854 has a default, hiccup, cycle-by-cycle, over-current limiting control. The current-limit circuit employs both a high-side current limit and a low-side "valley" current-sensing algorithm. The MP8854 uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element for the valley current limit. If the magnitude of the high-side current-sense signal is above the current-limit threshold, the PWM on pulse is terminated, and the LS-FET is turned on. Afterward, the inductor current is monitored by the voltage between GND and SW. GND is used as the positive current sensing node, so GND should be connected to the source terminal of the bottom MOSFET. PWM is not allowed to initiate a new cycle before the inductor current falls to the valley threshold.

After the cycle-by-cycle over-current limit occurs, the output voltage drops until VOUT is below the under-voltage (UV) threshold (typically 60% below the reference). Once UV is triggered, the MP8854 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MP8854 exits hiccup mode once the over-current condition is removed.

Short the output to ground first, and then power on the part. The MP8854's I²C is disabled in this condition. The I²C resumes operation after the short circuit is removed. When the Hiccup OCP bit D[1] in register 01 is set to 0 by the I²C, a latch-off occurs if OCP is triggered, and FB UVP is triggered.

Power Good (PG)

Power good (PG) indicates whether the output voltage is in the normal range compared to the internal reference voltage. PG is an open-drain structure. An external pull-up supply is required. During power-up, the PG output is pulled low. This indicates to the system to remain off and keep the load on the output to a minimum. This helps reduce inrush current at start-up.

When the output voltage is higher than 90% and lower than 115% of the internal reference voltage and the soft start is finished, then the PG signal is pulled high. When the output voltage is lower than 85% after the soft start finishes, the PG signal remains low. When the output voltage is higher than 115% of the internal reference, PG is switched low. The PG signal rises high again after the output voltage drops below 105% of the internal reference voltage.

PG implements an adjustable deglitch time via the I²C whenever VOUT crosses the UV/OV rising and falling threshold. This guarantees the correct indication when the output voltage is scaled through the I²C.

The PG output is pulled low immediately when EN UVLO, input UVLO, OCP, or over-temperature protection (OTP) is triggered.

Input Over-Voltage Protection (VIN OVP)

The MP8854 monitors VIN to detect an input over-voltage event. This function is active only when the output is in an over-voltage (OV) or soft-stop condition. When the output is in over-voltage protection (OVP), or soft stop is enabled, output discharge is enabled to charge the input voltage high. When the input voltage exceeds the input OVP threshold, both the HS-FET and LS-FET stop switching.

Output Over-Voltage Protection (OVP)

The MP8854 monitors both FB and VOUT to detect an over-voltage event. An internal comparator monitors FB. When the FB voltage rises higher than 125% of the internal reference voltage, the controller enters dynamic regulation mode, and the input voltage may be charged up during this time. When input OVP is triggered, the IC stops switching. If OVP mode is set to auto-retry in the I^2C, the IC begins switching once the input voltage drops below the VIN OVP recover threshold. Otherwise, the MP8854 latches off. OVP auto-retry mode or latch-off mode occurs only if the soft start has finished.

Dynamic regulation mode can be operated by turning on the low side until the low-side negative current limit is triggered. Then the body diode of the HS-FET free-wheels the current.

The output power charges the input, which may trigger the VIN OVP function. In VIN OVP, neither the HS-FET or LS-FET turn on and stop charging VIN. If the output is still over voltage and the input voltage drops below the VIN OVP threshold, repeat the operation. If the output voltage is below 110% of the internal reference voltage, then the MP8854 exits output OVP.

Output Absolute Over-Voltage Protection (OVP_ABS)

The MP8854's VOUT can be adjusted by the output reference voltage and the external resistor dividers. The MP8854's output voltage must be lower than the absolute OVP threshold (typically 6.5V). The MP8854 monitors VOUT to detect absolute OVP. When VOUT is larger than 6.5V, the controller enters dynamic regulation mode if the OVP Retry bit is set to 1 in the I^2C register 01. Otherwise, the MP8854 latches off when output OVP and input OVP are both triggered. Absolute OVP works once both the input voltage and EN are higher than their rising thresholds. This means that this function can work even during a soft start.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 160°C, the entire chip shuts down. When the temperature is less than its lower threshold (typically 140°C), the chip is enabled again.

The D[1] and D[2] bits can be monitored in register 06 for more information about IC silicon temperature.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.4V with a 150mV hysteresis. The bootstrap capacitor voltage is regulated by VIN internally through D1, M1, C4, L1, and C2 (see Figure 6). If V_{BST} - V_{SW} exceeds 3.3V, U1 regulates M1 to maintain a 3.3V BST voltage across C4.

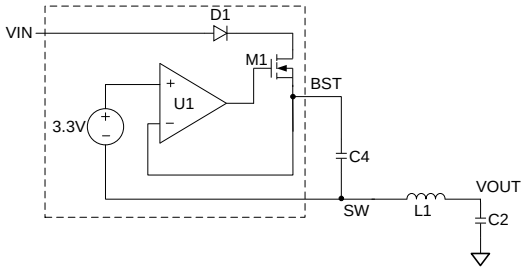


Figure 6: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If VIN, VCC, and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries. Several events can shut down the chip: EN low, VIN low, VCC low, thermal shutdown, OVP latch, and OCP latch. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The EAO voltage and the internal supply rail are then pulled down.

I²C Control and Default Output Voltage

When the MP8854 is enabled, the output voltage is determined by the FB resistors with a programmed soft-start time. Afterward, the I²C bus can communicate with the master. If the chip does not receive an I²C communication signal continuously, it can work well through FB and perform behavior similar to a traditional non-I²C part. The output voltage is determined by the resistor dividers R1, R2, and FB reference voltage. V_{OUT} can be calculated using Equation (3):

$$V_{OUT} = V_{REF} \times (\frac{R1+R2}{R2}) \quad (3)$$

Note that the output voltage cannot be set higher than an absolute OVP threshold (typically 6.5V).

I²C Slave Address

To support multiple devices used on the same I²C bus, A0 can be used to select four different addresses. A resistor divider from VCC to GND can achieve an accurate reference voltage. Connect A0 to this reference voltage to set a different I²C slave address (see Figure 7). The internal circuit changes the I²C address accordingly.

When the master sends an 8-bit address value, the 7-bit I²C address should be followed by 0 or 1 to indicate a write or read operation, respectively. Table 2 shows the recommended I²C address selection by the A0 voltage.

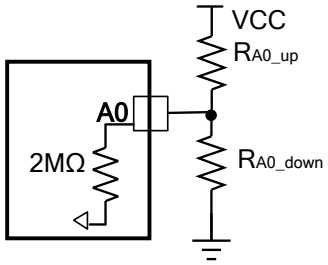


Figure 7: I²C Slave Address Selection Set-Up

Table 2: Recommended I²C Slave Address Selection by A0 Resistor Divider

A0 Upper Resistor R_{A0_up} (kΩ)	A0 Lower Resistor R_{A0_down} (kΩ)	I²C Slave Address	
		Binary	Hex
No connect	No connect	110 0001	61H
500	300	110 0011	63H
300	500	110 0101	65H
100	No connect	110 0111	67H

I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MP8854 interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled by the I²C interface instantaneously.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 8).

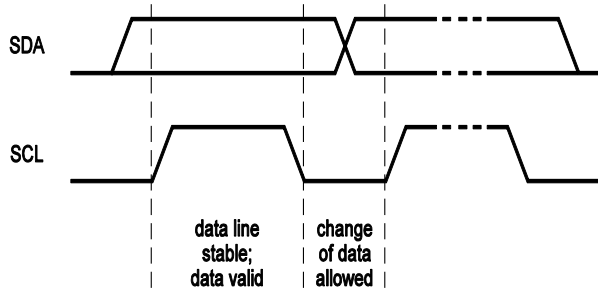


Figure 8: Bit Transfer on the I²C Bus

Start and stop are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 9).

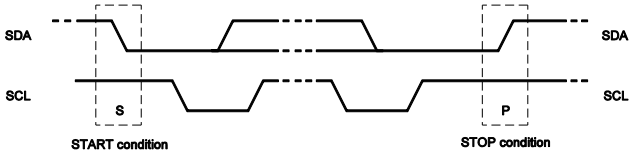


Figure 9: Start and Stop Conditions

Start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition, and is considered to be free again after a minimum of 4.7μs after the stop condition. The bus remains busy if a repeated start (Sr) is generated instead of a stop condition. The start (S) and repeated start (Sr) conditions are identical functionally.

Transfer Data

Every byte put on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains low stably during the high period of this clock pulse.

Data transfers follow the format shown in Figure 10. After the start condition (S), a slave address is sent. This address is seven bits long followed by an eighth data direction bit (r/w). 0 indicates a transmission (write), and 1 indicates a request for data (read). A data transfer is always terminated by a stop condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition (Sr) and address another slave without first generating a stop condition.

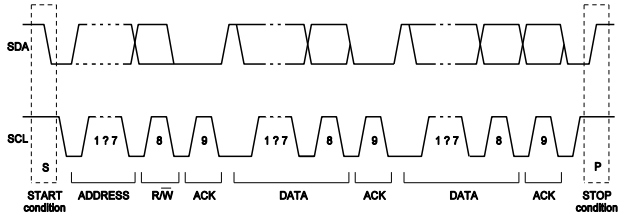


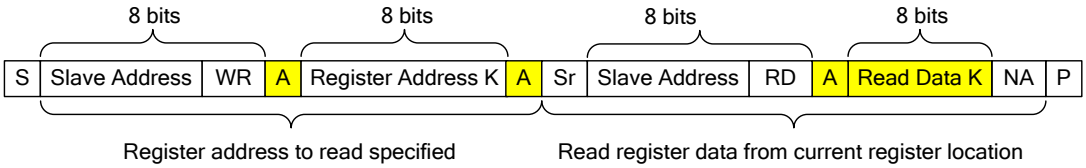
Figure 10: Complete Data Transfer

The MP8854 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP8854 acknowledges this by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP8854. The MP8854 performs an update on the falling edge of the LSB byte.

I²C Write and Read Sequence Example

Master to Slave
Slave to Master
A = Acknowledge (SDA = LOW)
NA = NOT Acknowledge (SDA = HIGH)
S = Start Condition
P = Stop Condition
WR Write = 0
RD Read = 1

I²C Write Example – Write Register



Master to Slave
Slave to Master
A = Acknowledge (SDA = LOW)
NA = NOT Acknowledge (SDA = HIGH)
S = Start Condition
P = Stop Condition
Sr = Repeat Start Condition
WR Write = 0
RD Read = 1

I²C Read Example – Read Register

REGISER DESCRIPTION

Register Map

The MP8854 contains six write or read registers. Register 00 is the output voltage selection register. Register 01 is the first system control register and can be used to set the slew rate, hiccup OCP, etc. Register 02 is the second system control register and can be used to set the switching frequency, current limit, etc.

Register 03 and register 04 are output current and output voltage indicating registers, respectively. Register 05 is the IC ID register. Register 06 is the IC status indication register and can be used to check if the IC is in OCP, OTP, etc. The register map is shown below.

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	r/w	Reserved	Output Reference						
01	SysCntlreg1	r/w	EN	GO_BIT	Slew Rate			Retry OVP	Hiccup OCP	Mode
02	SysCntlreg2	r/w	PG Deglitch Time		Switching Frequency		Soft Stop	Current Limit Adjust		
03	Output Current	r	Output Current							
04	Output Voltage	r	Output Voltage							
05	ID1	r	Vendor ID				Die ID			
06	Status	r	Reserved				OC	OTEW	OT	PG

Register Description

1) Reg00 VSEL

Register 00 is the output reference voltage selection register. The MP8854 default output voltage is determined by the FB resistor divider after the MP8854 power start-up or EN start-up. The reference voltage is adjustable from 0.6V to 1.108V. Before adjusting the output reference voltage, the bit GO_BIT of the first system control register 01 should be set to 1, and then the reference voltage can be adjusted by the lower seven bits of register 00. When the output reference voltage setting command is finished, GO_BIT auto-resets to 0 to prevent false operation of the VOUT scaling. GO_BIT should be set to 1 before adjusting the output reference voltage via the I^2C.

Table 3 shows the output reference voltage selection chart from 0.6V to 1.108V via the I^2C.

NAME	BITS	DEFAULT	DESCRIPTION
Reserved	D[7]	1	Reserved for further use.
Output Reference	D[6:0]	001 1110	Sets the output voltage from 0.6V to 1.108V (see Table 3). The default value is 0.72V.

Table 3: Output Reference Voltage Selection Chart

D[6:0]	VOUT (V)	D[6:0]	VOUT (V)	D[6:0]	VOUT (V)	D[6:0]	VOUT (V)
000 0000	0.6	010 0000	0.728	100 0000	0.856	110 0000	0.984
000 0001	0.604	010 0001	0.732	100 0001	0.86	110 0001	0.988
000 0010	0.608	010 0010	0.736	100 0010	0.864	110 0010	0.992
000 0011	0.612	010 0011	0.74	100 0011	0.868	110 0011	0.996
000 0100	0.616	010 0100	0.744	100 0100	0.872	110 0100	1
000 0101	0.62	010 0101	0.748	100 0101	0.876	110 0101	1.004
000 0110	0.624	010 0110	0.752	100 0110	0.88	110 0110	1.008
000 0111	0.628	010 0111	0.756	100 0111	0.884	110 0111	1.012
000 1000	0.632	010 1000	0.76	100 1000	0.888	110 1000	1.016
000 1001	0.636	010 1001	0.764	100 1001	0.892	110 1001	1.02
000 1010	0.64	010 1010	0.768	100 1010	0.896	110 1010	1.024
000 1011	0.644	010 1011	0.772	100 1011	0.9	110 1011	1.028
000 1100	0.648	010 1100	0.776	100 1100	0.904	110 1100	1.032
000 1101	0.652	010 1101	0.78	100 1101	0.908	110 1101	1.036
000 1110	0.656	010 1110	0.784	100 1110	0.912	110 1110	1.04
000 1111	0.66	010 1111	0.788	100 1111	0.916	110 1111	1.044
001 0000	0.664	011 0000	0.792	101 0000	0.92	111 0000	1.048
001 0001	0.668	011 0001	0.796	101 0001	0.924	111 0001	1.052
001 0010	0.672	011 0010	0.8	101 0010	0.928	111 0010	1.056
001 0011	0.676	011 0011	0.804	101 0011	0.932	111 0011	1.06
001 0100	0.68	011 0100	0.808	101 0100	0.936	111 0100	1.064
001 0101	0.684	011 0101	0.812	101 0101	0.94	111 0101	1.068
001 0110	0.688	011 0110	0.816	101 0110	0.944	111 0110	1.072
001 0111	0.692	011 0111	0.82	101 0111	0.948	111 0111	1.076
001 1000	0.696	011 1000	0.824	101 1000	0.952	111 1000	1.08
001 1001	0.7	011 1001	0.828	101 1001	0.956	111 1001	1.084
001 1010	0.704	011 1010	0.832	101 1010	0.96	111 1010	1.088
001 1011	0.708	011 1011	0.836	101 1011	0.964	111 1011	1.092
001 1100	0.712	011 1100	0.84	101 1100	0.968	111 1100	1.096
001 1101	0.716	011 1101	0.844	101 1101	0.972	111 1101	1.1
001 1110	0.72	011 1110	0.848	101 1110	0.976	111 1110	1.104
001 1111	0.724	011 1111	0.852	101 1111	0.98	111 1111	1.108

2) Reg01 SysCntlreg1

Register 01 is the first system control register.

The highest bit, EN, can be used to turn the part on or off when the external EN is high. When the external EN is high, the part shuts down by setting the EN bit to 0, and then the HS-FET and LS-FET stop switching. The part resumes switching by setting the EN bit to 1 again. When the external EN is low, the converter is off, and the I^2C shuts down.

Set GO_BIT to 1 to enable the I^2C authority of writing the output reference. When the command is finished, GO_BIT auto-resets to 0 to prevent false operation of the VOUT scaling.

The IC switches to forced PWM mode when GO_BIT is set to 1 to achieve a smooth output waveform during the output dynamic scaling. After the output scaling is complete, GO_BIT is set to 0 automatically, and the IC operation mode switches to the original mode set by the Mode bit.

The 3-bit Slew Rate D[5:3] is used for slew rate selection during the output voltage dynamic scaling. A proper slew rate reduces the inrush current, voltage overshoot, and voltage undershoot. Eight different slew rate levels can be selected.

The bit Retry OVP defines the protection mode when OVP is triggered. When Retry OVP is set to 1, the part enters auto-recovery when OVP is removed. When Retry OVP is set to 0, the part latches off once output OVP occurs, and VIN OVP is triggered until VIN or EN are toggled.

The bit Hiccup OCP defines the over-current protection mode. When Hiccup OCP is set to 1, the part enters hiccup mode when OCP and UVP are both triggered. When Hiccup OCP is set to 0, the part enters latch-off when OCP and UVP are both triggered.

The lowest bit, Mode, is used for selecting forced PWM or auto-PFM/PWM mode at light load. When Mode is set to 0, auto-PFM/PWM mode is enabled at light load. When Mode is set to 1, forced PWM mode is enabled at light load.

<table>
<tr><th>NAME</th><th>BITS</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>EN</td><td>D[7]</td><td>1</td><td>I²C controlled turn-on or turn-off of the part. When the external EN is low, the converter is off, and I²C shuts down. When EN is high, the EN bit takes over. The default EN bit is 1.</td></tr>
<tr><td>GO_BIT</td><td>D[6]</td><td>0</td><td>Switch bit of the I²C writing authority for the output reference command only. Set GO_BIT = 1 to enable the I²C authority of writing the output reference. When the command is finished, GO_BIT auto-resets to 0 to prevent false operation of the Vref scaling.
Voltage scaling examples:
1) Set GO_BIT = 1.
2) Write register 00: set the output reference.
3) Read back the GO_BIT value to see if the output scaling is finished. If GO_BIT = 0, the voltage scaling is done. Otherwise, Vref is still in adjustment.
4) Set GO_BIT = 1 if output voltage scaling is needed a second time.
5) Write register 00: set the output reference.</td></tr>
<tr><td>Slew Rate</td><td>D[5:3]</td><td>100</td><td>The slew rate during the I²C controlled voltage change is defined by three bits. The output voltage changes linearly from the previous voltage to the new set voltage with a slew rate (see below). This helps reduce the inrush current, voltage overshoot, and voltage undershoot greatly.
<table>
<tr><th>D[5:3]</th><th>Slew Rate</th><th>D[5:3]</th><th>Slew Rate</th></tr>
<tr><td>000</td><td>40mV/µs</td><td>100</td><td>5mV/µs</td></tr>
<tr><td>001</td><td>30mV/µs</td><td>101</td><td>2.5mV/µs</td></tr>
<tr><td>010</td><td>20mV/µs</td><td>110</td><td>1.25mV/µs</td></tr>
<tr><td>011</td><td>10mV/µs</td><td>111</td><td>0.625mV/µs</td></tr>
</table></td></tr>
<tr><td>Retry OVP</td><td>D[2]</td><td>1</td><td>FB or Vref over-voltage protection mode selection bit. 1 means the part auto-recovers when OVP is removed. 0 means the part latches off once output OVP and VIN OVP are both triggered until VIN or EN is power reset.</td></tr>
<tr><td>Hiccup OCP</td><td>D[1]</td><td>1</td><td>Over-current protection mode selection. 1 means hiccup mode OCP. 0 means latch-off type OCP.</td></tr>
<tr><td>Mode</td><td>D[0]</td><td>0</td><td>Set Mode to 0 to enable PFM mode. Set Mode to 1 to disable auto-PFM/PWM mode. The default is auto-PFM/PWM mode for light load.</td></tr>
</table>

3) Reg02 SysCntlreg2

Register 02 is the second system control register.

The highest two bits of PG Deglitch Time D[7:6] define the power good signal rising and falling edge delay times. When output OVP or UVP is triggered, the PG signal goes low or high after a delay time. There are four levels of PG delay time that can be programmed by the I^2C in different conditions.

The two Switching Frequency bits D[5:4] are used for switching frequency selection. The MP8854 supports up to 1.25MHz of switching frequency by setting the two bits to 11. The MP8854 maximum programmable switching frequency is limited by an internal minimum on-time (see Table 1).

The bit Soft Stop defines the output voltage discharge behavior after an EN shutdown. When Soft Stop is set to 0, the output voltage is not controlled after an EN shutdown. When Soft Stop is set to 1, the output voltage is discharged linearly to zero with the set soft-stop time.

The lowest three bits, Current Limit Adjust D[2:0], are used for peak and valley current-limit selection. There are eight levels of current limit that can be selected for different application conditions.

<table>
<tr><th>NAME</th><th>BITS</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="4">PG Deglitch Time</td><td rowspan="4">D[7:6]</td><td rowspan="4">11</td><td colspan="4">Power good signal rising and falling edges' delay time. When FB or VOUT is out of the regulation window, the PG comparator is triggered, but needs a delay time before the PG signal can turn high or low.</td></tr>
<tr><td>D[7:6]</td><td>PG Deglitch</td><td>D[7:6]</td><td>PG Deglitch</td></tr>
<tr><td>00</td><td><1µs</td><td>10</td><td>12µs</td></tr>
<tr><td>01</td><td>6µs</td><td>11</td><td>30µs</td></tr>
<tr><td rowspan="4">Switching Frequency</td><td rowspan="4">D[5:4]</td><td rowspan="4">00</td><td colspan="4">Switching frequency set bit. There is no dedicated frequency oscillator inside the part. The switching frequency is fairly fixed by controlling the T_{ON} timer.</td></tr>
<tr><td>D[5:4]</td><td>Frequency</td><td>D[5:4]</td><td>Frequency</td></tr>
<tr><td>00</td><td>500kHz</td><td>10</td><td>1MHz</td></tr>
<tr><td>01</td><td>750kHz</td><td>11</td><td>1.25MHz</td></tr>
<tr><td>Soft Stop</td><td>D[3]</td><td>0</td><td colspan="4">This bit defines the VOUT discharge behavior after an EN shutdown. 0 means VOUT is not controlled after an EN shutdown. 1 means VOUT is discharged linearly to zero with the set soft-stop time.</td></tr>
<tr><td rowspan="5">Current Limit Adjust</td><td rowspan="5">D[2:0]</td><td rowspan="5">001</td><td>D[2:0]</td><td>Valley Current Limit (A)</td><td>D[2:0]</td><td>Valley Current Limit (A)</td></tr>
<tr><td>000</td><td>9.6</td><td>100</td><td>5.1</td></tr>
<tr><td>001</td><td>8.4</td><td>101</td><td>4.2</td></tr>
<tr><td>010</td><td>7.2</td><td>110</td><td>3.6</td></tr>
<tr><td>011</td><td>6</td><td>111</td><td>3</td></tr>
</table>

4) Reg03 Output Current

Register 03 is an output current-indicating register. After the part starts up, the DC output current information can be read through the I²C communication.

When the inductor current is in discontinuous conduction mode (DCM), the output current sense is not very accurate. The Mode bit can be set to 1 (PWM mode) for good current sensing accuracy at light load.

When the inductor current enters CCM, the output current sense accuracy is excellent (typical accuracy is 5% when the output current is higher than 2A).

Table 4 shows the output current chart from 0A to 6.75A.

NAME	BITS	DEFAULT	DESCRIPTION
Output Current	D[7:0]	0000 0000	Output current monitor bits. Table 4 shows the output current monitor chart.

Table 4: Output Current Chart

D[7:0]	I_{OUT}(A)	D[7:0]	I_{OUT}(A)
0000 0000	0	0010 1011	2.15
0000 0001	0.05	0010 1100	2.2
0000 0010	0.1	0010 1101	2.25
0000 0011	0.15	0010 1110	2.3
0000 0100	0.2	0010 1111	2.35
0000 0101	0.25	0011 0000	2.4
0000 0110	0.3	0011 0001	2.45
0000 0111	0.35	0011 0010	2.5
0000 1000	0.4	0011 0011	2.55
0000 1001	0.45	0011 0100	2.6
0000 1010	0.5	0011 0101	2.65
0000 1011	0.55	0011 0110	2.7
0000 1100	0.6	0011 0111	2.75
0000 1101	0.65	0011 1000	2.8
0000 1110	0.7	0011 1001	2.85
0000 1111	0.75	0011 1010	2.9
0001 0000	0.8	0011 1011	2.95
0001 0001	0.85	0011 1100	3
0001 0010	0.9	0011 1101	3.05
0001 0011	0.95	0011 1110	3.1
0001 0100	1	0011 1111	3.15
0001 0101	1.05	0100 0000	3.2
0001 0110	1.1	0100 0001	3.25
0001 0111	1.15	0100 0010	3.3
0001 1000	1.2	0100 0011	3.35
0001 1001	1.25	0100 0100	3.4
0001 1010	1.3	0100 0101	3.45
0001 1011	1.35	0100 0110	3.5
0001 1100	1.4	0100 0111	3.55
0001 1101	1.45	0100 1000	3.6
0001 1110	1.5	0100 1001	3.65
0001 1111	1.55	0100 1010	3.7
0010 0000	1.6	0100 1011	3.75
0010 0001	1.65	0100 1100	3.8
0010 0010	1.7	0100 1101	3.85
0010 0011	1.75	0100 1110	3.9
0010 0100	1.8	0100 1111	3.95
0010 0101	1.85	0101 0000	4

5) Reg04 Output Voltage

Register 04 is an output voltage-indicating register. After the part starts up, the output voltage can be read through the I²C communication. In light load, if the mode bit is set to 0, the MP8854 works in PFM mode. At an extremely light-load or no-load condition, the ADC only works when the first pulse comes, and then the MP8854 refreshes the output voltage register before entering sleep mode.

At this moment, the sensed output voltage is at its maximum value, not the average output voltage. Therefore, the I²C read-back voltage is slightly higher than the set point. When applying a load to the part, a higher sense accuracy can be achieved. The Mode bit can be set to 1 (PWM mode) for good voltage sensing accuracy at light load. Table 5 shows the output voltage chart from 0.5V to 5.643V.

NAME	BITS	DEFAULT	DESCRIPTION
Output voltage	D[7:0]	0000 0000	Output voltage monitor bits. Table 5 shows the output voltage monitor chart.

Table 5: Output Voltage Chart

D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)
0000 0000	0.500	0010 1011	1.367	0101 0110	2.235	1000 0001	3.102	1010 1100	3.969	1101 0111	4.837
0000 0001	0.520	0010 1100	1.387	0101 0111	2.255	1000 0010	3.122	1010 1101	3.989	1101 1000	4.857
0000 0010	0.540	0010 1101	1.408	0101 1000	2.275	1000 0011	3.142	1010 1110	4.010	1101 1001	4.877
0000 0011	0.561	0010 1110	1.428	0101 1001	2.295	1000 0100	3.162	1010 1111	4.030	1101 1010	4.897
0000 0100	0.581	0010 1111	1.448	0101 1010	2.315	1000 0101	3.183	1011 0000	4.050	1101 1011	4.917
0000 0101	0.601	0011 0000	1.468	0101 1011	2.335	1000 0110	3.203	1011 0001	4.070	1101 1100	4.937
0000 0110	0.621	0011 0001	1.488	0101 1100	2.356	1000 0111	3.223	1011 0010	4.090	1101 1101	4.958
0000 0111	0.641	0011 0010	1.509	0101 1101	2.376	1000 1000	3.243	1011 0011	4.110	1101 1110	4.978
0000 1000	0.661	0011 0011	1.529	0101 1110	2.396	1000 1001	3.263	1011 0100	4.131	1101 1111	4.998
0000 1001	0.682	0011 0100	1.549	0101 1111	2.416	1000 1010	3.283	1011 0101	4.151	1110 0000	5.018
0000 1010	0.702	0011 0101	1.569	0110 0000	2.436	1000 1011	3.304	1011 0110	4.171	1110 0001	5.038
0000 1011	0.722	0011 0110	1.589	0110 0001	2.456	1000 1100	3.324	1011 0111	4.191	1110 0010	5.058
0000 1100	0.742	0011 0111	1.609	0110 0010	2.477	1000 1101	3.344	1011 1000	4.211	1110 0011	5.079
0000 1101	0.762	0011 1000	1.630	0110 0011	2.497	1000 1110	3.364	1011 1001	4.231	1110 0100	5.099
0000 1110	0.782	0011 1001	1.650	0110 0100	2.517	1000 1111	3.384	1011 1010	4.252	1110 0101	5.119
0000 1111	0.803	0011 1010	1.670	0110 0101	2.537	1001 0000	3.404	1011 1011	4.272	1110 0110	5.139
0001 0000	0.823	0011 1011	1.690	0110 0110	2.557	1001 0001	3.425	1011 1100	4.292	1110 0111	5.159
0001 0001	0.843	0011 1100	1.710	0110 0111	2.578	1001 0010	3.445	1011 1101	4.312	1110 1000	5.179
0001 0010	0.863	0011 1101	1.730	0110 1000	2.598	1001 0011	3.465	1011 1110	4.332	1110 1001	5.200
0001 0011	0.883	0011 1110	1.751	0110 1001	2.618	1001 0100	3.485	1011 1111	4.352	1110 1010	5.220
0001 0100	0.903	0011 1111	1.771	0110 1010	2.638	1001 0101	3.505	1100 0000	4.373	1110 1011	5.240
0001 0101	0.924	0100 0000	1.791	0110 1011	2.658	1001 0110	3.526	1100 0001	4.393	1110 1100	5.260
0001 0110	0.944	0100 0001	1.811	0110 1100	2.678	1001 0111	3.546	1100 0010	4.413	1110 1101	5.280
0001 0111	0.964	0100 0010	1.831	0110 1101	2.699	1001 1000	3.566	1100 0011	4.433	1110 1110	5.300
0001 1000	0.984	0100 0011	1.851	0110 1110	2.719	1001 1001	3.586	1100 0100	4.453	1110 1111	5.321
0001 1001	1.004	0100 0100	1.872	0110 1111	2.739	1001 1010	3.606	1100 0101	4.473	1111 0000	5.341
0001 1010	1.024	0100 0101	1.892	0111 0000	2.759	1001 1011	3.626	1100 0110	4.494	1111 0001	5.361
0001 1011	1.045	0100 0110	1.912	0111 0001	2.779	1001 1100	3.647	1100 0111	4.514	1111 0010	5.381
0001 1100	1.065	0100 0111	1.932	0111 0010	2.799	1001 1101	3.667	1100 1000	4.534	1111 0011	5.401
0001 1101	1.085	0100 1000	1.952	0111 0011	2.820	1001 1110	3.687	1100 1001	4.554	1111 0100	5.421
0001 1110	1.105	0100 1001	1.972	0111 0100	2.840	1001 1111	3.707	1100 1010	4.574	1111 0101	5.442
0001 1111	1.125	0100 1010	1.993	0111 0101	2.860	1010 0000	3.727	1100 1011	4.595	1111 0110	5.462
0010 0000	1.145	0100 1011	2.013	0111 0110	2.880	1010 0001	3.747	1100 1100	4.615	1111 0111	5.482
0010 0001	1.166	0100 1100	2.033	0111 0111	2.900	1010 0010	3.768	1100 1101	4.635	1111 1000	5.502
0010 0010	1.186	0100 1101	2.053	0111 1000	2.920	1010 0011	3.788	1100 1110	4.655	1111 1001	5.522
0010 0011	1.206	0100 1110	2.073	0111 1001	2.941	1010 0100	3.808	1100 1111	4.675	1111 1010	5.543
0010 0100	1.226	0100 1111	2.093	0111 1010	2.961	1010 0101	3.828	1101 0000	4.695	1111 1011	5.563
0010 0101	1.246	0101 0000	2.114	0111 1011	2.981	1010 0110	3.848	1101 0001	4.716	1111 1100	5.583
0010 0110	1.266	0101 0001	2.134	0111 1100	3.001	1010 0111	3.868	1101 0010	4.736	1111 1101	5.603
0010 0111	1.287	0101 0010	2.154	0111 1101	3.021	1010 1000	3.889	1101 0011	4.756	1111 1110	5.623
0010 1000	1.307	0101 0011	2.174	0111 1110	3.041	1010 1001	3.909	1101 0100	4.776	1111 1111	5.643
0010 1001	1.327	0101 0100	2.194	0111 1111	3.062	1010 1010	3.929	1101 0101	4.796		
0010 1010	1.347	0101 0101	2.214	1000 0000	3.082	1010 1011	3.949	1101 0110	4.816		

6) Reg05 ID1

Register 05 is the IC information-indicating register. The highest four bits, Vendor ID D[7:4], are set to 1000 internally.

The lowest four bits, IC Revision ID D[3:0], indicates IC revision information.

NAME	BITS	DESCRIPTION
Vendor ID	D[7:4]	1000.
IC Revision ID	D[3:0]	IC revision (0111).

7) Reg06 Status

Register 06 is a fault condition-indicating register. The highest four bits, D[7:4], are reserved for future use.

The bit OC is the output over-current indication. When the bit is set to 1, the IC is in hiccup mode or OC latch-off.

The bit OTEW is the die temperature early warning indication. When the bit is set to 1, the IC die temperature is higher than 120°C.

The bit PG is the output power good indication. When the bit is set to 1, the output power is normal.

NAME	BITS	DESCRIPTION
Reserved	D[7:4]	**Reserved for future use.**
OC	D[3]	**Output over-current indication.** When this bit is high, the IC is in hiccup mode or trips OC latch off.
OTEW	D[2]	**Die temperature early warning bit.** When the bit is high, the die temperature is higher than 120˚C.
OT	D[1]	**Over temperature indication.** When the bit is high, the IC is in thermal shutdown.
PG	D[0]	**Output power good indication.** When the bit is high, the VOUT power is normal. This means VOUT is higher than 95% and lower than 115% of the designed regulation voltage. PG compares FB/VOUT with REF.

APPLICATION INFORMATION

Setting the Output Voltage in a FB Control Loop

The MP8854 can be controlled by the FB loop. The output voltage can be set by the external resistor dividers. The FB loop reference voltage is a default value (0.72V) and can be programmed by the I²C.

The FB loop network is shown in Figure 11.

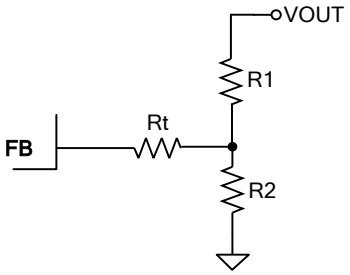


Figure 11: FB Loop Network

Choose R1 and R2 with Equation (4):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.72V} - 1} \quad (4)$$

Table 6 lists the recommended feedback resistor values for common output voltages.

Table 6: Resistor Selection for Common Output Voltages (8)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)	L (μH)
1.0	80.6	205	10	1.5
1.2	80.6	121	10	1.5
1.5	80.6	74.4	10	1.5
1.8	80.6	53.6	10	1.5
2.5	80.6	32.4	10	2.2
3.3	80.6	22.6	10	2.2
5	80.6	13.7	10	3.3

NOTE:

6) The recommended parameters are based on a 12V input voltage and 22μFx4 output capacitor. Different input voltage and output capacitor values may affect the selection of R1 and R2. For other components' parameters, please refer to the Typical Application Circuits on page 33-35.

Output Voltage Dynamic Scale

The output voltage dynamic scaling can be done only via the I²C. Refer to Figure 12 and follow the steps below.

1) Write GO_BIT (reg01[6]) to 1.
2) Write reg00 to set the reference voltage by Output Reference (reg00 [6:0]) simultaneously. When the command is finished, GO_BIT auto-resets to 0 to prevent false operation of the VOUT scaling.

Repeat the two steps above if the output voltage needs to be changed to a different voltage.

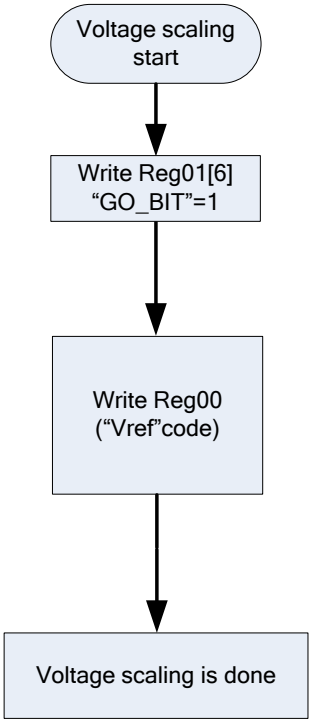


Figure 12: Output Voltage Dynamic Scale Flow Chart

Selecting the Inductor

Use a 0.47μH to 5μH inductor with a DC current rating at least 25% higher than the maximum load current for most applications. For the highest efficiency, use an inductor with a DC resistance less than 5mΩ. For most designs, the inductance value can be derived from Equation (5):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (5)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current.

The maximum inductor peak current can be calculated with Equation (6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Use a larger inductor for improved efficiency under light-load conditions below 100mA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use two 22µF capacitors.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (7):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The worst-case condition occurs at VIN = 2VOUT, shown in Equation (8):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by the capacitance can be estimated with Equation (9):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (10)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP8854 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator given the following conditions:

- VOUT is 5V or 3.3V
- Duty cycle is high: D > 50%

In these cases, add an external BST diode from VCC to BST (see Figure 13).

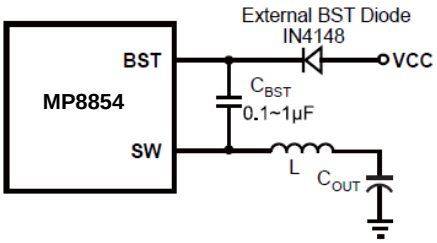


Figure 13: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1µF to 1µF.

Connect VCC to VIN at a Low Input Voltage

VCC can be connected to VIN directly when VIN is lower than 3.5V. This helps improve the MP8854's low input voltage efficiency performance. To use this application set-up, the VIN spike voltage must be limited below 4V; otherwise, VCC may be damaged.

PCB Layout Guidelines [9]

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 14 and follow the guidelines below. A four-layer layout is strongly recommended to achieve better thermal performance.

1. Place the high-current paths (PGND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Keep the VIN and PGND pads connected with large copper planes.
3. Use at least two layers for the VIN and PGND trace to achieve better thermal performance.
4. Add several vias close to the VIN and PGND pads to help with thermal dissipation.
5. Place the input capacitors as close to VIN and PGND as possible.
6. Place the decoupling capacitor as close to VCC and PGND as possible.
7. Place the external feedback resistors next to FB.
8. Ensure that there is no via on the FB trace.
9. Keep the switching node SW short and away from the feedback network.
10. Keep the BST voltage path (BST, C3, and SW) as short as possible.

NOTE:

9) The recommended layout is based on the Typical Application Circuits on page 35-37.

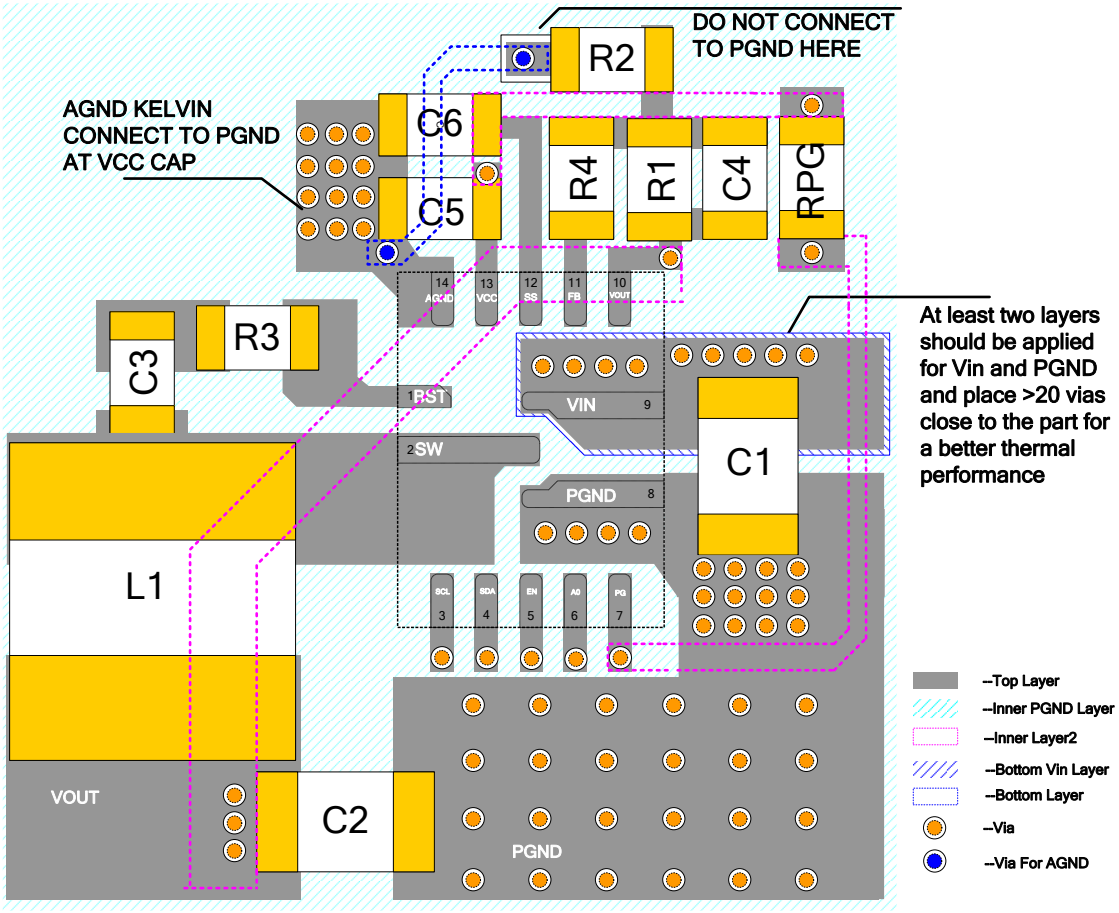


Figure 14: Recommend Layout

Design Example

Table 7 is a design example following the application guidelines for the specifications below.

Table 7: Design Example

V_{IN}	12V
V_{OUT}	1V
I_{OUT}	4A

The detailed application schematics are shown in Figure 15 through Figure 21. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS (10)

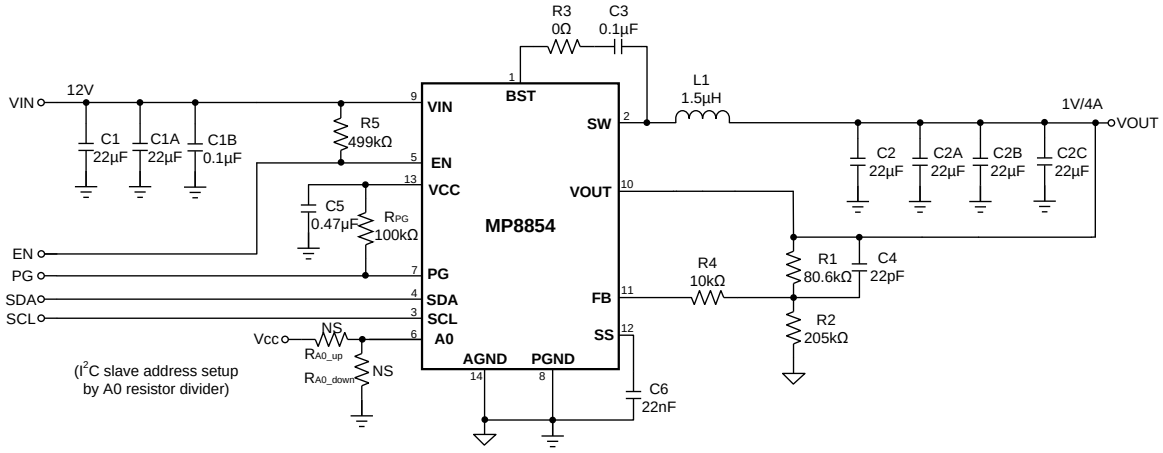


Figure 15: VIN = 12V, VOUT = 1V, I_{OUT} = 4A

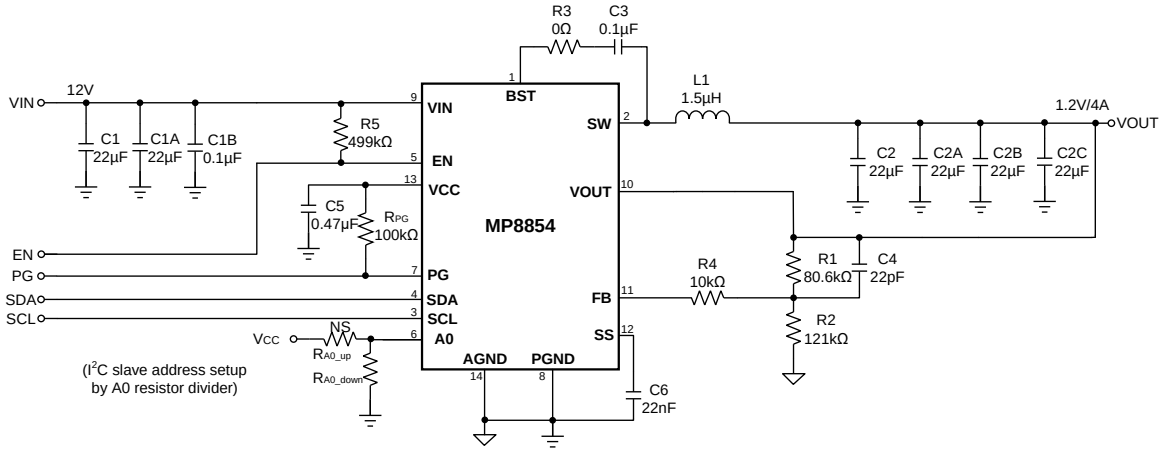


Figure 16: VIN = 12V, VOUT = 1.2V, I_{OUT} = 4A

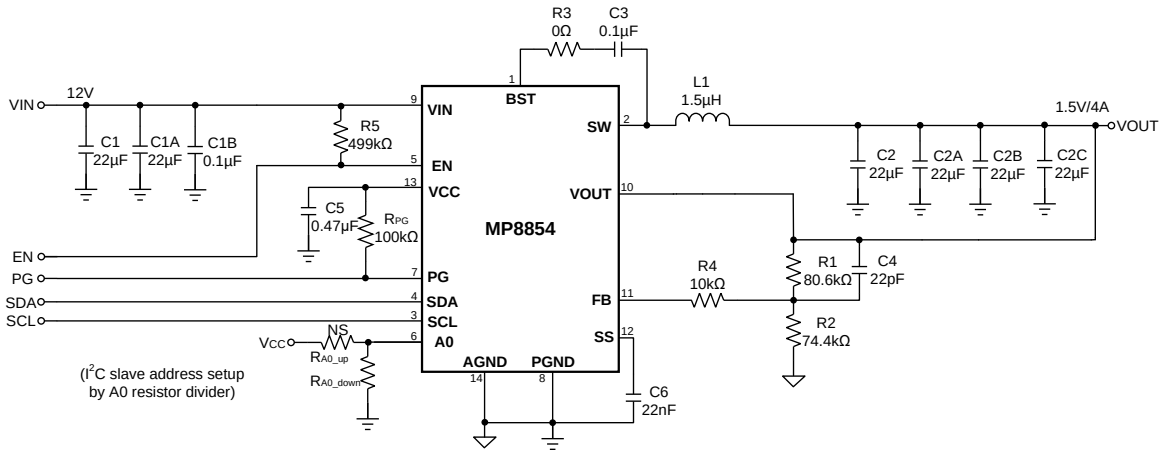


Figure 17: VIN = 12V, VOUT = 1.5V, I_{OUT} = 4A

TYPICAL APPLICATION CIRCUITS *(continued)*

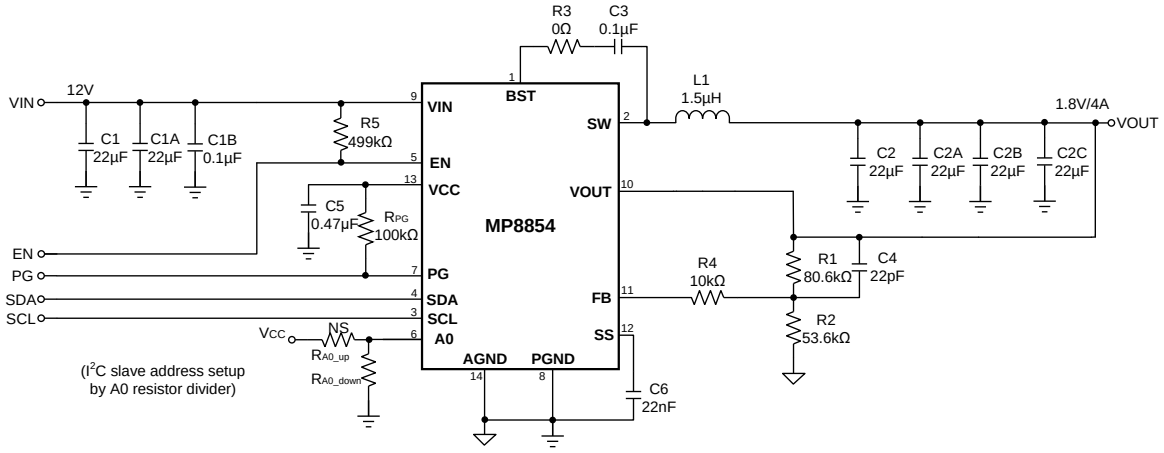


Figure 18: VIN = 12V, VOUT = 1.8V, I_{OUT} = 4A

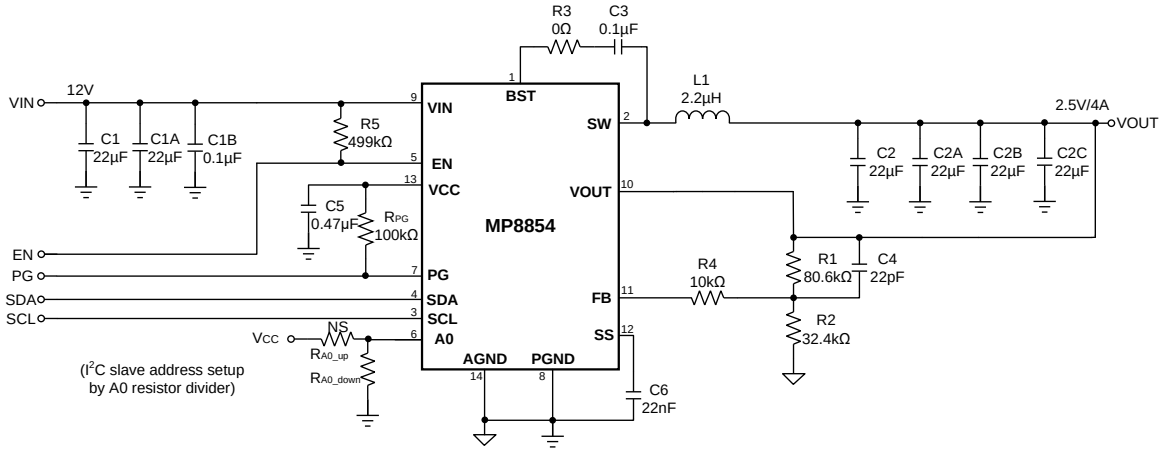


Figure 19: VIN = 12V, VOUT = 2.5V, I_{OUT} = 4A

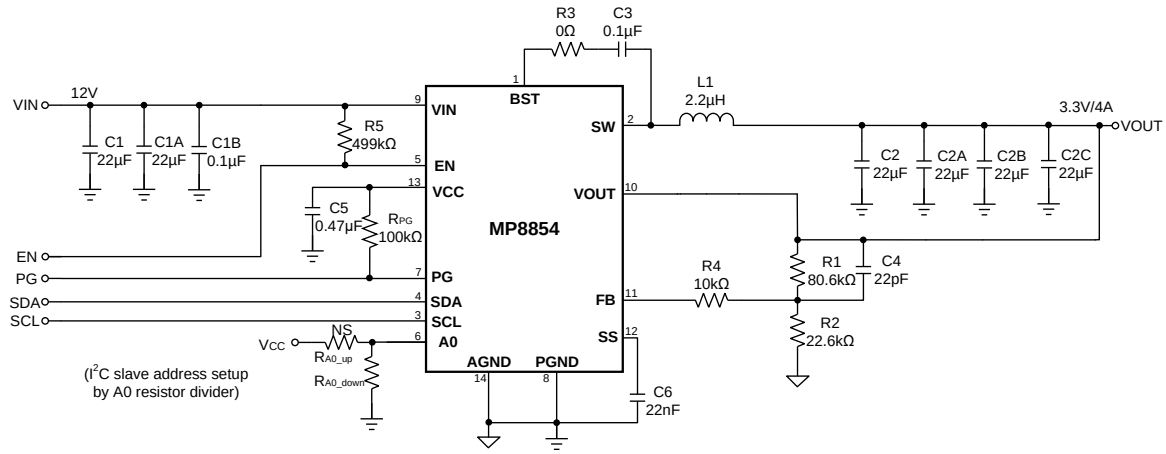


Figure 20: VIN = 12V, VOUT = 3.3V, I_{OUT} = 4A

TYPICAL APPLICATION CIRCUITS *(continued)*

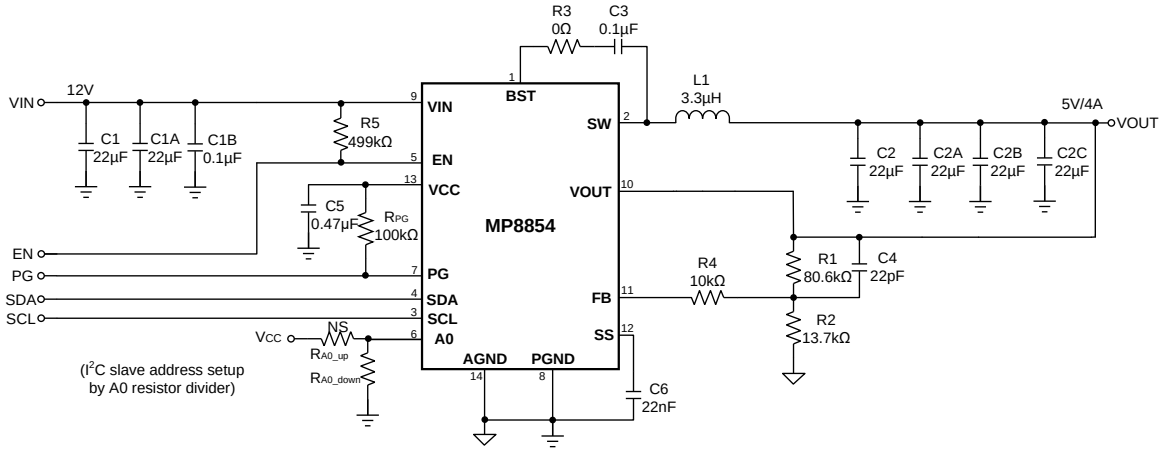
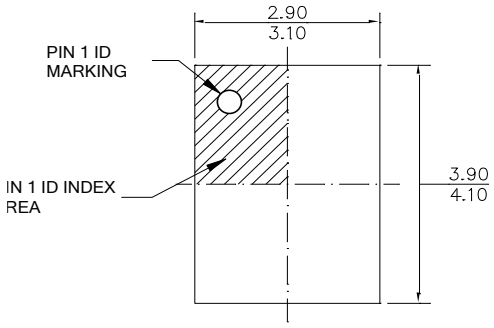


Figure 21: VIN = 12V, VOUT = 5V, I_{OUT} = 4A

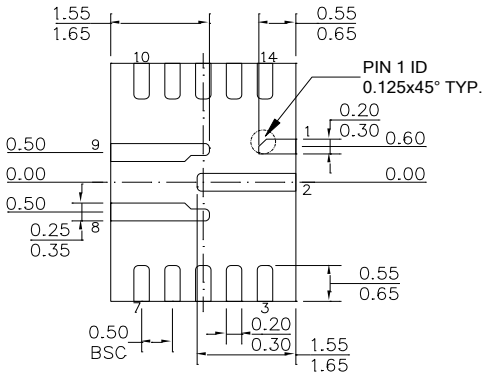
NOTE:
10) All circuits are based on a 0.72V default reference voltage.

PACKAGE INFORMATION

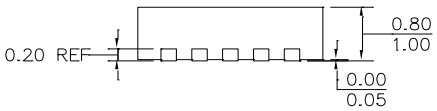
QFN-14 (3mmx4mm)



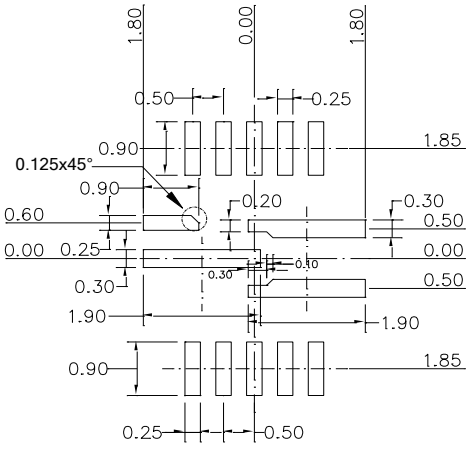
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMET MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.