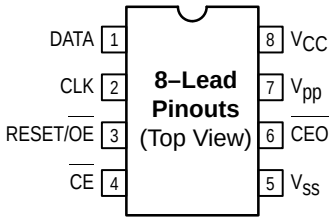
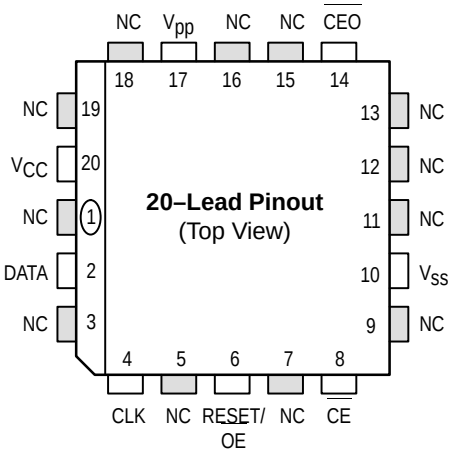
MPA17000 Serial EPROMs

The MPA17128 and MPA1765 are serial OTP EPROMs. They provide a compact, low pin count, non–volatile configuration store for the MPA1000 devices.

MPA17000 devices can be cascaded for increased memory capacity when needed. They are available in the standard 8–pin plastic DIP (P suffix), 8–pin SOIC (D suffix) and 20–pin PLCC (FN suffix) packages.

- Configuration EPROM for MPA1000 Devices
- Voltage Range — 4.5 to 6.0V
- Maximum Read Current of 10mA
- Standby Current of 10μA, Typical
- Industry Standard Synchronous Serial Interface
- Full Static Operation
- 10MHz Maximum Clock Rate at 5.0V
- Programmable Polarity on Hardware Reset
- Programs With Industry Standard Programmers
- Electrostatic Discharge Protection > 2000 Volts
- 8–Pin PDIP and SOIC; 20–Pin PLCC Packages
- Commercial (0 to +70°C) and Industrial (–40 to +85°C)

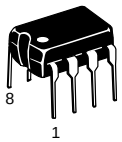




MPA17128
MPA1765

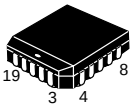
128K, 64K SERIAL EPROM

2



P SUFFIX
PLASTIC PACKAGE
CASE 626–05

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–05



FN SUFFIX
PLCC PACKAGE
CASE 775–02

PIN NAMES

Pins	Function
DATA	Data I/O
CLK	Clock
RESET/OE	Reset Input and Output Enable
CE	Chip Enable Input
VSS	Ground
CEO	Chip Enable Output
VPP	Programming Voltage Supply
VCC	+4.5 to 6.0V Power Supply
NC	Not Connected

MOTOROLA

Table 2–1. MAXIMUM RATINGS*

Parameter	Value	Unit
V_{CC} and Input Voltages W.R.T. V_{SS}	–6.0 to V_{DD} + 0.6	V
V_{PP} Voltage W.R.T. V_{SS} During Programming	–0.6 to +14.0	V
Output Voltage W.R.T. V_{SS}	–0.6 to V_{CC} + 0.6	V
Storage Temperature Range	–65 to +150	°C
Ambient Temperature With Power Applied	–65 to +125	°C
Soldering Temperature of Leads (10 Seconds)	+300	°C
ESD Protection on All Leads	≥2	kV

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

2

Table 2–2. DC CHARACTERISTICS (V_{CC} = 4.5 to 6.0V; Commercial (C) T_A = 0 to +70°C; Industrial (I) T_A = –40 to +85°C)

Symbol	Characteristic		Min	Max	Unit	Condition
V_{IH}	Input Voltage High	DATA, CE, CEO, Reset	2.0	V_{CC}	V	
V_{IL}	Input Voltage Low	DATA, CE, CEO, Reset	–0.3	0.8	V	
V_{OH}	Output Voltage High	DATA, CE, CEO, Reset	3.86 2.40		V	I_{OH} = –4mA; V_{CC} ≥ 4.5V
V_{OL}	Output Voltage Low	DATA, CE, CEO, Reset		0.32	V	I_{OL} = 4.0mA
I_{LI}	Input Leakage Current		–10	10	µA	V_{IN} = 0.1V to V_{CC}
I_{LO}	Output Leakage Current		–10	10	µA	V_{OUT} = 0.1V to V_{CC}
C_{INT}	Internal Capacitance	(All Inputs/Outputs)		10	pF	V_{CC} = 5.0V (Note 1); T_A = 25°C; f_{clk} = 1MHz
I_{CC} Read	Operating Current			10	mA	V_{CC} = 6.0V; CLK = 10MHz
I_{CCS}	Standby Current			500	µA	V_{CC} = 6.0V

1. This parameter is initially characterized and not 100% tested.

Applications Information

DATA

Three–state DATA output for reading and function as the input during programming.

CLOCK

Clock input. Used to increment the internal address and bit counters for reading and programing.

RESET/$\overline{OE}$

Reset and Output Enable input. A Low level both the $\overline{CE}$ and RESET/OE inputs enables the data output driver. A High level on RESET/OE resets both the address and bit counters. In the MPA17128, the logic polarity of this input is programmable as either RESET/OE or OE/RESET. This document describes the pin as RESET/OE although the opposite polarity is also possible, this option is defined and set at device program time.

$\overline{CE}$

Chip Enable input. Used for device selection. A Low level on both CE and OE enables the data output driver. A High level on CE disables both the address and bit counters and forces the device into a low power mode.

$\overline{CEO}$

Chip Enable Out output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as CE and OE are both Low. It will then follow CE until OE goes High. Thereafter CEO will stay High until the entire PROM is read again. This pin also used to sense the status of RESET polarity when program mode is entered.

V_{PP}

Programming Voltage Supply. Used to enter programming mode (+10V) and to program the memory (+13V) Must be connected directly to V_{CC} for normal Read operation. No overshoot above +15.5V permitted.

USING THE MPA17000 WITH MPA1000 DEVICES

Connections between the MPA devices and the Serial EPROMs are:

- The DATA output of the MPA17000 drives D0 (data in).
- The CLK input of the MPA17000 is driven by the data clock DCLK output.
- MPA17000s can be cascaded using the $\overline{CEO}$ output to drive the CE input of the next MPA17000.
- For normal Read operations V_{PP} must be connected to V_{CC}. Do not leave V_{PP} open.

The connections between an MPA device and an MPA17000 device are shown in Figure 2–1. The MPA D[0] line is connected to the MPA17000 CLK. At power–up or upon reconfiguration, the MEMCE signal goes Low, enabling the MPA17000 DATA output. During the configuration process, D[0] reads data from the MPA17000 on every rising DCLK edge. The MEMCE signal goes High at the end of configuration and resets the internal address counters of the MPA17000.

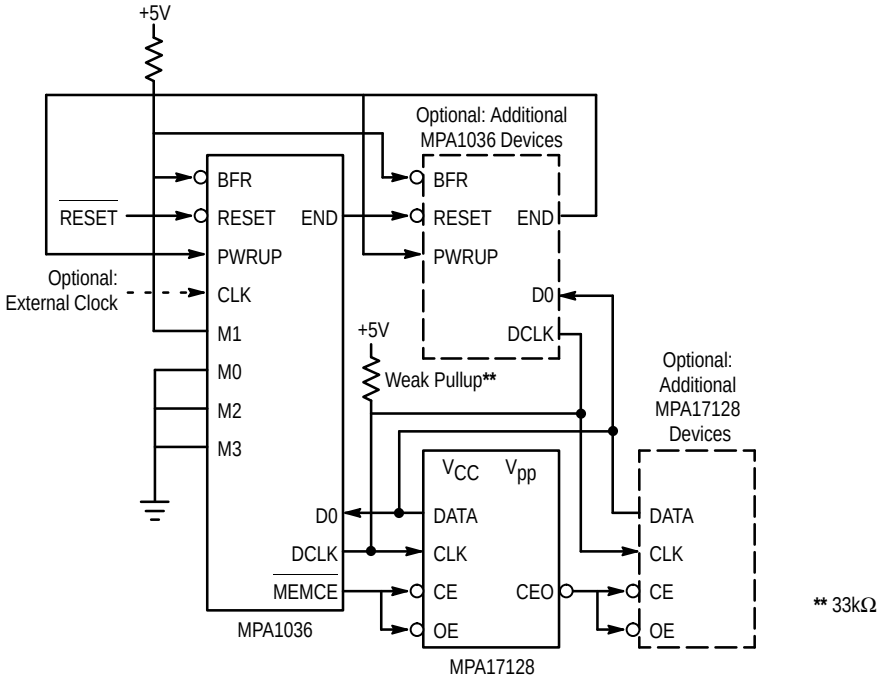


Figure 2–1. MPA1036 Configuration Using MPA17128 Serial EPROM

Cascading Serial Configuration PROMs

Cascading MPA17000s provide additional memory for multiple MPA1000s or for MPA1000s requiring larger configuration memories.

When the last bit from the first MPA17000 is read, the next clock signal to the MPA17000 asserts its CEO output Low and disables its DATA line. The second MPA17000 recognizes the Low level on its CE input and enables its DATA output. (See Figure 2–1).

Additional logic may be required if cascaded memories are so large that the rippled chip enable is not fast enough to activate successive MPA17000s.

STANDBY MODE

The MPA17128 enters a low power standby mode whenever CE is High. In standby mode, the MPA17000 consumes less than 500µA of current. The output will remain in a high impedance state regardless of the state of the OE input.

PROGRAMMING MODE

Programming mode is entered by holding V_{PP} High for at least two clock edges and is exited by removing power from the device or by a Low on both CE and OE. Figure 2–4 through Figure 2–9 shows the programming algorithm.

MPA17128 RESET POLARITY

The MPA17128 lets the user choose the reset polarity as either RESET/OE or OE/RESET. Any third–party commercial programmer should prompt the user for the desired reset polarity.

The programming of the overflow word should be handled transparently by the PROM programmer; it is mentioned here as supplemental information only.

The polarity is programmed into the first overflow word location, max address+1. 00000000 in these locations makes the reset active Low, FFFFFFFF in these locations makes the reset active High. The default condition is RESET active High.

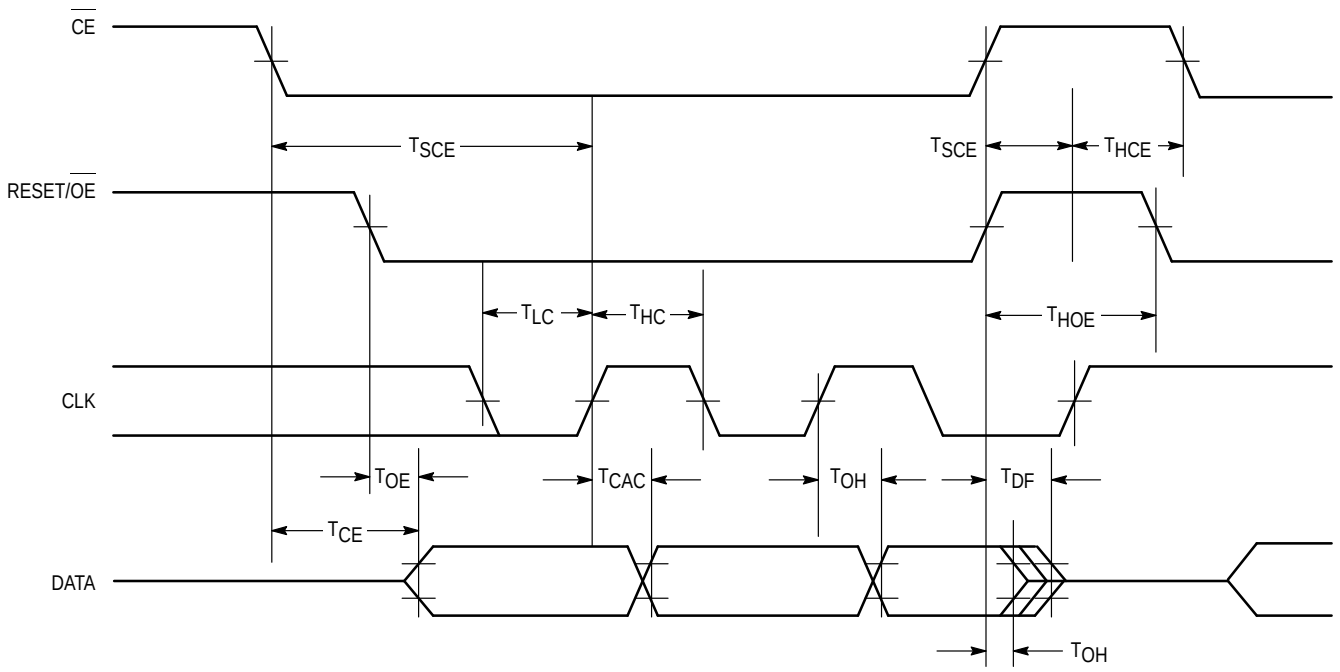


Figure 2–2. AC Characteristics Over Operating Conditions

Table 2–3. AC OPERATING CONDITIONS

Symbol	Parameter	Limit 4.5V ≤ V_{CC} ≤ 6.0V		Unit	Condition
		Min	Max		
T_{OE}	OE to Data Delay		45	ns	
T_{CE}	CE to Data Delay		50	ns	
T_{CAC}	CLK to Data Delay		60	ns	
T_{OH}	Data Hold From OE, CE or CLK	0		ns	
T_{DF}	OE or CE to Data Float Delay		50	ns	Note 1
T_{LC}	CLK Low Time	25		ns	Note 2
T_{HC}	CLK High Time	25		ns	Note 2
T_{SCE}	CE Setup Time to CLK (To Guarantee Proper Counting)	25		ns	
T_{HCE}	CE Hold Time to CLK (To Guarantee Proper Counting)	0		ns	Note 2
T_{HOE}	OE High Time (Guarantees Counters are Reset)	20		ns	Note 2
CLK_{max}	Clock Frequency		10	MHz	

1. Float delays are measured with minimum tester AC load and maximum DC load.
2. Guarantee by design, not tested.

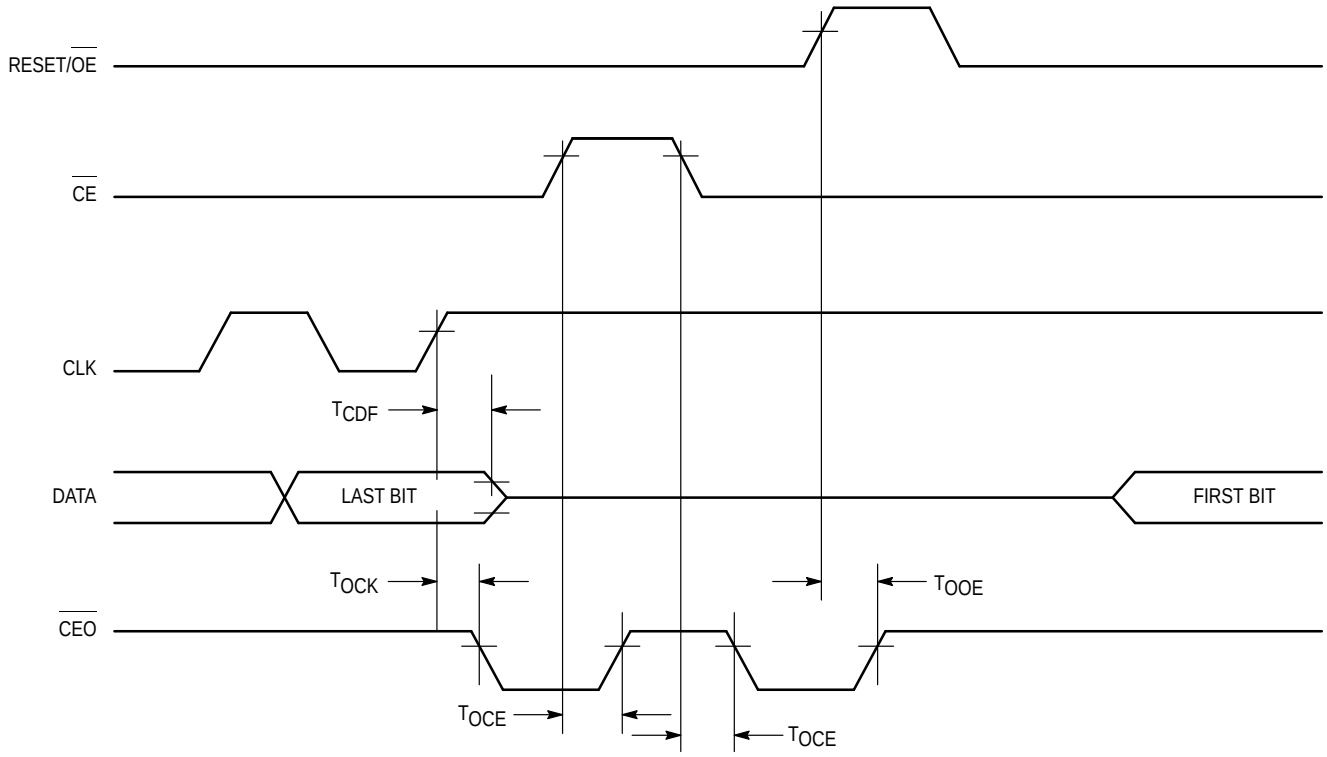


Figure 2–3.

Table 2–4.

Symbol	Parameter	Limit 4.5V ≤ V_{CC} ≤ 6.0V		Unit	Condition
		Min	Max		
T_{CDF}	CLK to Data Float Delay		50	ns	
T_{OCK}	CLK to CEO Delay		40	ns	
T_{OCE}	CE to CEO Delay		40	ns	
T_{OOE}	RESET/OE to CEO Delay		40	ns	

Table 2–5. PIN ASSIGNMENTS IN THE PROGRAMMING MODE

Pin Name	DIP	PLCC	I/O	Function
DATA	1	2	I/O	The rising edge of the clock shifts a data word in or out of the PROM one bit at a time.
CLK	2	4	I	Clock input. Used to increment the internal address/word counter for reading and programming operation.
RESET/$\overline{OE}$	3	6	I	The rising edge of CLK shifts a data word into the PROM when $\overline{CE}$ and $\overline{OE}$ are High; it shifts a data word out of the PROM when $\overline{CE}$ is Low and $\overline{OE}$ is High. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held High and $\overline{OE}$ is held Low. Note: Any modified polarity of the RESET/$\overline{OE}$ pin is ignored in the programming mode.
$\overline{CE}$	4	8	I	The rising edge of CLK shifts a data word into the PROM when $\overline{CE}$ and $\overline{OE}$ are High; it shifts a data word out of the PROM when $\overline{CE}$ is Low and $\overline{OE}$ is High. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held High and $\overline{OE}$ is held Low.
GND	5	10	—	Ground pin.
$\overline{CEO}$	6	14	O	The polarity of the RESET/$\overline{OE}$ pin can be read by sensing the $\overline{CEO}$ pin. Note: The polarity of the RESET/$\overline{OE}$ pin is ignored while in the programming mode. In final verification, this pin must be monitored to go Low one clock cycle after the last data bit has been read.
V_{PP}	7	17	—	Programming Voltage Supply. Programming mode is entered by holding $\overline{CE}$ and $\overline{OE}$ High and V_{PP} at V_{PP1} for two rising clock edges and then lowering V_{PP} to V_{PP2} for one more rising clock edge. A word is programmed by strobing the device with V_{PP} for the duration TPGM V_{PP} must be tied to V_{CC} for normal operation.
V_{CC}	8	20	—	+5 V power supply input.

Table 2–6. DC PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Limit		Unit	Condition
		Min	Max		
V_{CCP}	Supply Voltage During Programming	5.0	6.0	V	
V_{IL}	Input Voltage Low	0	0.5	V	
V_{IH}	Input Voltage High	2.4	V_{CC}	V	
V_{OL}	Output Voltage Low		0.4	V	
V_{OH}	Output Voltage High	3.7		V	
V_{PP1}	Programming Voltage	12.5	13.5	V	Note 1
V_{PP2}	Programming Mode Access Voltage	V_{CCP}	V_{CCP} + 1	V	
I_{PPP}	Supply Current in Programming Mode		100	mA	
I_L	Input or Output Leakage Current	–10	10	µA	
V_{CCL}	First Pass Supply Voltage Low for Final Verification	2.8	3.0	V	
V_{CCH}	Second Pass Supply Voltage High for Final Verification	6.0	6.2	V	

1. No overshoot is permitted on this signal. V_{PP} must not be allowed to exceed V_{PP1} max.

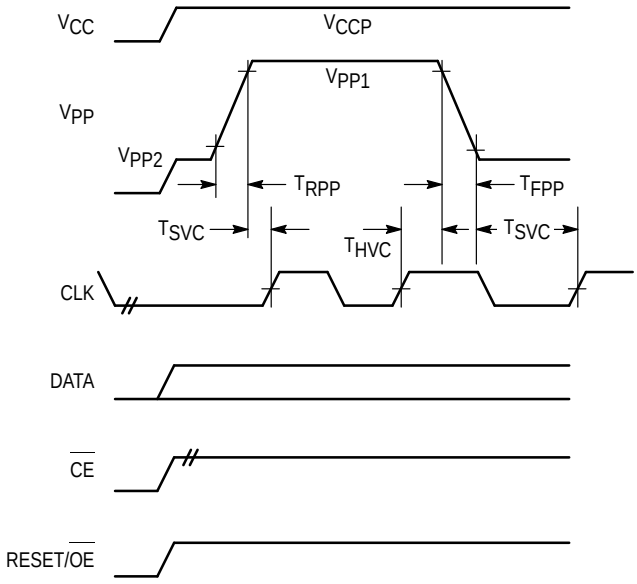


Figure 2–4. Enter Programming Mode

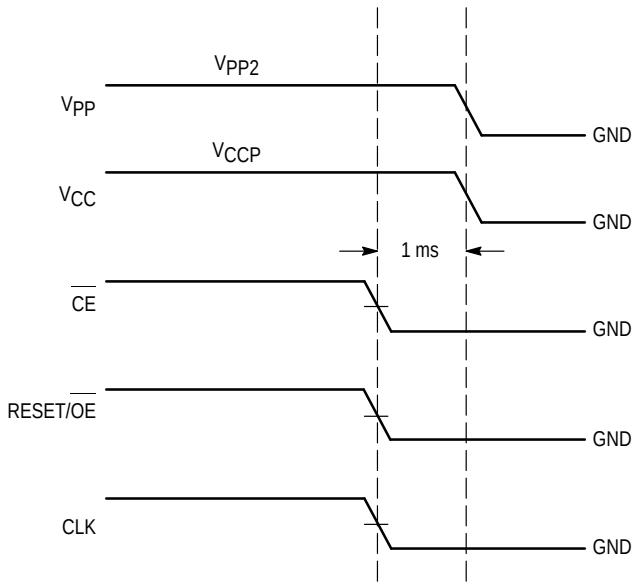


Figure 2–5. Exit Programming Mode

2

Table 2–7. AC PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Limit		Unit	Condition
		Min	Max		
T_{RPP}	Rise Time of V_{PP} (10 to 90%)	50		ns	
T_{FPP}	Fall Time of V_{PP} (90 to 10%)	50		ns	
T_{PGM}	V_{PP} Programming Pulse Width	0.95	1.05	ms	
T_{SVC}	V_{PP} Setup to CLK for Entering Programming Mode	100		ns	
T_{HVC}	V_{PP} Hold from CLK for Entering Programming Mode	300		ns	
T_{SDP}	Data Setup to CLK for Programming	50		ns	
T_{HDP}	Data Hold from CLK for Programming	0		ns	
T_{SCC}	$\overline{CE}$ Setup to CLK for Programming/Verifying	100		ns	Note 1
T_{HCC}	$\overline{CE}$ Hold from CLK for Programming/Verifying	200		ns	
T_{SCV}	$\overline{CE}$ Setup to V_{PP} for Programming	100		ns	
T_{HCV}	$\overline{CE}$ Hold from V_{PP} for Programming	50		ns	
T_{SIC}	$\overline{OE}$ Setup to CLK for Incrementing Address Counter	100		ns	
T_{HIC}	$\overline{OE}$ Hold from CLK for Incrementing Address Counter	0		ns	
T_{CAC}	CLK to Data Valid		400	ns	
T_{OH}	Data Hold from CLK	0		ns	
T_{CE}	$\overline{CE}$ Low to Data Valid		250	ns	

1. While in programming mode, CE should only be changed while CLK is High and has been High for 200ns.

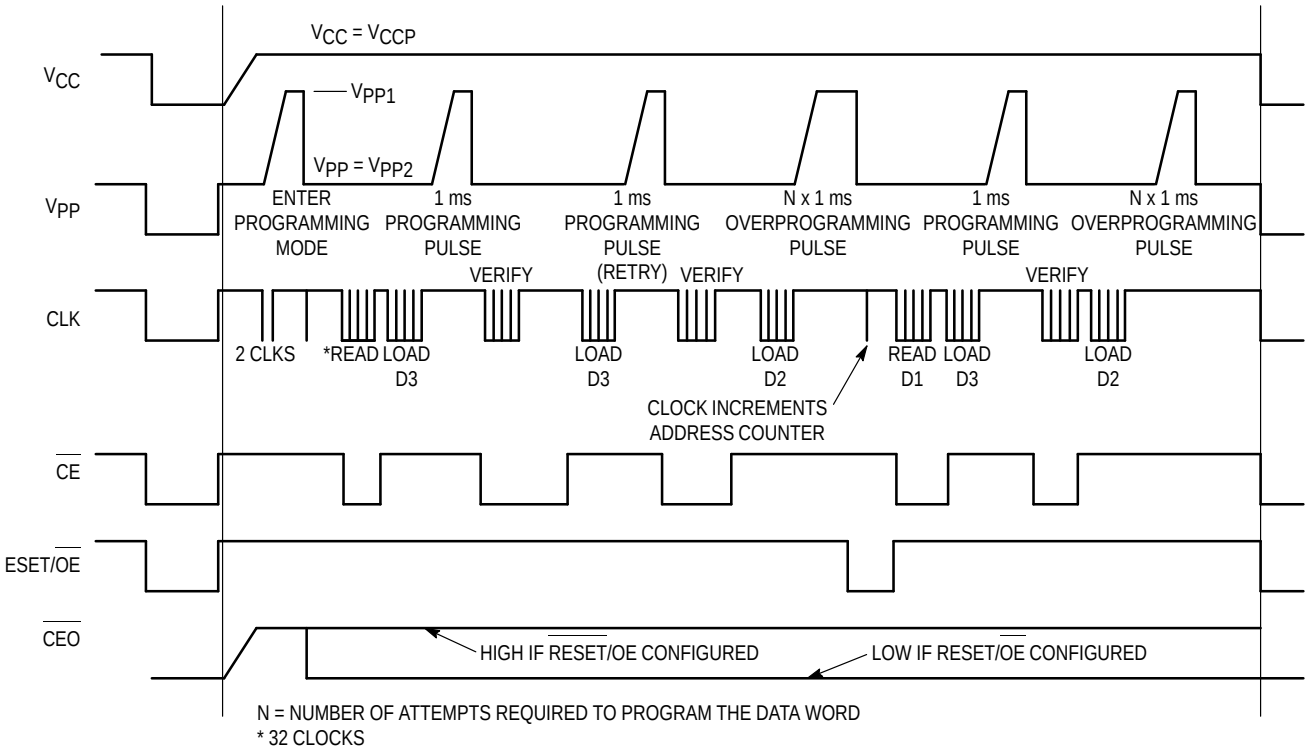


Figure 2–6. Programming Cycle Overview

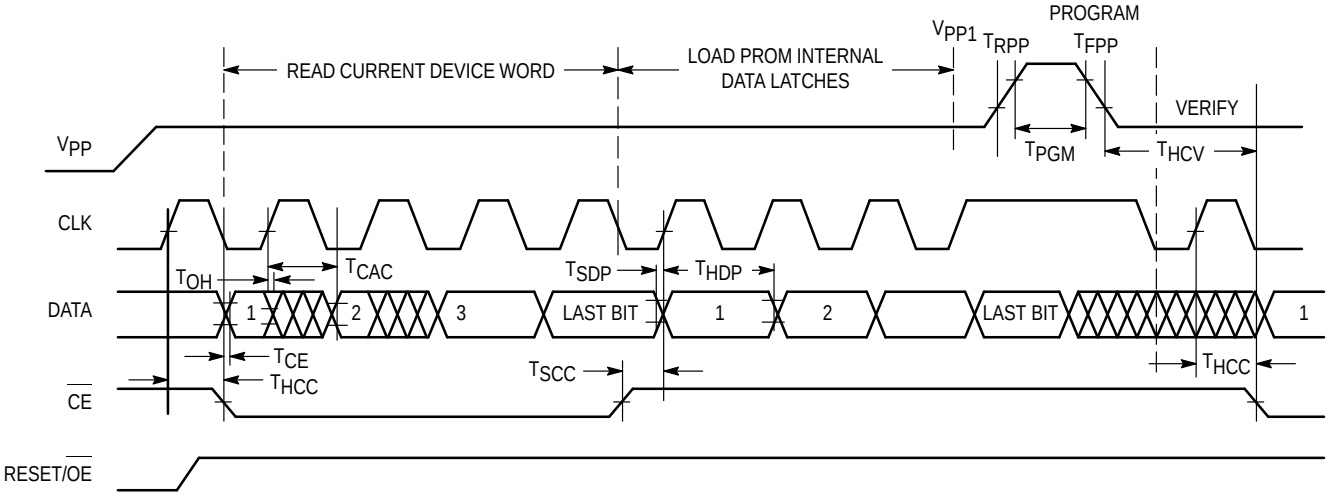


Figure 2–7. Details of Read/Program/Verify Cycle

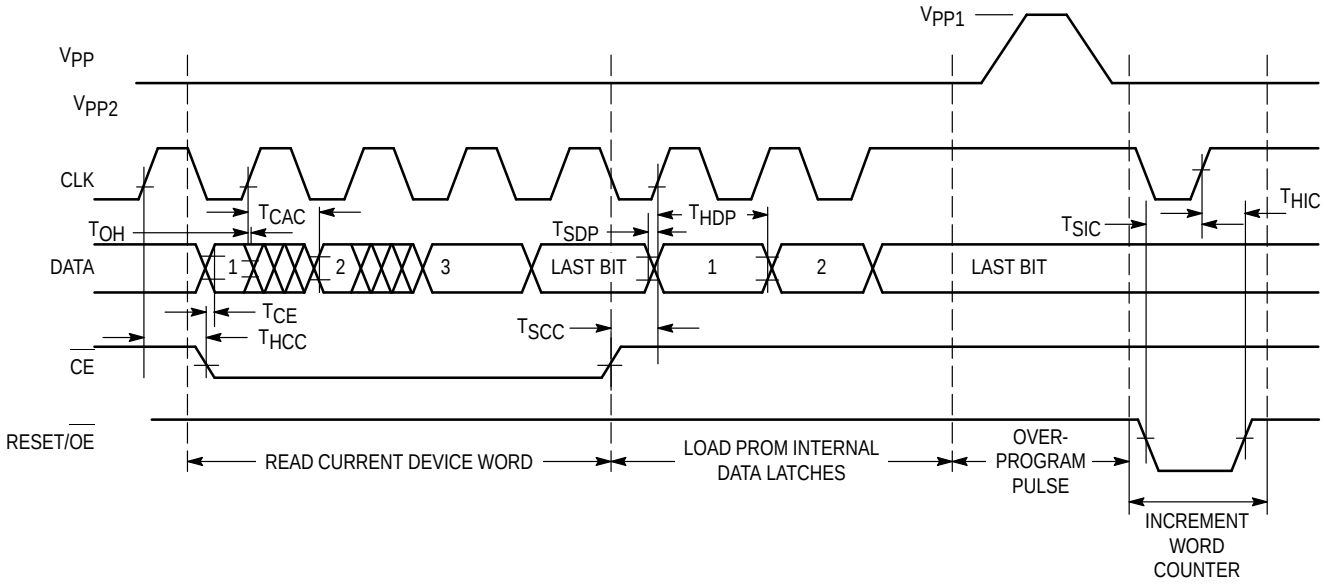


Figure 2–8. Overprogramming Detail

2

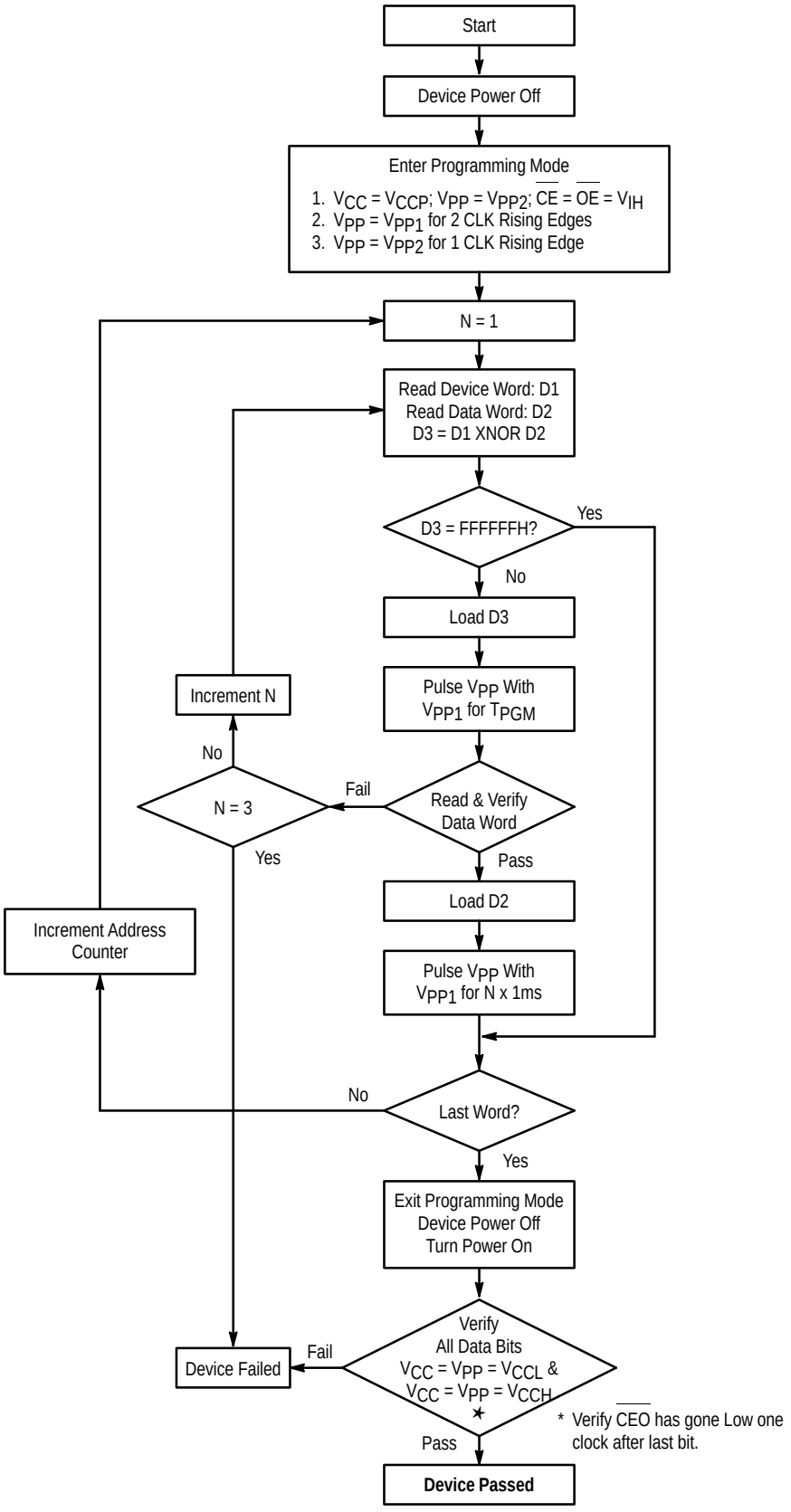
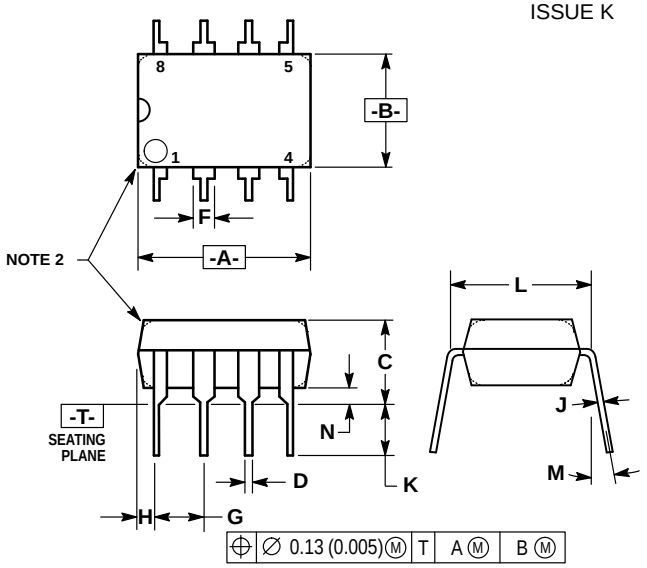


Figure 2–9. MPA17128 Programming Spec

OUTLINE DIMENSIONS

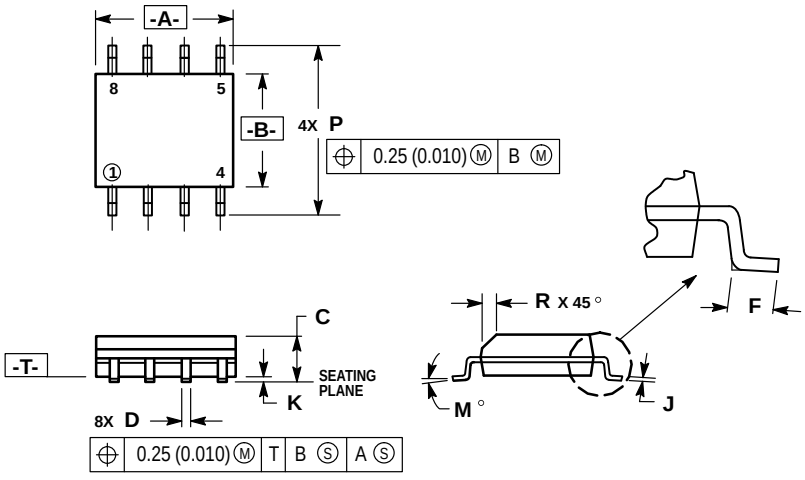
P SUFFIX
PLASTIC PACKAGE
CASE 626-05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05
ISSUE M

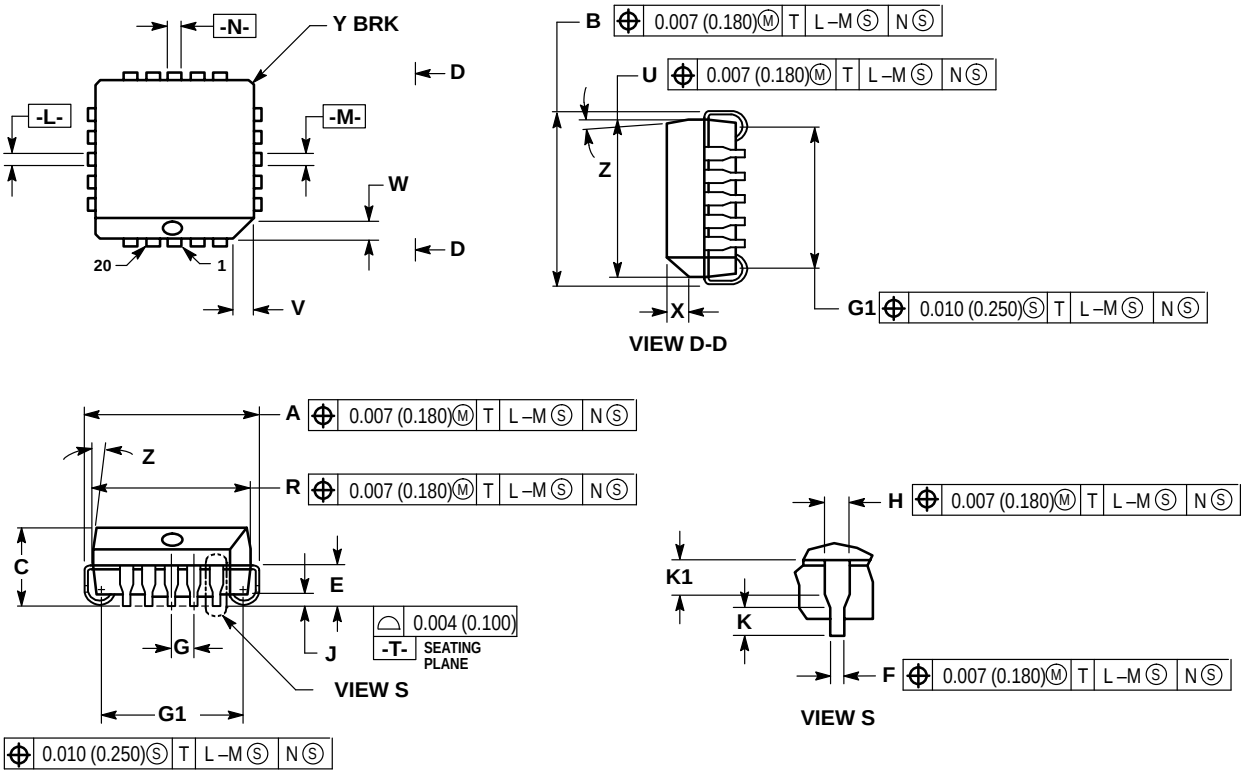


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

OUTLINE DIMENSIONS

FN SUFFIX
PLCC PACKAGE
CASE 775-02
ISSUE C



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

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