MPC1100-54-0000

High-Efficiency, Non-Isolated, Fixed Ratio 300W Digital DC/DC Power Module

NOT RECOMMENDED FOR NEW DESIGNS. REFER TO MPC1100A-54-0000

DESCRIPTION

The MPC1100-54-0000 is a high-efficiency, non-isolated LLC-DCX power card module with a fixed 10:1 transformer turns ratio. It operates from a 40V to 60V DC primary bus and a 4V to 6V output voltage. It can deliver up to 300W of power.

The MPC1100-54-0000 employs MPS's MP2981 (a digital LLC controller) and MP8500 (a smart synchronous rectifier). These devices can adjust the PWM to optimize the MPC1100-54-0000, and ensure the MPC1100-54-0000 works at resonant frequency.

The built-in, multiple-time programmable (MTP) memory can store and restore device configurations. The fault status, input and output voltage, current, and temperature can be easily monitored via the PMBus/I²C interface. The MPC1100-54-0000 is available in a surface-mount (27mmx18mmx6mm) package.

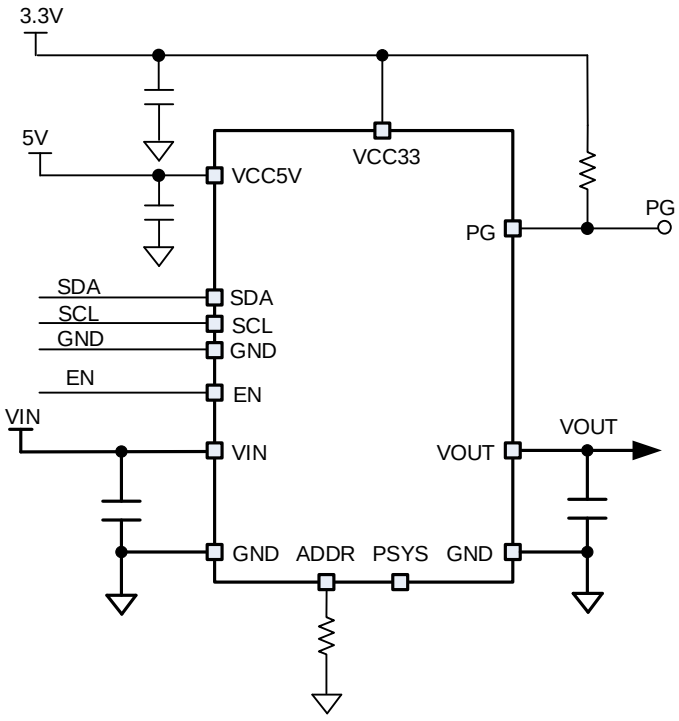
FEATURES

- Up to 60A Continuous Secondary Current
- PMBus/I²C Compliant
- Built-In MTP to Store Custom Configurations
- Monitoring for Input Voltage, Output Voltage, Output Current, Output Power, and Temperature
- V_{IN} UVLO, Output OVP/UVP, OCP_TDC/OCP_SPIKE, and OTP Protections
- Available in a Surface-Mount (27mmx18mmx6mm) Package

APPLICATIONS

- Datacenters
- DC Power Distribution
- High-End Computing Systems

TYPICAL APPLICATION



NOT RECOMMENDED FOR NEW DESIGNS. REFER TO MPC1100A-54-0000

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPC1100-54-0000	Surface-Mount	MPC1100-54	3

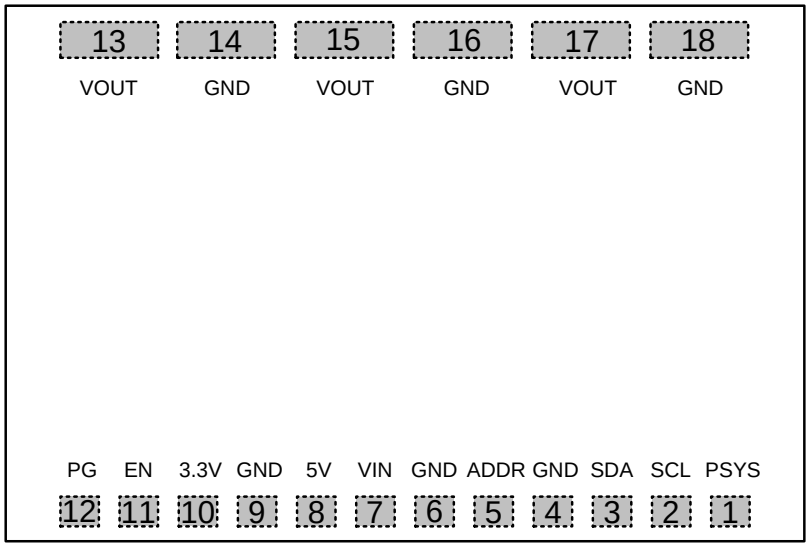
*For Tape & Reel, add suffix –Z (e.g. MPC1100-54-0000–Z).

TOP MARKING

Date code
Vendor's serial number
LOT ID
MPC1100-54

PACKAGE REFERENCE

TOP VIEW



Surface-Mount (27mmx18mmx6mm)

PIN FUNCTIONS

Pin #	Name	I/O	Description
1	PSYS	A[O]	**Output power indicator.** Current-source output. Connect a resistor to GND to convert this current to a voltage signal.
2	SCL	D[I/O]	**PMBus/I²C clock signal.**
3	SDA	D[I]	**PMBus/I²C data signal.**
5	ADDR	A[I]	**PMBus/I²C address 4-LSB pin setting.**
7	VIN	Power	**Input main power supply.**
8	5V	Power	**5V power supply input.** Power supply for primary-side driver. Connect a 1μF capacitor to ground.
10	3.3V	Power	**3.3V power supply input.** Power supply for the controller (MP2981) and synchronous rectifier (MP8500). Connect a 4.7uF capacitor to ground.
11	EN	D[I]	**Enable control.**
12	PG	D[O]	**Power good output.** The output of PG is an open-drain signal.
13, 15, 17	VOUT	Power	**Secondary-side power output.**
4, 6, 9, 14, 16, 18	GND	Power	**Power ground.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +80V
Aux voltage (V_{CC33}) .....-0.3V to +4.0V
Aux voltage (V_{CC5V}) .....-0.3V to +6.5V
Address PIN (ADDR) .....-0.3V to +2.0V
Output voltage (V_{OUT}).....-0.3V to +7.0V
All other pins ..... -0.3V to V_{CC33} + 0.3V
Junction temperature .....150°C
Lead temperature .....260°C

Recommended Operating Conditions (2)

Supply voltage (V_{IN}) .....40V to 60V
Aux voltage (V_{CC33}) .....3.15V to 3.45V
Aux voltage (V_{CC5V}) .....4.5V to 5.5V
Operating junction temp (T_J).... -40°C to +125°C

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.

ELECTRICAL CHARACTERISTICS

V_{CC33} = 3.3V, V_{CC5V} = 5V, V_{IN} = 54V, f_{SW} = 813kHz, current going into the pin is positive, typical values are at T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input						
Input voltage	V_{IN}		40	54	59.5	V
Input current (V_{IN} quiescent current)	I_{VIN_Q}	Disabled, V_{IN} = 54V, EN low, V_{CC33} = 3.3V, V_{CC5V} = 5V			200	µA
Input current at no load	$I_{VIN\_NO\_LOAD}$	Enabled, V_{IN} = 54V, EN high, V_{CC33} = 3.3V, V_{CC5V} = 5V		28		mA
Auxiliary 3.3V Supply						
Supply voltage	V_{CC33}		3.15	3.3	3.45	V
Supply current (V_{CC33} quiescent current)	I_{VCC33_Q}	Disabled, V_{IN} = 54V, EN low, V_{CC33} = 3.3V, V_{CC5V} = 5V		35		mA
Supply current at no load	$I_{VCC33\_NO\_LOAD}$	Enabled, V_{IN} = 54V, EN high, V_{CC33} = 3.3V, V_{CC5V} = 5V		142		mA
Auxiliary 5V Supply						
Supply voltage	V_{CC5V}		4.5	5	5.5	V
Supply current (V_{CC5} quiescent current)	I_{VCC5V_Q}	Disabled, V_{IN} = 54V, EN low, V_{CC33} = 3.3V, V_{CC5V} = 5V			280	µA
Supply current at no load	$I_{VCC5V\_NO\_LOAD}$	Enabled, V_{IN} = 54V, EN high, V_{CC33} = 3.3V, V_{CC5V} = 5V		26		mA
Output						
Transformer ratio	K	Primary side to secondary side, V_{IN} = 54V, I_{OUT} = 0A, K = V_{OUT}/V_{IN}		1/10		
Continuous output current (3)	I_{OUT_DC}	V_{IN} = 54V, T_A = 25°C		47		A
Output current pulse (3)	$I_{OUT\_DC\_PULSE}$	500µs pulse, 40V < V_{IN} < 59.5V	90			A
Output resistance (3)	R_{LL}	V_{IN} = 54V, I_{OUT} = 15A		3		mΩ
Switching frequency	f_{SW}	PMBus/I^2C reading t_{ON}, V_{IN}, I_{OUT} = 1A		813		kHz
Ambient efficiency	η	V_{IN} = 54V, I_{OUT} = 7.5A, T_A = 25°C		94		%
Protection						
Input voltage UVP	V_{IN_UVLO}	I_{OUT} = 0A	35.5	37	39.5	V
Input voltage OVP	V_{IN_OVP}	Latch mode, I_{OUT} = 0A	60	63	66	V
Output voltage UVP	V_{OUT_UVP}	Latch mode, I_{OUT} = 0A		3.0		V
Output voltage OVP	V_{OUT_OVP}	Latch mode, I_{OUT} = 0A		7.2		V
Output current OCP (3)	I_{OUT_OC}	Latch mode			140	A
Over-temperature shutdown threshold (3)	T_{OTP}			130		°C
Over-temperature recovery hysteresis (3)	T_{OTP_HYS}			30		°C
Protection recovery delay time (3)	t_{PRO_DELAY}				12.7	ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC33} = 3.3V, V_{CC5V} = 5V, V_{IN} = 54V, f_{SW} = 813kHz, current going into the pin is positive, typical values are at T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
EN						
Low-voltage input	$V_{IL(EN)}$				0.4	V
High-voltage input	$V_{IH(EN)}$		0.8			V
Enable high leakage	$I_{IH(EN)}$			3	8	µA
Enable delay (3)	t_A	EN high to soft start begins, V_{OUT} = 10%		0.8	1	ms
PSYS						
Output voltage (3)	V_{PSYS}	V_{IN} = 54V, I_{OUT} = 47A, R_{SYS} = 20kΩ		0.634		V
PG Output						
PG low voltage		I_{PG} = 20mA		0.1		V
PG high leakage current	IL_{PG}	V_{PG} = 3.3V	-3		+3	µA
PMBus/I²C DC Characteristics						
High-voltage input (3)	V_{IH}	SCL, SDA	1.35			V
Low-voltage input (3)	V_{IL}	SCL, SDA			0.8	V
Input leakage current		SCL, SDA, ALT#	-10		+10	µA
Pin capacitance (3)	C_{PIN}				10	pF
PMBus/I²C Timing Characteristics (3) (4)						
Operating frequency range	f_{PMB}		10		1000	kHz
Bus free time	t_{BUF}	Between stop and start condition	0.5			µs
Holding time	t_{HD_STA}		0.26			µs
Repeated start condition set-up time	t_{SU_STA}		0.26			µs
Stop condition set-up time	t_{SU_STO}		0.26			µs
Data hold time	t_{HD_DAT}		10			ns
Data set-up time	t_{SU_DAT}		50			ns
Clock low timeout	$t_{TIMEOUT}$		25		35	ms
Clock low period	t_{LOW}		0.5			µs
Clock high period	t_{HIGH}		0.26		50	µs
Clock/data falling time	t_F				120	ns
Clock/data rising time	t_R				120	ns

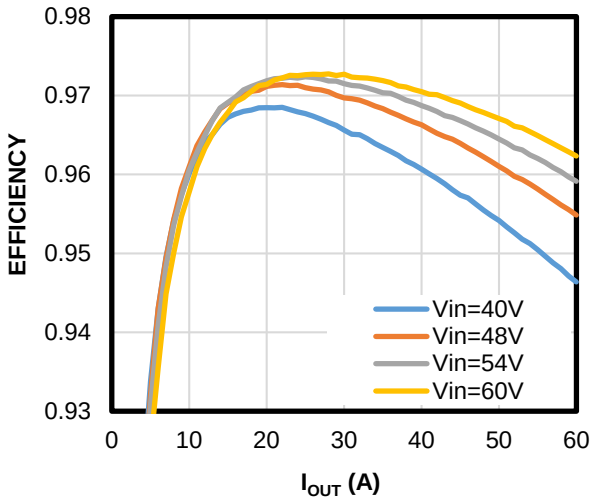
Notes:

3) Guaranteed by design or characterization data. Not tested in production.
4) The device supports 100kHz, 400kHz, and 1MHz bus speeds. The PMBus/I²C timing parameters in this table are for operation at 400kHz and 1MHz. If the PMBus/I²C operating frequency is 100kHz, refer to SMBus specifications for the timing parameters.

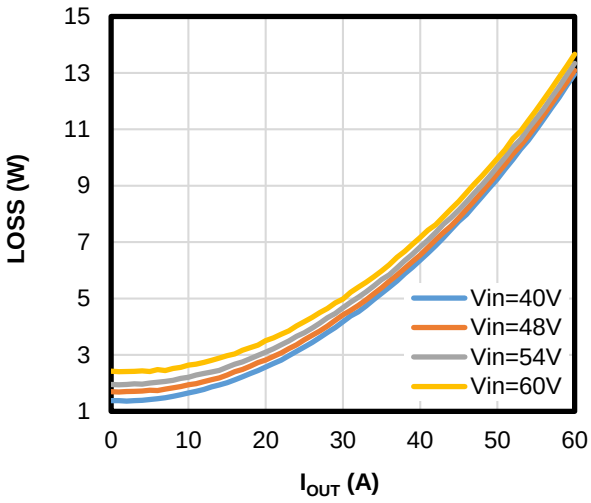
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C.

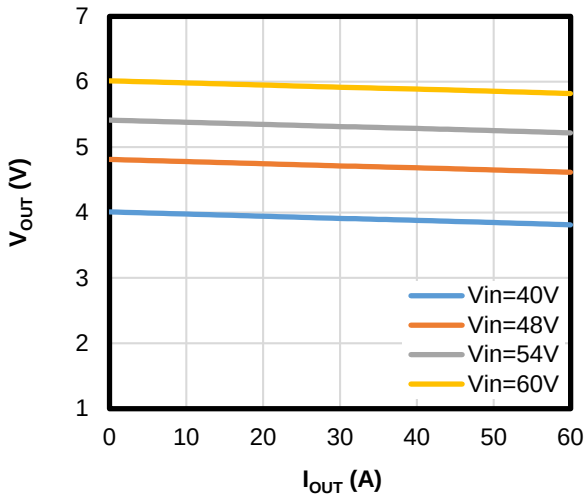
Efficiency vs. Output Current



Power Loss vs. Output Current



Output Voltage vs. Output Current

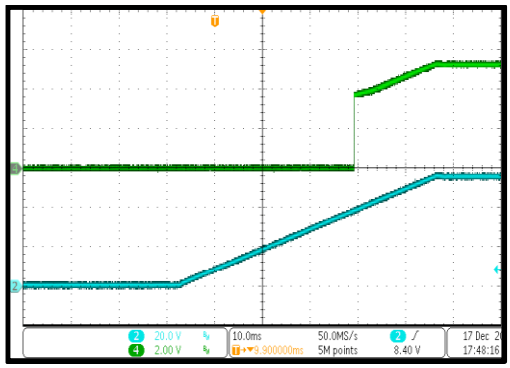


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

T_A = 25°C.

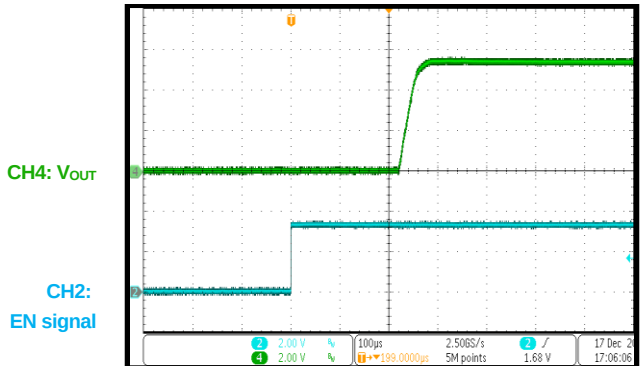
Input Voltage Start-Up

V_{IN} = 54V, I_{OUT} = 60A, full load



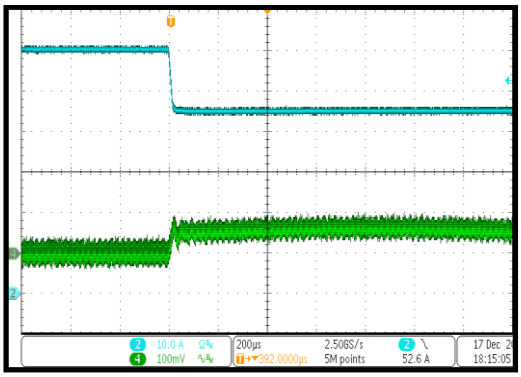
Remote On/Off

V_{IN} = 54V, I_{OUT} = 60A, full load



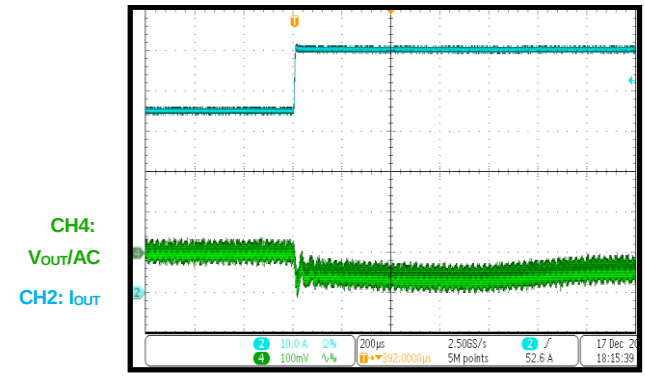
Transient Response

V_{IN} = 54V, 1A/µs step change in load from 100% to 75% of I_{O_MAX}



Transient Response

V_{IN} = 54V, 1A/µs step change in load from 75% to 100% of I_{O_MAX}



FUNCTIONAL BLOCK DIAGRAM

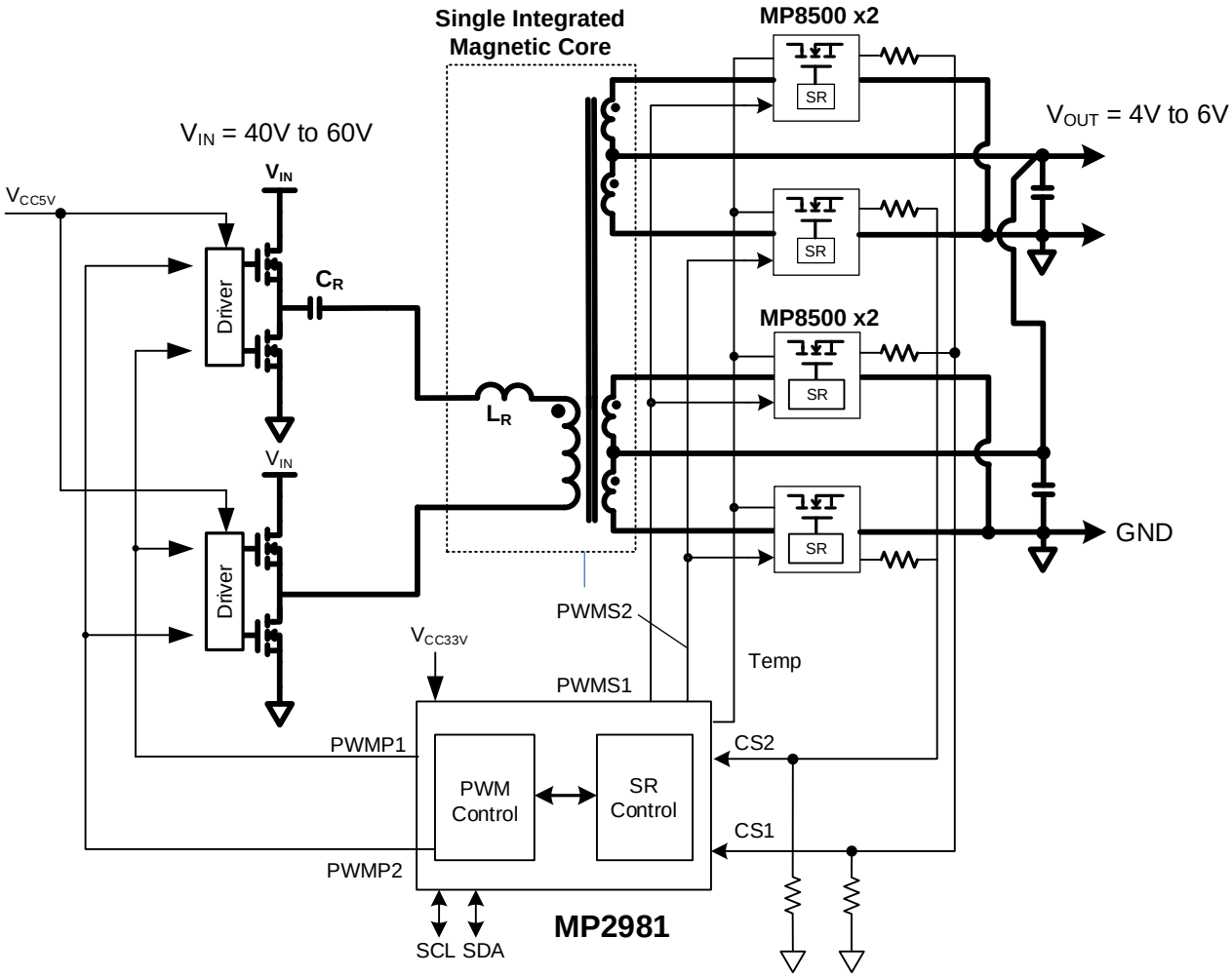


Figure 1: Functional Block Diagram

OPERATION

The MPC1100-54-0000 is a full-bridge LLC-DCX power converter module with a 10:1 transformer turns ratio. Its controller is the MP2981 digital LLC controller, which provides two PWM channels for primary-side control, and two PWM channels for secondary-side control.

The resonant frequency (f_R) can be calculated with Equation (1):

$$f_R = \frac{1}{2\pi\sqrt{L_R \times C_R}} \quad (1)$$

The LLC circuit is most efficient when working at the resonant frequency (see Figure 2). L_R and C_R have tolerances and temperature shifts that may cause the operating frequency to shift away from the resonant frequency.

With MPS's MP8500 (a smart synchronous rectifier), the MPC1100-54-0000 can be optimized to work at the resonant frequency, which improves the module's efficiency.

The MP8500 (4 MP8500 devices work with the MPC1100-54-0000) supports accurate current-sense functionality. Its CS pin sources a current that is proportional to the output current (5µA/A), and generates a voltage by connecting a resistor to GND. The MP2981 can use this signal to monitor and report the output current, as well as protect the MPC1100-54-0000 power card module.

The MP8500 can also send a zero-current detection threshold (ZCD) signal to the MP2981 once a 0A current is detected. Then the MP2981 aligns the PWM off time and ZCD signal by fine-tuning the PWM on time (t_{ON}) to let the MPC1100-54-0000 work at the resonant frequency.

During the dead time, the transformer magnetizing inductor current discharges the FET's output capacitor to zero before the FET turn on. This helps the FET achieve zero-voltage switching (ZVS) on its primary side. The MP8500 turns off once zero current is detected, and then zero-current switching (ZCS) is implemented.

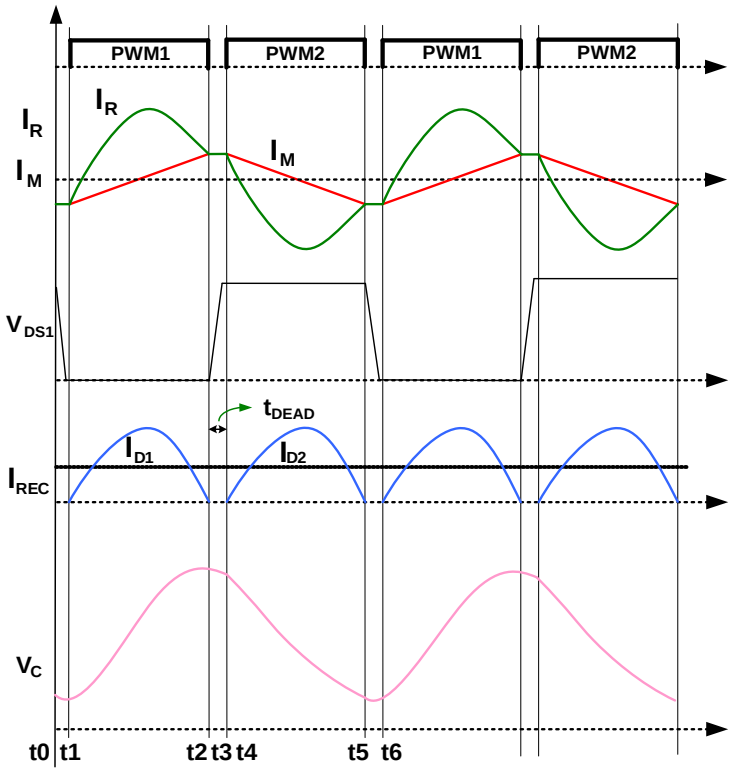


Figure 2: LLC Waveform

Power-On Sequence

MTP Operation

The MP2981 uses an MTP to store the application configuration parameters, including soft-start timing, switching frequency, and protection parameters. The default values are preconfigured during manufacturing. The data can be reconfigured using the STORE_USER_ALL command (17h) or STORE_ALL command (15h) via the PMBus/I²C.

The configurations are restored by the MTP during the power-on sequence, or by receiving the RESTORE_USER_ALL command (18h) or RESTORE_ALL command (16h) from the PMBus/I²C. Figure 3 shows the system state machine of the MPC1100-54-0000 (ENABLE_CMD means MSB of 01H is 1, MEMORY_OK means MTP has no signature error or CRC error, or MTP fault state is cleared after copying MTP).

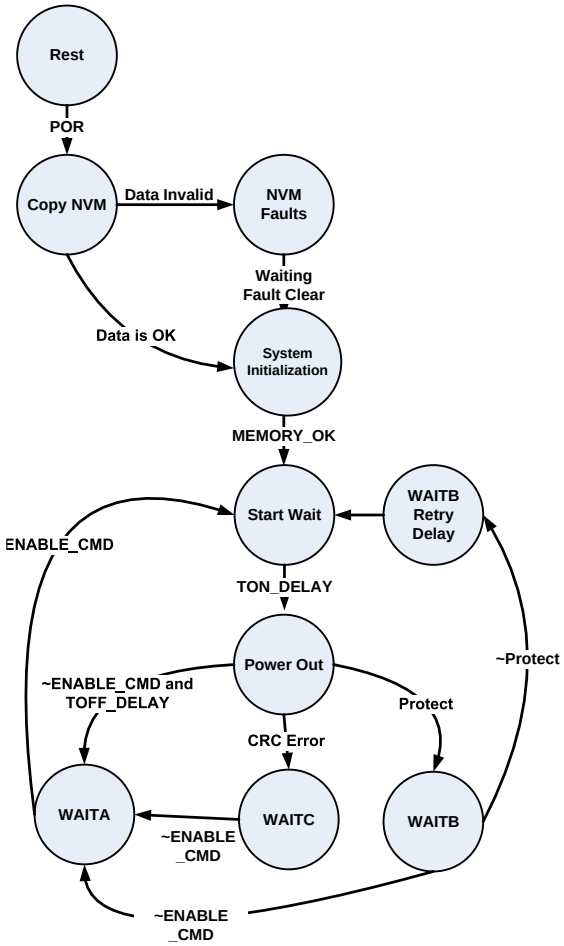


Figure 3: System State Machine

The operation of the MTP can be easily accomplished with MPS's GUI software. The MTP can be subject to more than 100,000 erase and write cycles.

Power-On Sequence

After VDD33 is ready, the internal reset of the MP2981 is released, and the clock starts ticking (see Figure 4). The MP2981 begins to copy data regardless of the EN pin's state. Then the MPC1100-54-0000 can be powered on by EN turning on, pulling VIN high, or by receiving an ON command.

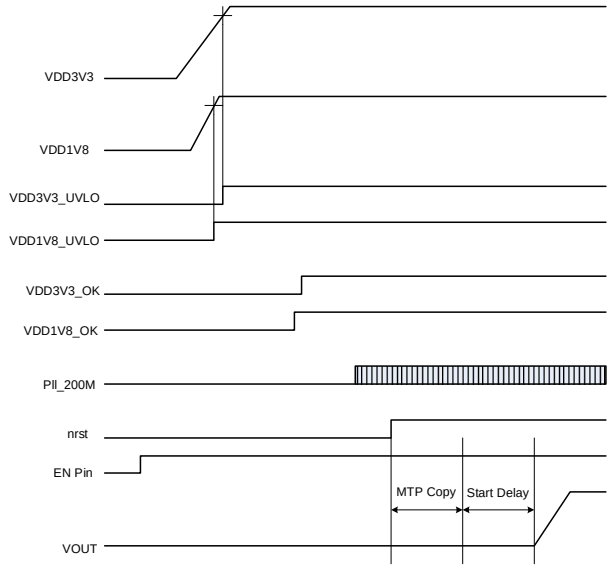


Figure 4: MP2981 Power-On Sequence

Soft Start

The MP2981 adopts PWM mode for the first PWM cycle during soft start. In the first t_{ON} increasing stage, PWM is run at the maximum frequency. The PWM on time begins at TON_MIN_LIM (1Fh, bits[13:8]) and increases to TON_MIN (1Ch).

The first dead time value is (TON_MIN + DEAD_TIME (1Bh) - TON_MIN_LIM), and it decreases to DEAD_TIME (1Bh), which is the normal working value. The frequency stays the same.

During the second t_{ON} increasing stage, the PWM frequency is reduced from its maximum to the resonant frequency. t_{ON} increases from TON_MIN to TON_NORMAL (1Eh), and the dead time is fixed. This helps reduce the inrush current during the first PWM cycles during soft

start, when compared to the traditional soft start method.

Primary ZCD Loop

The MP2981 detects ZCD signal from SR and adjusts PWM frequency to resonant value according to ZCD. ZCD going high (or low, selected by SEL_ZCD_NEG (0Fh, bits[14])), means that the SR current goes negative. Both phases have their own ZCD. They can be enabled together or separately (0Fh, bits[6:5]).

The valid area for detecting ZCD is set by 0Bh. For more details, see the Register Map section on page 25. If the ZCD edge shows up in the valid setting area, t_{ON} decrease by WEIGHTN_ZCD (29h, bits[15:8]). If not, t_{ON} increases by WEIGHTP_ZCD (29h, bits[6:0]). The adjusting speed is determined by register 29h. After 256 continuous valid ZCD pulses, including phase 1 and phase 2, t_{ON} is reduced by 5ns. If no valid ZCD occurs within 256 continuous PWM pulses, including phase 1 and phase 2, then t_{ON} increases by 5ns.

This function can be limited by the sampled SR current. The TDC current must be within the light-load and heavy-load limitations defined by register 0Ch if the load limit is enabled (0Ch, bits[4]). If the CS1 pin current is below CMP_CS1_ENTERFREQ (1Ah, bit[8] and 1Ah, bits[3:0]) in the corresponding valid area, or if the TDC current is below or equal to the level set by MFR_IOUT_LEVEL_L (49h, bits[7:0]), the ZCD adjusting frequency is held if LOADLOW_ZCDLOOP_EN (0Ch, bit[15]) is not enabled since SR ZCD is not accurate under light-load conditions.

If the t_{ON} difference between neighboring PWM periods is within ZCDLOOP_HYS (0Bh, bits[10:8]) for 256 PWM periods, the frequency is stable unless load changes. t_{ON} can be locked if ZCDLOOP_LATCHTON_EN (0Ch, bit[5]) is high. The synchronized ZCD in the MP2981 is delayed from SR current ZCD timing. The final t_{ON} can be cut off by TON_ZCDLOOP_DEC (0Fh, bits[11:8]) if ZCDLOOP_LATCHTON_EN (0Ch, bit[5]) is enabled.

Fault Monitoring and Protections

The MPC1100-54-0000 monitors the input voltage, output voltage, output current, MP8550 temperature, and MP2981 die temperature.

The MPC1100-54-0000 also supports various fault monitoring and protections, including V_{IN} under-voltage lockout (UVLO), V_{IN} over-voltage protection (OVP), over-current protection (OCP) spike, OCP thermal design current (TDC), output OVP, under-voltage protection (UVP), OTP (over-temperature protection), and DrMOS fault protection.

V_{IN} Under-Voltage Lockout (UVLO) and Over-Voltage Protection (OVP)

The input voltage is sensed and monitored by the ADC. The ADC sensed input voltage is converted to an unsigned binary format (READ_VIN (0.125V/LSB, 88h)) using the value set by VIN_CAL_GAIN (3Ah), which is proportional to the input voltage divider.

The READ_VIN value is compared with the VIN_ON (35h) and VIN_OFF (36h) values to control the input voltage under-voltage lockout (UVLO) threshold. If V_{IN} is below or equal to VIN_ON when the device is off (PWM is not generated during this time) or V_{IN} drops below VIN_OFF at any time, V_{IN} UVLO occurs (see Figure 5). The only exception is when MTP is copying at start-up.

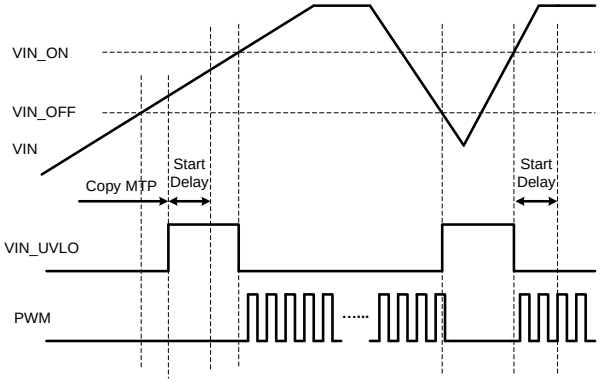


Figure 5: V_{IN} UVLO

V_{IN} UVLO is also enabled when both the DISABLE_ALL_PRO (68h, bit[0]) and RST_VIN_PRO (68h, bit[4]) are low. V_{IN} UVLO resets all shutdown protections. The chip restarts if V_{IN} ramps up, EN is on, and there is no off command.

When V_{IN} exceeds VIN_OV_FLT_LIM (40h), V_{IN} over-voltage protection (OVP) occurs, and the chip shuts down. OVP does not occur when the MTP is being restored during start-up. It is controlled by register 68h, bits[5:4] and 68h, bit[0].

V_{OUT} Under-Voltage Protection (UVP) and Over-Voltage Protection (OVP)

Output over-voltage (OV) and under-voltage protection (UVP) are designed to protect the output fault status. If V_{OUT} exceeds the VOUT_MAX value, the chip shuts down immediately. Based on the mode set by the VOUT_OVP_MAX_LATCH bit, the part responds by going into latch or hiccup mode. It can also take no action if OVP is disabled.

The OVP_MAX threshold (OVP1) has eight options ranging between 1V and 1.7V, with 0.1V/step. The over-voltage threshold (OVP2) has four tracking options: 110%, 120%, 130%, and 140% of the reference voltage (V_{REF}).

If V_{OUT} drops quickly and falls below the UVP_MIN threshold, the device shuts down after a short delay time (6Dh, bits[5:0]) (see Figure 6). The under-voltage threshold (UVP) has four tracking options: 90%, 80%, 70%, and 60% of the reference voltage (V_{REF}). Level 2 UVP (UVP2), also called V_{OUT} low protection, has four thresholds: 0.3V, 0.4V, 0.5V, and 0.6V.

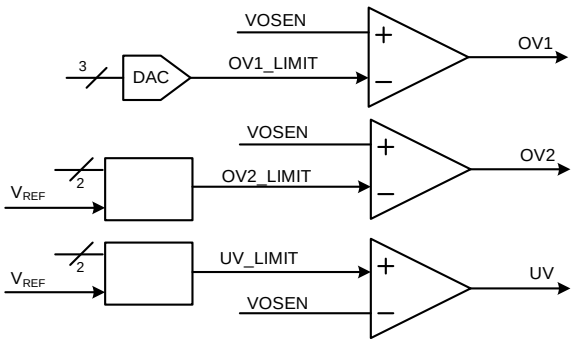


Figure 6: OVP1 & OVP2, UVP Protection Circuit

Over-Current Protection (OCP) Thermal Design Current (TDC)

All parallel SR DrMOS currents of the same phase flow together into their own CS register (R_{CS}). Two-phase CS voltages are added after the low pass filter, and are then outputted on the IMON pin after a three-time buffer.

The ADC samples the IMON voltage (see Figure 7). Then the digital part calculates (38h and 39h) READ_IOUT (8Ch) from the ADC result (9Bh), which is compared to the output current limit (6Ah) to determine whether an over-current condition has occurred.

If the thermal design current (TDC) stays high for longer than the set time (6Ah), this protection could shut down the module.

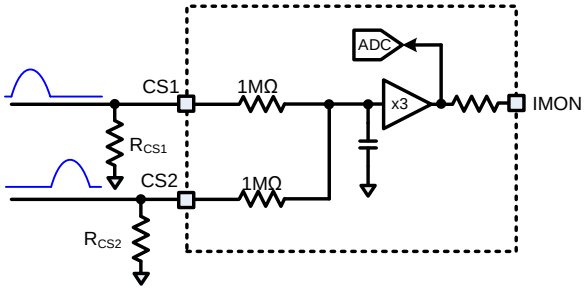


Figure 7: IMON Pin

Over-Current Protection (OCP) Spike

Over-current protection is designed to limit the output current when the load consumes more current than the circuit can handle. The MP8500's CS pin sources a current that is proportional to the output current (5µA/A), and generates a voltage by connecting a resistor refer to GND. The CS pins (CS1 and CS2) of both phases are compared to peak CS levels (OCSPK_H and OCSPK_L) (see Figure 8).

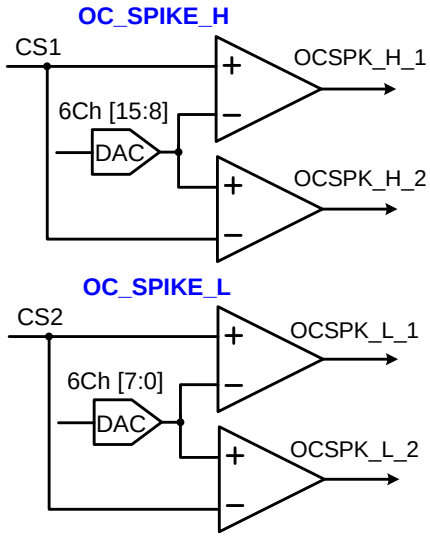


Figure 8: OC Spike Comparators

If the current drops to the lower level, the t_{ON} accumulator decreases by the weight of WEIGHT_OCSPK_L (32h) (see Figure 9). When it decreases to a sufficient value, t_{ON} decreases by 5ns. The minimum t_{ON} value is TON_MIN (1Ch). In each PWM cycle, the t_{ON} values for both phases are the same.

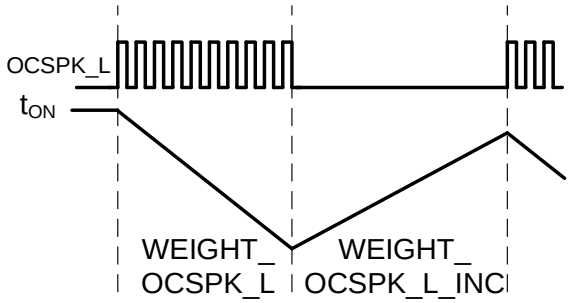


Figure 9: OCSPK_L

The two OC spikes cannot shut off the chip directly.

When the OC conditions are removed, t_{ON} gradually increases to the original value of WEIGHT_OCSPK_H or WEIGHT_OCSPK_L. The greater OC value has the higher priority.

The SR_PWM (PWM pin for MP8500) pins are designed to be able to turn off later than the PWMP (PWM signal for primary edge) pins on the MP2981 during an OC spike to reduce the SR current flowing through diodes. This is set by register 08h bits[15:12] and bits[6:4]. See the Register Map section on page 23 for more details.

Over-Temperature Protection (OTP)

The SR temperature and controller die temperature are both sensed by the ADC. These values trigger different responses that are independent from one another. However, the device will enter latch or hiccup mode if either condition is triggered.

The MP8500 sends the temperature-sense signal for the MP2981's TEMP pin. If the MP8500 triggers a CS fault and enters a protection mode, it pulls the TEMP pin to 3.3V. The MP2981 must have a half-divider on the TEMP pin, and then it can send the signal for the comparator and ADC.

MTP Fault

If the data in the MTP is determined to be invalid by the CRC, then the system enters the MTP fault state and waits for the error to be cleared.

Communication Failure

A data transmission fault occurs when information is not properly transferred between the devices. There are several data transmission faults, listed below:

- Sending too little data
- Reading too little data
- Host sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command codes

PMBus/I²C Communication

The MPC1100-54-0000 supports real-time monitoring for the VR operation parameters and status with PMBus/I²C.interface. Table 1 lists the monitored parameters.

Table 1: PMBus/I²C Monitored Parameters

Parameter	PMBus/I²C
Output voltage	62.5mV/LSB
Output current	0.25A/LSB
Temperature	1°C
Input voltage	0.125V/LSB
Die temperature	1°C
OVP	✓
UVP	✓
OCP	✓
OTP	✓
V_{IN} UVLO	✓
V_{IN} OV	✓
CML	✓

PMBus/I²C Interface

To support multiple VR devices using the same PMBus/I²C interface, the register MFR_ADDR_PMBus or the ADDR pin can program the PMBus/I²C address.

The address is a 7-bit code. The 3MSB bit is set by the register. The 4LSB bit address can either be set by the register or by the ADDR voltage. Address 00h is reserved as an all-call address, which can be set for a single chip.

The ADDR voltage is set by the voltage divider from the VDD18 voltage. Table 2 shows the resistor values for different PMBus/I²C addresses when 3MSB bit is set to 3'b010.

Table 2: Setting the PMBus/I²C Address (4LSB)

PMBus/I²C Address	Setting Point (V)	R_{TOP} (kΩ) 1%	R_{BOTTOM} (kΩ) 1%
20h	0	-	0
21h	0.031	33.2	0.576
22h	0.055	33.2	1.05
23h	0.084	33.2	1.62
24h	0.115	33.2	2.26
25h	0.156	33.2	3.16
26h	0.203	33.2	4.22
27h	0.266	33.2	5.76
28h	0.338	33.2	7.68
29h	0.432	33.2	10.5
2Ah	0.542	33.2	14.3
2Bh	0.677	33.2	20.0
2Ch	0.845	33.2	29.4
2Dh	1.049	33.2	46.4
2Eh	1.301	33.2	86.6
2Fh	1.549	33.2	20.5

There is a total of 5 transmission structures, listed below:

1. Send command only
2. Write byte
3. Write word
4. Read byte
5. Read word

To read or write the MPC1100-54-0000 registers, the PMBus/I²C or I²C command must be compliant with the byte number of the register in the table of PMBus/I²C memory Page 0 commands/registers.

The PMBus/I²C communication frequency can support 1MHz.

Figure 10 shows the supported PMBus/I²C transmission structure without packet error checking (PEC).

Figure 11 shows the supported PMBus/I²C transmission structure with PEC.

The PMBus/I²C or I²C commands and register map of the MPC1100-54-0000 is the same as the MP2981. Refer the MP2981 datasheet for additional details.

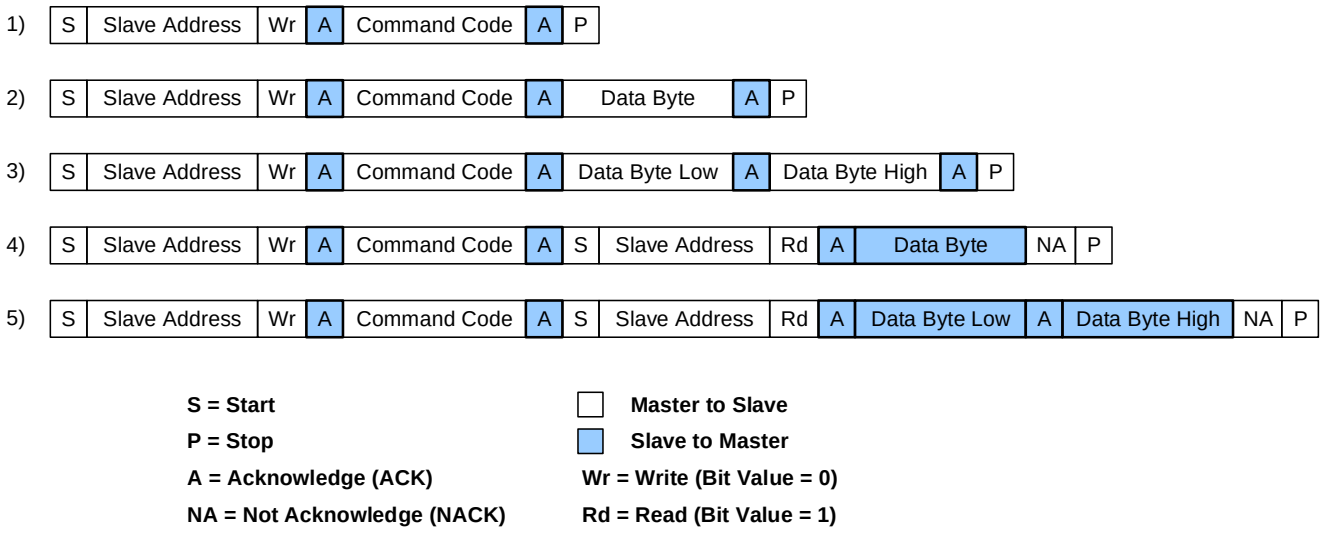


Figure 10: Supported PMBus/I²C Transmission Structure without PEC

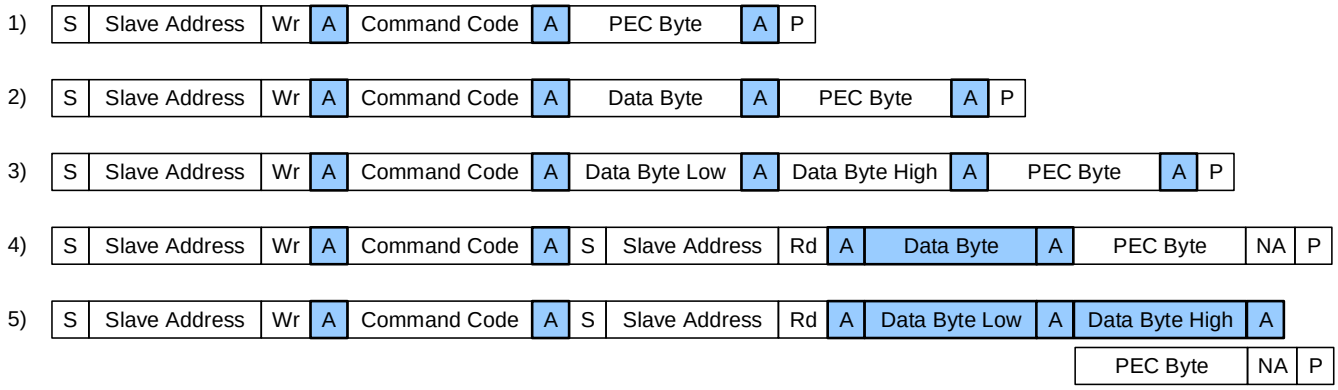


Figure 11: Supported PMBus/I²C Transmission Structure with PEC

PMBUS/I²C MEMORY PAGE 0 COMMANDS/REGISTERS

Command Code	Command Name	Type	Bytes
0x00	PAGE	R/W	1
0x01	OPERATION	R/W	1
0x03	CLEAR_FAULTS	Send	0
0x04	CTRL_PWM	R/W	2
0x05	MFR_ADC_HOLD_TIME	R/W	1
0x06	CTRL_VR	R/W	2
0x07	CTRL_MTP	R/W	2
0x08	CTRL_OC	R/W	2
0x09	LOW_POWER_SET_BIT	R/W	1
0x0b	ZCD_TIME_SET	R/W	2
0x0c	ZCD_LOOP_SET	R/W	2
0x0e	SKIP_SR_PWM_SET	R/W	2
0x0f	CTRL_PWM_BK	R/W	2
0x15	STORE_ALL	Send	0
0x16	RESTORE_ALL	Send	0
0x17	STORE_USER_ALL	Send	0
0x18	RESTORE_USER_ALL	Send	0
0x19	MFR_VOUT_SEL	R/W	2
0x1A	MFR_IOUT_SEL	R/W	2
0x1B	DEAD_TIME	R/W	1
0x1C	TON_MIN	R/W	2
0x1D	TON_MAX	R/W	2
0x1E	TON_NORMAL	R/W	2
0x1F	TON_MIN_LIM	R/W	2
0x21	MFR_REF_CONFIG	R/W	2
0x22	VOUT_TRIM	R/W	1
0x25	TRANSFORMER_RATIO	R/W	2
0x29	WEIGHT_ZCD	R/W	2
0x2A	SR_PWM_SETA_PRIDRV	R/W	2
0x2B	SS_SRNEG_SET	R/W	2
0x2C	SR_PWM_SETB	R/W	2
0x2D	MFR_SLOPE_SR	R/W	2
0x2E	MFR_SLOPE_BLK	R/W	2
0x2F	PRISETBLK_WEIGHT_SS	R/W	2
0x30	WEIGHT_2_1	R/W	2
0x31	WEIGHT_4_3	R/W	2
0x32	WEIGHT_OCSPK_L_N	R/W	2
0x33	WEIGHT_OCSPK_INC	R/W	2
0x34	MFR_VIN_DROP_SET	R/W	2
0x35	VIN_ON	R/W	2
0x36	VIN_OFF	R/W	2
0x38	IOUT_CAL_GAIN	R/W	2
0x39	IOUT_CAL_OFFSET	R/W	2

PMBUS/I²C MEMORY PAGE 0 COMMANDS/REGISTERS *(continued)*

Command Code	Command Name	Type	Bytes
0x3A	VIN_CAL_GAIN	R/W	2
0x3B	VOUT_CAL_GAIN	R/W	2
0x40	VIN_OV_FLT_LIM	R/W	2
0x42	TEMP_GAIN_OFFSET	R/W	2
0x43	DIETEMP_GAIN_OFFSET	R/W	2
0x44	MFR_USER_PWD	W	2
0x45	MFR_MTP_WP	R/W	1
0x46	SKIPDRMOS_SR_ERARLI	R/W	2
0x49	MFR_IOUT_LEVEL	R/W	2
0x4B	MFR_VCAL_I_MAX	R/W	2
0x4C	DC_TRIM	R/W	1
0x50	MPS_CODE	R/W	2
0x51	PRODUCT_CODE	R/W	2
0x52	CONFIG_ID	R/W	2
0x53	CONFIG_REV	R/W	2
0x5A	CALVO_LOW_TON_SS_L	R/W	2
0x5B	TON_SS_H	R/W	2
0x5E	POWER_GOOD_ON	R/W	2
0x5F	POWER_GOOD_OFF	R/W	2
0x60	PROTECT_DELAY	R/W	1
0x62	PWRGD_DELAY	R/W	1
0x63	START_DELAY	R/W	2
0x64	OFF_DELAY	R/W	2
0x65	MFR_OTP_SET	R/W	2
0x66	MFR_DIE_OTP_SET	R/W	2
0x67	PMBUS/I²C_ADDR_SET	R/W	1
0x68	MFR_PROTECT_CFG	R/W	2
0x69	OVP_UVP_VID_SET	R/W	2
0x6A	OCP_TDC_SET	R/W	2
0x6B	OCP_SPIKE_TIMES_SET	R/W	2
0x6C	OCP_SPIKE_LEVEL	R/W	2
0x6D	UVP_MIN_SET	R/W	1
0x79	STATUS_WORD	R	2
0x7A	STATUS_VOUT	R	1
0x7B	STATUS_IOUT	R	1
0x7C	PROTECT_SIG_GRP	R	2
0x7D	STATUS_TEMP	R	1
0x7E	STATUS_CML	R	1
0x80	SYS_STATE_DBG	R	1
0x81	FINAL_PMBUS/I²C_ADDR	R	1
0x82	REG_LAST_FAULT_MTP	R	2

PMBUS/I²C MEMORY PAGE 0 COMMANDS/REGISTERS *(continued)*

Command Code	Command Name	Type	Bytes
0x88	READ_VIN	R	2
0x8B	READ_VOUT	R	2
0x8C	READ_IOUT	R	2
0x8D	READ_TEMP	R	1
0x8E	READ_DIE_TEMP	R	1
0x90	USER_KEY_INPUT	W	2
0x96	READ_POUT	R	2
0x99	VIN_SENSE	R	2
0x9A	VOUT_SENSE	R	2
0x9B	IOUT_SENSE	R	2
0x9C	TEMP_SENSE	R	2
0x9D	DIE_TEMP_SENSE	R	2
0x9E	TON_PWMP	R	2
0x9F	TON_SR_PWM	R	2
0xF1	CLR_LAST_FAULT_WMTP	Send	0
0xF2	READ_LAST_FAULT_TRIG	Send	0
0xF3	CLEAR_STORE_FAULTS	Send	0
0xF4	CLEAR_MTP_FAULTS	Send	0

PAGE 0 REGISTER MAP

PAGE (00h)

The PAGE command configures, controls, and monitors the device through only one physical address to support normal operation, testing, and debugging.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function							PAGE	

Bits	Bit Name	Description
7:2	RESERVED	Unused. Bits[7:2] must be all 0 when changing [1:0].
1:0	PAGE	2'b00: Page 0. Normal and trim registers (read/write registers) can be stored in the MTP 2'b01: Page 1. Unused 2'b10: Page 2. Each PMBus/I^{2}C command (not including (00h)) will directly read/write the MTP cells 2'b11: Page 3. Debugging/testing registers. Not stored in the MTP Users should only use Page 0 to avoid entering test mode.

OPERATION (01h)

The OPERATION command turns the output on or off by working with the EN pin. The unit stays in the commanded operating mode until another different OPERATION command is sent, or the state of EN changes.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function								

Bits	Bit Name	Description
7	OPERATION	1'b1: Turn on 1'b0: Turn off
6:0	RESERVED	Unused. R/W bits are available, but these bits do not change the device.

CLEAR_FAULTS (03h)

This command clears any fault bit in the following status registers: STATUS_WORD(79h), STATUS_VOUT(7Ah), STATUS_IOUT(7Bh), STATUS_TEMP(7Dh), and STATUS_CML(7Eh).

This command is write-only. There is no data byte for this command.

CTRL_PWM (04h)

This command controls PWM operation. The positive and negative edges of the SR_PWM pins (SR_PWMs) can be adjusted using the PWMP pins. The SR_PWMs can be made to turn off earlier or later than the time set by the PWMP pins.

Command	CTRL_PWM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
14	SKIP_SS_EN	Enable bit to set the SKIP_EN pin high during soft start. 1'b1: Enable. SKIP_EN pin = high 1'b0: Disable. SKIP_EN pin = low
13	VOUT_SKIP_EN	Enable bit for V_{OUT} skipping. Determines what happens after V_{OUT} ramps above VOUT_SKIP_H (19h, bits[3:2]) and before V_{OUT} ramps below VOUT_SKIP_L (19h, bits[1:0]). 1'b1: Shut down both SR_PWM pins during dead time and after soft start. If 04h[10] = 0, the primary PWMs will also shut off 1'b0: No PWM is shut off
12	CLOSE_LOOP_EN	Enable bit for primary closed loop. 1'b1: Enable 1'b0: Disable
11	ZCD_LOOP_EN	Enable bit for primary zero-current detection (ZCD) loop. 1'b1: Enable 1'b0: Disable
10	VOUT_SKIP_PWMP_EN	Determines how the part responds when V_{OUT} skipping is enabled, and V_{OUT} exceeds its limit. 1'b1: PWMP stays on when V_{OUT} exceeds its limit during skip mode 1'b0: PWMP turns off when V_{OUT} exceeds its limit during skip mode
9	SKIPSR_VIN_DROP_EN	Enable bit to shut off SR_PWM when the chip detects that V_{IN} is dropping quickly, or VOSEN exceeds the V_{IN} ADC value. 1'b1: Enable 1'b0: Disable
8:7	RESERVED	Unused. R/W bits are available, but these bits do not change the device.
6	SR_ADJ_NORMAL_EN	Enable bit to adjust whether the SR_PWMs turn on/off earlier or later. 1'b1: Enable. If bits 0Fh[15] and 04h[4:1] are 1'b1, this bit should be set to 1'b1 1'b0: Disable. If bits 0Fh[15] and 04h[4:1] are 1'b0, this bit should be set to 1'b0
5	SR_NEG_ADJ_SS_EN	Enable bit to shut off SR_PWM later or earlier than PWMP during soft start, according to t_{ON}. This bit is related to 5Ah, 5Bh, and 2Bh. 1'b1: Enable 1'b0: Disable
4	SR_FIXED_DEC_EN	Enable bit to shut off SR_PWM before PWMP at a fixed time. Related to 2Ah. 1'b1: Enable 1'b0: Disable
3	SR_FIXED_EXT_EN	Enable bit to shut off SR_PWM after PWMP at a fixed time. Related to 2Ah. 1'b1: Enable 1'b0: Disable

2	SR_NEG_ADJ_EN	Enable bit to shut off SR_PWM before the next PWMP at a fixed time. Related to 2Ch. 1'b1: Enable 1'b0: Disable
1	SR_POS_DEC_EN	Enable bit to turn on SR_PWM later than PWMP. Related to 2Ch. 1'b1: Enable 1'b0: Disable
0	SR_EN	Enable bit to make SR_PWM equal to PWMP if no other adjusting function is enabled. Only enabled when the part is not in soft start, and 04h[6] = 0. 1'b1: SR_PWM = PWMP 1'b0: SR_PWM = 0

MFR_ADC_HOLD_TIME (05h)

The MFR_ADC_HOLD_TIME command sets the waiting time between finishing one channel sampling and starting the next channel sampling.

Command	MFR_ADC_HOLD_TIME							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	MFR_ADC_HOLD_TIME						

Bits	Bit Name	Description
6:0	MFR_ADC_HOLD_TIME	The time after one channel finishes, and before the next channel starts. 100ns/LSB.

CTRL_VR (06h)

This command configures certain chip functions, excluding pulse-width modulation (PWM).

Command	CTRL_VR															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
14	CHOP_BG	Output to analog to enable bandgap (BG) chop. 1'b1: Enable 1'b0: Disable
13	PSYS_SEL_2W	Selects the PSYS current rate by sending different READ_POUT (96h) data. 1'b1: 2 w/ LSB, send READ_POUT (96h) bits[10:1] to the 10-bit PSYS DAC (digital-to-analog converter) 1'b0: 1 w/ LSB, send 96h[9:0] to the DAC
12	DC_CAL_EN	DC loop enable bit. 1'b1: Enable 1'b0: Disable

11	DIE_TEMP_RATE_NEG	Selects the die temperature V-T (voltage vs. temperature) rate. 1'b1: Negative 1'b0: Positive
10:9	RESERVED	Unused. R/W bits are available, but these bits do not change the device.
8	PMBUS/I²C_ADDR_KEEP_SAMP	1'b1: The ADC constantly samples the ADDRP pin 1'b0: The ADC samples ADDRP only seven times after the MTP address reaches 8'h20
7:4	PMBus/I²C_FILTER_SET	PMBus/I²C filter in digital side. 10ns/LSB.
3	WAIT_VIN_START	1'b1: Wait until V_{IN} is ready (READ_VIN > VIN_ON) before ramping V_{REF} and generating PWMs 1'b0: Do not wait until V_{IN} is ready (READ_VIN > VIN_ON) before ramping V_{REF} and generating PWMs
2	SEL_PWRGD_1REF_0TON	Selects V_{REF} ramping or t_{ON} increasing as the PG reference. 1'b1: V_{REF} 1'b0: t_{ON}
1	MFR_ONOFFDLY_CLK_1L0S	Selects the counting clock for START_DELAY and OFF_DELAY during start-up and shutdown. 1'b1: 20kHz 1'b0: 50kHz
0	KEEP_TON_MIN_LMT_SS	Enable bit for waiting V_{OUT} before increasing t_{ON} during SS. 1'b1: t_{ON} stays at the TON_MIN_LIM (1Fh) value and does not increase until V_{OUT} exceeds VOUT UVP_MIN (19h) 1'b0: t_{ON} does not stay at the TON_MIN_LIM (1Fh) value, and begins increasing before V_{OUT} exceeds VOUT UVP_MIN (19h)

CTRL_MTP (07h)

This command sets the MTP parameters. It is recommended to use the vendor's preset configurations.

Command	CTRL_MTP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															

Bits	Bit Name	Description
15	CRC_FAULT_USER_EN	CRC enable bit for the MTP user. 1'b1: Enable 1'b0: Disable
14	CRC_FAULT_TRIM_EN	CRC enable bit for the MTP trim. 1'b1: Enable 1'b0: Disable
13	CRC_FAULT_TOT_EN	CRC enable bit for the total MTP. Do not set this bit to 1 when using 17h (STORE_USER_ALL) to write MTP. 1'b1: Enable 1'b0: Disable
12	MTP_FAULT_BLOCK_EN	Enable bit that determines whether an MTP fault prevents start-up, including the signature fault and CRC fault. 1'b1: Enable. If an MTP fault occurs, the chip enters the MTP fault state, and a CLEAR_MTP_FAULTS (F4h) command must be sent to exit the state 1'b0: Disable. The chip starts up if an MTP fault occurs

11	LAST_FAULT_BLOCK_EN	Enable bit to prevent start-up if the data read from the MTP LAST_FAULT_ADDR is not 0. 1'b1: Enable. If the last fault exists, the chip must receive a CLEAR_STORE_FAULTS (F3h) command to start up 1'b0: Disable. The chip starts up, even if the last fault exists
10:6	RESERVED	Unused. R/W bits are available, but the bits do not change the device.
5	CAL_FAULT_CRC_DIS	1'b1: Do not include MTP FAULT_RECORD ADDR (the two bytes in MTP that store protection faults such as OVP) when calculating CRC_TOT 1'b0: Include MTP FAULT_RECORD ADDR when calculating CRC_TOT
4	NO_FAULT_STORE	1'b1: Store 00h data to MTP FAULT_RECORD ADDR 1'b0: Store the value of MEMORY ADDR 7Ah to MTP FAULT_RECORD ADDR when storing is not triggered by a fault
3	FAULT_SINGLE_EN	1'b1: Only store the 2-byte MTP FAULT_RECORD ADDR 1'b0: Store the whole third section of the MTP when storing FAULT_RECORD
2	RESERVED	Unused. R/W bits are available, but this bits does not change the device.
1	PROTECT_FAULT_ RECORD_EN	FAULT_RECORD enable bit. 1'b1: Enable 1'b0: Disable
0	MFR_MTP_COPY_EN	Enable bit to read the MTP (16h or 18h or F6h) when the device outputs power; ineffective to READ_LAST_FAULT command (F2h) or the reading MTP commands (16h or 18h or F6h) under Page 2. 1'b1: Enable 1'b0: Disable

CTRL_OC (08h)

This command configures the over-current (OC) spike function. The PWM t_{ON} is reduced when an OC spike occurs, and recovers after the OC spike condition is removed (see Figure 12). This protection cannot shut down the chip directly.

Command	CTRL_OC															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X															

Bits	Bit Name	Description
15:12	SR_DLY_OCSPK	Sets the time lengths of the SR_PWM pins' wait period before turning off after the PWMP pins when an OC spike occurs. If any [6:4] bit is high, there must be a <1Bh (dead time setting). 5ns/LSB.
11:8	TON_MIN_OCSPK_H	When an over-current spike on CS1 (OCSPK_H) occurs, the minimum t_{ON} can be calculated with the equation below: (TON_MIN_OCSPK_H + 1) x 5ns
7	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
6	SR_DLY_OCSPK_H_ SS_EN	Enable bit to turn off the SR_PWM pins later than the PWMP pins when an over-current spike on CS1 (OCSPK_H) occurs during soft start. 1'b1: Enable 1'b0: Disable

5	SR_DLY_OCSPK_H_EN	Enable bit to turn off the SR_PWM pins after the PWMP pins when an over-current spike on CS1 (OCSPK_H) occurs during a time that is not soft start. 1'b1: Enable 1'b0: Disable
4	SR_DLY_OCSPK_L_EN	Enable bit for to turn off the SR_PWM pins after the PWMP pins when an over-current spike on CS1 (OCSPK_H) occurs during normal operation. 1'b1: Enable. SR_DLY_OCSPK_H_EN must be 1'b1 1'b0: Disable
3	OC_TRIG_SR_EN	Enable bit to turn on the SR_PWM pins immediately if they are not on when an over-current spike on CS1 or CS2 (OCSPK_H or OCSPK_L, respectively) occurs while PWMP is on. 1'b1: Enable 1'b0: Disable
2	OCSPK_H_TON_SS_EN	Enable bit to adjust t_{ON} when an over-current spike on CS1 (OCSPK_H) occurs during soft start. 1'b1: Enable 1'b0: Disable
1	OCSPK_H_TON_EN	Enable bit to adjust t_{ON} when an over-current spike on CS1 (OCSPK_H) occurs during a time that is not soft start. 1'b1: Enable 1'b0: Disable
0	OCSPK_L_TON_EN	Enable bit to adjust t_{ON} when an over-current spike on CS2 (OCSPK_L) occurs. This cannot be adjusted during soft start. 1'b1: Enable 1'b0: Disable

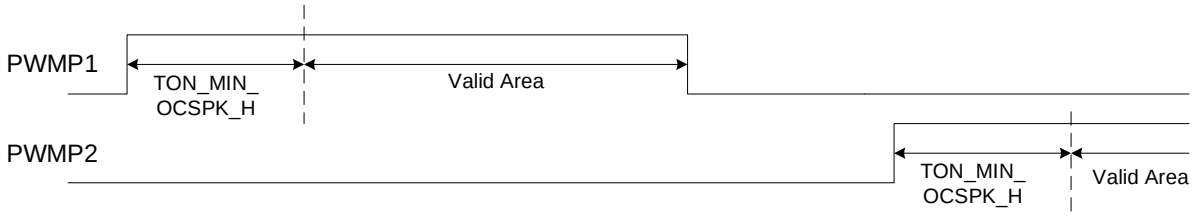


Figure 12: OCSPK_H

LOW_POWER_SET_BIT (09h)

This register controls low-power mode.

Command	LOW_POWER_SET_BIT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R/W	R/W
Function	X	X	X	X	X	X		

Bits	Bit Name	Description
1	RESERVED	Unused. R/W bits are available, but this bits does not change the device.
0	LOW_POWER_SET_BIT	1'b1: The chip remains in low-power mode when the EN pin is low 1'b0: The chip operates normally when the EN pin is low

ZCD_TIME_SET (0Bh)

This command configures the adjusting frequency by the zero-current detection (ZCD) function (primary ZCD loop). Figure 13 shows the valid ZCD1 area for this function. The valid ZCD2 area is determined by SR_PWM2. When ZCD occurs within the valid area, t_{ON} decreases by the weight of WEIGHTN_ZCD (29h, bits[15:8]). When a ZCD event occurs outside the valid area, t_{ON} increases by WEIGHTP_ZCD (29h, bits[6:0]).

If the difference between neighboring t_{ON} values is within ZCDLOOP_HYS (0Bh, bits[10:8]) for more than 256 periods, and there is no load change or another conditional change, frequency adjusting is completed.

Command	ZCD_TIME_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	TON_HYS				ZCD_VALID_DLY			ZCD_BLK_TIME			

Bits	Bit Name	Description
10:8	ZCDLOOP_HYS	When t_{ON} stays between TON_LAST_PERIOD ± ZCDLOOP_HYS for about 256 periods, the loop is stable. 5ns/LSB.
7	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
6:4	ZCD_VALID_DLY	The ZCD valid area after the delayed SR_PWM. 5ns/LSB.
3:0	ZCD_BLK_TIME	The beginning area of SR_PWM is invalid for ZCD. 10ns/LSB. The ZCD blanking time can be calculated with the following equation: ZCD blank time = (ZCD_BLK_TIME x 2 + 1) x 5ns

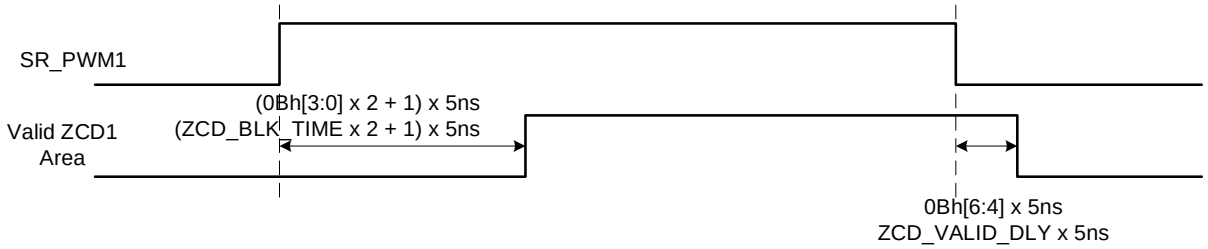


Figure 13: Valid ZCD1 Area for ZCD Loop Function

ZCD_LOOP_SET (0Ch)

This command configures the adjusting frequency via the zero-current detection (ZCD) function (primary ZCD loop). If ZCDLOOP_LATCHTON_EN (0Ch, bit[5]) is enabled, and the frequency adjustment finishes (t_{ON} keeps inside hysteresis for more than 256 periods), t_{ON} is fixed to TON_ZCDLOOP_DEC (0Fh[11:8]) (the 256th t_{ON}). If ZCDLOOP_LATCHTON_EN (0Ch, bit[5]) is not enabled, the adjustment continues calculating. If ZCDLOOP_LOADLMT_EN (0C, bit[4]) = 1, the ZCD loop is only enabled when the TDC current is between the load limitation.

Command	ZCD_LOOP_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		LOADLMT_H											LOADLMT_L			

Bits	Bit Name	Description
15	LOADLOW_ZCDLOOP_EN	When the voltage of CS1 pin is below the skip SR_PWMs level (1Ah, bit[8] and 1Ah, bits[3:0]) or (READ_IOUT / 2 (READ_IOUT is 8Ch) is less than or equal to MFR_IOUT_LEVEL_L (49h, bits[7:0])). 1'b1: Enable the ZCD loop function 1'b0: Disable the ZCD loop function
14:8	ZCDLOOP_LOADLMT_H	The load's high limit to enable the ZCD loop, when compared with READ_IOUT / 8 (from ADC sampling and then calculation). 2A/LSB.
7:6	RESERVED	Unused. R/W bits are available, but these bits do not change the device.
5	ZCDLOOP_LATCHTON_EN	Enable bit to latch t_{ON} after t_{ON} stays in hysteresis for 256 periods. 1'b1: Enable 1'b0: Disable
4	ZCDLOOP_LOADLMT_EN	Enables the load limitation for the ZCD loop. 1'b1: Enable 1'b0: Disable
3:0	ZCDLOOP_LOADLMT_L	The load low limit for enabling ZCD loop, when compared with READ_IOUT / 4 (from ADC sampling and then calculation). 1A/LSB.

SKIP_SR_PWM_SET (0Eh)

This command configures the function that allows the SR_PWMs to be skipped under light-load conditions. Figure 14 shows the valid skip areas. When the CS1 pin is below CMP_CS1_ENTERFREQ (1Ah), the signal from CMP_CS1_ENTERFREQ goes high. The valid area to detect this comparator output to enter skipping is defined below as bits[10:0]. This command is only valid for phase 1.

Command	SKIP_SR_PWM_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	EN	NUM				SEL	BLKP						BLKN			

Bits	Bit Name	Description
15	SKIP_SR_PWM_EN	Enable bit to turn off SR_PWM when CS is too low. 1'b1: Enable 1'b0: Disable
14:12	SKIP_SR_PWM_NUM	Sets the off time for the SR_PWM periods. After the skip delay, the SKIP_SR_PWM_NUM and SR_PWM periods (phase 1 and 2) are skipped.
11	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
10	SKIP_SR_PWM_BLKN_SEL	Selects the valid area of SKIP SR_PWM before or after the PWM1 pull-down pulse. 1'b1: Valid area before PWM1 pull-down pulse 1'b0: Valid area after PWM1 pull-down pulse
9:4	SKIP_SR_PWM_BLKP	Sets the blanking time of the valid area after a PWM1 pull-up pulse. The blanking time can be estimated with the equation below: Skip blank time = (SKIP_SR_PWM_BLKP x 10ns + 5ns)

3:0	SKIP_SR_PWM_BLKN	Sets the blanking time for the valid area border to the PWM1 pull-down pulse. If SKIP_SR_PWM_BLKN_SEL = 1, the valid area border ahead of the PWM1 pull-down pulse is SKIP_SR_PWM_BLKN x 10ns. If SKIP_SR_PWM_BLKN_SEL = 0, the valid area border after PWM1 pull-down pulse changes based on the following scenarios: • SKIP_SR_PWM_BLKN = 0: 5ns • 0 < BLKN < 2Ah[3:0]: (2Ah[3:0] + 2 SKIP_SR_PWM_BLKN) x 5ns • BLKN > 2Ah[3:0]: (2Ah[3:0] + 2) x 5ns

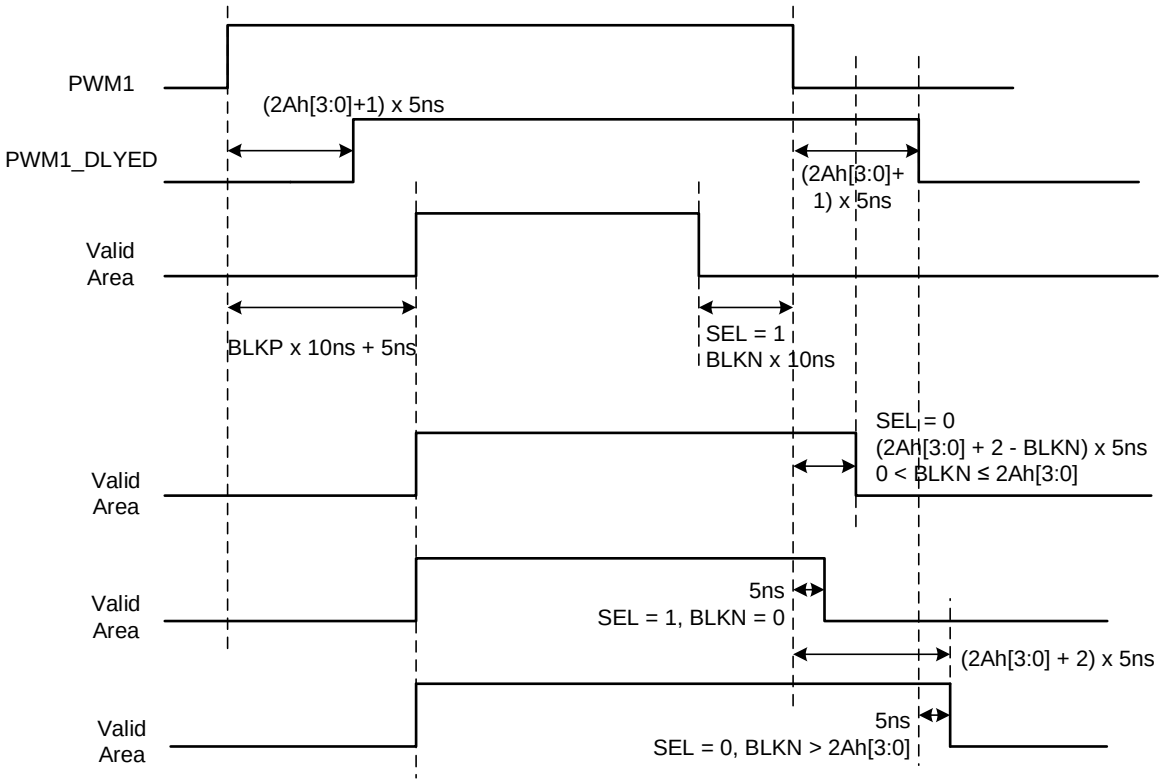


Figure 14: Valid Skip Area

CTRL_PWM_BK (0Fh)

This command sets the PWM working options.

Command	CTRL_PWM_BK															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function					TON_ZCDLOOP_DEC											

Bits	Bit Name	Description
15	SR_POS_EARLIERER_EN	Enable bit to turn SR_PWM earlier than PWMP. Related to 46h. 1'b1: Enable 1'b0: Disable
14	SEL_ZCD_NEG	1'b1: ZCD negative edge effective 1'b0: ZCD positive edge effective
13	CALVOUT_LOW_LMT_TONL	1'b1: Disable the function that makes the SR_PWMs turn off after the PWMP pins when READ_VOUT[8:1] exceeds CALVOUT_LOW_LVL[5:0] 1'b0: Enable the SR_PWMs to always turn off after the PWMPs

12	RM_VOUTLOW_SS_ TONLOW	1'b1: Disable the turning off later function during the V_{OUT} low stage, the V_{OUT} low (VOSEN < level, t_{ON} keeps TON_MIN_LIM) area during SS is not included in TONLL or TONL 1'b0: Enable the SR_PWM pins to turn off after the PWMP pins
11:8	TON_ZCDLOOP_DEC	If ZCDLOOP_LATCHTON_EN is enabled, t_{ON} is fixed to the t_{ON} value at the 256th cycle. 5ns/LSB. t_{ON} can be calculated with the following equation: t_{ON} - TON_ZCDLOOP_DEC x 5ns
7	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
6	ZCD1_EN	ZCD1 enable bit. 1'b1: Enable 1'b0: Disable
5	ZCD2_EN	ZCD2 enable bit. 1'b1: Enable 1'b0: Disable
4	SR_ZCD_SEPARATE	1'b1: ZCD2 = ZCD2 pin 1'b0: ZCD2 = ZCD1 pin
3:0	RESERVED	Unused. R/W bits are available, but these bits do not change the device.

STORE_ALL (15h)

The STORE_ALL command instructs the PMBus/I²C slave device (the chip) to copy the R/W contents from the Page 0 registers of the operating memory to the matching locations in the MTP when the command is sent for Page 0, Page 1, or Page 3 (not for Page 2). This command can be used while the device is outputting power.

This command is write-only. There is no data byte for this command. Other unused MTP addresses are written to 0.

RESTORE_ALL (16h)

The RESTORE_ALL command instructs the PMBus/I²C slave device (the chip) to copy the contents of the MTP to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the MTP. Any items that do not have matching locations in the operating memory are ignored. This command cannot be used while the device is outputting power, unless MFR_MTP_COPY_EN (register 07h, bit[0] on Page 0) is set to 1.

This command is write-only. There is no data byte for this command.

STORE_USER_ALL (17h)

The STORE_USER_ALL command instructs the PMBus/I²C slave device (the chip) to copy the read and write Page 0 registers of the operating memory except the trim registers to the matching locations in the MTP (inside MTP address 8'h00 to 8'hDF) when the command is sent for Page 0, Page 1, or Page 3 (not for Page 2). This command can be used while the device is outputting power.

This command is write-only. There is no data byte for this command. Other unused MTP addresses inside MTP address 8'h00 to 8'hDF are written to 0.

RESTORE_USER_ALL (18h)

The RESTORE_USER_ALL command instructs the PMBus/I²C slave device (the chip) to copy the R/W contents of the MTP address 8'h00 to 8'hDF to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the MTP. Any items that do not have matching locations in the operating memory are ignored. It is not permitted to use this command while the device is outputting power unless MFR_MTP_COPY_EN (register 07h, bit[0] on Page 0) is set to 1.

This command is write-only. There is no data byte for this command.

MFR_VOUT_SEL (19h)

This command configures VOUT_OVP_MAX, OVP_VID, UVP_VID, UVP_MIN, and VOUT_SKIP, then compares these values with the VOSEN pin.

Command	MFR_VOUT_SEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				OVP_MAX			OVP_VID		UVP_VID		UVP_MIN		SKIP_H		SKIP_L	

Bits	Bit Name	Description
15:13	RESERVED	Unused. R/W bits are available, but these bits do not change the device.
12:10	OVP_MAX_LVL_SEL	See the tables below for more information. V_{REF} in OVP_VID, UVP_VID and VOUT_SKIP level is the V_{OUT} reference DAC output (e.g. 21h[7:0] x 6.25mV).
9:8	OVP_VID_LVL_SEL	
7:6	UVP_VID_LVL_SEL	
5:4	UVP_MIN_LVL_SEL	
3:2	VOUT_SKIP_H_SEL	
1:0	VOUT_SKIP_L_SEL	

OVP_MAX_LVL_SEL	0	1	2	3	4	5	6	7
OVP_MAX Level (V)	1	1.1	1.2	1.3	1.4	1.5	1.6	1.7

Level Select	0	1	2	3
OVP_VID_LVL_SEL OVP_VID Level (V)	V_{REF} x 140%	V_{REF} x 130%	V_{REF} x 120%	V_{REF} x 110%
UVP_VID_LVL_SEL UVP_VID Level (V)	V_{REF} x 90%	V_{REF} x 80%	V_{REF} x 70%	V_{REF} x 60%
UVP_MIN_LVL_SEL UVP_MIN Level (V)	0.3	0.4	0.5	0.6
VOUT_SKIP_H_SEL VOUT_SKIP_H Level	V_{REF} + 50mV	V_{REF} + 40mV	V_{REF} + 30mV	V_{REF} + 20mV
VOUT_SKIP_L_SEL VOUT_SKIP_L Level	V_{REF} + 40mV	V_{REF} + 30mV	V_{REF} + 20mV	V_{REF} + 10mV

MFR_IOUT_SEL (1Ah)

This command configures the light-load levels (CMP_CS1_EXITSKIP level and CMP_CS1_ENTERFREQ level), which are compared with the CS1 pin. After CS1 exceeds CMP_CS1_EXITSKIP, the DrMOS stops skipping (SKIP_DRMOS_EN, 46h). When CS1 is below CMP_CS1_ENTERFREQ, the SR_PWMs skip after a delay (SKIP_SR_PWM_EN function, 0Eh) for configurable PWM periods.

Command	MFR_IOUT_SEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:11	RESERVED	Unused. R/W bits are available, but these bits do not change the device.
10:9	CMP_CS1_EXITSKIP_ GAIN	Selects the current level's analog buffer gain the when exiting skip mode. 2'b0x: Gain = 1 2'b10: Gain = 2 2'b11: Gain = 4
8	CMP_CS1_ ENTERFREQ_GAIN	Selects the current level's analog buffer gain when entering skip mode. 1'b1: Gain = 2 1'b0: Gain = 1
7:4	CMP_CS1_ EXITSKIP_SEL	The final level is the level determined by bits[7:4], multiplied by the buffer gain.
3:0	CMP_CS1_ ENTERFREQ_SEL	The final level is the level determined by bits[3:0], multiplied by the buffer gain.

Table 3 and Table 4 list the values for the CMP_CS1_EXIT and CMP_CS1_ENTER bits.

Table 3: CMP_CS1_EXITSKIP Values

CMP_CS1_EXITSKIP (V)	CMP_CS1_EXITSKIP_ GAIN[10:9]		
	0 or 1	2	3
CMP_CS1_EXITSKIP_ SEL[3:0]	Mul 1	Mul 2	Mul 4
0	0.08	0.160	0.320
1	0.085	0.170	0.340
2	0.09	0.180	0.360
3	0.095	0.190	0.380
4	0.1	0.200	0.400
5	0.105	0.210	0.420
6	0.11	0.220	0.440
7	0.115	0.230	0.460
8	0.12	0.240	0.480
9	0.125	0.250	0.500
10	0.13	0.260	0.520
11	0.135	0.270	0.540
12	0.14	0.280	0.560
13	0.145	0.290	0.580
14	0.15	0.300	0.600
15	0.155	0.310	0.620

Table 4: CMP_CS1_ENTER Values

CMP_CS1_ENTERFREQ (V)	CMP_CS1_ENTERFREQ_ GAIN[8]	
	0	1
CMP_CS1_ENTERFREQ_ SEL[3:0]	Mul 1	Mul 2
0	0.03	0.06
1	0.035	0.070
2	0.04	0.080
3	0.045	0.090
4	0.05	0.100
5	0.055	0.110
6	0.06	0.120
7	0.065	0.130
8	0.07	0.140
9	0.075	0.150
10	0.08	0.160
11	0.085	0.170
12	0.09	0.180
13	0.095	0.190
14	0.1	0.200
15	0.105	0.21

DEAD_TIME (1Bh)

This register sets the normal working dead time. During soft start, t_{ON} begins at TON_MIN_LIM (1Fh, bits[13:8]), and the dead time is (TON_MIN (1Ch) + DEAD_TIME (1Bh) - TON_MIN_LIM). After V_{OUT} reaches UVP_MIN, and the KEEP_TON_MIN_LMT_SS bit (06h, bit[0]) is set high, t_{ON} starts increasing. At the same time, the dead time decreases, but stays at the same frequency (see Figure 15).

If KEEP_TON_MIN_LMT_SS is not enabled, t_{ON} and the dead time start immediately. When t_{ON} reaches TON_MIN, the dead time is DEAD_TIME (1Bh). The dead time stays at this value, and t_{ON} keeps ramping until t_{ON} equals to TON_NORMAL (1Eh), until soft start completes. For more details on the t_{ON} increasing speed, see the PRISETBLK_WEIGHT_SS section on page 36.

Command	DEAD_TIME							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	DEAD_TIME						

Bits	Bit Name	Description
6:0	DEAD_TIME	The real normal working dead time = ([6:0] + 1) x 5ns.

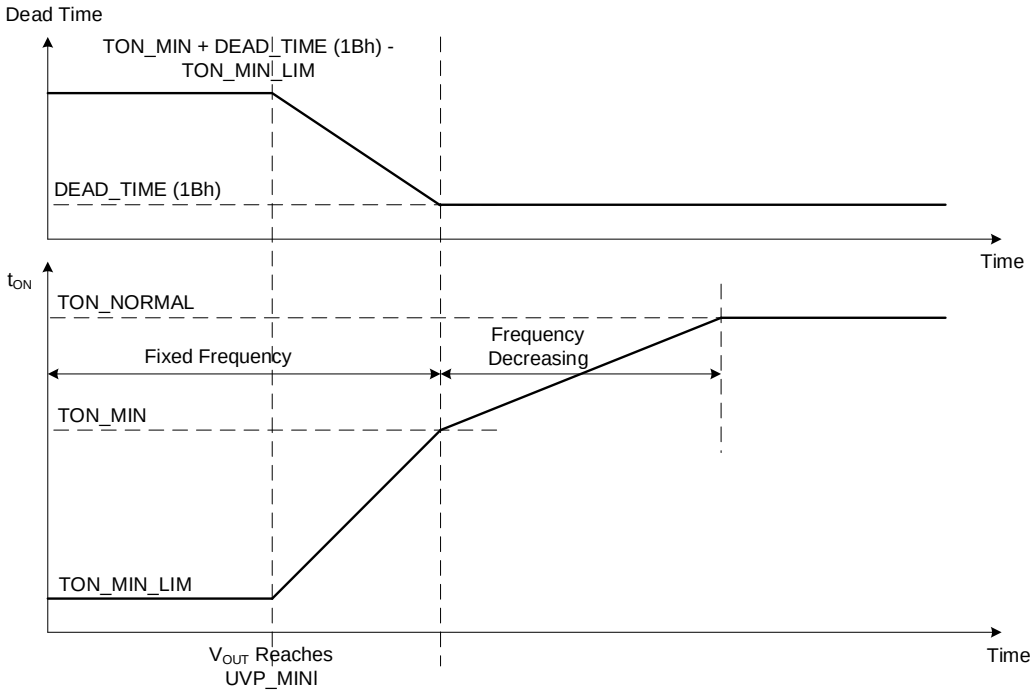


Figure 15: Soft Start t_{ON} and Dead Time

TON_MIN (1Ch)

This register sets the minimum t_{ON} in the zero-current detection (ZCD) loop and primary closed loop. It is also the end of soft start's first stage (for more details, see the DEAD_TIME (1Bh) section on page 31).

Command	TON_MIN															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	TON_MIN									

Bits	Bit Name	Description
9:0	TON_MIN	5ns/LSB.

TON_MAX (1Dh)

This register sets the maximum t_{ON}. In the zero-current detection (ZCD) loop and primary closed loop, t_{ON} is adjusted according to ZCD and the set signals. The adjusting process is limited between TON_MIN (1Ch) and TON_MAX (1Dh).

Command	TON_MAX															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	TON_MAX									

Bits	Bit Name	Description
9:0	TON_MAX	5ns/LSB.

TON_NORMAL (1Eh)

This register sets the normal working t_{ON}. It is also the final t_{ON} for soft start, and the t_{ON} for open-loop operation.

Command	TON_NORMAL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	TON_NORMAL									

Bits	Bit Name	Description
9:0	TON_NORMAL	The real t_{ON} is (TON_NORMAL + 1) x 5ns.

TON_MIN_LIM (1Fh)

This register sets the starting t_{ON} for PWM during soft start.

Command	TON_MIN_LIM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function			TON_MIN_LIM (Primary)													

Bits	Bit Name	Description
15:14	RESERVED	Unused. R/W bits are available, but these bits do not change the device.
13:8	TON_MIN_LIM	The beginning of the soft-start pulse width. Only used during soft start. Pulse width = (TON_MIN_LIM + 1) x 5ns
7:0	RESERVED	Unused. R/W bits are available, but these bits do not change the device.

MFR_REF_SR_CTRL (21h)

This register configures the V_{OUT} DAC input (named as VID or V_{REF}) and controls its slew rate. V_{REF} works as a reference in primary closed-loop operation, and is the base reference for OVP_VID and UVP_VID.

Command	MFR_REF_SR_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		VID_COUNTING_STEP							MFR_REF_SET							

Bits	Bit Name	Description
15	CLK_COUNTING_SEL	Selects the clock counting rate. 1'b1: 1μs 1'b0: 0.1μs
14:8	VID_COUNTING_STEP	Every [14:8] x (1μs or 0.1μs) time, VID increases or decreases by 6.25mV.
7:0	MFR_REF_SET	VID(V) = [7:0] x 6.25mV. 6.25mv/LSB.

VOUT_TRIM (22h)

This register sets the value to compensate the system error between V_{REF} and VOSEN. The error used for the DC loop is (21h[7:0] x 4 + VOUT_TRIM - VOUT_SENSE). VOUT_SENSE is the 10-bit ADC sampling result of VOSEN.

Command	VOUT_TRIM							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Function	X	X	X	X	VOUT_TRIM			

Bits	Bit Name	Description
3:0	VOUT_TRIM	1.5625mV/LSB.

TRANSFORMER_RATIO (25h)

The TRANSFORMER_RATIO command records the transformer ratio of the specific application.

Command	TRANSFORMER_RATIO															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:4	RESERVED	Unused. R/W bits are available, but these bits do not change the device.
3:0	TRANSFORMER_RATIO	Records the transformer ratio.

Table 5 lists the values for 25h, bits[3:0], and their respective transformer ratios.

Table 5: Transformer Ratios

25h[3:0]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Transformer Ratio	/	1	1/2	1/3	1/4	1/5	1/6	1/7	1/8	1/9	1/10	1/11	1/12	1/13	1/14	1/15

WEIGHT_ZCD (29h)

This register defines the positive and negative weights used when adjusting the frequency set by zero-current detection (ZCD) functionality. Assume t_{ON} changes from INITIAL_TON (ns) to FINAL_TON (ns), and the dead time stays the same (DEAD_TIME (ns)). The adjusting time can be calculated with Equation (2):

$$TIME(ns) = \frac{256 \times 5}{WEIGHT\_ABS} \times n \times (TON\_INIT\_D + DT\_D + 2 + \frac{n-1}{2})(ns) \quad (2)$$

Where all variables are unitless, TON_INIT_D = INITIAL_TON(ns) / 5ns - 1, TON_FIN_D = FINAL_TON(ns) / 5ns - 1, n = TON_FIN_D - TON_INIT_D + 1, DT = DEAD_TIME(ns) / 5ns - 1, and WEIGHT_ABS is the absolute value of WEIGHTN_ZCD or WEIGHTP_ZCD.

The time above does not include the 256 PWM periods during which t_{ON} stays within the t_{ON} hysteresis (0Bh, bits[10:8]) for t_{ON} latch (0Ch, bit[5]).

Command	WEIGHT_ZCD															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	WEIGHTN_ZCD									WEIGHTP_ZCD						

Bits	Bit Name	Description
15:8	WEIGHTN_ZCD	When zero-current detection (ZCD) occurs in a valid ZCD time (0Bh), t_{ON} decreases by this weight. Cannot be set to 0 or 0xFF.
7	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
6:0	WEIGHTP_ZCD	When zero-current detection (ZCD) does not occur in a valid ZCD time (0Bh), t_{ON} increases by this weight. Cannot be set to 0 or 0x01.

SR_PWM_SETA_PRIDRV (2Ah)

This register controls the SR_PWM setting and sets the simulated primary driver chip delay. For more information, see the CTRL_PWM section on page 19.

Command	SR_PWM_SETA_PRIDRV															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	PWM_NEG_FIXED												PRI_DRV_DLY_SIM			

Bits	Bit Name	Description
15:12	PWM_NEG_FIXED	If SR_FIXED_DEC_EN = 1 with other setting, SR_PWM shuts off earlier than the PWMP pin of its own phase, and the delta is ([15:12]) x 5ns. If SR_FIXED_EXT_EN = 1 with other setting, SR_PWM shuts off later than PWMP, and the delta is ([15:12] + 1) x 5ns.
11:6	RESERVED	Unused. R/W bits are available, but these bits do not change the device.
5	RM_PWMDEC_REDUND	Digital internal use.
4	PWM_EXT_DN_CFG	Digital internal use.
3:0	PRI_DRV_DLY_SIM	This bit delays the internal PWMPs from the output PWMPs. The time length simulates the primary-drive chip delay. The delay time can be calculated with the following equation: Delay time = ([3:0] + 1) x 5ns

SS_SRNEG_SET (2Bh)

This register sets the time length that determines when the SR_PWM pin turns off (before or after PWMP during soft start). This register works with 5Ah and 5Bh. For more information, see the CTRL_PWM section on page 19.

Command	SS_SRNEG_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	SS_TONHH_DEC				SS_TONH_DEC				SS_TONL_DLY				SS_TONLL_DLY			

Bits	Bit Name	Description
15:12	SRNEG_SS_TONHH_DEC	If t_{ON} ≥ TON_LVL_SS_HH during soft start, turn off SR_PWM before PWMP by [15:12] x 5ns.
11:8	SRNEG_SS_TONH_DEC	If TON_LVL_SS_HH > t_{ON} ≥ TON_LVL_SS_H, turn off SR_PWM before PWMP by [11:8] x 5ns.
7:4	SRNEG_SS_TONL_DLY	If TON_LVL_SS_L > t_{ON} ≥ TON_LVL_SS_LL during soft start, turn off SR_PWM after PWMP by ([7:4] + 1) x 5ns.
3:0	SRNEG_SS_TONLL_DLY	If t_{ON} < TON_LVL_SS_LL, turn off SR_PWM after PWMP by ([3:0] + 1) x 5ns.

SR_PWM_SETB (2Ch)

This register controls the SR_PWM pins' settings. For more information, see the CTRL_PWM section on page 19.

Command	SR_PWM_SETB															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				NEG_ADJ					POS_DECH				POS_DECL			

Bits	Bit Name	Description
15:13	RESERVED	Unused. R/W bits are available, but these bits do not change the device
12:8	SR_PWM_NEG_ADJ	SR_PWM shuts off before or after PWMP. The time length between SR_PWM's negative edge and the other phase's PWMP positive edge is ([12:8] + 1) x 5ns.
7:4	SR_PWM_POS_DECH	When SR_POS_DEC_EN = 1 under conditions other than light load, SR_PWM turns on after PWMP by ([7:4] + 1) x 5ns (the SKIP_EN pin is low).
3:0	SR_PWM_POS_DECL	When SR_POS_DEC_EN = 1 under light-load conditions, SR_PWM turns on after PWMP by ([3:0] + 1) x 5ns (the SKIP_EN pin is high).

MFR_SLOPE_SR (2Dh)

This register defines the capacitor's slope charge number and current.

Command	MFR_SLOPE_SR															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	8 - CAP			SLOPE_CURRENT					

Bits	Bit Name	Description
8:6	SLOPE_CAP_SET	Parallel capacitor number is (8 - [8:6]), each capacitor is 3.7pF.
5:0	SLOPE_CURRENT	Slope charge current. 250nA/LSB.

MFR_SLOPE_BLK (2Eh)

This register defines the slope discharge time.

Command	MFR_SLOPE_BLK															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	MFR_SLOPE_BLK													

Bits	Bit Name	Description
13:8	MFR_SLOPE_BLK	Discharge slope during dead time, excluding the first 5ns of dead time and the first ([13:8] + 1) x 5ns of PWMP pulses.
7:0	RESERVED	Unused. R/W bits are available, but these bits do not change the device.

PRISETBLK_WEIGHT_SS (2Fh)

This register sets the blanking time of the primary set loop (primary closed loop). It is a time length at the beginning of the PWMP period. t_{ON} adjusting resulting from the set loop is blanked during this time. This command also configures how quickly t_{ON} increases during soft start. There are two t_{ON} increasing stages: fixed frequency and frequency decreasing. The first-stage cost time can be calculated with Equation (3):

$$t_{SS1} = \frac{(TON\_MIN + DEAD\_TIME + 1) \times 256 \times 5ns}{WEIGHT\_SS} \times (TON\_MIN - TON\_MIN\_LIM) \quad (3)$$

Where DEAD_TIME = 1Bh[6:0], TON_MIN_LIM = 1Fh[13:8], WEIGHT_SS = 2Fh[6:0]. The second-stage cost time can be estimated with Equation (4):

$$t_{SS2} = \frac{u \times n + \frac{(n-1) \times n}{2} + (DEAD\_TIME + 1) \times n}{WEIGHT\_SS} \times 256 \times 5ns \quad (4)$$

Where u = TON_MIN = 1Ch[9:0], n = TON_NORMAL - TON_MIN, and TON_NORMAL = 1Eh[9:0].

Command	PRISETBLK_WEIGHT_SS															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	BLK_TIME													

Bits	Bit Name	Description
13:8	BLK_TIME	Blank PWMP Ton adjusting (only primary closed loop) at the beginning of the PWMP period. 5ns/LSB.
7	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
6:0	WEIGHT_SS	Accumulation step during soft start.

WEIGHT_2_1 (30h)

This register configures the value at which t_{ON} increases in the primary closed loop when the set signal is received during the last two quarters of the remaining PWMP pulse, and BLK_TIME (2Fh) is disabled.

Command	WEIGHT_2_1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		WEIGHT_2								WEIGHT_1						

Bits	Bit Name	Description
15	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
14:8	WEIGHT_2	Value at which the primary closed-loop t_{ON} increases when the set signal occurs during the third quarter of the remaining PWMP period (PWMP with BLK_TIME is disabled).
7	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
6:0	WEIGHT_1	Value at which the primary closed-loop t_{ON} increases when the set signal is received during the final quarter (not including the last 5ns) of the remaining PWMP period (PWMP with BLK_TIME is disabled).

WEIGHT_4_3 (31h)

This register configures the value at which t_{ON} increases in the primary closed loop when the set signal shows on the first two quarters of remain PWMP pulse with BLK_TIME (2Fh) part removed.

Command	WEIGHT_4_3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		WEIGHT_4								WEIGHT_3						

Bits	Bit Name	Description
15	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
14:8	WEIGHT_4	Value at which the primary closed-loop t_{ON} increases when the set signal is received during the first quarter of the remaining PWMP period (PWMP with BLK_TIME is disabled).
7	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
6:0	WEIGHT_3	Value at which the primary closed-loop t_{ON} increases when the set signal is received during the second quarter of the remaining PWMP period (PWMP with BLK_TIME is disabled).

WEIGHT_OCSPK_L_N (32h)

This register defines the t_{ON} decreasing weight of the primary closed loop and OCSPK_L.

Command	WEIGHT_OCSPK_L_N															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	WEIGHT_OCSPK_L								WEIGHT_N							

Bits	Bit Name	Description
15:8	WEIGHT_OCSPK_L	Value at which t_{ON} decreases when an over-current spike occurs on CS2 (OCSPK_L).
7:0	WEIGHT_N	Value at which the primary closed-loop t_{ON} decreases when no set pulses appear during the PWMP period while BLK_TIME is disabled.

WEIGHT_OCSPK_INC (33h)

This register sets the t_{ON} recovering (increasing) value after an over-current spike on CS1 or CS2 (OCSPK_H or OCSPK_L, respectively) goes low.

Command	WEIGHT_OCSPK_INC															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		WEIGHT_OCSPK_H_INC								WEIGHT_OCSPK_L_INC						

Bits	Bit Name	Description
15	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
14:8	WEIGHT_OCSPK_H_INC	Value at which t_{ON} recovers (increases) after an over-current spike on CS1 (OCSPK_H) goes low.
7	RESERVED	Unused. R/W bits are available, but this bit does not change the device.
6:0	WEIGHT_OCSPK_L_INC	Value at which t_{ON} recovers (increases) after an over-current spike on CS2 (OCSPK_L) goes low.

MFR_VIN_DROP_SET (34h)

This register configures the two functions when V_{IN} drops.

Command	MFR_VIN_DROP_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	RESERVED					VINL_VOUTH_DELTA				VODROP_DAC			

Bits	Bit Name	Description
12:8	RESERVED	Unused. R/W bits are available, but these bits do not change the device.
7:4	VINL_VOUTH_DELTA	When VINSEN drops below VOSEN - VINL_VOUTH_DELTA, the SR_PWM pins start skipping.
3:0	VODROP_DAC	When VINSEN exceeds VOSEN + VODROP_DAC, the SR_PWM pins start generating.

VIN_ON (35h)

This register defines the levels for V_{IN} to start working. After V_{IN} ramps up to VIN_ON, it starts to count START_DELAY (PROTECT_DELAY must finish counting before START_DELAY) and then to generate PWMs. It should be greater than VIN_OFF.

Command	VIN_ON															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	VIN_ON								

Bits	Bit Name	Description
8:0	VIN_ON	When READ_VIN ≤ VIN_ON when the power is off or READ_VIN < VIN_OFF at any moment, V_{IN} under-voltage lockout (UVLO) occurs. 0.25V/LSB.

VIN_OFF (36h)

This register defines the V_{IN} level when the device is on and V_{IN} starts working. It should be below VIN_ON.

Command	VIN_OFF															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	VIN_OFF								

Bits	Bit Name	Description
8:0	VIN_OFF	When READ_VIN ≤ VIN_ON and when the power is off or READ_VIN < VIN_OFF at any time, VIN_UVLO occurs. 0.25V/LSB.

IOUT_CAL_GAIN (38h)

This register helps calculate READ_IOUT (register 8Ch, bits[9:0], 0.25A/LSB). IOUT_CAL_GAIN can be calculated with Equation (5):

$$IOUT\_CAL\_GAIN = k_{CS} \times R_{CS} \times \frac{1}{2} \times 3 \times 2^{14} \quad (5)$$

Where k_{CS} is the DrMOS current-sense (CS) gain (e.g. if the CS gain is 5μA/A, k_{CS} = 5e - 6) (in A/A), and R_{CS} is the CS1/CS2 to GND resistor (in Ω).

Command	IOUT_CAL_GAIN															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	IOUT_CAL_GAIN									

Bits	Bit Name	Description
9:0	IOUT_CAL_GAIN	This bit helps calculate READ_IOUT.

IOUT_CAL_OFFSET (39h)

This register calculates READ_IOUT (Register 8Ch, bits[9:0], 0.25A/LSB). It is in signed binary format and uses complements. READ_IOUT can be estimated with Equation (6):

$$READ\_IOUT = \frac{IOUT\_SENSE \times 205}{2 \times IOUT\_CAL\_GAIN} + IOUT\_CAL\_OFFSET \quad (6)$$

Where IOUT_SENSE is the 10-bit ADC sampling result on the IMON pin.

Command	IOUT_CAL_OFFSET															
Format	Signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	X	IOUT_CAL_OFFSET					

Bits	Bit Name	Description
5:0	IOUT_CAL_OFFSET	Calculates READ_IOUT.

VIN_CAL_GAIN (3Ah)

This register calculates READ_VIN (Register 88h, bits[9:0], 0.125V/LSB). VIN_CAL_GAIN can be calculated with Equation (7):

$$VIN\_CAL\_GAIN = GAIN \times 2^{14} \quad (7)$$

Where GAIN is the V_{IN} divider ratio (e.g. if 48V V_{IN} results in 1V on the VINSEN pin with the resistor divider, then GAIN = 1/48). READ_VIN can then be estimated with Equation (8):

$$READ\_VIN = \frac{VIN\_SENSE \times 205}{VIN\_CAL\_GAIN} \quad (8)$$

Where VIN_SENSE is the 10-bit ADC sampling result on the VINSEN pin.

Command	VIN_CAL_GAIN															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	VIN_CAL_GAIN									

Bits	Bit Name	Description
9:0	VIN_CAL_GAIN	Calculates READ_VIN.

VOUT_CAL_GAIN (3Bh)

This register helps calculate READ_VOUT (Register 8Bh, bits[8:0], 62.5mV/LSB). VOUT_CAL_GAIN can be calculated with Equation (9):

$$VOUT\_CAL\_GAIN = GAIN \times 2^{11} \quad (9)$$

Where GAIN is the V_{OUT} divider ratio (e.g. if 6V V_{OUT} results in 1V on the VOSEN pin with the resistor divider, then GAIN = 1/6).

READ_VOUT can then be calculated with Equation (10):

$$READ\_VOUT = \frac{VOUT\_SENSE \times 205}{4 \times VOUT\_CAL\_GAIN} \quad (10)$$

Where VOUT_SENSE is the 10-bit ADC sampling result of VOSEN pin.

Command	VOUT_CAL_GAIN															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	VOUT_CAL_GAIN									

Bits	Bit Name	Description
9:0	VOUT_CAL_GAIN	For READ_VOUT calculation. See the explanation above these two tables.

VIN_OV_FLT_LIM (40h)

V_{IN} over-voltage protection (OVP) fault limit. Compared with READ_VIN (88h, bits[9:1]).

Command	VIN_OV_FLT_LIM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	VIN_OV_FLT_LIM								

Bits	Bit Name	Description
8:0	VIN_OV_FLT_LIM	V_{IN} over-voltage protection (OVP) limit. 0.25V/LSB.

TEMP_GAIN_OFFSET (42h)

This register calculates READ_TEMP (8Dh, bits[7:0], 1°C/LSB). MFR_TEMP_GAIN is an unsigned binary, while MFR_TEMP_OFFSET is a signed binary and uses the complement format. READ_TEMP is calculated from the TEMP pin, and reflects the DrMOS temperature (T(°C)). Assuming the TEMP pin voltage (V) = *k* x (T(°C) - a), then READ_TEMP can be estimated with Equation (11):

$$READ\_TEMP = \frac{TEMP\_PIN\_SENSE \times MFR\_TEMP\_GAIN}{512} + MFR\_TEMP\_OFFSET \quad (11)$$

Where TEMP_PIN_SENSE is the 10-bit ADC sampling result on the TEMP pin, and MFR_TEMP_GAIN and MFR_TEMP_OFFSET can be calculated with Equation (12) and Equation (13), respectively:

$$MFR\_TEMP\_GAIN = \frac{0.8}{k} \quad (12)$$

$$MFR\_TEMP\_OFFSET = a \quad (13)$$

Command	TEMP_GAIN_OFFSET															
Format	Unsigned binary, signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_TEMP_GAIN (unsigned)								MFR_TEMP_OFFSET (signed)							

Bits	Bit Name	Description
15:8	MFR_TEMP_GAIN	Proportional to the V-T (voltage vs. temperature) line gain.
7:0	MFR_TEMP_OFFSET	Proportional to the voltage value when T = 0°C.

DIETEMP_GAIN_OFFSET (43h)

This register calculates READ_DIE_TEMP (8Eh, bits[7:0], 1°C/LSB). MFR_DIE_TEMP_GAIN is an unsigned binary, while MFR_DIE_TEMP_OFFSET is signed and uses complement format. The MP2981 senses the die temperature on the chip (not the TEMP pin). READ_DIE_TEMP can be calculated with the sensed ADC results using Equation (14):

$$READ\_DIE\_TEMP = \frac{DIE\_TEMP\_SENSE \times GAIN}{512} + OFFSET \quad (14)$$

MFR_DIE_TEMP_GAIN and MFR_DIE_TEMP can be estimated with Equation (15) and Equation (16), respectively:

$$MFR\_DIE\_TEMP\_GAIN = \frac{0.8}{k} \quad (15)$$

$$MFR\_DIE\_TEMP\_OFFSET = a \quad (16)$$

Assume the voltage (V) input to ADC = *k* x (T(°C) - a) during positive mode (06h[11] = 0), which is the default mode. Positive mode is the default V-T wave mode. The second mode is negative mode (06h[11] = 1). In negative mode, READ_DIE_TEMP can be calculated with Equation (17):

$$READ\_DIE\_TEMP = -\frac{DIE\_TEMP\_SENSE \times (GAIN + 256)}{512} + OFFSET + 350 \quad (17)$$

Where DIE_TEMP_SENSE is the 10-bit ADC sampling result of the chip's sensed temperature, GAIN is short for MFR_DIE_TEMP_GAIN, and OFFSET is short for MFR_DIE_TEMP_OFFSET.

In VBE mode, MFR_DIE_TEMP_GAIN and MFR_DIE_TEMP_OFFSET can be estimated with Equation (18) and Equation (19), respectively:

$$MFR\_DIE\_TEMP\_GAIN = -\frac{0.8}{k} - 256 \quad (18)$$

$$MFR\_DIE\_TEMP\_OFFSET = a - 350 \quad (19)$$

Command	DIETEMP_GAIN_OFFSET															
Format	Unsigned binary, signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_DIE_TEMP_GAIN (unsigned)								MFR_DIE_TEMP_OFFSET (signed)							

Bits	Bit Name	Description
15:8	DIE_TEMP_GAIN	Helps calculate READ_DIE_TEMP.
7:0	DIE_TEMP_OFFSET	Helps calculate READ_DIE_TEMP.

MFR_USER_PWD (44h)

This is the configured user password for PMBus/I²C communication. Write-only. All reads are 0.

Command	MFR_USER_PWD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Function																

Bits	Bit Name	Description
15:0	MFR_USER_PWD	Configures the user password for PMBus/I²C communication.

MFR_MTP_WP (45h)

MTP writing protection. The MTP store command cannot be executed if this byte is not 8'h63.

Command	MFR_MTP_WP							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_MTP_WP							

Bits	Bit Name	Description
7:0	MFR_MTP_WP	MTP write protection.

SKIPDRMOS_SR_EARLI (46h)

This register allows the device to skip the DrMOS function under light-load conditions. Related to 1Ah and 49h. This register also sets the time length at which SR_PWM turns on before PWMP.

Command	SKIPDRMOS_SR_EARLI															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				SR_POS_EARLIER							SKIPSR_DELAY					

Bits	Bit Name	Description
15:13	RESERVED	Unused. R/W bits are available, but these bits do not change the device.
12:8	SR_POS_EARLIER	This bit determines how early SR_PWM turns on before PWMP. 5ns/LSB.
7	RESERVED	Unused. R/W bits are available, but these bits do not change the device.
6	SKIP_DRMOS_EN	Enable bit to bypass the DrMOS function (the SKIP_EN pin). 1'b1: Enable 1'b0: Disable
5:0	SKIPSR_DELAY_TIME	If SR_PWM is triggered by SKIP_PWM_EN or SKIP_DRMOS_EN before skipping under light-load conditions, the current must stay low for this set time. One whole ADC sample round/LSB, which is about 18µs/LSB if MFR_ADC_HOLD_TIME (05H) is set to 2µs.

MFR_IOUT_LEVEL (49h)

This register configures the TDC I_{OUT} values to skip the DrMOS function during light-load conditions (SKIP_EN pin on the MP2981, 46h and 1Ah). If the load increases and READ_IOUT/2 (in 8Ch) exceeds MFR_IOUT_LEVEL_H, the SKIP_EN pin goes low, and the MOS in DrMOS starts working.

The other way to exit skipping is for the CS1 pin to exceed CMP_CS1_EXITSKIP(1Ah). The only condition to enter DrMOS skip mode is that READ_IOUT/2 (in 8Ch) $\leqslant$ MFR_IOUT_LEVEL_L for a configured time (46h).

Command	MFR_IOUT_LEVEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_IOUT_LEVEL_H								MFR_IOUT_LEVEL_L							

Bits	Bit Name	Description
15:8	MFR_IOUT_LEVEL_H	Sets the TDC I_{OUT} value to exit DrMOS skip mode.

7:0	MFR_IOUT_LEVEL_L	Sets the TDC I_{OUT} value to enter DrMOS skipping.

MFR_VCAL_I_MAX (4Bh)

This register defines the integration factor and the max limit of the DC loop.

Command	MFR_VCAL_I_MAX															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MFR_VCAL_I								MFR_VO_CMPS_MAX							

Bits	Bit Name	Description
15:8	MFR_VCAL_I	The integration factor of the DC loop.
7:0	MFR_VO_CMPS_MAX	The maximum limit of the value input into VO_COMP DAC.

DC_TRIM (4Ch)

This register can set the initial value of VO_COMP DAC. The initial VO_COMP is DC_TRIM x 8. When the DC loop is enabled, VO_COMP = DC_TRIM x 8 - (DC loop result). If the DC loop is disabled, the data input to VO_COMP DAC keeps the value before disabling. The DAC output is divided by 2 then added to VOSEN. The sum signal is one input of the primary closed-loop comparator.

Command	DC_TRIM							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function				DC_TRIM				

Bits	Bit Name	Description
7:5	RESERVED	Unused. R/W bits are available, but these bits do not change the device.
4:0	DC_TRIM	DC_TRIM x 8 is the initial value input into VO_COMP DAC.

MPS_CODE (50h)

This register is written with a code that represents MPS.

Command	MPS_CODE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	MPS_CODE	The code representing MPS.

PRODUCT_CODE (51h)

This register is written with “2981” (hex code), and represents the MP2981 chip.

Command	PRODUCT_CODE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	PRODUCT_CODE	The code represents the MP2981 chip. It is 2981 (hex radix).

CONFIG_ID (52h)

This register should be written with the specific application programming code.

Command	CONFIG_ID															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	CONFIG_ID	Specific application programming code.

CONFIG_REV (53h)

This register should be written with a version of the specific application programming code or complement programming code.

Command	CONFIG_REV															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	CONFIG_REV	Write with a version of a specific application programming code or complement programming code.

CALVO_LOW_TON_SS_L (5Ah)

This register defines the upper limit of V_{OUT} to enable the two stages (TONLL and TONL stages) of the SR_PWM pins turning off later than the PWMPs in SS. If V_{OUT} > CALVOUT_LOW_LVL x 0.125V, TONLL and TONL are invalid. It also sets the two t_{ON} boundaries of these two stages. TON_LVL_SS_L must be greater than or equal to TON_LVL_SS_LL.

Command	CALVO_LOW_TON_SS_L															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CALVOUT_LOW_LVL						TON_LVL_SS_L						TON_LVL_SS_LL			

Bits	Bit Name	Description
15:10	CALVOUT_LOW_LVL	When READ_VOUT / 2 (8Bh) > CALVOUT_LOW_LVL, the TONLL and TONL stages during soft start can be disabled by setting CALVOUT_LOW_LMT_TONL (in 0Fh) high. 125mv/LSB.
9:4	TON_LVL_SS_L	When TON_LVL_SS_L > t_{ON} ≥ TON_LVL_SS_LL during soft start, turn off the SR_PWM pins after the PWMP pins by (SRNEG_SS_TONL_DLY + 1) x 5ns. Related to 2Bh. 5ns/LSB.
3:0	TON_LVL_SS_LL	When t_{ON} < TON_LVL_SS_LL during soft start, turn off the SR_PWM pins after the PWMP pins by (SRNEG_SS_TONLL_DLY + 1) x 5ns. Related to 2Bh. 5ns/LSB.

TON_SS_H (5Bh)

This register sets the two t_{ON} boundaries that turn the SR_PWM pins off before the PWMP pins during soft start. TON_LVL_SS_HH must be greater than or equal to TON_LVL_SS_H.

Command	TON_SS_H															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	TON_LVL_SS_H							TON_LVL_SS_HH							

Bits	Bit Name	Description
14:8	TON_LVL_SS_H	When TON_LVL_SS_HH > t_{ON} ≥ TON_LVL_SS_H during soft start, the SR_PWM pnis turn off before the PWMP pins by (SRNEG_SS_TONH_DEC x 5ns). Related to 2Bh. 5ns/LSB.
7:0	TON_LVL_SS_HH	When t_{ON} ≥ TON_LVL_SS_HH during soft start, the SR_PWM pins turn off before the PWMP pins by (SRNEG_SS_TONHH_DEC x 5ns). Related to 2Bh. 5ns/LSB.

POWER_GOOD_ON (5Eh)

This register defines a VID level close to the VID target (21h, bits[7:0]). This means that VID ramping up is almost completed, and the PG on delay starts to count VID instead of t_{ON} as the PG reference (06H, bit[2]).

Command	POWER_GOOD_ON															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	POWER_GOOD_ON							

Bits	Bit Name	Description
7:0	POWER_GOOD_ON	VID level that means VID ramping up is almost done. Must be set below or equal to the VID target (21h, bits[7:0]). 6.25mV/LSB.

POWER_GOOD_OFF (5Fh)

If VID is below or equal to this register and VID is selected as the PG reference (06h, bit[2]), PG goes low.

Command	POWER_GOOD_OFF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	POWER_GOOD_OFF							

Bits	Bit Name	Description
7:0	POWER_GOOD_OFF	VID level of PG off if VID is selected as the PG reference. Must be set below POWER_GOOD_ON (5Eh, bits[7:0]). 6.25mV/LSB.

PROTECT_DELAY (60h)

After a shutdown protection that does not include an over-current (OC) spike (Phase OC, OCSPK_H, and OCSPK_L) occurs, the device starts counting PROTECT_DELAY. After this delay, the chip starts to count START_DELAY (63h), and then generates PWMs and ramps VID up again.

If the device has been configured to hiccup or retry mode, the restart times are not complete (VOUT_OVP_MAX, OVP_VID, UVP_VID, UVP_MIN, OCP_TDC, or OCP_SPIKE), and are reset by VIN_UVLO.

Command	PROTECT_DELAY							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	PROTECT_DELAY						

Bits	Bit Name	Description
6:0	PROTECT_DELAY	The delay between a protection shutdown and when the device restarts. 100µs/LSB.

PWRGD_DELAY (62h)

This register sets the delay period between the end of PG reference (t_{ON} increasing to TON_NORMAL (1Eh) or VID ramping up to POWER_GOOD_ON (5Eh)) ramping to when the PG pin turns on.

Command	PWRGD_DELAY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	SEL	PWRGD_DELAY						

Bits	Bit Name	Description
7	PWRGD_DELAY_SEL	1’b1: 20kHz 1’b0: 50kHz
6:0	PWRGD_DELAY	After VID reaches POWER_GOOD_ON (5Eh) or t_{ON} reaches TON_NORMAL (1Eh), this delay time starts counting. After this delay finishes, PG goes high. If 62h[7] = 1, the PWRGD_DELAY time = [6:0] x 50µs If 62h[7] = 0, the PWRGD_DELAY time = [6:0] x 20µs

START_DELAY (63h)

This register sets the time length for which the EN pin must stay high during start-up, after the MTP finishes restoring, and before VID starts slewing up and PWM switches.

Command	START_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	START_DELAY	The bit determines if the device requires a continuously high EN pin during start-up. The resolution is determined by MFR_ONOFFDLY_CLK_1L0S (06h, T). The time length can be calculated with the following equation: Length = 256 x T x START_DELAY[15:8] + T x START_DELAY[7:0]

OFF_DELAY (64h)

This register sets the delay time after the EN pin turns off or PMBus/I²C sends an off command. This is during normal operation, and before shutting down VID, PG, and the PWM pins.

Command	OFF_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	OFF_DELAY	This bit determines the part's delay before shutting down. The resolution is determined by MFR_ONOFFDLY_CLK_1L0S (06h, T). The delay can be calculated with the following equation: Delay = 256 x T x OFF_DELAY[15:8] + T x OFF_DELAY[7:0]

MFR_OTP_SET (65h)

This register controls the TEMP pin's parameters if over-temperature protection (OTP) occurs.

Command	MFR_OTP_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	L	HYS							LIMIT							

Bits	Bit Name	Description
15	MFR_OTP_LATCH	1'b1: Latch 1'b0: Hiccup
14:8	MFR_OTP_HYS	The TEMP pin's over-temperature (OT) hysteresis limit. When READ_TEMP (8Dh) ≤ (MFR_OTP_LIMIT - MFR_OTP_HYS), the OT comparator goes low. 1°C/LSB.
7:0	MFR_OTP_LIMIT	TEMP pin over-temperature (OT) limit. 1°C/LSB.

MFR_DIE_OTP_SET (66h)

This register controls the die temperature's parameters if over-temperature protection (OTP) occurs.

Command	MFR_DIE_OTP_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	L	HYS							LIMIT							

Bits	Bit Name	Description
15	MFR_DIE_OTP_LATCH	1'b1: Latch mode 1'b0: Hiccup mode
14:8	MFR_DIE_OTP_HYS	Hysteresis of die temperature over-temperature (OT) limit. When READ_TEMP (8Dh) ≤ (MFR_DIE_OTP_LIMIT - MFR_DIE_OTP_HYS), the OT comparator goes low. 1°C/LSB.
7:0	MFR_DIE_OTP_LIMIT	Die temperature over-temperature (OT) limit. 1°C/LSB.

PMBUS/I²C_ADDR_SET (67h)

This register configures the 7-bit PMBus/I²C slave address (the chip's PMBus/I²C address).

Command	PMBUS/I²C_ADDR_SET							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function								

Bits	Bit Name	Description
7:0	PMBUS/I²C_ADDR_SET	Final PMBus/1²C address [6:4] = 67h[6:4]. If bit[7] = 1, the final PMBus/I²C address [3:0] comes from sampling the ADDRP pin. If bit[7] = 0, the final PMBus/I²C address [6:0] = 67h[6:0].

MFR_PROTECT_CFG (68h)

This register controls certain device protections.

Command	MFR_PROTECT_CFG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	UVLO_STARTUP_MTP_EN	1'b1: Only store V_{IN} under-voltage lockout (UVLO) conditions that occur when power is being delivered to the MTP. 1'b0: Store all V_{IN} UVLO occurrences in the MTP.
14:12	RESERVED	Unused. R/W bits are available, but these bits do not change the device.
11	DrMOS_OC_LATCH	Selects the trigger mode for DrMOS over-current protection (OCP). 1'b1: Latch mode 1'b0: Hiccup mode
10	DrMOS_OC_EN	Enable bit of DrMOS OC protection. 1'b1: Enable 1'b0: Disable
9	VOUT_OVP_MAX_LATCH	Selects VOUT_OVP_MAX protection mode 1'b1: Latch mode 1'b0: Hiccup mode
8	VOUT_OVP_MAX_EN	Enable bit for VOUT_OVP_MAX protection. 1'b1: Enable 1'b0: Disable
7	DIE_TEMP_PRO_EN	1'b1: Disable DIE_TEMP protection 1'b0: Enable DIE_TEMP protection
6	TEMP_PRO_EN	1'b1: Disable over-temperature protection (OTP) from the TEMP pin (not including DrMOS OC or DIE_TEMP) 1'b0: Enable OTP from the TEMP pin
5	MFR_VIN_OVP_LATCH	Determines how the device responds when a V_{IN} protection is enabled (RST_VIN_PRO = 0). 1'b1: Latch mode 1'b0: Hiccup mode

4	RST_VIN_PRO	1'b1: Disable V_{IN} protection, including V_{IN} under-voltage lockout (UVLO) and V_{IN} over-voltage protection (OVP) 1'b0: Enable V_{IN} protection, including V_{IN} UVLO and V_{IN} OVP
3	UVLO_STARTUP_STATUS_EN	1'b1: Only store V_{IN} under-voltage lockout (UVLO) occurrences while power is delivered to STATUS_WORD 1'b0: Store all V_{IN} UVLO occurrences to STATUS_WORD.
2	RST_STATUS_EN	Enable bit to reset STATUS_XX during a restart, and after the EN pin is off, or operation is off. 1'b1: Reset STATUS_XX during a restart 1'b0: Do not reset STATUS_XX during a restart
1	SS_EXT_CLK_SEL	Select the clock counting the 4-clock delay after t_{ON} reaches TON_NORMAL, and before OVP_VID, UVP_VID, and UVP_MIN can be enabled. 1'b1: 20kHz 1'b0: 50kHz
0	DISABLE_ALL_PRO	1'b1: Disable all protection features 1'b0: Enable all protection features There are two protections that cannot be controlled by this bit: • PWM t_{ON} change during over-current spikes on the CS1 or CS2 pins (OCSPK_H and OCSPK_L, respectively) • Counting of over-current spikes on CS1 (OCSPK_H) before the device shuts down

OVP_UVP_VID_SET (69h)

This register controls VOUT_OVP_VID and UVP_VID protection. Their levels are defined in 19h.

Command	OVP_UVP_VID_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OVP MD			OVP DELAY					UVP MD		UVP DELAY					

Bits	**Bit Name**	**Description**
15:14	OVP_VID_MODE	2'b00: No action 2'b01: Latch mode 2'b10: Hiccup mode 2'b11: Retry 3 times or 6 times based on OVP_VID_RETRY_TIMES
13	OVP_VID_RETRY_TIMES	1'b1: Retry 3 times 1'b1: Retry 6 times, when MFR_OVP_SET_MODE is 11b
12:8	OVP_VID_DELAYTIME	If V_{OUT} stays high for a set time, VOUT over-voltage protection (OVP) is triggered. 200ns/LSB.
7:6	UVP_VID_MODE	2'b00: No action 2'b01: Latch mode 2'b10: Hiccup mode 2'b11: Retry 6 times
5:0	UVP_VID_DELAYTIME	If V_{OUT} stays low for the set time, V_{OUT} under-voltage protection (UVP) is triggered. 20µs/LSB.

OCP_TDC_SET (6Ah)

This register controls TDC OCP.

Command	OCP_TDC_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MODE		DELAY						LEVEL							

Bits	Bit Name	Description
15:14	OCP_TDC_MODE	2'b00: No action 2'b01: Latch mode 2'b10: Hiccup mode 2'b11: Retry 6 times
13:8	OCP_TDC_DELAYTIME	If the TDC current stays high for this set time, over-current protection (OCP) is triggered. 100µs/LSB.
7:0	OCP_TDC_LEVEL	1A/LSB.

OCP_SPIKE_TIMES_SET (6Bh)

This register controls the over-current (OC) spike time, which can shut down the chip.

Command	OCP_SPIKE_TIMES_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	SS	RANGE					MODE		TIMES					

Bits	Bit Name	Description
13	DIS_OCP_SPIKE_SS	1'b1: Disable the OCP_SPIKE_TIMES protection during soft start 1'b0: Enable the OCP_SPIKE_TIMES protection during soft start
12:8	OCP_SPIKE_RANGE	The time length in which to count OC spikes on CS1 (OCSPK_H), and the time length before starting one OCSPK_H pulse. 1 PWMP period/LSB. The set time can be calculated with the following equation: Time length = (PWM1 t_{ON} + PWM2 t_{ON} + 2 dead time) x [12:8]
7:6	OCP_SPIKE_MODE	2'b00: No action 2'b01: Latch mode 2'b10: Hiccup mode 2'b11: Retry 6 times
5:0	OCP_SPIKE_TIMES	If the pulse time of OC spikes on CS1 (OCSPK_H) (both PWM1 and PWM2) exceeds OCP_SPIKE_TIMES during OCP_SPIKE_RANGE, a protection is triggered. If the OCSPK_H (both PWM1 and PWM2) pulse time is below OCP_SPIKE_TIMES during OCP_SPIKE_RANGE, OCSPK_H pulses are recounted from 0. The next OC pulse and the detection time window (OCP_SPIKE_RANGE) also restart.

OCP_SPIKE_LEVEL (6Ch)

This register sets the higher and lower OCP_SPIKE levels. Both levels are compared with the CS1 and CS2 pins.

Command	OCP_SPIKE_LEVEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Higher level								Lower level							

Bits	Bit Name	Description
15:8	HIGHER_SPIKE_LVL	Digital value of the higher OCP_SPIKE DAC. 2V range, 8-bit DAC. The DAC output is [15:8] x 2V / 256.
7:0	LOWER_SPIKE_LVL	Digital value into of the lower OCP_SPIKE DAC.; 2V range, 8-bit DAC. The DAC output is [7:0] x 2V / 256.

UVP_MIN_SET (6Dh)

This register controls the V_{OUT} UVP_MIN protection.

Command	UVP_MIN_SET							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	MODE		DELAY					

Bits	Bit Name	Description
7:6	UVP_MIN_MODE	2'b00: No action 2'b01: Latch mode 2'b10: Hiccup mode 2'b11: Retry 6 times
5:0	UVP_MIN_DELAY	If V_{OUT} stays low for this time length, the protection is triggered. 0.4µs/LSB.

STATUS_WORD (79h)

This register records general protections and the real-time on/off state. It is reset by EN or OPERATION restart if the RST_STATUS_EN bit (68h, bit[2]) is high, the CLEAR_FAULTS command (03h in Page 0, Page 1, and Page 3, but not in Page 2) is received, or power is cycled on VCC3V3.

Command	STATUS_WORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15	VOUT OVP or UVP	VOUT_OVP_MAX, OVP_VID, UVP_VID, and UVP_MIN fault indicator. If output over-voltage protection (OVP) or under-voltage protection (UVP) occurs, this bit is set and latched. The specific protection can be viewed by STATUS_VOUT (7Ah). 1'b0: No V_{OUT} OV or UV fault has occurred 1'b1: A V_{OUT} OV or UV fault has occurred
14	OCP	OCP_TDC or OCP_SPIKE_TIMES fault indicator. If either of these I_{OUT} protections occurs, or an under-voltage (UV) fault occurs at the beginning of OCP_TDC, this bit is set and latched. The specific protection can be viewed by STATUS_IOUT (7Bh). 1'b0: No I_{OUT} over-current (OC) fault has occurred 1'b1: An I_{OUT} OC fault has occurred
13	VIN_UVLO_FLAG	V_{IN} under-voltage lockout (UVLO) protection indicator. If READ_VIN ≤ VIN_ON while the device is off, or READ_VIN < VIN_OFF at any time except during the reset all protection stages, this bit is pulled high.
12	VIN_OVP	V_{IN} OVP fault indicator. If input over-voltage protection (OVP) occurs, this bit is set and latched. 1'b0: No V_{IN} over-voltage (OV) fault has occurred 1'b1: A V_{IN} OV fault has occurred
11	PG	PG pin state indicator. PG is set high after PWRGD_DELAY. When any protection or fault occurs during normal operation (power out state), PG is pulled down.
10	RESERVED	Unused. Reads are always 0.
9	DrMOS_OCP	DrMOS OCP fault indicator. If the TEMP pin reaches VCC3V3 (which means DrMOS OCP fault has occurred), this bit is set and latched. Specific protections can be viewed by PROTECT_SIG_GRP (7Ch). 1'b0: No DrMOS OC fault has occurred 1'b1: DrMOS OC fault has occurred
8:7	RESERVED	Unused. Reads are always 0.
6	EN_SS	Chip working state indicator. 1'b1: The chip is not outputting PWMs or V_{REF}, and the state is off 1'b0: State is on, and PWMs are switching
5	OVP_MAX or OVP_VID_POS	V_{OUT} over-voltage (OV) positive edge fault indicator. If output over-voltage MAX or VID positive edge protection occurs, this bit is set and latched. Unlike STATUS_VOUT (7Ah), this bit can be cleared by CLEAR_FAULTS(03h) when the protection signal stays high. 1'b0: No V_{OUT} over-voltage (OV) positive edge fault has occurred 1'b1: V_{OUT} OV positive edge fault has occurred
4	OCP_TDC_POS	I_{OUT} over-current (OC) positive-edge fault indicator. If output OC positive-edge protection occurs, this bit is set and latched. Unlike STATUS_IOUT (7Bh), this bit can be cleared by CLEAR_FAULTS(03h) when the protection signal stays high. 1'b0: No I_{OUT} over-current (OC) positive edge fault has occurred 1'b1: I_{OUT} over-current (OC) positive edge fault has occurred
3	UVP_VID or UVP_MIN_POS	V_{OUT} under-voltage (UV) positive edge fault indicator. If output UV VID or MIN positive-edge protection occurs, this bit is set and latched. Unlike STATUS_VOUT (7Ah), this bit can be cleared by CLEAR_FAULTS(03h) when a protection signal stays high. 1'b0: No V_{OUT} under-voltage (UV) positive edge fault has occurred 1'b1: V_{OUT} under-voltage (UV) positive edge fault has occurred

2	TEMP OTP or DIE_OTP	Over-temperature protection (OTP) positive edge fault indicator. If an OTP from TEMP pin sampling or the 2981 internal DIE_TEMP sensor fault occurs, this bit is set and latched. Specific protections can be viewed by STATUS_TEMP (7Dh). 1'b0: No over-temperature (OT) fault has occurred 1'b1: OT fault has occurred
1	STATUS_CML_NONZERO	CML positive edge fault indicator. If a CML fault occurs, this bit is set and latched. Specific protections can be viewed by STATUS_CML (7Ch). 1'b0: No CML fault has occurred 1'b1: CML fault has occurred
0	RESERVED	Unused. Reads are always 0.

STATUS_VOUT (7Ah)

This register records the V_{OUT} protection status. It can be reset by EN or OPERATION restarting if RST_STATUS_EN bit (68h, bit[2]) is high, by sending a CLEAR_FAULTS command (03h in Page 0, Page 1, or Page 3, but not on Page 2), or by cycling the power on VCC3C3.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Description
7	OVP_MAX	V_{OUT} OVP_MAX fault indicator. If V_{OUT} exceeds VOUT_MAX, this bit is set and latched. 1'b0: No V_{OUT} OVP_MAX fault has occurred 1'b1: V_{OUT} OVP_MAX fault has occurred
6	OVP_VID	V_{OUT} OVP_VID fault indicator. If V_{OUT} exceeds OVP_VID for a set time, this bit is set and latched. 1'b0: No V_{OUT} OVP_VID fault has occurred 1'b1: V_{OUT} OVP_VID fault has occurred
5	UVP_VID	V_{OUT} UVP_VID fault indicator. If V_{OUT} drops below UVP_VID for a set time, this bit is set and latched. 1'b0: No V_{OUT} OVP_MAX fault has occurred 1'b1: V_{OUT} OVP_MAX fault has occurred
4	UVP_MIN	V_{OUT} OVP_MAX fault indicator. If V_{OUT} drops below UVP_MIN, this bit is set and latched. 1'b0: No V_{OUT} OVP_MAX fault has occurred 1'b1: V_{OUT} OVP_MAX fault has occurred
3:0	RESERVED	Unused. Reads are always 0.

STATUS_IOUT (7Bh)

This register records the I_{OUT} protection status. It can be reset by EN or OPERATION restarting if RST_STATUS_EN bit (68h, bit[2]) is high, by sending a CLEAR_FAULTS command (03h on Page 0, Page 1, and Page 3, but not Page 2), or by cycling the power on VCC3V3.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Description
7	OCP_TDC	Normal I_{OUT} over-current protection (OCP) TDC fault indicator. If the TDC remains high for longer than the set time (6Ah), this bit is set and latched. 1'b0: No over-current protection (OCP) TDC fault has occurred 1'b1: OCP TDC fault has occurred
6	OCP_TDC_UV	Under-voltage (UV) fault caused by I_{OUT} over-current protection (OCP) TDC fault indicator. If the UV comparator output is effective when TDC OCP occurs (after the delay), this bit is set and latched. 1'b0: No over-current protection (OCP) TDC under-voltage (UV) fault has occurred 1'b1: OCP TDC UV fault has occurred
5	OCP_SPIKE_TIMES	Under-voltage (UV) fault caused by I_{OUT} OCP TDC fault indicator. If the CS peak exceeds the OC SPIKE H level, and the counting pulse number exceeds the set number (6Bh, bits[5:0]) in the configured range (6Bh, bits[12:8]), this bit is set and latched. 1'b0: No over-current protection (OCP) TDC under-voltage (UV) fault has occurred 1'b1: OCP TDC UV fault has occurred
4:0	RESERVED	Unused. Reads are always 0.

PROTECT_SIG_GRP (7Ch)

This register records all protections that can result in shutdown. This register can be stored in the MTP.

Command	PROTECT_SIG_GRP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:12	RESERVED	Unused. Reads are always 0.
11	DRMOS_OCP	DrMOS over-current protection (OCP) indicator. If the TEMP pin voltage exceeds 1.8V, a DrMOS OCP fault occurs. This triggers DRMOS_OCP protection, and the bit is set and latched. When OC conditions occur, DrMOS sets its TEMP pin to VCC. 1'b0: No DrMOS over-current protection (OCP) has occurred 1'b1: DrMOS OCP has occurred
10	RESERVED	Unused. Reads are always 0.

9	OCP_TDC	I_{OUT} TDC over-current protection (OCP) indicator. If I_{OUT} TDC OCP occurs and triggers TDC OCP protection, this bit is set and latched. 1'b0: No TDC over-current protection (OCP) has occurred 1'b1: TDC OCP has occurred
8	OCP_SPIKE_TIMES	OCP_SPIKE_TIMES protection indicator. If an OCP_SPIKE_TIMES fault occurs and triggers a protection, this bit is set and latched. 1'b0: No OCP_SPIKE_TIMES protection has occurred 1'b1: OCP_SPIKE_TIMES protection has occurred
7	VIN_OVP	V_{IN} over-voltage protection (OVP) indicator. If V_{IN} OVP is triggered, this bit is set and latched. 1'b0: No V_{IN} over-voltage protection (OVP) has occurred 1'b1: V_{IN} OVP has occurred
6	VIN_UVLO	V_{IN} under-voltage lockout (UVLO) indicator. If V_{IN} UVLO occurs when delivering power or UVLO_STARTUP_MTP_EN (68h, bit[15]) is enabled, this bit is set and latched. 1'b0: No V_{IN} under-voltage lockout (UVLO) fault has occurred 1'b1: A V_{IN} UVLO fault has occurred
5	OTP	Over-temperature protection (OTP) from sampling the TEMP pin indicator. If this fault occurs and triggers the protection, this bit is set and latched. 1'b0: No over-temperature protection (OTP) has occurred 1'b1: OTP has occurred
4	DIE_OTP	Die over-temperature protection (OTP) protection indicator. If the MP2981 die temperature exceeds its OT limit and triggers the protection, this bit is set and latched. 1'b0: No DIE over-temperature protection (OTP) has occurred 1'b1: A DIE_OTP protection has occurred
3	OVP_MAX	V_{OUT} OVP_MAX protection indicator. If a V_{OUT} over-voltage protection (OVP) MAX fault occurs and triggers the protection, this bit is set and latched. 1'b0: No V_{OUT} OVP_MAX protection has occurred 1'b1: A V_{OUT} OV_MAX protection has occurred
2	OVP_VID	V_{OUT} OVP_VID protection indicator. If V_{OUT} over-voltage protection (OVP) VID fault occurs and triggers the protection, this bit is set and latched. 1'b0: No V_{OUT} OVP_MAX protection has occurred 1'b1: A V_{OUT} OV_MAX protection has occurred
1	UVP_VID	V_{OUT} UVP_VID protection indicator. If a V_{OUT} UVP_VID fault occurs and triggers the protection, this bit is set and latched. 1'b0: No V_{OUT} UVP_VID protection has occurred 1'b1: A V_{OUT} UVP_VID protection has occurred
0	UVP_MIN	V_{OUT} UVP_MIN protection indicator. If a VOUT UVP_MIN fault occurs and triggers the protection, this bit is set and latched. 1'b0: No V_{OUT} UVP_MIN protection has occurred 1'b1: A V_{OUT} UVP_MIN protection has occurred

STATUS_TEMP (7Dh)

This register records the protection statuses related to the TEMP pin. It can be reset by EN or OPERATION restarting if RST_STATUS_EN bit (68h, bit[2]) is high, by sending a CLEAR_FAULTS command (03h on Page 0, Page 1, and Page 3, but not on Page 2), or by cycling the power on VCC3V3.

Command	STATUS_TEMP							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Description
7	OTP	Over-temperature protection (OTP) fault indicator. If an OT fault is sampled on the TEMP pin, this bit is set and latched. 1'b0: No over-temperature protection (OTP) fault has occurred 1'b1: An OTP fault has occurred
6	DIE_OTP	Die over-temperature protection (OTP) fault indicator. If the MP2981 chip senses that die temperature has exceeded its OT threshold, this bit is set and latched. 1'b0: No die over-temperature protection (OTP) has occurred 1'b1: Die OTP has occurred
5	DRMOS_OCP	DrMOS over-current protection (OCP) fault indicator. If the TEMP pin exceeds 1.8V and a DrMOS OCP fault occurs, this bit is set and latched. When an OC condition occurs, DrMOS sets its TEMP pin to VCC. 1'b0: No DrMOS over-current protection (OCP) has occurred 1'b1: DrMOS OCP has occurred
4:0	RESERVED	Unused. Reads are always 0.

STATUS_CML (7Eh)

This register records the status between PMBus/I^{2}C and MTP communication. It can be reset by sending a CLEAR_FAULTS command (03h on Page 0, 1, and 3, but not on Page 2).

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Description
7	CML_INVALID_CMD	CML invalid command fault indicator. If the received PMBus/I^{2}C command is not defined, this bit is set and latched. 1'b0: No CML invalid command fault has occurred 1'b1: CML invalid command fault has occurred
6	Internal debug	Used for debugging.
5	CML_PEC_FAULT	CML peculiar fault indicator. If the received PMBus/I^{2}C command does not match the command sent by the master, this bit is set and latched. 1'b0: No CML peculiar fault has occurred 1'b1: CML peculiar fault has occurred

4	LATCHED_WRFAIL	WRFAIL is a flag signal from MTP. It signifies that 1 byte written to the MTP has failed. The MTP WRFAIL output is reset at the start of writing the next byte. This bit is the latched result of the MTP WRFAIL signal. This bit is reset by sending a CLEAR_FAULTS command (03h) and the beginning of the next MTP write process (not writing the next byte) after the current MTP storing process finishes.
3	CRC_FAULT_ENABLED	If at least one of the three CRC faults occurs, the corresponding CRC enable bit (07h, bits[15:13]) is set to 1: 1. The CRC of the first two sections of the MTP (8'h00 to 8'hDD MTP addresses, 8'hDE and 8'hDF store the CRC calculation result). Valid in STORE_ALL (15h), RESTORE_ALL (16h), STORE_USER_AL L(17h), and RESTORE_USER_ALL (18h). The enable bit is 07h[15]. 2. The CRC of the third section of MTP (8'hE0 to 8'hFB MTP addresses, 8'hFC, and 8'hFD are the calculated CRC). Valid in STORE_ALL (15h), RESTORE_ALL (16h), STORE_S3 (F5h), and RESTORE_S3 (F6h). Its enable bit is 07h[14]. 3. The total MTP CRC (8'h00 to 8'hFD MTP addresses, 8'hFE and 8'hFF store the calculated CRC). Valid in STORE_ALL (15h) and RESTORE_ALL (16h). This CRC cannot be enabled or configured by the user due to the commands STORE_USER_ALL (17h) and RESTORE_USER_ALL (18h). If RESTORE_ALL (16h) is sent after STORE_USER_ALL (17h), this CRC error is a false alarm. Its enable bit is 07h[13].
2	STORE_OK	MTP storing state indicator. If MTP storing has finished without errors, this bit is set. The stored MTP commands are: STORE_ALL (15h), STORE_USER_ALL (17h), STORE_S3 (F5h), and DBG_MTP (F7h). 1'b0: MTP storing is not complete 1'b1: MTP storing has completed without errors
1	CML_OTHER_FAULT	Other CML fault indicator. If a false start or stop bit shows up during a normal I2C command, this bit is set and latched. 1'b0: No other CML fault has occurred 1'b1: A different CML fault has occurred
0	MTP_SIGNATURE_ FAULT	MTP signature fault indicator. If the first 2 bytes of the MTP are not 16'h1234, this bit is set and latched. 1'b0: No MTP_SIGNATURE_FAULT has occurred 1'b1: MTP_SIGNATURE_FAULT has occurred

SYS_STATE_DBG (80h)

This register records the state machine working in digital format. It is for debugging use.

Command	SYS_STATE_DBG							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	0	CHIP_PWR_ON_STATE			VR_OFF	SYS_CRTL_STATE		

Bits	Bit Name	Description
7	RESERVED	Unused. Reads are always 0.
6:4	CHIP_PWR_ON_STATE	MTP restoration status after VCC3V3 powers on. 0x03: MTP copying is complete without errors. Normal operation resumes 0x04: There is an MTP signature or CRC error 0x06: A protection occurred and was stored into the MTP during the last VCC3V3 on time

3	VR_OFF	CRC or MTP fault indicator. If CRC_FAULT_TOT_EN is high and an MTP_SIGNATURE_FAULT (the first 2 bytes of MTP are not 1234h) or a CRC fault occurs, this bit is set and latched.
2:0	SYS_CRTL_STATE	Indicates the state of the chip. 0x03: Waiting for V_{IN} to exit under-voltage lockout (UVLO) conditions 0x04: Normal operation 0x07: Protection

FINAL_I2C_ADDR (81h)

This register shows the final 7-bit I²C slave address, regardless of how the pin or register is configured.

Command	FINAL_I2C_ADDR							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	0	FINAL_I2C_ADDR						

Bits	Bit Name	Description
6:0	FINAL_I2C_ADDR	Final I²C address of this chip.

REG_LAST_FAULT_MTP (82h)

If PROTECT_FAULT_RECORD_EN bit (07h, bit[1]) is set high when any one of the eleven protections in PROTECT_SIG_GRP (7Ch) except VIN_UVLO occurs, PROTECT_SIG_GRP (including the VIN_UVLO bit) are stored into the MTP addresses (8'hF4 and 8'hF5, FAULT_RECORD bytes).

During the MTP restore process including the 2 FAULT_RECORD bytes (RESTORE_ALL (16h) and restore_s3 (F6h) and Page 2 byte read commands), if the first 2 bytes of the MTP are correct (16'h1234), then REG_LAST_FAULT_MTP (82h) is updated.

Command	REG_LAST_FAULT_MTP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:0	REG_LAST_FAULT_MTP	Read result of the recorded PROTECT_SIG_GRP (Register 7Ch) in the MTP. Can be reset by sending a CLR_LAST_FAULT_WMTP command (F1h) on Page 0, Page 1, Page or 3, but not on Page 2 when there is no writing or reading on MTP. It is updated during MTP restoration, which includes the 2 FAULT_RECORD MTP addresses (8'hf4 and 8'hf5), if the first 2 bytes of the MTP are 16'h1234.

READ_VIN (88h)

This register shows the calculated V_{IN} from the ADC sampling result on the VINSEN pin.

Command	READ_VIN															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	0	READ_VIN									

Bits	Bit Name	Description
9:0	READ_VIN	0.125V/LSB.

READ_VOUT (8Bh)

This register shows the calculated V_{OUT} from the ADC sampling result on the VOSEN pin.

Command	READ_VOUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	0	0	READ_VOUT								

Bits	Bit Name	Description
8:0	READ_VOUT	62.5mV/LSB.

READ_IOUT (8Ch)

This register shows the calculated I_{OUT} from the ADC sampling result on the IMON pin.

Command	READ_IOUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	0	READ_IOUT									

Bits	Bit Name	Description
9:0	READ_IOUT	0.25A/LSB.

READ_TEMP (8Dh)

This register shows the calculated DrMOS temperature from the ADC sampling result on the TEMP pin.

Command	READ_TEMP							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Description
7:0	READ_TEMP	1°C/LSB.

READ_DIE_TEMP (8Eh)

This register shows the calculated MP2981 die temperature from the ADC sampling result of the chip die temperature sensing.

Command	READ_DIE_TEMP							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function								

Bits	Bit Name	Description
7:0	READ_DIE_TEMP	1°C/LSB.

USER_KEY_INPUT (90h)

After 90h is written with the value of MFR_USER_PWD (44h), writing Page 0 registers is allowed after the start-up restoration. If MFR_USER_PWD is all 0s, it is also allowed. This command is write-only. It is not stored in the MTP. After MTP start-up restoration is complete, send the PMBus command to switch to Page 0, and then set register 90h to be equal to MFR_USER_PWD.

Command	USER_KEY_INPUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Function																

Bits	Bit Name	Description
15:0	USER_KEY_INPUT	Password for PMBus/I^{2}C communication on Page 0. Set by the user. Write-only.

READ_POUT (96h)

This register shows the monitored output power (P_{OUT}) calculated from READ_VOUT and READ_IOUT. The PSYS pin value comes from this register. If PSYS_SEL_2W (06h, bit[13]) is high, READ_POUT[10:1] is sent to the internal PSYS DAC. If PSYS_SEL_2W (06h, bit[13]) is low, READ_POUT[9:0] (READ_POUT[10] = 1 means 10'h3ff) is sent to DAC. The DAC is 10 bits with a 1.28V range. The DAC output voltage is converted to current flowing out of PSYS with a 1μA/10mV resolution. Calculate the PSYS current with Equation (20):

$$PSYS\_CURRENT = \frac{1}{0.01V} \times \frac{1.28V}{DAC\_IN\_10BIT} (\mu A) \quad (20)$$

Where DAC_IN_10BIT is the 10-bit data input into the PSYS DAC.

Command	READ_POUT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	READ_POUT										

Bits	Bit Name	Description
10:0	READ_POUT	1W/LSB.

VIN_SENSE (99h)

This register shows the VISEN pin's 10-bit ADC sampling result. Used for debugging.

Command	VIN_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	0	VIN_SENSE									

Bits	Bit Name	Description
9:0	VIN_SENSE	VINSEN(V) x 1024 / 1.6(V).

VOUT_SENSE (9Ah)

This register shows the VOSEN pin's 10-bit ADC sampling result. Used for debugging.

Command	VOUT_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	0	VOUT_SENSE									

Bits	Bit Name	Description
9:0	VOUT_SENSE	VOSEN(V) x 1024 / 1.6(V).

IOUT_SENSE (9Bh)

This register shows the IMON pin's 10-bit ADC sampling result. Used for debugging.

Command	IOUT_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	0	IOUT_SENSE									

Bits	Bit Name	Description
9:0	IOUT_SENSE	VIMON(V) x 1024 / 1.6(V).

TEMP_SENSE (9Ch)

This register shows the TEMP pin's 10-bit ADC sampling result. Used for debugging.

Command	TEMP_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	0	TEMP_SENSE									

Bits	Bit Name	Description
9:0	TEMP_SENSE	TEMP(V) x 1024 / 1.6(V).

DIE_TEMP_SENSE (9Dh)

This register shows the 10-bit ADC sampling result of the chip's sensed die temperature. Used for debugging.

Command	DIE_TEMP_SENSE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	0	DIE_TEMP_SENSE									

Bits	Bit Name	Description
9:0	DIE_TEMP_SENSE	The ADC result of the temperature from the internal temperature sensor, typically by design. DIE_TEMP_SENSE can be calculated with the following equation: DIE_TEMP_SENSE = INTERNAL_VOLTAGE x 1024 / 1.6 In default mode, the internal temp voltage (mV) = 9.83T(°C) - 109.8. In VBE mode, voltage(mV) = -1.99T(°C) + 724.0.

TON_PWMP (9Eh)

This register monitors the output PWMP t_{ON}. Used for debugging.

Command	TON_PWMP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	0	TON_PWMP									

Bits	Bit Name	Description
9:0	TON_PWMP	t_{ON} for output PWMPs. 5ns/LSB.

TON_SR_PWM (9Fh)

This register monitors the output SR_PWMs t_{ON}. Used for debugging.

Command	TON_SR_PWM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	0	0	0	0	0	0	TON_SR_PWM									

Bits	Bit Name	Description
9:0	TON_SR_PWM	t_{ON} for output SR_PWMs. 5ns/LSB.

CLR_LAST_FAULT_WMTP (F1h)

This command writes the two FAULT_RECORD bytes of MTP to 0000h, and clears the REG_LAST_FAULT_MTP register (82h on Page 0). It can be sent by Page 0, Page 1, Page or 3, but not Page 2.

This command is only valid when MTP is not locked, meaning this is not a write protection. When the FAULT_SINGLE_EN bit (07h, bit[3]) is 0, sending F1h writes all 32 bytes of the third section of the MTP (8'hE0 to 8'hFF MTP addresses), but the 2 FAULT_RECORD bytes are written to 0000h. When FAULT_SINGLE_EN = 1, sending F1h only writes the 2 bytes of MTP, and not all 32 bytes.

READ_LAST_FAULT_TRIG (F2h)

Do not send this command.

CLEAR_STORE_FAULTS (F3h)

If start-up is paused by MTP_LAST_FAULT (the data of the 2 FAULT_RECORD bytes in the MTP is not all zeros, or found during the start-up restoration), sending F3h forces the device to continue start-up. The REG_LAST_FAULT_MTP register (82h) and the 2 bytes in the MTP are not reset by this command. It can be sent by Page 0, Page 1, or Page 3, but not Page 2.

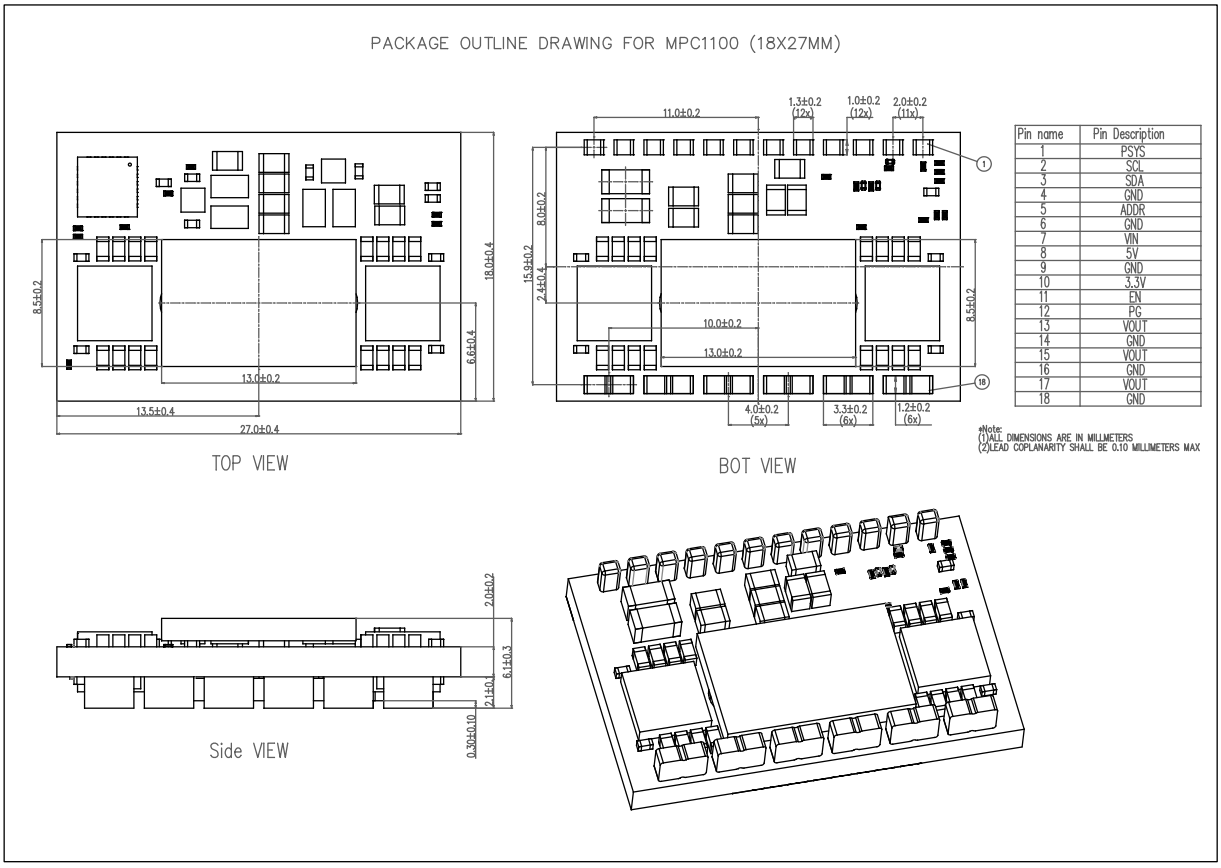
CLEAR_MTP_FAULTS (F4h)

If start-up is paused due to an MTP SIGNATURE fault (the first 2 bytes of MTP are not 1234h) or a CRC fault, sending the F4h message forces the device into the next state (checking REG_LAST_FAULT_MTP (82h)), and start-up continues.

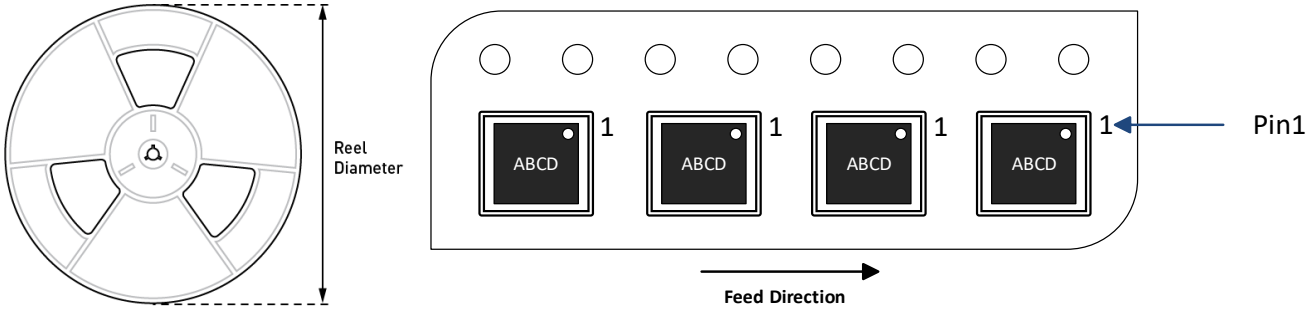
This command clears all CRC errors, MTP_SIGN_FAULT, and resets the DBG_MTP_OK signal (the result of automatically reading MTP after the DBG_MTP command (F7h) is correct) to 1. It can be sent by Page 0, Page 1, or Page 3, but not Page 2.

PACKAGE INFORMATION

Surface-Mount (18mmx27mmx6mm)



CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPC1100-54-0000–Z	Surface-Mount Module (18mmx27mmx6mm)	300	N/A	13in	44mm	24mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.1	8/5/2020	Updated part description	1
		Updated PMBus to PMBus/I^{2}C	4–65
		Update protection mode from hiccup to latch mode, quiescent current label formatting	5
		Updated Figure 13 reference in register description	25
		Updated reference to CTRL_PWM section on page 19	34–35
		Updated 35h and 26h register descriptions	38–39
		Updated datasheet title and header for each page	All
		Grammar/formatting updates	All