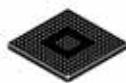


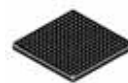


## MPC5668x

### MPC5668x Microcontroller Data Sheet



MAPBGA-208  
17 mm x 17 mm



MAPBGA-256  
17 mm x 17 mm

MPC5668x features:

- 32-bit CPU core complex (e200z650)
  - Compliant with Power Architecture embedded category
  - 32 KB unified cache with line locking and eight-entry store buffer
  - Execution speed static to 116 MHz
- 32-bit I/O processor (e200z0)
  - Execution speed static to 1/2 CPU core speed (58 MHz)
- 2 MB on-chip flash
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 512 KB + 80 KB (592 KB) on-chip ECC SRAM (MPC5668G)
- 128 KB on-chip ECC SRAM (MPC5668E)
- 16-entry Memory Protection Unit (MPC5668E only)
- Direct memory access controller
  - 16-channel on MPC5668G
  - 32-channel on MPC5668E
- Fast ethernet controller
  - Supports 10-Mbps and 100-Mbps IEEE 802.3 MII, 10-Mbps 7-wire interface
  - IEEE 802.3 MAC (compliant with IEEE 802.3 1998 edition)
- Media Local Bus (MLB) interface (MPC5668G only)
  - Supports 16 logical channels, max speed 1024 Fs
- Interrupt controller (INTC) supports 316 external interrupt vectors (22 are reserved)
- System clocks
  - Frequency-modulated phase-locked loop (FMPLL)
  - 4 – 40 MHz crystal oscillator (XTAL)
  - 32 kHz crystal oscillator (XTAL)
  - Dedicated 16 MHz and 128 kHz internal RC oscillators
- Analog to Digital Converter (ADC) module
  - 10-bit A/D resolution
  - 32 external channels
  - 36 internal channels (MPC5668G)
  - 64 internal channels (MPC5668E)
- Cross-Triggering Unit (MPC5668E only)
  - Internal conversion triggering for ADC
  - Triggerable by internal timers or eMIOS200
- Deserial Serial Peripheral Interface (DSPI)
  - Four individual DSPI modules
  - Full duplex, synchronous transfers
  - Master or slave operation
- Inter-IC communication (I<sup>2</sup>C) interface
  - Four individual I<sup>2</sup>C modules
  - Multi-master operation
- Serial Communication Interface (eSCI) module
  - Two-channel DMA interface
  - Configurable as LIN bus master
- eMIOS200 timed input/output
  - 24 channels, 16-bit timers (MPC5668G)
  - 32 channels, 16-bit timers (MPC5668E)
- Controller Area Network (FlexCAN) module
  - Compliant with CAN protocol specification, Version 2.0B active
  - 64 mailboxes, each configurable as transmit or receive
- Dual-channel FlexRay controller
  - Full implementation of FlexRay Protocol Specification 2.1, RevA
  - 128 message buffers
- JTAG controller (MPC5668G only)
  - Compliant with the IEEE 1149.1-2001
- Nexus Development Interface (NDI)
  - Available in 256 MAPBGA package only
  - Compliant with IEEE-ISTO 5001-2003
  - Nexus class 3 development support on e200z650
  - Nexus class 2+ development support on e200z0
- Internal voltage regulator allows operation from single 3.3 V or 5 V supply

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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Preliminary—Subject to Change Without Notice

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5668x products in 208 and 256 MAPBGA packages

# Table of Contents

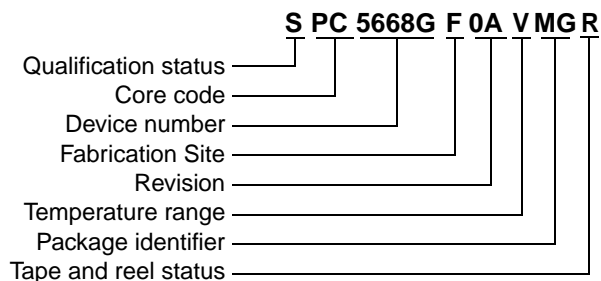
|       |  |    |        |  |    |
|-------|--|----|--------|--|----|
| 1     | Ordering Information   | 3  | 4.8    | Low Voltage Characteristics                                    | 36 |
| 1.1   | Orderable Parts  | 3  | 4.9    | Oscillators Electrical Characteristics                         | 36 |
| 2     | MPC5668x Block Diagrams  | 4  | 4.10   | FMPLL Electrical Characteristics                               | 38 |
| 3     | Pin Assignments  | 6  | 4.11   | ADC Electrical Characteristics                                 | 39 |
| 3.1   | 208-ball MAPBGA Pin Assignments                                  | 6  | 4.12   | Flash Memory Electrical Characteristics                        | 39 |
| 3.2   | 256-ball MAPBGA Pin Assignments                                  | 7  | 4.13   | Pad AC Specifications  | 40 |
| 3.3   | Pin Muxing and Reset States                                      | 8  | 4.14   | AC Timing  | 43 |
| 3.3.1 | Power and Ground Supply Summary                                  | 25 | 4.14.1 | Reset and Boot Configuration Pins                              | 43 |
| 4     | Electrical Characteristics                                       | 26 | 4.14.2 | External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins | 43 |
| 4.1   | Maximum Ratings  | 26 | 4.14.3 | JTAG (IEEE 1149.1) Interface                                   | 44 |
| 4.2   | Thermal Characteristics  | 27 | 4.14.4 | Nexus Debug Interface  | 47 |
| 4.2.1 | General Notes for Specifications at Maximum Junction Temperature | 28 | 4.14.5 | Enhanced Modular I/O Subsystem (eMIOS)                         | 49 |
| 4.3   | ESD Characteristics  | 30 | 4.14.6 | Deserial Serial Peripheral Interface (DSPI)                    | 50 |
| 4.4   | VRC Electrical Specifications                                    | 30 | 4.14.7 | MLB Interface  | 55 |
| 4.5   | DC Electrical Specifications                                     | 30 | 4.14.8 | Fast Ethernet Interface  | 57 |
| 4.6   | Operating Current Specifications                                 | 32 | 5      | Package Characteristics  | 61 |
| 4.7   | I/O Pad Current Specifications                                   | 34 | 5.1    | Package Mechanical Data  | 61 |
| 4.7.1 | I/O Pad $V_{DD33}$ Current Specifications                        | 35 | 6      | Revision History   | 65 |

**Table 1. MPC5668G/MPC5668E Comparison**

| Feature                    | MPC5668G  |            | MPC5668E  |            |
|----------------------------|---|------------|---|------------|
|                            | 208 MAPBGA  | 256 MAPBGA | 208 MAPBGA  | 256 MAPBGA |
| RAM with ECC               | 592 KB  |            | 128 KB  |            |
| MPU                        | No  |            | 16 entry  |            |
| DMA                        | 16-channel  |            | 32-channel  |            |
| Ethernet (FEC)             | Yes   |            | No  |            |
| MediaLB (MLB-DIM)          | Yes   |            | No  |            |
| FlexRay                    | Yes (128 Message Buffers)                             |            | No  |            |
| ADC (10-bit)               | 36 internal channels<br>Supports 32 external channels |            | 64 internal channels<br>Supports 32 external channels |            |
| Total Timer I/O (eMIOS200) | 24 channels, 16-bit                                   |            | 32 channels, 16-bit                                   |            |
| Cross Trigger Unit (CTU)   | No  |            | Yes   |            |
| SCI (eSCI)                 | 6   |            | 12  |            |
| SPI (DSPI)                 | 4   |            | 4   |            |
| CAN (FlexCAN)              | 6   |            | 5   |            |
| I <sup>2</sup> C           | 4   |            | 4   |            |
| Nexus3 Debug (e200Z6)      | —   |            | —   |            |
| Nexus2+ Debug (e200Z0)     | Supported on 256BGA emulation package                 |            | Supported on 256BGA emulation package                 |            |

# 1 Ordering Information

## 1.1 Orderable Parts



### Qualification Status

P = Prototype  
M = Fully spec. qualified, general market flow  
S = Fully spec. qualified, automotive flow

**Core Code** PC = Power Architecture

### Fabrication Site

F = Freescale

### Temperature Range

V = -40 °C to 105 °C

### Package Identifier

MG = 208 MAPBGA Pb-free  
MJ = 256 MAPBGA Pb-free

### Tape and Reel Status

R = Tape and reel  
(blank) = Trays

**Note:** Not all options are available on all devices. Refer to [Table 1](#).

[Table 1](#) shows the orderable part numbers for the MPC5668x.

**Table 1. Orderable Part Numbers**

| Freescale Part Number <sup>1</sup> | Package Description                               | Speed (MHz)                          | Operating Temperature <sup>2</sup> |                       |
|------------------------------------|---|--------------------------------------|------------------------------------|-----------------------|
|                                    |   | Max <sup>3</sup> (f <sub>MAX</sub> ) | Min (T <sub>L</sub> )              | Max (T <sub>H</sub> ) |
| SPC5668GF0AVMG                     | MPC5668G 208 MAPBGA package<br>Lead-free (PbFree) | 116                                  | -40 °C                             | 105 °C                |
| SPC5668GF0AVMJ <sup>4</sup>        | MPC5668G 256 MAPBGA package<br>Lead-free (PbFree) | 116                                  | -40 °C                             | 105 °C                |

<sup>1</sup> All packaged devices are PPC5668x, rather than MPC5668x or SPC5668x, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete. Not all configurations are available in the PPC parts.

<sup>2</sup> The lowest ambient operating temperature (T<sub>A</sub>) is referenced by T<sub>L</sub>; the highest ambient operating temperature is referenced by T<sub>H</sub>.

<sup>3</sup> Maximum speed is the maximum frequency allowed including frequency modulation (FM).

<sup>4</sup> The 256 MAPBGA package for the MPC5668x is not intended for full production qualification, and is supplied for development use only.

# 2 MPC5668x Block Diagrams

Figure 1 shows a top-level block diagram of the MPC5668G device.

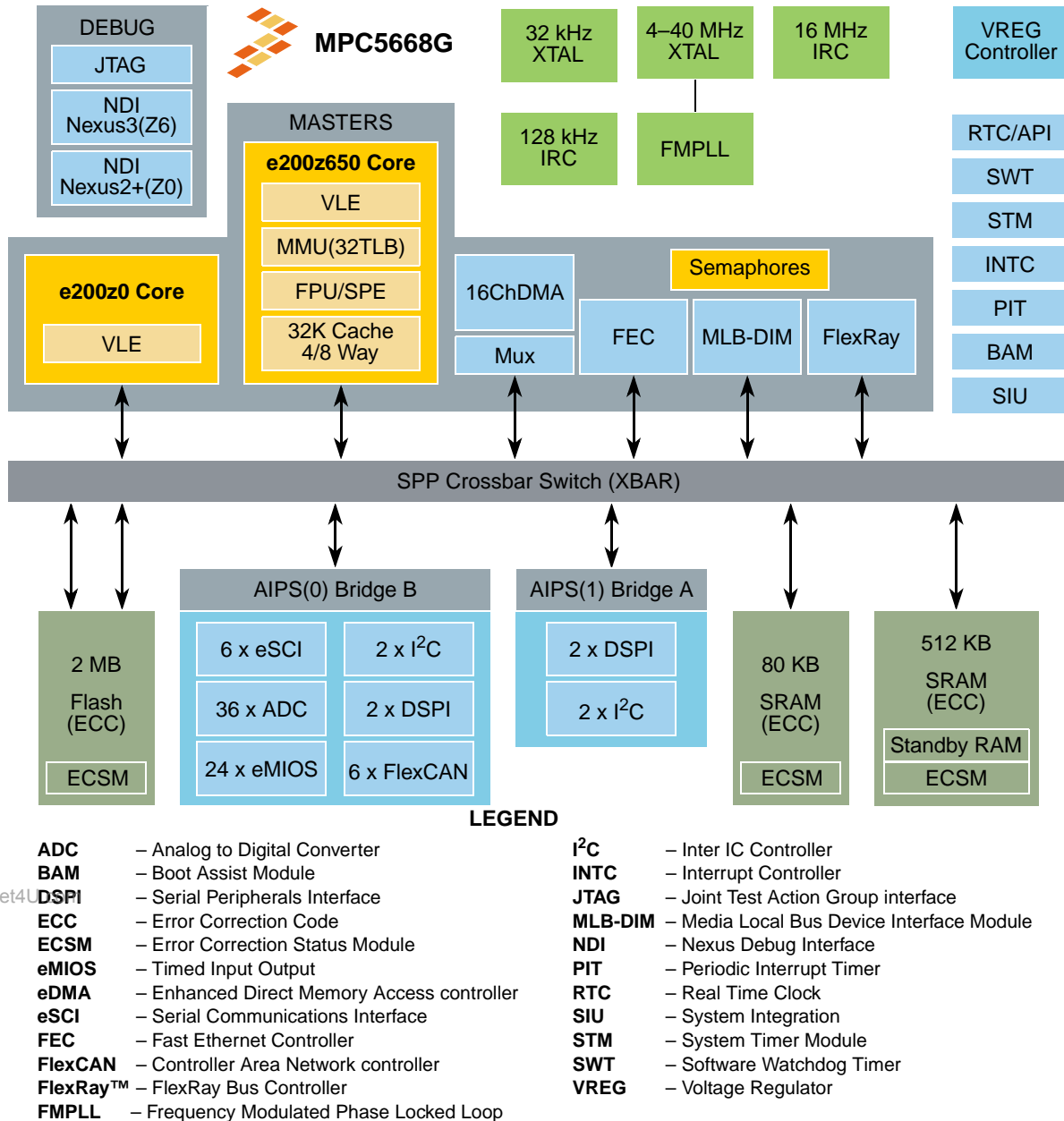
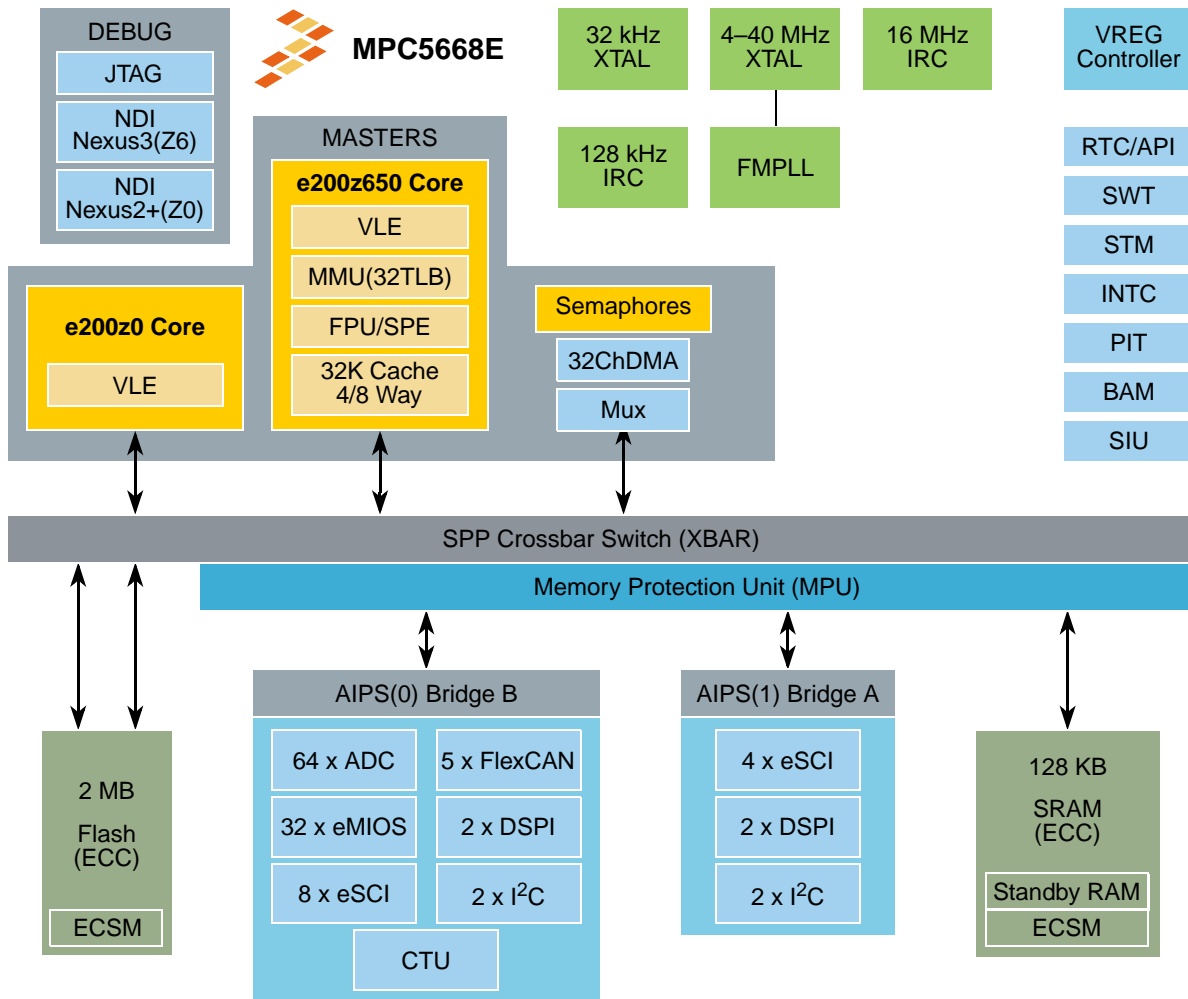


Figure 1. MPC5668G Block Diagram

Figure 2 shows a top level block diagram for the MPC5668E device.



**LEGEND**

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- |  |   |
|--|---|
| <b>ADC</b> – Analog to Digital Converter               | <b>I<sup>2</sup>C</b> – Inter IC Controller     |
| <b>BAM</b> – Boot Assist Module                        | <b>INTC</b> – Interrupt Controller              |
| <b>CTU</b> – Cross Triggering Unit                     | <b>JTAG</b> – Joint Test Action Group interface |
| <b>DSPI</b> – Serial Peripheral Interface controller   | <b>MPU</b> – Memory Protection Unit             |
| <b>ECC</b> – Error Correction Code                     | <b>NDI</b> – Nexus Debug Interface              |
| <b>ECSCM</b> – Error Correction Status Module          | <b>PIT</b> – Periodic Interrupt Timer           |
| <b>eDMA</b> – Enhanced Direct Memory Access controller | <b>RTC</b> – Real Time Clock                    |
| <b>eMIOS200</b> – Timed Input Output                   | <b>SIU</b> – System Integration                 |
| <b>eSCI</b> – Serial Communications Interface          | <b>STM</b> – System Timer Module                |
| <b>FlexCAN</b> – Controller Area Network controller    | <b>SWT</b> – Software Watchdog Timer            |
| <b>FMPLL</b> – Frequency Modulated Phase Locked Loop   | <b>VREG</b> – Voltage Regulator                 |

**Figure 2. MPC5668E Block Diagram**

# 3 Pin Assignments

## 3.1 208-ball MAPBGA Pin Assignments

Figure 3 shows the 208-ball MAPBGA pin assignments.

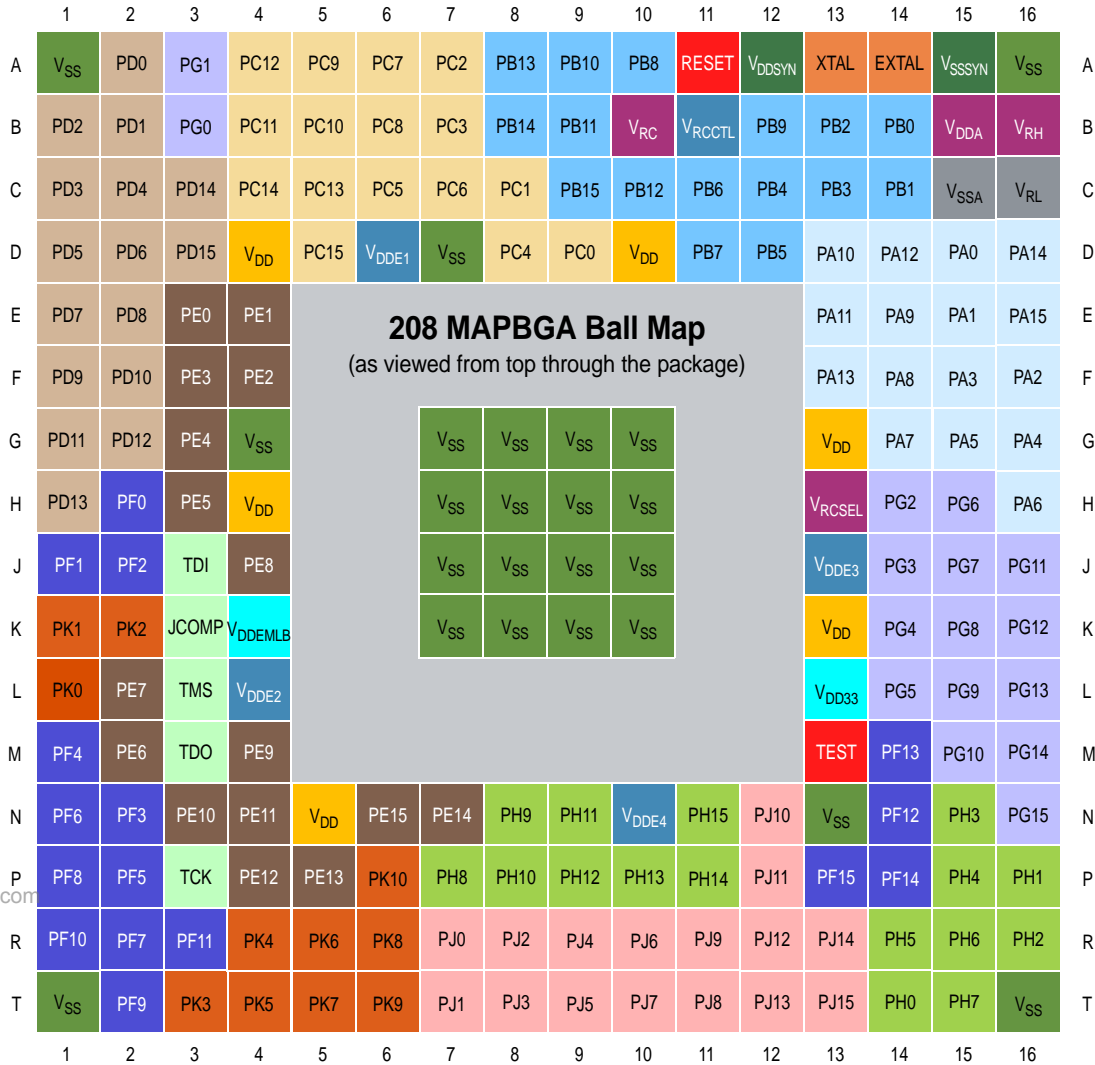


Figure 3. MPC5668x 208-ball MAPBGA (full diagram)

### 3.2 256-ball MAPBGA Pin Assignments

Figure 4 shows the 256-ball MAPBGA pin assignments.

**256 MAPBGA Ball Map**  
(as viewed from top through the package)

|   | 1               | 2    | 3     | 4                   | 5               | 6                   | 7                   | 8               | 9               | 10                | 11                 | 12                  | 13                 | 14              | 15                 | 16              |      |   |
|---|-----------------|------|-------|---------------------|-----------------|---------------------|---------------------|-----------------|-----------------|-------------------|--------------------|---------------------|--------------------|-----------------|--------------------|-----------------|------|---|
| A | V <sub>SS</sub> | PD0  | PG1   | PC12                | PC9             | PC7                 | PC2                 | PB13            | PB10            | PB8               | RESET              | V <sub>DDSYN</sub>  | XTAL               | EXTAL           | V <sub>SSSYN</sub> | V <sub>SS</sub> | A    |   |
| B | PD2             | PD1  | PG0   | PC11                | PC10            | PC8                 | PC3                 | PB14            | PB11            | V <sub>RC</sub>   | V <sub>RCCTL</sub> | PB9                 | PB2                | PB0             | V <sub>DDA</sub>   | V <sub>RH</sub> | B    |   |
| C | PD3             | PD4  | PD14  | PC14                | PC13            | PC5                 | PC6                 | PC1             | PB15            | PB12              | PB6                | PB4                 | PB3                | PB1             | V <sub>SSA</sub>   | V <sub>RL</sub> | C    |   |
| D | PD5             | PD6  | PD15  | V <sub>DD</sub>     | PC15            | V <sub>DDE1</sub>   | V <sub>SS</sub>     | PC4             | PC0             | V <sub>DD</sub>   | PB7                | PB5                 | PA10               | PA12            | PA0                | PA14            | D    |   |
| E | PD7             | PD8  | PE0   | PE1                 | MDO0            | V <sub>DDENEX</sub> | V <sub>SS</sub>     | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>    | V <sub>SS</sub>     | PA11               | PA9             | PA1                | PA15            | E    |   |
| F | PD9             | PD10 | PE3   | PE2                 | MDO1            | V <sub>SS</sub>     | V <sub>SS</sub>     | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>    | V <sub>SS</sub>     | PA13               | PA8             | PA3                | PA2             | F    |   |
| G | PD11            | PD12 | PE4   | V <sub>SS</sub>     | MDO2            | V <sub>SS</sub>     | V <sub>SS</sub>     | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>    | V <sub>SS</sub>     | V <sub>DD</sub>    | PA7             | PA5                | PA4             | G    |   |
| H | PD13            | PF0  | PE5   | V <sub>DD</sub>     | MDO3            | MDO4                | V <sub>SS</sub>     | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>    | V <sub>SS</sub>     | V <sub>RCSEL</sub> | PG2             | PG6                | PA6             | H    |   |
| J | PF1             | PF2  | TDI   | PE8                 | MDO6            | MDO5                | V <sub>SS</sub>     | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>    | V <sub>SS</sub>     | V <sub>DDE3</sub>  | PG3             | PG7                | PG11            | J    |   |
| K | PK1             | PK2  | JCOMP | V <sub>DDEMLB</sub> | MDO7            | V <sub>SS</sub>     | V <sub>SS</sub>     | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>    | V <sub>DDENEX</sub> | V <sub>SS</sub>    | V <sub>DD</sub> | PG4                | PG8             | PG12 | K |
| L | PK0             | PE7  | TMS   | V <sub>DDE2</sub>   | MDO8            | V <sub>SS</sub>     | V <sub>DDENEX</sub> | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>    | V <sub>SS</sub>     | V <sub>DD33</sub>  | PG5             | PG9                | PG13            | L    |   |
| M | PF4             | PE6  | TDO   | PE9                 | MDO9            | MDO10               | MDO11               | MSE01           | MSE00           | MCKO              | EVTI               | EVTO                | TEST               | PF13            | PG10               | PG14            | M    |   |
| N | PF6             | PF3  | PE10  | PE11                | V <sub>DD</sub> | PE15                | PE14                | PH9             | PH11            | V <sub>DDE4</sub> | PH15               | PJ10                | V <sub>SS</sub>    | PF12            | PH3                | PG15            | N    |   |
| P | PF8             | PF5  | TCK   | PE12                | PE13            | PK10                | PH8                 | PH10            | PH12            | PH13              | PH14               | PJ11                | PF15               | PF14            | PH4                | PH1             | P    |   |
| R | PF10            | PF7  | PF11  | PK4                 | PK6             | PK8                 | PJ0                 | PJ2             | PJ4             | PJ6               | PJ9                | PJ12                | PJ14               | PH5             | PH6                | PH2             | R    |   |
| T | V <sub>SS</sub> | PF9  | PK3   | PK5                 | PK7             | PK9                 | PJ1                 | PJ3             | PJ5             | PJ7               | PJ8                | PJ13                | PJ15               | PH0             | PH7                | V <sub>SS</sub> | T    |   |

Figure 4. MPC5668x 256-ball MAPBGA (full diagram)

## Pin Assignments

### 3.3 Pin Muxing and Reset States

Table 2 shows the signals properties for each pin on MPC5668x. For all port pins that have an associated SIU\_PCR $n$  register to control pin properties, the supported functions column lists the functions associated with the programming of the SIU\_PCR $n$ [PA] bit in the order: general-purpose input/output (GPIO), function 1, function 2, and function 3 (see Figure 5). When an alternate function is not implemented for a value of SIU\_PCR $n$ [PA], a dash is shown in the Description column and the respective value in the PA bitfield is reserved.

| Supported Functions <sup>2</sup> | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup> | Description                   |
|----------------------------------|-----------------------------|-----------------|-------------------------------|
| PA[0]                            | 0                           | 00              | Port A GPI ← GPIO             |
| AN[0]                            |                             | 01              | ADC Analog Input ← Function 1 |
|                                  |                             | 10              | —                             |
|                                  |                             | 11              | —                             |
|                                  |                             |                 |                               |

Figure 5. Supported Functions Example

Table 2. MPC5668x Signal Properties

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup> | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup> | Description      | I/O Type | Voltage          | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|----------------------------------|-----------------------------|-----------------|------------------|----------|------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |                                  |                             |                 |                  |          |                  |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| <b>Port A (16)</b>    |                                  |                             |                 |                  |          |                  |                       |                           |                          |                       |         |
| PA0                   | PA[0]<br>AN[0]                   | 0                           | 00              | Port A GPI       | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | D15                   | D15     |
|                       |                                  |                             | 01              | ADC Analog Input | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                | —        |                  |                       |                           |                          |                       |         |
| PA1                   | PA[1]<br>AN[1]                   | 1                           | 00              | Port A GPI       | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | E15                   | E15     |
|                       |                                  |                             | 01              | ADC Analog Input | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                | —        |                  |                       |                           |                          |                       |         |
| PA2                   | PA[2]<br>AN[2]                   | 2                           | 00              | Port A GPI       | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | F16                   | F16     |
|                       |                                  |                             | 01              | ADC Analog Input | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                | —        |                  |                       |                           |                          |                       |         |
| PA3                   | PA[3]<br>AN[3]                   | 3                           | 00              | Port A GPI       | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | F15                   | F15     |
|                       |                                  |                             | 01              | ADC Analog Input | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                | —        |                  |                       |                           |                          |                       |         |
| PA4                   | PA[4]<br>AN[4]                   | 4                           | 00              | Port A GPI       | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | G16                   | G16     |
|                       |                                  |                             | 01              | ADC Analog Input | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                | —        |                  |                       |                           |                          |                       |         |
| PA5                   | PA[5]<br>AN[5]                   | 5                           | 00              | Port A GPI       | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | G15                   | G15     |
|                       |                                  |                             | 01              | ADC Analog Input | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                | —        |                  |                       |                           |                          |                       |         |



Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup> | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup> | Description                 | I/O Type | Voltage          | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|----------------------------------|-----------------------------|-----------------|-----------------------------|----------|------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |                                  |                             |                 |                             |          |                  |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PA6                   | PA[6]<br>AN[6]                   | 6                           | 00              | Port A GPI                  | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | H16                   | H16     |
|                       |                                  |                             | 01              | ADC Analog Input            | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                           | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                           | —        |                  |                       |                           |                          |                       |         |
| PA7                   | PA[7]<br>AN[7]                   | 7                           | 00              | Port A GPI                  | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | G14                   | G14     |
|                       |                                  |                             | 01              | ADC Analog Input            | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                           | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                           | —        |                  |                       |                           |                          |                       |         |
| PA8                   | PA[8]<br>AN[8]                   | 8                           | 00              | Port A GPI                  | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | F14                   | F14     |
|                       |                                  |                             | 01              | ADC Analog Input            | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                           | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                           | —        |                  |                       |                           |                          |                       |         |
| PA9                   | PA[9]<br>AN[9]                   | 9                           | 00              | Port A GPI                  | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | E14                   | E14     |
|                       |                                  |                             | 01              | ADC Analog Input            | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                           | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                           | —        |                  |                       |                           |                          |                       |         |
| PA10                  | PA[10]<br>AN[10]                 | 10                          | 00              | Port A GPI                  | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | D13                   | D13     |
|                       |                                  |                             | 01              | ADC Analog Input            | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                           | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                           | —        |                  |                       |                           |                          |                       |         |
| PA11                  | PA[11]<br>AN[11]                 | 11                          | 00              | Port A GPI                  | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | E13                   | E13     |
|                       |                                  |                             | 01              | ADC Analog Input            | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                           | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                           | —        |                  |                       |                           |                          |                       |         |
| PA12                  | PA[12]<br>AN[12]                 | 12                          | 00              | Port A GPI                  | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | D14                   | D14     |
|                       |                                  |                             | 01              | ADC Analog Input            | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                           | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                           | —        |                  |                       |                           |                          |                       |         |
| PA13                  | PA[13]<br>AN[13]                 | 13                          | 00              | Port A GPI                  | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | F13                   | F13     |
|                       |                                  |                             | 01              | ADC Analog Input            | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | —                           | —        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                           | —        |                  |                       |                           |                          |                       |         |
| PA14                  | PA[14]<br>AN[14]<br>EXTAL32      | 14                          | 00              | Port A GPI                  | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | D16                   | D16     |
|                       |                                  |                             | 01              | ADC Analog Input            | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | External 32 kHz Crystal In  | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                           | —        |                  |                       |                           |                          |                       |         |
| PA15                  | PA[15]<br>AN[15]<br>XTAL32       | 15                          | 00              | Port A GPI                  | I        | V <sub>DDA</sub> | IHA                   | —                         | —                        | E16                   | E16     |
|                       |                                  |                             | 01              | ADC Analog Input            | I        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 10              | External 32 kHz Crystal Out | O        |                  |                       |                           |                          |                       |         |
|                       |                                  |                             | 11              | —                           | —        |                  |                       |                           |                          |                       |         |

## Pin Assignments

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup> | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup>      | Description   | I/O Type           | Voltage           | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|----------------------------------|-----------------------------|----------------------|---|--------------------|-------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |                                  |                             |                      |   |                    |                   |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| <b>Port B (16)</b>    |                                  |                             |                      |   |                    |                   |                       |                           |                          |                       |         |
| PB0                   | PB[0]<br>AN[16]/ANW              | 16                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input/Mux In<br>—<br>—                      | I/O<br>I<br>—<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | B14                   | B14     |
| PB1                   | PB[1]<br>AN[17]/ANX              | 17                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input/Mux In<br>—<br>—                      | I/O<br>I<br>—<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | C14                   | C14     |
| PB2                   | PB[2]<br>AN[18]/ANY              | 18                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input/Mux In<br>—<br>—                      | I/O<br>I<br>—<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | B13                   | B13     |
| PB3                   | PB[3]<br>AN[19]/ANZ              | 19                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input/Mux In<br>—<br>—                      | I/O<br>I<br>—<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | C13                   | C13     |
| PB4                   | PB[4]<br>AN[20]                  | 20                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input<br>—<br>—                             | I/O<br>I<br>—<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | C12                   | C12     |
| PB5                   | PB[5]<br>AN[21]                  | 21                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input<br>—<br>—                             | I/O<br>I<br>—<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | D12                   | D12     |
| PB6                   | PB[6]<br>AN[22]                  | 22                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input<br>—<br>—                             | I/O<br>I<br>—<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | C11                   | C11     |
| PB7                   | PB[7]<br>AN[23]                  | 23                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input<br>—<br>—                             | I/O<br>I<br>—<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | D11                   | D11     |
| PB8                   | PB[8]<br>AN[24]<br>PCS_A[2]      | 24                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input<br>DSPI_A Peripheral Chip Select<br>— | I/O<br>I<br>O<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | A10                   | A10     |
| PB9                   | PB[9]<br>AN[25]<br>PCS_A[3]      | 25                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input<br>DSPI_A Peripheral Chip Select<br>— | I/O<br>I<br>O<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | B12                   | B12     |

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup> | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup>      | Description   | I/O Type           | Voltage           | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|----------------------------------|-----------------------------|----------------------|---|--------------------|-------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |                                  |                             |                      |   |                    |                   |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PB10                  | PB[10]<br>AN[26]<br>PCS_B[4]     | 26                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input<br>DSPI_B Peripheral Chip Select<br>— | I/O<br>I<br>O<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | A9                    | A9      |
| PB11                  | PB[11]<br>AN[27]<br>PCS_B[5]     | 27                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input<br>DSPI_B Peripheral Chip Select<br>— | I/O<br>I<br>O<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | B9                    | B9      |
| PB12                  | PB[12]<br>AN[28]<br>PCS_C[1]     | 28                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input<br>DSPI_C Peripheral Chip Select<br>— | I/O<br>I<br>O<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | C10                   | C10     |
| PB13                  | PB[13]<br>AN[29]<br>PCS_C[2]     | 29                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input<br>DSPI_C Peripheral Chip Select<br>— | I/O<br>I<br>O<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | A8                    | A8      |
| PB14                  | PB[14]<br>AN[30]<br>PCS_D[3]     | 30                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input<br>DSPI_D Peripheral Chip Select<br>— | I/O<br>I<br>O<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | B8                    | B8      |
| PB15                  | PB[15]<br>AN[31]<br>PCS_D[4]     | 31                          | 00<br>01<br>10<br>11 | Port B GPIO<br>ADC Analog Input<br>DSPI_D Peripheral Chip Select<br>— | I/O<br>I<br>O<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | C9                    | C9      |
| <b>Port C (16)</b>    |                                  |                             |                      |   |                    |                   |                       |                           |                          |                       |         |
| PC0                   | PC[0]<br>AN[32]                  | 32                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>—<br>—                             | I/O<br>I<br>—<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | D9                    | D9      |
| PC1                   | PC[1]<br>AN[33]                  | 33                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>—<br>—                             | I/O<br>I<br>—<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | C8                    | C8      |
| PC2                   | PC[2]<br>AN[34]<br>EVTI          | 34                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>Nexus Event In<br>—                | I/O<br>I<br>I<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | A7                    | A7      |
| PC3                   | PC[3]<br>AN[35]<br>EVTO          | 35                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>Nexus Event Out<br>—               | I/O<br>I<br>O<br>— | V <sub>DDE1</sub> | SHA                   | —                         | —                        | B7                    | B7      |

## Pin Assignments

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup> | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup>      | Description   | I/O Type             | Voltage           | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|----------------------------------|-----------------------------|----------------------|---|----------------------|-------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |                                  |                             |                      |   |                      |                   |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PC4                   | PC[4]<br>AN[36]                  | 36                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>—<br>—                               | I/O<br>I<br>—<br>—   | V <sub>DDE1</sub> | SHA                   | —                         | —                        | D8                    | D8      |
| PC5                   | PC[5]<br>AN[37]<br>Z6NMI         | 37                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>Z6 Core Non-Maskable Interrupt<br>—  | I/O<br>I<br>I<br>—   | V <sub>DDE1</sub> | SHA                   | —                         | —                        | C6                    | C6      |
| PC6                   | PC[6]<br>AN[38]<br>Z0NMI         | 38                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>Z0 Core Non-Maskable Interrupt<br>—  | I/O<br>I<br>I<br>—   | V <sub>DDE1</sub> | SHA                   | —                         | —                        | C7                    | C7      |
| PC7                   | PC[7]<br>AN[39]<br>FR_DBG3       | 39                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>FlexRay Debug<br>—                   | I/O<br>I<br>O<br>—   | V <sub>DDE1</sub> | SHA                   | —                         | —                        | A6                    | A6      |
| PC8                   | PC[8]<br>AN[40]<br>FR_DBG2       | 40                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>FlexRay Debug<br>—                   | I/O<br>I<br>O<br>—   | V <sub>DDE1</sub> | SHA                   | —                         | —                        | B6                    | B6      |
| PC9                   | PC[9]<br>AN[41]<br>FR_DBG1       | 41                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>FlexRay Debug<br>—                   | I/O<br>I<br>O<br>—   | V <sub>DDE1</sub> | SHA                   | —                         | —                        | A5                    | A5      |
| PC10                  | PC[10]<br>AN[42]<br>FR_DBG0      | 42                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>FlexRay Debug<br>—                   | I/O<br>I<br>O<br>—   | V <sub>DDE1</sub> | SHA                   | —                         | —                        | B5                    | B5      |
| PC11                  | PC[11]<br>AN[43]<br>—<br>SCL_C   | 43                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>—<br>I <sup>2</sup> C_C Serial Clock | I/O<br>I<br>—<br>I/O | V <sub>DDE1</sub> | SHA                   | —                         | —                        | B4                    | B4      |
| PC12                  | PC[12]<br>AN[44]<br>—<br>SDA_C   | 44                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>—<br>I <sup>2</sup> C_C Serial Data  | I/O<br>I<br>—<br>I/O | V <sub>DDE1</sub> | SHA                   | —                         | —                        | A4                    | A4      |
| PC13                  | PC[13]<br>AN[45]<br>—<br>MA[0]   | 45                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>—<br>ADC Ext. Mux Address Select     | I/O<br>I<br>—<br>O   | V <sub>DDE1</sub> | SHA                   | —                         | —                        | C5                    | C5      |
| PC14                  | PC[14]<br>AN[46]<br>—<br>MA[1]   | 46                          | 00<br>01<br>10<br>11 | Port C GPIO<br>ADC Analog Input<br>—<br>ADC Ext. Mux Address Select     | I/O<br>I<br>—<br>O   | V <sub>DDE1</sub> | SHA                   | —                         | —                        | C4                    | C4      |

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup>  | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup> | Description                     | I/O Type | Voltage           | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|-----------------------------------|-----------------------------|-----------------|---------------------------------|----------|-------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |                                   |                             |                 |                                 |          |                   |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PC15                  | PC[15]<br>AN[47]<br>—<br>MA[2]    | 47                          | 00              | Port C GPIO                     | I/O      | V <sub>DDE1</sub> | SHA                   | —                         | —                        | D5                    | D5      |
|                       |                                   |                             | 01              | ADC Analog Input                | I        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 10              | —                               | —        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 11              | ADC Ext. Mux Address Select     | O        |                   |                       |                           |                          |                       |         |
| <b>Port D (16)</b>    |                                   |                             |                 |                                 |          |                   |                       |                           |                          |                       |         |
| PD0                   | PD[0]<br>CNTX_A                   | 48                          | 00              | Port D GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | A2                    | A2      |
|                       |                                   |                             | 01              | FlexCAN_A Transmit              | O        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 10              | —                               | —        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 11              | —                               | —        |                   |                       |                           |                          |                       |         |
| PD1                   | PD[1]<br>CNRX_A                   | 49                          | 00              | Port D GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | B2                    | B2      |
|                       |                                   |                             | 01              | FlexCAN_A Receive               | I        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 10              | —                               | —        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 11              | —                               | —        |                   |                       |                           |                          |                       |         |
| PD2                   | PD[2]<br>CNTX_B                   | 50                          | 00              | Port D GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | B1                    | B1      |
|                       |                                   |                             | 01              | FlexCAN_B Transmit              | O        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 10              | —                               | —        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 11              | —                               | —        |                   |                       |                           |                          |                       |         |
| PD3                   | PD[3]<br>CNRX_B                   | 51                          | 00              | Port D GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | C1                    | C1      |
|                       |                                   |                             | 01              | FlexCAN_B Receive               | I        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 10              | —                               | —        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 11              | —                               | —        |                   |                       |                           |                          |                       |         |
| PD4                   | PD[4]<br>CNTX_C                   | 52                          | 00              | Port D GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | C2                    | C2      |
|                       |                                   |                             | 01              | FlexCAN_C Transmit              | O        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 10              | —                               | —        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 11              | —                               | —        |                   |                       |                           |                          |                       |         |
| PD5                   | PD[5]<br>CNRX_C                   | 53                          | 00              | Port D GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | D1                    | D1      |
|                       |                                   |                             | 01              | FlexCAN_C Receive               | I        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 10              | —                               | —        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 11              | —                               | —        |                   |                       |                           |                          |                       |         |
| PD6                   | PD[6]<br>CNTX_D<br>TXD_K<br>SCL_B | 54                          | 00              | Port D GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | D2                    | D2      |
|                       |                                   |                             | 01              | FlexCAN_D Transmit              | O        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 10              | SCI_K Transmit                  | O        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 11              | I <sup>2</sup> C_B Serial Clock | I/O      |                   |                       |                           |                          |                       |         |
| PD7                   | PD[7]<br>CNRX_D<br>RXD_K<br>SDA_B | 55                          | 00              | Port D GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | E1                    | E1      |
|                       |                                   |                             | 01              | FlexCAN_D Receive               | I        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 10              | SCI_K Receive                   | I        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 11              | I <sup>2</sup> C_B Serial Data  | I/O      |                   |                       |                           |                          |                       |         |
| PD8                   | PD[8]<br>CNTX_E<br>TXD_L<br>SCL_C | 56                          | 00              | Port D GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | E2                    | E2      |
|                       |                                   |                             | 01              | FlexCAN_E Transmit              | O        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 10              | SCI_L Transmit                  | O        |                   |                       |                           |                          |                       |         |
|                       |                                   |                             | 11              | I <sup>2</sup> C_C Serial Clock | I/O      |                   |                       |                           |                          |                       |         |

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup>   | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup>      | Description  | I/O Type             | Voltage           | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|------------------------------------|-----------------------------|----------------------|--|----------------------|-------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |                                    |                             |                      |  |                      |                   |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PD9                   | PD[9]<br>CNRX_E<br>RXD_L<br>SDA_C  | 57                          | 00<br>01<br>10<br>11 | Port D GPIO<br>FlexCAN_E Receive<br>SCI_L Receive<br>I <sup>2</sup> C_C Serial Data    | I/O<br>I<br>I<br>I/O | V <sub>DDE2</sub> | SH                    | —                         | —                        | F1                    | F1      |
| PD10                  | PD[10]<br>CNTX_F<br>TXD_M<br>SCL_D | 58                          | 00<br>01<br>10<br>11 | Port D GPIO<br>FlexCAN_F Transmit<br>SCI_M Transmit<br>I <sup>2</sup> C_D Serial Clock | I/O<br>O<br>O<br>I/O | V <sub>DDE2</sub> | SH                    | —                         | —                        | F2                    | F2      |
| PD11                  | PD[11]<br>CNRX_F<br>RXD_M<br>SDA_D | 59                          | 00<br>01<br>10<br>11 | Port D GPIO<br>FlexCAN_F Receive<br>SCI_M Receive<br>I <sup>2</sup> C_D Serial Data    | I/O<br>I<br>I<br>I/O | V <sub>DDE2</sub> | SH                    | —                         | —                        | G1                    | G1      |
| PD12                  | PD[12]<br>TXD_A                    | 60                          | 00<br>01<br>10<br>11 | Port D GPIO<br>eSCI_A Transmit<br>—<br>—   | I/O<br>O<br>—<br>—   | V <sub>DDE2</sub> | SH                    | —                         | —                        | G2                    | G2      |
| PD13                  | PD[13]<br>RXD_A                    | 61                          | 00<br>01<br>10<br>11 | Port D GPIO<br>eSCI_A Receive<br>—<br>—  | I/O<br>I<br>—<br>—   | V <sub>DDE2</sub> | SH                    | —                         | —                        | H1                    | H1      |
| PD14                  | PD[14]<br>TXD_B                    | 62                          | 00<br>01<br>10<br>11 | Port D GPIO<br>eSCI_B Transmit<br>—<br>—   | I/O<br>O<br>—<br>—   | V <sub>DDE2</sub> | SH                    | —                         | —                        | C3                    | C3      |
| PD15                  | PD[15]<br>RXD_B                    | 63                          | 00<br>01<br>10<br>11 | Port D GPIO<br>eSCI_B Receive<br>—<br>—  | I/O<br>I<br>—<br>—   | V <sub>DDE2</sub> | SH                    | —                         | —                        | D3                    | D3      |
| <b>Port E (16)</b>    |                                    |                             |                      |  |                      |                   |                       |                           |                          |                       |         |
| PE0                   | PE[0]<br>TXD_C<br>eMIOS[31]        | 64                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_C Transmit<br>eMIOS Channel<br>—                                   | I/O<br>O<br>I/O<br>— | V <sub>DDE2</sub> | SH                    | —                         | —                        | E3                    | E3      |
| PE1                   | PE[1]<br>RXD_C<br>eMIOS[30]        | 65                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_C Receive<br>eMIOS Channel<br>—                                    | I/O<br>I<br>I/O<br>— | V <sub>DDE2</sub> | SH                    | —                         | —                        | E4                    | E4      |
| PE2                   | PE[2]<br>TXD_D<br>eMIOS[29]        | 66                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_D Transmit<br>eMIOS Channel<br>—                                   | I/O<br>O<br>I/O<br>— | V <sub>DDE2</sub> | SH                    | —                         | —                        | F4                    | F4      |

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup> | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup>      | Description  | I/O Type        | Voltage           | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|----------------------------------|-----------------------------|----------------------|--|-----------------|-------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |                                  |                             |                      |  |                 |                   |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PE3                   | PE[3]<br>RXD_D<br>eMIOS[28]      | 67                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_D Receive<br>eMIOS Channel<br>—                  | I/O<br>I<br>I/O | V <sub>DDE2</sub> | SH                    | —                         | —                        | F3                    | F3      |
| PE4                   | PE[4]<br>TXD_E<br>eMIOS[27]      | 68                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_E Transmit<br>eMIOS Channel<br>—                 | I/O<br>O<br>I/O | V <sub>DDE2</sub> | SH                    | —                         | —                        | G3                    | G3      |
| PE5                   | PE[5]<br>RXD_E<br>eMIOS[26]      | 69                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_E Receive<br>eMIOS Channel<br>—                  | I/O<br>I<br>I/O | V <sub>DDE2</sub> | SH                    | —                         | —                        | H3                    | H3      |
| PE6                   | PE[6]<br>TXD_F<br>eMIOS[25]      | 70                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_F Transmit<br>eMIOS Channel<br>—                 | I/O<br>O<br>I/O | V <sub>DDE2</sub> | SH                    | —                         | —                        | M2                    | M2      |
| PE7                   | PE[7]<br>RXD_F<br>eMIOS[24]      | 71                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_F Receive<br>eMIOS Channel<br>—                  | I/O<br>I<br>I/O | V <sub>DDE2</sub> | SH                    | —                         | —                        | L2                    | L2      |
| PE8                   | PE[8]<br>TXD_G<br>PCS_A[1]       | 72                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_G Transmit<br>DSPI_A Peripheral Chip Select<br>— | I/O<br>O<br>O   | V <sub>DDE2</sub> | SH                    | —                         | —                        | J4                    | J4      |
| PE9                   | PE[9]<br>RXD_G<br>PCS_A[4]       | 73                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_G Receive<br>DSPI_A Peripheral Chip Select<br>—  | I/O<br>I<br>O   | V <sub>DDE2</sub> | SH                    | —                         | —                        | M4                    | M4      |
| PE10                  | PE[10]<br>TXD_H<br>PCS_B[3]      | 74                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_H Transmit<br>DSPI_B Peripheral Chip Select<br>— | I/O<br>O<br>O   | V <sub>DDE2</sub> | SH                    | —                         | —                        | N3                    | N3      |
| PE11                  | PE[11]<br>RXD_H<br>PCS_B[2]      | 75                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_H Receive<br>DSPI_B Peripheral Chip Select<br>—  | I/O<br>I<br>O   | V <sub>DDE2</sub> | SH                    | —                         | —                        | N4                    | N4      |
| PE12                  | PE[12]<br>TXD_J<br>PCS_C[5]      | 76                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_J Transmit<br>DSPI_C Peripheral Chip Select<br>— | I/O<br>O<br>O   | V <sub>DDE2</sub> | SH                    | —                         | —                        | P4                    | P4      |
| PE13                  | PE[13]<br>RXD_J<br>PCS_C[3]      | 77                          | 00<br>01<br>10<br>11 | Port E GPIO<br>eSCI_J Receive<br>DSPI_C Peripheral Chip Select<br>—  | I/O<br>I<br>O   | V <sub>DDE2</sub> | SH                    | —                         | —                        | P5                    | P5      |

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup>          | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup> | Description                     | I/O Type | Voltage           | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|---|-----------------------------|-----------------|---------------------------------|----------|-------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |   |                             |                 |                                 |          |                   |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PE14                  | PE[14]<br>SCL_A<br>PCS_D[2]               | 78                          | 00              | Port E GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | N7                    | N7      |
|                       |   |                             | 01              | I <sup>2</sup> C_A Serial Clock | I/O      |                   |                       |                           |                          |                       |         |
|                       |   |                             | 10              | DSPI_D Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 11              | —                               | —        |                   |                       |                           |                          |                       |         |
| PE15                  | PE[15]<br>SDA_A<br>PCS_D[5]               | 79                          | 00              | Port E GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | N6                    | N6      |
|                       |   |                             | 01              | I <sup>2</sup> C_A Serial Data  | I/O      |                   |                       |                           |                          |                       |         |
|                       |   |                             | 10              | DSPI_D Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 11              | —                               | —        |                   |                       |                           |                          |                       |         |
| <b>Port F (16)</b>    |   |                             |                 |                                 |          |                   |                       |                           |                          |                       |         |
| PF0                   | PF[0]<br>SCK_A                            | 80                          | 00              | Port F GPIO                     | I/O      | V <sub>DDE2</sub> | MH                    | —                         | —                        | H2                    | H2      |
|                       |   |                             | 01              | DSPI_A Serial Clock             | I/O      |                   |                       |                           |                          |                       |         |
|                       |   |                             | 10              | —                               | —        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 11              | —                               | —        |                   |                       |                           |                          |                       |         |
| PF1                   | PF[1]<br>SOUT_A                           | 81                          | 00              | Port F GPIO                     | I/O      | V <sub>DDE2</sub> | MH                    | —                         | —                        | J1                    | J1      |
|                       |   |                             | 01              | DSPI_A Serial Data Out          | O        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 10              | —                               | —        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 11              | —                               | —        |                   |                       |                           |                          |                       |         |
| PF2                   | PF[2]<br>SIN_A                            | 82                          | 00              | Port F GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | J2                    | J2      |
|                       |   |                             | 01              | DSPI_A Serial Data In           | I        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 10              | —                               | —        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 11              | —                               | —        |                   |                       |                           |                          |                       |         |
| PF3                   | PF[3]<br>PCS_A[0]<br>PCS_B[5]<br>PCS_C[4] | 83                          | 00              | Port F GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | N2                    | N2      |
|                       |   |                             | 01              | DSPI_A Peripheral Chip Select   | I/O      |                   |                       |                           |                          |                       |         |
|                       |   |                             | 10              | DSPI_B Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 11              | DSPI_C Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
| PF4                   | PF[4]<br>SCK_B<br>PCS_A[1]<br>PCS_C[2]    | 84                          | 00              | Port F GPIO                     | I/O      | V <sub>DDE2</sub> | MH                    | —                         | —                        | M1                    | M1      |
|                       |   |                             | 01              | DSPI_B Serial Clock             | I/O      |                   |                       |                           |                          |                       |         |
|                       |   |                             | 10              | DSPI_A Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 11              | DSPI_C Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
| PF5                   | PF[5]<br>SOUT_B<br>PCS_A[2]<br>PCS_C[3]   | 85                          | 00              | Port F GPIO                     | I/O      | V <sub>DDE2</sub> | MH                    | —                         | —                        | P2                    | P2      |
|                       |   |                             | 01              | DSPI_B Serial Data Out          | O        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 10              | DSPI_A Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 11              | DSPI_C Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
| PF6                   | PF[6]<br>SIN_B<br>PCS_A[3]<br>PCS_C[5]    | 86                          | 00              | Port F GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | N1                    | N1      |
|                       |   |                             | 01              | DSPI_B Serial Data In           | I        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 10              | DSPI_A Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 11              | DSPI_C Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
| PF7                   | PF[7]<br>PCS_B[0]<br>PCS_C[5]<br>PCS_D[4] | 87                          | 00              | Port F GPIO                     | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | R2                    | R2      |
|                       |   |                             | 01              | DSPI_B Peripheral Chip Select   | I/O      |                   |                       |                           |                          |                       |         |
|                       |   |                             | 10              | DSPI_C Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
|                       |   |                             | 11              | DSPI_D Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |



Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup>           | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup> | Description                   | I/O Type | Voltage           | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|--|-----------------------------|-----------------|-------------------------------|----------|-------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |  |                             |                 |                               |          |                   |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PF8                   | PF[8]<br>SCK_C                             | 88                          | 00              | Port F GPIO                   | I/O      | V <sub>DDE2</sub> | MH                    | —                         | —                        | P1                    | P1      |
|                       |  |                             | 01              | DSPI_C Serial Clock           | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | —                             | —        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | —                             | —        |                   |                       |                           |                          |                       |         |
| PF9                   | PF[9]<br>SOUT_C                            | 89                          | 00              | Port F GPIO                   | I/O      | V <sub>DDE2</sub> | MH                    | —                         | —                        | T2                    | T2      |
|                       |  |                             | 01              | DSPI_C Serial Data Out        | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | —                             | —        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | —                             | —        |                   |                       |                           |                          |                       |         |
| PF10                  | PF[10]<br>SIN_C                            | 90                          | 00              | Port F GPIO                   | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | R1                    | R1      |
|                       |  |                             | 01              | DSPI_C Serial Data In         | I        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | —                             | —        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | —                             | —        |                   |                       |                           |                          |                       |         |
| PF11                  | PF[11]<br>PCS_C[0]<br>PCS_D[5]<br>PCS_A[4] | 91                          | 00              | Port F GPIO                   | I/O      | V <sub>DDE2</sub> | SH                    | —                         | —                        | R3                    | R3      |
|                       |  |                             | 01              | DSPI_C Peripheral Chip Select | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | DSPI_D Peripheral Chip Select | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | DSPI_A Peripheral Chip Select | O        |                   |                       |                           |                          |                       |         |
| PF12                  | PF[12]<br>SCK_D                            | 92                          | 00              | Port F GPIO                   | I/O      | V <sub>DDE3</sub> | MH                    | —                         | —                        | N14                   | N14     |
|                       |  |                             | 01              | DSPI_D Serial Clock           | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | —                             | —        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | —                             | —        |                   |                       |                           |                          |                       |         |
| PF13                  | PF[13]<br>SOUT_D                           | 93                          | 00              | Port F GPIO                   | I/O      | V <sub>DDE3</sub> | MH                    | —                         | —                        | M14                   | M14     |
|                       |  |                             | 01              | DSPI_D Serial Data Out        | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | —                             | —        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | —                             | —        |                   |                       |                           |                          |                       |         |
| PF14                  | PF[14]<br>SIN_D                            | 94                          | 00              | Port F GPIO                   | I/O      | V <sub>DDE3</sub> | SH                    | —                         | —                        | P14                   | P14     |
|                       |  |                             | 01              | DSPI_D Serial Data In         | I        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | —                             | —        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | —                             | —        |                   |                       |                           |                          |                       |         |
| PF15                  | PF[15]<br>PCS_D[0]<br>PCS_A[5]<br>PCS_B[4] | 95                          | 00              | Port F GPIO                   | I/O      | V <sub>DDE3</sub> | SH                    | —                         | —                        | P13                   | P13     |
|                       |  |                             | 01              | DSPI_D Peripheral Chip Select | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | DSPI_A Peripheral Chip Select | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | DSPI_B Peripheral Chip Select | O        |                   |                       |                           |                          |                       |         |
| <b>Port G (16)</b>    |  |                             |                 |                               |          |                   |                       |                           |                          |                       |         |
| PG0                   | PG[0]<br>PCS_A[4]<br>PCS_B[3]<br>AN[48]    | 96                          | 00              | Port G GPIO                   | I/O      | V <sub>DDE2</sub> | SHA                   | —                         | —                        | B3                    | B3      |
|                       |  |                             | 01              | DSPI_A Peripheral Chip Select | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | DSPI_B Peripheral Chip Select | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | ADC Analog Input              | I        |                   |                       |                           |                          |                       |         |
| PG1                   | PG[1]<br>PCS_A[5]<br>PCS_B[4]<br>AN[49]    | 97                          | 00              | Port G GPIO                   | I/O      | V <sub>DDE2</sub> | SHA                   | —                         | —                        | A3                    | A3      |
|                       |  |                             | 01              | DSPI_A Peripheral Chip Select | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | DSPI_B Peripheral Chip Select | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | ADC Analog Input              | I        |                   |                       |                           |                          |                       |         |

## Pin Assignments

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup>           | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup> | Description                     | I/O Type | Voltage           | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|--|-----------------------------|-----------------|---------------------------------|----------|-------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |  |                             |                 |                                 |          |                   |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PG2                   | PG[2]<br>PCS_D[1]<br>SCL_C<br>AN[50]       | 98                          | 00              | Port G GPIO                     | I/O      | V <sub>DDE3</sub> | SHA                   | —                         | —                        | H14                   | H14     |
|                       |  |                             | 01              | DSPI_D Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | I <sup>2</sup> C_C Serial Clock | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | ADC Analog Input                | I        |                   |                       |                           |                          |                       |         |
| PG3                   | PG[3]<br>PCS_D[2]<br>SDA_C<br>AN[51]       | 99                          | 00              | Port G GPIO                     | I/O      | V <sub>DDE3</sub> | SHA                   | —                         | —                        | J14                   | J14     |
|                       |  |                             | 01              | DSPI_D Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | I <sup>2</sup> C_C Serial Data  | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | ADC Analog Input                | I        |                   |                       |                           |                          |                       |         |
| PG4                   | PG[4]<br>PCS_D[3]<br>SCL_B<br>AN[52]       | 100                         | 00              | Port G GPIO                     | I/O      | V <sub>DDE3</sub> | SHA                   | —                         | —                        | K14                   | K14     |
|                       |  |                             | 01              | DSPI_D Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | I <sup>2</sup> C_B Serial Clock | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | ADC Analog Input                | I        |                   |                       |                           |                          |                       |         |
| PG5                   | PG[5]<br>PCS_D[4]<br>SDA_B<br>AN[53]       | 101                         | 00              | Port G GPIO                     | I/O      | V <sub>DDE3</sub> | SHA                   | —                         | —                        | L14                   | L14     |
|                       |  |                             | 01              | DSPI_D Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | I <sup>2</sup> C_C Serial Data  | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | ADC Analog Input                | I        |                   |                       |                           |                          |                       |         |
| PG6                   | PG[6]<br>PCS_C[1]<br>FEC_MDC<br>AN[54]     | 102                         | 00              | Port G GPIO                     | I/O      | V <sub>DDE3</sub> | MHA                   | —                         | —                        | H15                   | H15     |
|                       |  |                             | 01              | DSPI_C Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | Ethernet Mgmt. Data Clock       | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | ADC Analog Input                | I        |                   |                       |                           |                          |                       |         |
| PG7                   | PG[7]<br>PCS_C[2]<br>FEC_MDIO<br>AN[55]    | 103                         | 00              | Port G GPIO                     | I/O      | V <sub>DDE3</sub> | MHA                   | —                         | —                        | J15                   | J15     |
|                       |  |                             | 01              | DSPI_C Peripheral Chip Select   | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | Ethernet Mgmt. Data I/O         | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | ADC Analog Input                | I        |                   |                       |                           |                          |                       |         |
| PG8                   | PG[8]<br>eMIOS[7]<br>FEC_TX_CLK<br>AN[56]  | 104                         | 00              | Port G GPIO                     | I/O      | V <sub>DDE3</sub> | SHA                   | —                         | —                        | K15                   | K15     |
|                       |  |                             | 01              | eMIOS Channel                   | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | Ethernet Transmit Clock         | I        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | ADC Analog Input                | I        |                   |                       |                           |                          |                       |         |
| PG9                   | PG[9]<br>eMIOS[6]<br>FEC_CRIS<br>AN[57]    | 105                         | 00              | Port G GPIO                     | I/O      | V <sub>DDE3</sub> | SHA                   | —                         | —                        | L15                   | L15     |
|                       |  |                             | 01              | eMIOS Channel                   | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | Ethernet Carrier Sense          | I        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | ADC Analog Input                | I        |                   |                       |                           |                          |                       |         |
| PG10                  | PG[10]<br>eMIOS[5]<br>FEC_TX_ER<br>AN[58]  | 106                         | 00              | Port G GPIO                     | I/O      | V <sub>DDE3</sub> | MHA                   | —                         | —                        | M15                   | M15     |
|                       |  |                             | 01              | eMIOS Channel                   | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | Ethernet Transmit Error         | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | ADC Analog Input                | I        |                   |                       |                           |                          |                       |         |
| PG11                  | PG[11]<br>eMIOS[4]<br>FEC_RX_CLK<br>AN[59] | 107                         | 00              | Port G GPIO                     | I/O      | V <sub>DDE3</sub> | SHA                   | —                         | —                        | J16                   | J16     |
|                       |  |                             | 01              | eMIOS Channel                   | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | Ethernet Receive Clock          | I        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | ADC Analog Input                | I        |                   |                       |                           |                          |                       |         |
| PG12                  | PG[12]<br>eMIOS[3]<br>FEC_TXD[0]<br>AN[60] | 108                         | 00              | Port G GPIO                     | I/O      | V <sub>DDE3</sub> | MHA                   | —                         | —                        | K16                   | K16     |
|                       |  |                             | 01              | eMIOS Channel                   | I/O      |                   |                       |                           |                          |                       |         |
|                       |  |                             | 10              | Ethernet Transmit Data          | O        |                   |                       |                           |                          |                       |         |
|                       |  |                             | 11              | ADC Analog Input                | I        |                   |                       |                           |                          |                       |         |

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup>           | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup>      | Description  | I/O Type             | Voltage           | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|--|-----------------------------|----------------------|--|----------------------|-------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |  |                             |                      |  |                      |                   |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PG13                  | PG[13]<br>eMIOS[2]<br>FEC_TXD[1]<br>AN[61] | 109                         | 00<br>01<br>10<br>11 | Port G GPIO<br>eMIOS Channel<br>Ethernet Transmit Data<br>ADC Analog Input | I/O<br>I/O<br>O<br>I | V <sub>DDE3</sub> | MHA                   | —                         | —                        | L16                   | L16     |
| PG14                  | PG[14]<br>eMIOS[1]<br>FEC_TXD[2]<br>AN[62] | 110                         | 00<br>01<br>10<br>11 | Port G GPIO<br>eMIOS Channel<br>Ethernet Transmit Data<br>ADC Analog Input | I/O<br>I/O<br>O<br>I | V <sub>DDE3</sub> | MHA                   | —                         | —                        | M16                   | M16     |
| PG15                  | PG[15]<br>eMIOS[0]<br>FEC_TXD[3]<br>AN[63] | 111                         | 00<br>01<br>10<br>11 | Port G GPIO<br>eMIOS Channel<br>Ethernet Transmit Data<br>ADC Analog Input | I/O<br>I/O<br>O<br>I | V <sub>DDE3</sub> | MHA                   | —                         | —                        | N16                   | N16     |
| <b>Port H (16)</b>    |  |                             |                      |  |                      |                   |                       |                           |                          |                       |         |
| PH0                   | PH[0]<br>eMIOS[31]<br>FEC_COL              | 112                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>Ethernet Collision<br>—                    | I/O<br>I/O<br>I<br>— | V <sub>DDE3</sub> | SH                    | —                         | —                        | T14                   | T14     |
| PH1                   | PH[1]<br>eMIOS[30]<br>FEC_RX_DV            | 113                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>Ethernet Receive Data Valid<br>—           | I/O<br>I/O<br>I<br>— | V <sub>DDE3</sub> | SH                    | —                         | —                        | P16                   | P16     |
| PH2                   | PH[2]<br>eMIOS[29]<br>FEC_TX_EN            | 114                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>Ethernet Transmit Enable<br>—              | I/O<br>I/O<br>O<br>— | V <sub>DDE3</sub> | MH                    | —                         | —                        | R16                   | R16     |
| PH3                   | PH[3]<br>eMIOS[28]<br>FEC_RX_ER            | 115                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>Ethernet Receive Error<br>—                | I/O<br>I/O<br>I<br>— | V <sub>DDE3</sub> | SH                    | —                         | —                        | N15                   | N15     |
| PH4                   | PH[4]<br>eMIOS[27]<br>FEC_RXD[0]           | 116                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>Ethernet Receive Data<br>—                 | I/O<br>I/O<br>I<br>— | V <sub>DDE3</sub> | SH                    | —                         | —                        | P15                   | P15     |
| PH5                   | PH[5]<br>eMIOS[26]<br>FEC_RXD[1]           | 117                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>Ethernet Receive Data<br>—                 | I/O<br>I/O<br>I<br>— | V <sub>DDE3</sub> | SH                    | —                         | —                        | R14                   | R14     |
| PH6                   | PH[6]<br>eMIOS[25]<br>FEC_RXD[2]           | 118                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>Ethernet Receive Data<br>—                 | I/O<br>I/O<br>I<br>— | V <sub>DDE3</sub> | SH                    | —                         | —                        | R15                   | R15     |

## Pin Assignments

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup> | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup>      | Description  | I/O Type             | Voltage           | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|----------------------------------|-----------------------------|----------------------|--|----------------------|-------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |                                  |                             |                      |  |                      |                   |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PH7                   | PH[7]<br>eMIOS[24]<br>FEC_RXD[3] | 119                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>Ethernet Receive Data<br>—         | I/O<br>I/O<br>I<br>— | V <sub>DDE3</sub> | SH                    | —                         | —                        | T15                   | T15     |
| PH8                   | PH[8]<br>eMIOS[23]               | 120                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>—<br>—                             | I/O<br>I/O<br>—<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | P7                    | P7      |
| PH9                   | PH[9]<br>eMIOS[22]               | 121                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>—<br>—                             | I/O<br>I/O<br>—<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | N8                    | N8      |
| PH10                  | PH[10]<br>eMIOS[21]              | 122                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>—<br>—                             | I/O<br>I/O<br>—<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | P8                    | P8      |
| PH11                  | PH[11]<br>eMIOS[20]              | 123                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>—<br>—                             | I/O<br>I/O<br>—<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | N9                    | N9      |
| PH12                  | PH[12]<br>eMIOS[19]              | 124                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>—<br>—                             | I/O<br>I/O<br>—<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | P9                    | P9      |
| PH13                  | PH[13]<br>eMIOS[18]              | 125                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>—<br>—                             | I/O<br>I/O<br>—<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | P10                   | P10     |
| PH14                  | PH[14]<br>eMIOS[17]              | 126                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>—<br>—                             | I/O<br>I/O<br>—<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | P11                   | P11     |
| PH15                  | PH[15]<br>eMIOS[16]              | 127                         | 00<br>01<br>10<br>11 | Port H GPIO<br>eMIOS Channel<br>—<br>—                             | I/O<br>I/O<br>—<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | N11                   | N11     |
| <b>Port J (16)</b>    |                                  |                             |                      |  |                      |                   |                       |                           |                          |                       |         |
| PJ0                   | PJ[0]<br>eMIOS[15]<br>PCS_A[4]   | 128                         | 00<br>01<br>10<br>11 | Port J GPIO<br>eMIOS Channel<br>DSPI_A Peripheral Chip Select<br>— | I/O<br>I/O<br>O<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | R7                    | R7      |

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup> | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup>      | Description  | I/O Type             | Voltage           | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|----------------------------------|-----------------------------|----------------------|--|----------------------|-------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |                                  |                             |                      |  |                      |                   |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PJ1                   | PJ[1]<br>eMIOS[14]<br>PCS_A[5]   | 129                         | 00<br>01<br>10<br>11 | Port J GPIO<br>eMIOS Channel<br>DSPI_A Peripheral Chip Select<br>— | I/O<br>I/O<br>O<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | T7                    | T7      |
| PJ2                   | PJ[2]<br>eMIOS[13]<br>PCS_B[1]   | 130                         | 00<br>01<br>10<br>11 | Port J GPIO<br>eMIOS Channel<br>DSPI_B Peripheral Chip Select<br>— | I/O<br>I/O<br>O<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | R8                    | R8      |
| PJ3                   | PJ[3]<br>eMIOS[12]<br>PCS_B[2]   | 131                         | 00<br>01<br>10<br>11 | Port J GPIO<br>eMIOS Channel<br>DSPI_B Peripheral Chip Select<br>— | I/O<br>I/O<br>O<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | T8                    | T8      |
| PJ4                   | PJ[4]<br>eMIOS[11]<br>PCS_C[3]   | 132                         | 00<br>01<br>10<br>11 | Port J GPIO<br>eMIOS Channel<br>DSPI_C Peripheral Chip Select<br>— | I/O<br>I/O<br>O<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | R9                    | R9      |
| PJ5                   | PJ[5]<br>eMIOS[10]<br>PCS_C[4]   | 133                         | 00<br>01<br>10<br>11 | Port J GPIO<br>eMIOS Channel<br>DSPI_C Peripheral Chip Select<br>— | I/O<br>I/O<br>O<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | T9                    | T9      |
| PJ6                   | PJ[6]<br>eMIOS[09]<br>PCS_D[5]   | 134                         | 00<br>01<br>10<br>11 | Port J GPIO<br>eMIOS Channel<br>DSPI_D Peripheral Chip Select<br>— | I/O<br>I/O<br>O<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | R10                   | R10     |
| PJ7                   | PJ[7]<br>eMIOS[08]<br>PCS_D[1]   | 135                         | 00<br>01<br>10<br>11 | Port J GPIO<br>eMIOS Channel<br>DSPI_D Peripheral Chip Select<br>— | I/O<br>I/O<br>O<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | T10                   | T10     |
| PJ8                   | PJ[8]<br>eMIOS[07]               | 136                         | 00<br>01<br>10<br>11 | Port J GPIO<br>eMIOS Channel<br>—<br>—                             | I/O<br>I/O<br>—<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | T11                   | T11     |
| PJ9                   | PJ[9]<br>eMIOS[06]               | 137                         | 00<br>01<br>10<br>11 | Port J GPIO<br>eMIOS Channel<br>—<br>—                             | I/O<br>I/O<br>—<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | R11                   | R11     |
| PJ10                  | PJ[10]<br>eMIOS[05]              | 138                         | 00<br>01<br>10<br>11 | Port J GPIO<br>eMIOS Channel<br>—<br>—                             | I/O<br>I/O<br>—<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | N12                   | N12     |
| PJ11                  | PJ[11]<br>eMIOS[04]              | 139                         | 00<br>01<br>10<br>11 | Port J GPIO<br>eMIOS Channel<br>—<br>—                             | I/O<br>I/O<br>—<br>— | V <sub>DDE4</sub> | SH                    | —                         | —                        | P12                   | P12     |

## Pin Assignments

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup> | Supported Functions <sup>2</sup>         | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup> | Description                   | I/O Type | Voltage             | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|-----------------------|--|-----------------------------|-----------------|-------------------------------|----------|---------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                       |  |                             |                 |                               |          |                     |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PJ12                  | PJ[12]<br>eMIOS[03]                      | 140                         | 00              | Port J GPIO                   | I/O      | V <sub>DDE4</sub>   | SH                    | —                         | —                        | R12                   | R12     |
|                       |  |                             | 01              | eMIOS Channel                 | I/O      |                     |                       |                           |                          |                       |         |
|                       |  |                             | 10              | —                             | —        |                     |                       |                           |                          |                       |         |
|                       |  |                             | 11              | —                             | —        |                     |                       |                           |                          |                       |         |
| PJ13                  | PJ[13]<br>eMIOS[02]                      | 141                         | 00              | Port J GPIO                   | I/O      | V <sub>DDE4</sub>   | SH                    | —                         | —                        | T12                   | T12     |
|                       |  |                             | 01              | eMIOS Channel                 | I/O      |                     |                       |                           |                          |                       |         |
|                       |  |                             | 10              | —                             | —        |                     |                       |                           |                          |                       |         |
|                       |  |                             | 11              | —                             | —        |                     |                       |                           |                          |                       |         |
| PJ14                  | PJ[14]<br>eMIOS[01]                      | 142                         | 00              | Port J GPIO                   | I/O      | V <sub>DDE4</sub>   | SH                    | —                         | —                        | R13                   | R13     |
|                       |  |                             | 01              | eMIOS Channel                 | I/O      |                     |                       |                           |                          |                       |         |
|                       |  |                             | 10              | —                             | —        |                     |                       |                           |                          |                       |         |
|                       |  |                             | 11              | —                             | —        |                     |                       |                           |                          |                       |         |
| PJ15                  | PJ[15]<br>eMIOS[00]                      | 143                         | 00              | Port J GPIO                   | I/O      | V <sub>DDE4</sub>   | SH                    | —                         | —                        | T13                   | T13     |
|                       |  |                             | 01              | eMIOS Channel                 | I/O      |                     |                       |                           |                          |                       |         |
|                       |  |                             | 10              | —                             | —        |                     |                       |                           |                          |                       |         |
|                       |  |                             | 11              | —                             | —        |                     |                       |                           |                          |                       |         |
| <b>Port K (11)</b>    |  |                             |                 |                               |          |                     |                       |                           |                          |                       |         |
| PK0                   | PK[0]<br>MLBCLK<br>SCK_B<br>CLKOUT       | 144                         | 00              | Port K GPIO                   | I/O      | V <sub>DDEMLB</sub> | F                     | —                         | —                        | L1                    | L1      |
|                       |  |                             | 01              | Media Local Bus Clock         | I        |                     |                       |                           |                          |                       |         |
|                       |  |                             | 10              | DSPI_B Serial Clock           | I/O      |                     |                       |                           |                          |                       |         |
|                       |  |                             | 11              | CLKOUT (Test Only)            | O        |                     |                       |                           |                          |                       |         |
| PK1                   | PK[1]<br>MLBSIG<br>SOUT_B<br>PCS_D[4]    | 145                         | 00              | Port K GPIO                   | I/O      | V <sub>DDEMLB</sub> | F                     | —                         | —                        | K1                    | K1      |
|                       |  |                             | 01              | Media Local Bus Signal        | I/O      |                     |                       |                           |                          |                       |         |
|                       |  |                             | 10              | DSPI_B Serial Data Out        | O        |                     |                       |                           |                          |                       |         |
|                       |  |                             | 11              | DSPI_D Peripheral Chip Select | O        |                     |                       |                           |                          |                       |         |
| PK2                   | PK[2]<br>MLBDAT<br>SIN_B<br>PCS_D[5]     | 146                         | 00              | Port K GPIO                   | I/O      | V <sub>DDEMLB</sub> | F                     | —                         | —                        | K2                    | K2      |
|                       |  |                             | 01              | Media Local Bus Data          | I/O      |                     |                       |                           |                          |                       |         |
|                       |  |                             | 10              | DSPI_B Serial Data In         | I        |                     |                       |                           |                          |                       |         |
|                       |  |                             | 11              | DSPI_D Peripheral Chip Select | O        |                     |                       |                           |                          |                       |         |
| PK3                   | PK[3]<br>FR_A_RX<br>MA[0]<br>PCS_C[1]    | 147                         | 00              | Port K GPIO                   | I/O      | V <sub>DDE2</sub>   | SH                    | —                         | —                        | T3                    | T3      |
|                       |  |                             | 01              | FlexRay A Receive Data        | I        |                     |                       |                           |                          |                       |         |
|                       |  |                             | 10              | ADC Ext. Mux Address Select   | O        |                     |                       |                           |                          |                       |         |
|                       |  |                             | 11              | DSPI_C Peripheral Chip Select | O        |                     |                       |                           |                          |                       |         |
| PK4                   | PK[4]<br>FR_A_TX<br>MA[1]<br>PCS_C[2]    | 148                         | 00              | Port K GPIO                   | I/O      | V <sub>DDE2</sub>   | MH                    | —                         | —                        | R4                    | R4      |
|                       |  |                             | 01              | FlexRay A Transmit Data       | O        |                     |                       |                           |                          |                       |         |
|                       |  |                             | 10              | ADC Ext. Mux Address Select   | O        |                     |                       |                           |                          |                       |         |
|                       |  |                             | 11              | DSPI_C Peripheral Chip Select | O        |                     |                       |                           |                          |                       |         |
| PK5                   | PK[5]<br>FR_A_TX_EN<br>MA[2]<br>PCS_C[3] | 149                         | 00              | Port K GPIO                   | I/O      | V <sub>DDE2</sub>   | MH                    | —                         | —                        | T4                    | T4      |
|                       |  |                             | 01              | FlexRay A Transmit Enable     | O        |                     |                       |                           |                          |                       |         |
|                       |  |                             | 10              | ADC Ext. Mux Address Select   | O        |                     |                       |                           |                          |                       |         |
|                       |  |                             | 11              | DSPI_C Peripheral Chip Select | O        |                     |                       |                           |                          |                       |         |

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup>     | Supported Functions <sup>2</sup>                   | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup>      | Description   | I/O Type                | Voltage             | Pad Type <sup>5</sup> | Status                    |                          | Package Pin Locations |         |
|---------------------------|--|-----------------------------|----------------------|---|-------------------------|---------------------|-----------------------|---------------------------|--------------------------|-----------------------|---------|
|                           |  |                             |                      |   |                         |                     |                       | During Reset <sup>6</sup> | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| PK6                       | PK[6]<br>FR_B_RX<br>PCS_B[1]<br>PCS_C[4]           | 150                         | 00<br>01<br>10<br>11 | Port K GPIO<br>FlexRay B Receive Data<br>DSPI_B Peripheral Chip Select<br>DSPI_C Peripheral Chip Select                   | I/O<br>I<br>O<br>O      | V <sub>DDE2</sub>   | SH                    | —                         | —                        | R5                    | R5      |
| PK7                       | PK[7]<br>FR_B_TX<br>PCS_B[2]<br>PCS_C[5]           | 151                         | 00<br>01<br>10<br>11 | Port K GPIO<br>FlexRay B Transmit Data<br>DSPI_B Peripheral Chip Select<br>DSPI_C Peripheral Chip Select                  | I/O<br>O<br>O<br>O      | V <sub>DDE2</sub>   | MH                    | —                         | —                        | T5                    | T5      |
| PK8                       | PK[8]<br>FR_B_TX_EN<br>PCS_B[3]<br>PCS_A[1]        | 152                         | 00<br>01<br>10<br>11 | Port K GPIO<br>FlexRay B Transmit Enable<br>DSPI_B Peripheral Chip Select<br>DSPI_A Peripheral Chip Select                | I/O<br>O<br>O<br>O      | V <sub>DDE2</sub>   | MH                    | —                         | —                        | R6                    | R6      |
| PK9                       | PK[9]<br>CLKOUT<br>PCS_D[1]<br>PCS_A[2]<br>BOOTCFG | 153                         | 00<br>01<br>10<br>11 | Port K GPIO<br>CLKOUT (User mode)<br>DSPI_D Peripheral Chip Select<br>DSPI_A Peripheral Chip Select<br>Boot Configuration | I/O<br>O<br>O<br>O<br>I | V <sub>DDE2</sub>   | MH                    | BOOT CFG<br>(Pull-down)   | GPIO                     | T6                    | T6      |
| PK10                      | PK[10]<br>PCS_B[5]<br>PCS_D[2]<br>PCS_A[3]         | 154                         | 00<br>01<br>10<br>11 | Port K GPIO<br>DSPI_B Peripheral Chip Select<br>DSPI_D Peripheral Chip Select<br>DSPI_A Peripheral Chip Select            | I/O<br>O<br>O<br>O      | V <sub>DDE2</sub>   | SH                    | —                         | —                        | P6                    | P6      |
| <b>Nexus Pins (17)</b>    |  |                             |                      |   |                         |                     |                       |                           |                          |                       |         |
| $\overline{\text{EVTI}}$  | $\overline{\text{EVTI}}$                           | —                           | —                    | Nexus Event In  | I                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | M11     |
| $\overline{\text{EVTO}}$  | $\overline{\text{EVTO}}$                           | —                           | —                    | Nexus Event Out   | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | M12     |
| $\overline{\text{MSEO0}}$ | $\overline{\text{MSEO}}[0]$                        | —                           | —                    | Nexus Message Start/End Out   | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | M9      |
| $\overline{\text{MSEO1}}$ | $\overline{\text{MSEO}}[1]$                        | —                           | —                    | Nexus Message Start/End Out   | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | M8      |
| MCKO                      | MCKO   | —                           | —                    | Nexus Message Clock Out   | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | M10     |
| MDO0                      | MDO[0]   | —                           | —                    | Nexus Message Data Out  | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | E5      |
| MDO1                      | MDO[1]   | —                           | —                    | Nexus Message Data Out  | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | F5      |
| MDO2                      | MDO[2]   | —                           | —                    | Nexus Message Data Out  | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | G5      |
| MDO3                      | MDO[3]   | —                           | —                    | Nexus Message Data Out  | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | H5      |
| MDO4                      | MDO[4]   | —                           | —                    | Nexus Message Data Out  | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | H6      |
| MDO5                      | MDO[5]   | —                           | —                    | Nexus Message Data Out  | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | J6      |
| MDO6                      | MDO[6]   | —                           | —                    | Nexus Message Data Out  | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | J5      |
| MDO7                      | MDO[7]   | —                           | —                    | Nexus Message Data Out  | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | K5      |
| MDO8                      | MDO[8]   | —                           | —                    | Nexus Message Data Out  | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | L5      |
| MDO9                      | MDO[9]   | —                           | —                    | Nexus Message Data Out  | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | M5      |
| MDO10                     | MDO[10]  | —                           | —                    | Nexus Message Data Out  | O                       | V <sub>DDENEX</sub> | F                     | —                         | —                        | —                     | M6      |

## Pin Assignments

Table 2. MPC5668x Signal Properties (continued)

| Pin Name <sup>1</sup>         | Supported Functions <sup>2</sup> | GPIO (PCR) Num <sup>3</sup> | PA <sup>4</sup> | Description   | I/O Type | Voltage             | Pad Type <sup>5</sup> | Status                              |                          | Package Pin Locations |         |
|-------------------------------|----------------------------------|-----------------------------|-----------------|---|----------|---------------------|-----------------------|-------------------------------------|--------------------------|-----------------------|---------|
|                               |                                  |                             |                 |   |          |                     |                       | During Reset <sup>6</sup>           | After Reset <sup>7</sup> | 208 BGA               | 256 BGA |
| MDO11                         | MDO[11]                          | —                           | —               | Nexus Message Data Out                                | O        | V <sub>DDENEX</sub> | F                     | —                                   | —                        | —                     | M7      |
| <b>Miscellaneous Pins (9)</b> |                                  |                             |                 |   |          |                     |                       |                                     |                          |                       |         |
| EXTAL                         | EXTAL<br>EXTCLK                  | —                           | —               | Main Crystal Oscillator Input<br>External Clock Input | I<br>I   | V <sub>DDSYN</sub>  | A                     | EXTAL                               |                          | A14                   | A14     |
| XTAL                          | XTAL                             | —                           | —               | Main Crystal Oscillator Output                        | O        | V <sub>DDSYN</sub>  | A                     | XTAL                                |                          | A13                   | A13     |
| TDI                           | TDI                              | —                           | —               | JTAG Test Data Input                                  | I        | V <sub>DDE2</sub>   | SH                    | TDI (Pull Up)                       |                          | J3                    | J3      |
| TDO                           | TDO                              | —                           | —               | JTAG Test Data Output                                 | O        | V <sub>DDE2</sub>   | MH                    | TDO (Pull Up <sup>8</sup> )         |                          | M3                    | M3      |
| TMS                           | TMS                              | —                           | —               | JTAG Test Mode Select Input                           | I        | V <sub>DDE2</sub>   | MH                    | TMS (Pull Up)                       |                          | L3                    | L3      |
| TCK                           | TCK                              | —                           | —               | JTAG Test Clock Input                                 | I        | V <sub>DDE2</sub>   | SH                    | TCK (Pull Down)                     |                          | P3                    | P3      |
| JCOMP                         | JCOMP                            | —                           | —               | JTAG Compliancy                                       | I        | V <sub>DDE2</sub>   | SH                    | JCOMP (Pull Down)                   |                          | K3                    | K3      |
| TEST                          | TEST                             | —                           | —               | Test Mode Select                                      | I        | V <sub>DDE3</sub>   | IH                    | TEST <sup>9</sup>                   |                          | M13                   | M13     |
| $\overline{\text{RESET}}$     | $\overline{\text{RESET}}$        | —                           | —               | External Reset  | I/O      | V <sub>DDE1</sub>   | MH                    | $\overline{\text{RESET}}$ (Pull Up) |                          | A11                   | A11     |

<sup>1</sup> The primary signal name is used as the pin label on the BGA map for identification purposes.

<sup>2</sup> Each line in the Signal Name column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, or GPIO signal functions are designated in the PA field of the System Integration Unit (SIU) PCR registers except where explicitly noted.

<sup>3</sup> The GPIO number is the same as the corresponding pad configuration register (SIU\_PCR $n$ ) number.

<sup>4</sup> The PA bitfield in the SIU\_PCR $n$  register selects the signal function for the pin. A dash in the Description field of this table indicates that this value for PC is reserved on this pin, and should not be used.

<sup>5</sup> The pad type is indicated by one or more of the following abbreviations: A—analogue, F—fast speed, H—high voltage, I—input-only, M—medium speed, S—slow speed. For example, pad type SH designates a slow high-voltage pad.

<sup>6</sup> The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. The terminology used in this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

<sup>7</sup> The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

<sup>8</sup> Pullup is enabled only when JCOMP is negated.

<sup>9</sup> Tie to V<sub>SS</sub> for normal operation.



### 3.3.1 Power and Ground Supply Summary

Table 3. MPC5668x Power/Ground

| Pin Name                         | Function Description              | Voltage <sup>1</sup>                | Package Pin Locations   |  |
|----------------------------------|-----------------------------------|-------------------------------------|---|--|
|                                  |                                   |                                     | 208   | 256  |
| V <sub>DD</sub>                  | Internal Logic Power              | 1.2 V                               | D4, D10, H4, G13, K13, N5   | D4, D10, H4, G13, K13, N5  |
| V <sub>DDE1</sub>                | External I/O Power                | 3.3–5.0 V                           | D6  | D6   |
| V <sub>DDE2</sub>                |                                   |                                     | L4  | L4   |
| V <sub>DDE3</sub>                |                                   |                                     | J13   | J13  |
| V <sub>DDE4</sub>                |                                   |                                     | N10   | N10  |
| V <sub>DDA</sub>                 | Analog Power                      | 3.3–5.0 V                           | B15   | B15  |
| V <sub>DD33</sub>                | 3.3 V I/O Power                   | 3.3 V                               | L13   | L13  |
| V <sub>DDEMLB</sub>              | Media Local Bus Power             | 2.5 or 3.3 V                        | K4  | K4   |
| V <sub>DDENEX</sub> <sup>2</sup> | Nexus Power                       | 3.3 V                               | —   | E6, K11, L7  |
| V <sub>RCSEL</sub>               | Voltage Regulator Select          | V <sub>SSA</sub> / V <sub>DDA</sub> | H13   | H13  |
| V <sub>RC</sub>                  | Voltage Regulator Control Voltage | 3.3–5.0 V                           | B10   | B10  |
| V <sub>RCCTL</sub>               | Voltage Regulator Control Output  | — <sup>3</sup>                      | B11   | B11  |
| V <sub>DDSYN</sub>               | Clock Synthesizer Power           | 3.3 V                               | A12   | A12  |
| V <sub>RH</sub>                  | Analog High Voltage Reference     | 3.3–5.0 V                           | B16   | B16  |
| V <sub>RL</sub>                  | Analog Low Voltage Reference      | 0 V                                 | C16   | C16  |
| V <sub>SS</sub>                  | Ground                            | 0 V                                 | A1, A16, D7, G4, G[7:10], H[7:10], J[7:10], K[7:10], N13, T1, T16 | A1, A16, D7, E[7:12], F[7:12], G4, G[6:12], H[7:12], J[7:12], K[6:10], K12, L[8:10], L12, N13, T1, T16 |
| V <sub>SSA</sub>                 | Analog Ground                     | 0 V                                 | C15   | C15  |
| V <sub>SSSYN</sub>               | Clock Synthesizer Ground          | 0 V                                 | A15   | A15  |

<sup>1</sup> Nominal voltages.

<sup>2</sup> Dedicated Nexus power pin on 256-pin package only. On the 208-pin package, VDDENEX is tied to VSS internal to the package substrate and is not available externally.

<sup>3</sup> Base current to external NPN power transistor. Voltage may vary.

## 4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5668x.

### NOTE

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon the finalized specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

### 4.1 Maximum Ratings

Table 4. Absolute Maximum Ratings<sup>1</sup>

| Spec | Characteristic  | Symbol   | Min                                    | Max <sup>2</sup>                             | Unit |
|------|---|--|--|--|------|
| 1    | 1.2 V Core Supply Voltage   | $V_{DD}$   | -0.3                                   | 1.32 <sup>3</sup>                            | V    |
| 2    | 3.3 V Clock Synthesizer Voltage   | $V_{DDSYN}$  | -0.3                                   | 3.6  | V    |
| 3    | 3.3 V I/O Buffer Voltage  | $V_{DD33}$   | -0.3                                   | 3.6  | V    |
| 4    | 3.3–5.0 V Voltage Regulator Control Voltage   | $V_{RC}$   | -0.3                                   | 5.5  | V    |
| 5    | 3.3–5.0 V Analog Supply Voltage (reference to $V_{SSA}$ )   | $V_{DDA}$  | -0.3                                   | 5.5  | V    |
| 6    | 3.3–5.0 V External I/O Supply Voltage <sup>4</sup>  | $V_{DDE1}^5$<br>$V_{DDE2}^5$<br>$V_{DDE3}^5$<br>$V_{DDE4}^5$ | -0.3<br>-0.3<br>-0.3<br>-0.3           | 5.5<br>5.5<br>5.5<br>5.5                     | V    |
| 7    | 2.5–3.3 V External I/O Supply Voltage (MLB)   | $V_{DDEMLB}^5$   | -0.3                                   | 3.6  | V    |
| 8    | 3.3 V External I/O Supply Voltage (Nexus)   | $V_{DDENEX}^5$   | -0.3                                   | 3.6  | V    |
| 9    | DC Input Voltage <sup>6</sup><br>$V_{DDE1}$ , $V_{DDE2}$ , $V_{DDE3}$ , $V_{DDE4}$<br>$V_{DDEMLB}$ , $V_{DDENEX}$ | $V_{IN}$   | -1.0 <sup>7</sup><br>-1.0 <sup>6</sup> | $V_{DDEx} + 0.3 V^8$<br>$V_{DDEx} + 0.3 V^7$ | V    |
| 10   | Analog Reference High Voltage   | $V_{RH}$   | -0.3                                   | Minimum of<br>5.5<br>or<br>$V_{DDA} + 0.3$   | V    |
| 11   | Analog Reference Low Voltage  | $V_{RL}$   | -0.3                                   | 5.5  | V    |
| 12   | $V_{SS}$ to $V_{SSA}$ Differential Voltage  | $V_{SS} - V_{SSA}$   | -100                                   | 100  | mV   |
| 13   | $V_{SS}$ to $V_{SSSYN}$ Differential Voltage  | $V_{SS} - V_{SSSYN}$   | -100                                   | 100  | mV   |
| 14   | Maximum DC Digital Input Current <sup>9</sup> (per pin, applies to all digital F, MH, SH, and IH pins)            | $I_{MAXD}$   | -2                                     | 2  | mA   |
| 15   | Maximum DC Analog Input Current <sup>10</sup> (per pin, applies to all analog AE and A pins)                      | $I_{MAXA}$   | -3                                     | 3  | mA   |
| 16   | Storage Temperature Range   | $T_{STG}$  | -55.0                                  | 150.0  | °C   |
| 17   | Maximum Solder Temperature <sup>11</sup>  | $T_{SDR}$  | —                                      | 235.0  | °C   |
| 18   | Moisture Sensitivity Level <sup>12</sup>  | MSL  | —                                      | 3  |      |

- <sup>1</sup> Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
- <sup>2</sup> Absolute maximum specifications for device stress have not yet been determined.
- <sup>3</sup> 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.
- <sup>4</sup> All functional non-supply I/O pins are clamped to  $V_{SS}$  and  $V_{DDEx}$ .
- <sup>5</sup>  $V_{DDEx}$  are separate power segments and may be powered independently with no differential voltage constraints between the power segments.
- <sup>6</sup> AC signal over and undershoot of the input voltages of up to  $\pm 2.0$  V is permitted for a cumulative duration of 60 hours over the complete lifetime of the device (injection current does not need to be limited for this duration).
- <sup>7</sup> Internal structures will hold the input voltage above  $-1.0$  V if the injection current limit of 2 mA is met.
- <sup>8</sup> Internal structures hold the input voltage below this maximum voltage on all pads powered by  $V_{DDE}$  supplies, if the maximum injection current specification is met (25 mA for all pins) and  $V_{DDE}$  is within Operating Voltage specifications.
- <sup>9</sup> Total injection current for all pins (including both digital and analog) must not exceed 25 mA.
- <sup>10</sup> Total injection current for all analog input pins must not exceed 15 mA.
- <sup>11</sup> Solder profile per CDF-AEC-Q100.
- <sup>12</sup> Moisture sensitivity per JEDEC test method A112.

## 4.2 Thermal Characteristics

Table 5. Thermal Characteristics

| Spec | Characteristic   | Symbol           | Unit                        | Value      |            |
|------|--|------------------|-----------------------------|------------|------------|
|      |  |                  |                             | 208 MAPBGA | 256 MAPBGA |
| 1    | Junction to Ambient <sup>1, 2</sup><br>Natural Convection<br>(Single layer board)    | $R_{\theta JA}$  | $^{\circ}\text{C}/\text{W}$ | 39         | 39         |
| 2    | Junction to Ambient <sup>1, 3</sup><br>Natural Convection<br>(Four layer board 2s2p) | $R_{\theta JA}$  | $^{\circ}\text{C}/\text{W}$ | 24         | 24         |
| 3    | Junction to Ambient <sup>1, 3</sup><br>(@200 ft./min., Single layer board)           | $R_{\theta JMA}$ | $^{\circ}\text{C}/\text{W}$ | 31         | 31         |
| 4    | Junction to Ambient <sup>1, 3</sup><br>(@200 ft./min., Four layer board 2s2p)        | $R_{\theta JMA}$ | $^{\circ}\text{C}/\text{W}$ | 20         | 20         |
| 5    | Junction to Board <sup>4</sup>   | $R_{\theta JB}$  | $^{\circ}\text{C}/\text{W}$ | 13         | 13         |
| 6    | Junction to Case <sup>5</sup>  | $R_{\theta JC}$  | $^{\circ}\text{C}/\text{W}$ | 6          | 6          |
| 7    | Junction to Package Top <sup>6</sup><br>Natural Convection                           | $\Psi_{JT}$      | $^{\circ}\text{C}/\text{W}$ | 2          | 2          |

- <sup>1</sup> Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- <sup>2</sup> Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
- <sup>3</sup> Per JEDEC JESD51-6 with the board horizontal.
- <sup>4</sup> Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- <sup>5</sup> Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
- <sup>6</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

## Electrical Characteristics

## 4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature,  $T_J$ , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \text{Eqn. 1}$$

where:

$T_A$  = ambient temperature for the package ( $^{\circ}\text{C}$ )

$R_{\theta JA}$  = junction to ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$P_D$  = power dissipation in the package (W)

The supplied thermal resistances are provided based on JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined on the single-layer (1s) board and on the four-layer board with two signal layers and a power and a ground plane (2s2p) clearly demonstrate that the effective thermal resistance of the component is not a constant. It depends on the construction of the application board (number of planes), the effective size of the board which cools the component, how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz. (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than  $0.02 \text{ W}/\text{cm}^2$ .

The thermal performance of any component depends strongly on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \quad \text{Eqn. 2}$$

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where:

$T_J$  = junction temperature ( $^{\circ}\text{C}$ )

$T_B$  = board temperature at the package perimeter ( $^{\circ}\text{C}/\text{W}$ )

$R_{\theta JB}$  = junction to board thermal resistance ( $^{\circ}\text{C}/\text{W}$ ) per JESD51-8

$P_D$  = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition, with the component soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 3}$$

where:

$R_{\theta JA}$  = junction to ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$R_{\theta JC}$  = junction to case thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$R_{\theta CA}$  = case to ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$R_{\theta JC}$  is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance,  $R_{\theta CA}$ . For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter ( $\Psi_{JT}$ ) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 4}$$

where:

$T_T$  = thermocouple temperature on top of the package ( $^{\circ}\text{C}$ )

$\Psi_{JT}$  = thermal characterization parameter ( $^{\circ}\text{C}/\text{W}$ )

$P_D$  = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## References:

Semiconductor Equipment and Materials International  
3081 Zanker Road  
San Jose, CA 95134  
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at <http://www.jedec.org>.

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, "Thermal Modeling of a PBGA for Air-Cooled Applications," Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

## Electrical Characteristics

### 4.3 ESD Characteristics

Table 6. ESD Ratings<sup>1, 2</sup>

| Characteristic                            | Symbol | Value                | Unit   |
|---|--------|----------------------|--------|
| ESD for Human Body Model (HBM)            |        | 2000                 | V      |
| HBM Circuit Description                   | R1     | 1500                 | Ohm    |
|   | C      | 100                  | pF     |
| ESD for Field Induced Charge Model (FDCM) |        | 750 (corner pins)    | V      |
|   |        | 500 (all other pins) |        |
| Number of Pulses per pin:                 |        |                      |        |
| Positive Pulses (HBM)                     | —      | 1                    | —      |
| Negative Pulses (HBM)                     | —      | 1                    | —      |
| Interval of Pulses                        | —      | 1                    | second |

<sup>1</sup> All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

<sup>2</sup> A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

### 4.4 VRC Electrical Specifications

Table 7. VRC Electrical Specifications

| Spec | Characteristic  | Symbol          | Min            | Max   | Units |
|------|---|-----------------|----------------|-------|-------|
| 1    | Current which can be sourced by $V_{RCCTL}$   | $I_{V_{RCCTL}}$ | 6.25 $\mu$ A   | 20 mA | —     |
| 2    | Minimum Required Gain from external circuit:<br>$I_{DD} / I_{V_{RCCTL}} (@V_{DD} = 1.32 \text{ V})^1$<br>-40°C<br>25°C<br>150°C | BETA            | 50<br>50<br>50 | 500   |       |

<sup>1</sup> Assumes "typical usage" currents which will vary with application.

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### 4.5 DC Electrical Specifications

Table 8. DC Electrical Specifications

| Spec | Characteristic   | Symbol      | Min                                       | Max                 | Unit |
|------|--|-------------|---|---------------------|------|
| 1    | Maximum Operating Temperature Range — Die Junction Temperature   | $T_J$       | -40.0                                     | 150.0               | °C   |
| 2    | 3.3 V Clock Synthesizer Voltage <sup>1</sup>   | $V_{DDSYN}$ | 3.0                                       | 3.6 <sup>2, 3</sup> | V    |
| 3    | 3.3 V I/O Buffer Voltage <sup>1</sup>  | $V_{DD33}$  | 3.0                                       | 3.6 <sup>2, 3</sup> | V    |
| 4    | 3.3–5.0 V Voltage Regulator Reference Voltage <sup>1</sup><br>$V_{RCSEL} = V_{SSA}$<br>$V_{RCSEL} = V_{DDA}$ | $V_{VRC}$   | 3.0<br>4.5                                | 3.6<br>5.5          | V    |
| 5    | 3.3–5.0 V Analog Supply Voltage  | $V_{DDA}$   | maximum of<br>3.0 V or<br>$V_{VRC} - 0.1$ | 5.5 <sup>2, 4</sup> | V    |

Table 8. DC Electrical Specifications

| Spec | Characteristic  | Symbol   | Min   | Max  | Unit    |
|------|---|--|---|--|---------|
| 6    | 3.3–5.0 V External I/O Supply Voltage <sup>5</sup>  | $V_{DDE1}$<br>$V_{DDE2}$<br>$V_{DDE3}$<br>$V_{DDE4}$ | 3.0<br>3.0<br>3.0<br>3.0  | 5.5 <sup>2, 5</sup><br>5.5 <sup>2, 5</sup><br>5.5 <sup>2, 5</sup><br>5.5 <sup>2, 5</sup> | V       |
| 7    | 2.5 V – 3.3 V External I/O Supply Voltage (MLB)   | $V_{DDEMLB}$ <sup>2</sup>                            | 2.375   | 3.6 <sup>1, 2</sup>  | V       |
| 8    | 3.3 V External I/O Supply Voltage (Nexus)   | $V_{DDENEX}$ <sup>2</sup>                            | 3.0   | 3.6 <sup>1, 2</sup>  | V       |
| 9    | Pad Input High Voltage<br>Hysteresis enabled<br>Hysteresis disabled (IHA/SH/SHA/MH/MHA) <sup>6, 7</sup><br>Hysteresis disabled (F)                | $V_{IH}$   | $0.65 \times V_{DDE}$<br>$0.55 \times V_{DDE}$<br>$0.55 \times V_{DDE}$ | $V_{DDE} + 0.3$  | V       |
| 10   | Pad Input Low Voltage<br>Hysteresis enabled<br>Hysteresis disabled (IHA/SH/SHA/MH/MHA) <sup>6, 7</sup><br>Hysteresis disabled (F)                 | $V_{IL}$   | $V_{SS} - 0.3$  | $0.35 \times V_{DDE}$<br>$0.40 \times V_{DDE}$<br>$0.40 \times V_{DDE}$                  | V       |
| 11   | Pad Input Hysteresis  | $V_{HYS}$  | $0.1 \times V_{DDE}$  |  | V       |
| 12   | Analog (IHA) Input Voltage  | $V_{INDC}$   | $V_{SSA} - 0.3$   | $V_{DDA} + 0.3$  | V       |
| 13   | Pad Output High Voltage <sup>8, 9, 10</sup>   | $V_{OH}$   | $0.8 \times V_{DDE}$  | —  | V       |
| 14   | Pad Output Low Voltage <sup>1, 10</sup>   | $V_{OL}$   | —   | $0.2 \times V_{DDE}$   | V       |
| 15   | Input Capacitance (Digital Pins: Pad type F, MH, SH) <sup>6</sup>   | $C_{IN}$   | —   | 7  | pF      |
| 16   | Input Capacitance (Analog Pins: Pad type IHA) <sup>6, 7</sup>   | $C_{IN\_A}$  | —   | 10   | pF      |
| 17   | Input Capacitance (Shared digital/analog pins: MHA, SHA) <sup>6</sup>   | $C_{IN\_M}$  | —   | 12   | pF      |
| 18   | I/O Weak Pull Up/Down Absolute Current <sup>6, 11</sup><br>Pad F: 2.375 V – 3.6 V<br>Pad SH/MH/IHA: 3.0 V – 3.6 V<br>Pad SH/MH/IHA: 4.5 V – 5.5 V | $I_{ACT}$  | 25<br>10<br>35  | 180<br>95<br>200   | $\mu$ A |
| 19   | I/O Input Leakage Current <sup>12</sup>   | $I_{INACT\_D}$                                       | –2.5  | 2.5  | $\mu$ A |
| 20   | DC Injection Current (per pin)  | $I_{IC}$   | –1.0  | 1.0  | mA      |
| 21   | Analog Input Current, Channel Off <sup>13</sup> (Analog pins IHA) <sup>6, 7</sup>   | $I_{INACT\_A}$                                       | –150  | 150  | nA      |
| 22   | Analog Reference High Voltage   | $V_{RH}$   | $V_{DDA} - 500$   | $V_{DDA}$  | mV      |
| 23   | Analog Reference Low Voltage  | $V_{RL}$   | $V_{SSA}$   | $V_{SSA} + 500$  | mV      |
| 24   | $V_{SS}$ to $V_{SSA}$ Differential Voltage  | $V_{SS} - V_{SSA}$                                   | –100  | 100  | mV      |
| 25   | $V_{SSSYN}$ to $V_{SS}$ Differential Voltage  | $V_{SSSYN} - V_{SS}$                                 | –100  | 100  | mV      |
| 26   | Slew rate on $V_{DDA}$ , $V_{DDEx}$ , and $V_{DDR}$ power supply pins   | $V_{Ramp}$   | —   | 100  | V/ms    |
| 27   | Capacitive Supply Load ( $V_{DD}$ )   | $V_{Load}$   | 8   | —  | $\mu$ F |
| 28   | Capacitive Supply Load ( $V_{DD33}$ , $V_{DDSYN}$ )   | $V_{Load}$   | 1   | —  | $\mu$ F |

<sup>1</sup> When  $V_{RCSEL} = V_{SSA}$  (low),  $V_{DDSYN}$  and  $V_{DD33}$  are externally supplied. When  $V_{RCSEL} = V_{DDA}$  (high),  $V_{DDSYN}$  and  $V_{DD33}$  are generated by internal voltage regulators. When  $V_{RCSEL} = V_{SSA}$  (low),  $V_{DDSYN}$  and  $V_{DD33}$  cannot be 100 mV higher than  $V_{RC}$ .

## Electrical Characteristics

- <sup>2</sup> Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
- <sup>3</sup> 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.
- <sup>4</sup> 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.
- <sup>5</sup>  $V_{DDE1} - V_{DDE4}$  are separate power segments and may be powered independently with no differential voltage constraints between the power segments.  $V_{DDE1} - V_{DDE3}$  pad power segments contain ADC analog input channels and thus the input analog signal level may be clamped to the  $V_{DDE}$  level, resulting in inaccurate ADC results if the  $V_{DDE}$  voltage level is less than  $V_{DDA}$ .
- <sup>6</sup> The pad type is indicated by one or more of the following abbreviations: A—analogue, F—fast speed, H—high voltage, I—input-only, M—medium speed, S—slow speed. For example, pad type SH designates a slow high-voltage pad.
- <sup>7</sup> The IHA pads are related to  $V_{DDA}$ .
- <sup>8</sup> Characterization Based Capability:  
 $I_{OH\_F} = \{12, 20, 30, 40\}$  mA and  $I_{OL\_F} = \{24, 40, 50, 65\}$  mA for  $\{00, 01, 10, 11\}$  drive mode with  $V_{DDE} = 3.0$  V;  
 $I_{OH\_F} = \{7, 13, 18, 25\}$  mA and  $I_{OL\_F} = \{18, 30, 35, 50\}$  mA for  $\{00, 01, 10, 11\}$  drive mode with  $V_{DDE} = 2.25$  V;  
 $I_{OH\_F} = \{3, 7, 10, 15\}$  mA and  $I_{OL\_F} = \{12, 20, 27, 35\}$  mA for  $\{00, 01, 10, 11\}$  drive mode with  $V_{DDE} = 1.62$  V.
- <sup>9</sup> Characterization Based Capability:  
 $I_{OH\_S} = \{6, 11.6\}$  mA and  $I_{OL\_S} = \{9.2, 17.7\}$  mA for  $\{slow, medium\}$  I/O with  $V_{DDEH} = 4.5$  V;  
 $I_{OH\_S} = \{2.8, 5.4\}$  mA and  $I_{OL\_S} = \{4.2, 8.1\}$  mA for  $\{slow, medium\}$  I/O with  $V_{DDEH} = 3.0$  V
- <sup>10</sup> All  $V_{OL}/V_{OH}$  values 100% tested with  $\pm 2$  mA load.
- <sup>11</sup> Absolute value of current, measured at  $V_{IL}$  and  $V_{IH}$ .
- <sup>12</sup> Weak pull up/down inactive. Measured at  $V_{DDE} = 5.25$  V. Applies to pad types: pad\_sh, and pad\_mh.
- <sup>13</sup> Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to pad types: pad\_a and pad\_ae.

## 4.6 Operating Current Specifications

Table 9. Operating Currents

| Spec      | Characteristic  | Symbol     | Typ <sup>1</sup><br>25 °C<br>Ambient | Max <sup>1</sup><br>-40–150 °C<br>Junction | Unit                     |
|-----------|---|------------|--------------------------------------|--|--------------------------|
| Equations | $I_{TOTAL} = I_{DDE} + I_{DDA} + I_{RH} + I_{DD33} + I_{DDSYN} + I_{RC} + I_{DD}$<br>$I_{DDE} = I_{DDE1} + I_{DDE2} + I_{DDE3} + I_{DDE4} + I_{DDEMLB}$ | —          | —                                    | —  | —                        |
| 1         | $V_{DDE}$ Current<br>$V_{DDE(1,2,3,4)}$ @ 3.0 V – 5.5 V<br>$V_{DDEMLB}$ @ 2.375 V – 3.6 V<br>Static <sup>2</sup><br>Dynamic <sup>3</sup>                | $I_{DDE}$  | 0<br>Note 3                          | 30<br>25                                   | $\mu$ A<br>mA            |
| 2         | $V_{DDA}$ Current<br>$V_{DDA}$ @ 3.0 V – 5.5 V<br>Run mode<br>Sleep mode<br>– Optional 32 kHz osc enabled   | $I_{DDA}$  | 1<br>20<br>+5                        | 30<br>50<br>+15                            | mA<br>$\mu$ A<br>$\mu$ A |
| 3         | $V_{RH}$ Current<br>$V_{RH}$ @ 3.0 V – 5.5 V<br>Run mode<br>Sleep mode  | $I_{RH}$   | 300<br>1                             | 700<br>30                                  | $\mu$ A<br>$\mu$ A       |
| 4         | $V_{DD33}$ Current<br>$V_{DD33}$ @ 3.0 V – 3.6 V<br>Run mode<br>Sleep mode  | $I_{DD33}$ | 10<br>10                             | 20<br>20                                   | mA<br>$\mu$ A            |



Table 9. Operating Currents (continued)

| Spec | Characteristic   | Symbol             | Typ <sup>1</sup><br>25 °C<br>Ambient                              | Max <sup>1</sup><br>–40–150 °C<br>Junction                       | Unit   |
|------|--|--------------------|---|--|--|
| 5    | V <sub>DDSYN</sub> Current<br>V <sub>DD33</sub> @ 3.0 V – 3.6 V<br>Run mode<br>Sleep mode<br>– Optional <sup>4</sup> 4–40 MHz osc enabled w/ no clock<br>– Optional <sup>4</sup> 4–40 MHz osc enabled w/ clock   | I <sub>DDSYN</sub> | 5<br>1<br>+150<br>+300  | 10<br>20<br>+350<br>+400   | mA<br>μA<br>μA<br>μA                                     |
| 6    | V <sub>RC</sub> Current<br>V <sub>RC</sub> @ 3.135 V – 5.5 V<br>Run mode<br>Sleep mode<br>– Optional <sup>4</sup> 16MIRC enabled   | I <sub>RC</sub>    | 1<br>0<br>+40   | 10<br>10<br>+60  | mA<br>μA<br>μA   |
| 7    | V <sub>DD</sub> Current<br>V <sub>DD</sub> @ 1.08 V – 1.32 V<br>Run mode (Maximum @ 116 MHz)<br>Sleep mode<br>– Optional <sup>4</sup> 128KIRC enabled<br>– Optional <sup>4</sup> 16MIRC enabled<br>– Optional <sup>4</sup> 32 kHz osc enabled<br>– Optional <sup>4</sup> 4–40 MHz osc enabled w/ no clock<br>– Optional <sup>4</sup> 4–40 MHz osc enabled w/ clock<br>– Optional <sup>4</sup> 32 KB RAM<br>– Optional <sup>4</sup> 64 KB RAM<br>– Optional <sup>4</sup> 128 KB RAM | I <sub>DD</sub>    | 200<br>100<br>+5<br>+200<br>+5<br>+5<br>+150<br>+10<br>+20<br>+40 | 340<br>900<br>+10<br>+220<br>+20<br>+200<br>+150<br>+300<br>+600 | mA<br>μA<br>μA<br>μA<br>μA<br>μA<br>μA<br>μA<br>μA<br>μA |

- <sup>1</sup> Typ – Nominal voltage levels and functional activity. Max – Maximum voltage levels and functional activity.
- <sup>2</sup> Static state of pins is when input pins are disabled or not being toggled and driven to a valid input level, output pins are not toggling or driving against any current loads, and internal pull devices are disabled or not pulling against any current loads.
- <sup>3</sup> Dynamic current from pins is application-specific and depends on active pull devices, switching outputs, output capacitive and current loads, and switching inputs. Refer to Table 10 for more information.
- <sup>4</sup> Optional currents are values that should be added to their respective current specifications to obtain the actual value for that specification when the optional function is active. The plus sign (+) in the Typ and Max columns indicates these optional currents. For example, V<sub>DDSYN</sub> in Sleep mode draws 1 μA (typ). With the optional 4–40 MHz osc enabled w/ no clock, add 150 μA for a total of 151 μA (typ).

## Electrical Characteristics

## 4.7 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from [Table 10](#) based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in [Table 10](#).

**Table 10. I/O Pad Average  $I_{DDE}$  Specifications<sup>1</sup>**

| Spec | Pad Type <sup>2</sup> | Symbol             | Period (ns) | Load <sup>3</sup> (pF) | $V_{DDE}$ (V) | Drive/Slew Rate Select | $I_{DDE}$ Avg (mA) | $I_{DDE}$ RMS (mA) |
|------|-----------------------|--------------------|-------------|------------------------|---------------|------------------------|--------------------|--------------------|
| 1    | Slow                  | $I_{DRV\_SSR\_HV}$ | 15          | 50                     | 5.5           | 11                     | TBD                | TBD                |
| 2    |                       |                    | 30          | 50                     | 5.5           | 10                     | TBD                | TBD                |
| 3    |                       |                    | 50          | 50                     | 5.5           | 01                     | TBD                | TBD                |
| 4    |                       |                    | 300         | 50                     | 5.5           | 00                     | TBD                | TBD                |
| 5    |                       |                    | 300         | 200                    | 5.5           | 00                     | TBD                | TBD                |
| 6    | Medium                | $I_{DRV\_MSR\_HV}$ | 15          | 50                     | 5.5           | 11                     | TBD                | TBD                |
| 7    |                       |                    | 30          | 50                     | 5.5           | 10                     | TBD                | TBD                |
| 8    |                       |                    | 50          | 50                     | 5.5           | 01                     | TBD                | TBD                |
| 9    |                       |                    | 300         | 50                     | 5.5           | 00                     | TBD                | TBD                |
| 10   |                       |                    | 300         | 200                    | 5.5           | 00                     | TBD                | TBD                |
| 11   | Fast                  | $I_{DRV\_FC}$      | 10          | 50                     | 3.6           | 11                     | 50.4               | 101.6              |
| 12   |                       |                    | 10          | 30                     | 3.6           | 10                     | 14.2               | 57.3               |
| 13   |                       |                    | 10          | 20                     | 3.6           | 01                     | 16.4               | 43.6               |
| 14   |                       |                    | 10          | 10                     | 3.6           | 00                     | 9.8                | 15.9               |
| 15   |                       |                    | 10          | 50                     | 2.75          | 11                     | 22.9               | 45.3               |
| 16   |                       |                    | 10          | 30                     | 2.75          | 10                     | 6.7                | 25.3               |
| 17   |                       |                    | 10          | 20                     | 2.75          | 01                     | 4.5                | 17.3               |
| 18   |                       |                    | 10          | 10                     | 2.75          | 00                     | 3                  | 9.6                |
| 19   | Input                 | $I_{DRV\_I\_HV}$   | 7           | 0.5                    | 5.5           | N/A                    | TBD                | TBD                |

<sup>1</sup> These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

<sup>2</sup> Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See [Table 2](#).

<sup>3</sup> All loads are lumped.

## 4.7.1 I/O Pad $V_{DD33}$ Current Specifications

The power consumption of the  $V_{DD33}$  supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin  $V_{DD33}$  currents for all I/O segments. The output pin  $V_{DD33}$  current can be calculated from Table 11 based on the voltage, frequency, and load on all Pad F pins. The input pin  $V_{DD33}$  current can be calculated from Table 11 based on the voltage, frequency, and load on all Pad MH pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

Table 11. I/O Pad Average  $I_{DD33}$  Specifications<sup>1</sup>

| Spec | Pad Type <sup>2</sup> | Symbol             | Period (ns) | Load <sup>3</sup> (pF) | Drive Select | $I_{DD33}$ Avg ( $\mu$ A) | $I_{DD33}$ RMS ( $\mu$ A) |
|------|-----------------------|--------------------|-------------|------------------------|--------------|---------------------------|---------------------------|
| 1    | Slow                  | $I_{DRV\_SSR\_HV}$ | 100         | 50                     | 11           | 0.8                       | 235.7                     |
| 2    |                       |                    | 200         | 50                     | 01           | 0.04                      | 87.4                      |
| 3    |                       |                    | 800         | 50                     | 00           | 0.06                      | 47.4                      |
| 4    |                       |                    | 800         | 200                    | 00           | 0.009                     | 47                        |
| 5    | Medium                | $I_{DRV\_MSR\_HV}$ | 40          | 50                     | 11           | TBD                       | TBD                       |
| 6    |                       |                    | 100         | 50                     | 01           | 0.11                      | 76.5                      |
| 7    |                       |                    | 500         | 50                     | 00           | 0.02                      | 56.2                      |
| 8    |                       |                    | 500         | 200                    | 00           | 0.01                      | 56.2                      |
| 9    | Input                 | $I_{DRV\_I\_HV}$   | 7           | 0.5                    | N/A          | TBD                       | TBD                       |

<sup>1</sup> These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

<sup>2</sup> Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 2.

<sup>3</sup> All loads are lumped.

Table 12.  $I_{DD33}$  Pad Average DC Current<sup>1</sup>

| Spec | Pad Type <sup>2</sup> | Symbol        | Period (ns) | Load <sup>3</sup> (pF) | $V_{DD33}$ (V) | $V_{DDE}$ (V) | Drive Select | $I_{DD33}$ Avg ( $\mu$ A) | $I_{DD33}$ RMS ( $\mu$ A) |
|------|-----------------------|---------------|-------------|------------------------|----------------|---------------|--------------|---------------------------|---------------------------|
| 1    | Fast                  | $I_{DRV\_FC}$ | 10          | 50                     | 3.6            | 3.6           | 11           | 3.32                      | 11.77                     |
| 2    |                       |               | 10          | 30                     | 3.6            | 3.6           | 10           | 2.28                      | 7.07                      |
| 3    |                       |               | 10          | 20                     | 3.6            | 3.6           | 01           | 1.73                      | 5.75                      |
| 4    |                       |               | 10          | 10                     | 3.6            | 3.6           | 00           | 1.39                      | 4.77                      |
| 5    |                       |               | 10          | 50                     | 3.6            | 2.75          | 11           | 2.3                       | 7.81                      |
| 6    |                       |               | 10          | 30                     | 3.6            | 2.75          | 10           | 1.64                      | 4.96                      |
| 7    |                       |               | 10          | 20                     | 3.6            | 2.75          | 01           | 1.37                      | 4.31                      |
| 8    |                       |               | 10          | 10                     | 3.6            | 2.75          | 00           | 1.06                      | 4.09                      |

<sup>1</sup> These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

<sup>2</sup> Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 2.

<sup>3</sup> All loads are lumped.

## Electrical Characteristics

## 4.8 Low Voltage Characteristics

Table 13. Low Voltage Monitors

| Spec | Characteristic   | Symbol   | Min                          | Typical                      | Max                          | Unit |
|------|--|--|------------------------------|------------------------------|------------------------------|------|
| 1    | Power-on-Reset Assert Level <sup>1</sup>   | V <sub>POR</sub>   | 1.5                          | —                            | 2.8                          | V    |
| 2    | Low Voltage Monitor 3.3 V <sup>2</sup><br>Assert Level<br>De-assert Level  | V <sub>LVI33A</sub><br>V <sub>LVI33D</sub>   | 3.00<br>3.04                 | 3.05<br>3.12                 | 3.10<br>3.19                 | V    |
| 3    | Low Voltage Monitor Synthesizer <sup>3</sup><br>Assert Level<br>De-assert Level  | V <sub>LVISYNA</sub><br>V <sub>LVISYND</sub>   | 3.00<br>3.04                 | 3.05<br>3.12                 | 3.10<br>3.19                 | V    |
| 4    | Low Voltage Monitor 3.0 V Low Threshold <sup>1</sup><br>VRCSEL = V <sub>SSA</sub><br>Assert Level<br>De-assert Level<br>VRCSEL = V <sub>DDA</sub><br>Assert Level<br>De-assert Level | V <sub>LVI_VDDA_LOA</sub><br>V <sub>LVI_VDDA_LOD</sub><br>V <sub>LVI_VDDA_LOA</sub><br>V <sub>LVI_VDDA_LOD</sub> | 3.00<br>3.04<br>3.25<br>3.35 | 3.05<br>3.12<br>3.35<br>3.45 | 3.10<br>3.19<br>3.48<br>3.55 | V    |
| 5    | Low Voltage Monitor 5.0 V <sup>1, 4</sup><br>Assert Level<br>De-assert Level   | V <sub>LVI_VDDA_A</sub><br>V <sub>LVI_VDDA_D</sub>   | 4.40<br>4.50                 | 4.475<br>4.575               | 4.55<br>4.65                 | V    |
| 6    | Low Voltage Monitor 5.0 V High Threshold <sup>1, 5</sup><br>Assert Level<br>De-assert Level  | V <sub>LVI_VDDA_HA</sub><br>V <sub>LVI_VDDA_HD</sub>   | 4.55<br>4.55                 | 4.65<br>4.65                 | 4.75<br>4.75                 | V    |

<sup>1</sup> Monitors V<sub>DDA</sub>.<sup>2</sup> Monitors V<sub>DD33</sub>.<sup>3</sup> Monitors V<sub>DDSYN</sub>.<sup>4</sup> Disabled when V<sub>RCSEL</sub> = V<sub>SSA</sub>.

## 4.9 Oscillators Electrical Characteristics

Table 14. 3.3 V High Frequency External Oscillator

| Spec | Characteristic  | Symbol               | Min  | Max  | Unit |
|------|---|----------------------|--|--|------|
| 1    | Frequency Range   | f <sub>ref</sub>     | 4 <sup>1</sup>                                       | 40   | MHz  |
| 2    | Duty Cycle of reference   | t <sub>DC</sub>      | 40   | 60   | %    |
| 3    | EXTAL Input High Voltage<br>External crystal mode <sup>2</sup><br>External clock mode | V <sub>IHEXT</sub>   | V <sub>XTAL</sub> + 0.4<br>0.65 × V <sub>DDSYN</sub> | V <sub>DDSYN</sub> + 0.3<br>V <sub>DDSYN</sub> + 0.3 | V    |
| 4    | EXTAL Input Low Voltage<br>External crystal mode <sup>3</sup><br>External clock mode  | V <sub>ILEXT</sub>   | V <sub>DDSYN</sub> - 0.3<br>V <sub>DDSYN</sub> - 0.3 | V <sub>XTAL</sub> - 0.4<br>0.35 × V <sub>DDSYN</sub> | V    |
| 5    | XTAL Current <sup>4</sup>   | I <sub>XTAL</sub>    | 1  | 3  | mA   |
| 6    | Total On-chip stray capacitance on XTAL   | C <sub>S_XTAL</sub>  | —  | 3  | pF   |
| 7    | Total On-chip stray capacitance on EXTAL  | C <sub>S_EXTAL</sub> | —  | 3  | pF   |

**Table 14. 3.3 V High Frequency External Oscillator (continued)**

| Spec | Characteristic                                     | Symbol         | Min                       | Max  | Unit |
|------|--|----------------|---------------------------|--|------|
| 8    | Crystal manufacturer's recommended capacitive load | $C_L$          | See crystal specification | See crystal specification                        | pF   |
| 9    | Discrete load capacitance to be connected to EXTAL | $C_{L\_EXTAL}$ | —                         | $2 \times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}^5$ | pF   |
| 10   | Discrete load capacitance to be connected to XTAL  | $C_{L\_XTAL}$  | —                         | $2 \times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}^5$   | pF   |
| 11   | Startup Time                                       | $t_{startup}$  | —                         | 10   | ms   |

- <sup>1</sup> When PLL frequency modulation is active, reference frequencies less than 8 MHz will distort the modulated waveform and the effects of this on emissions is not characterized.
- <sup>2</sup> This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case,  $V_{extal} - V_{xtal} \geq 400$  mV criteria has to be met for oscillator's comparator to produce output clock.
- <sup>3</sup> This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case,  $V_{xtal} - V_{extal} \geq 400$  mV criteria has to be met for oscillator's comparator to produce output clock.
- <sup>4</sup>  $I_{xtal}$  is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.
- <sup>5</sup>  $C_{PCB\_EXTAL}$  and  $C_{PCB\_XTAL}$  are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

**Table 15. 5 V Low Frequency (32 kHz) External Oscillator**

| Spec | Characteristic                                     | Symbol        | Min.                      | Max                       | Unit    |
|------|--|---------------|---------------------------|---------------------------|---------|
| 1    | Frequency Range                                    | $f_{ref32}$   | 32                        | 40                        | kHz     |
| 2    | Duty Cycle of reference                            | $t_{dc32}$    | 40                        | 60                        | %       |
| 3    | XTAL32 Current <sup>1</sup>                        | $I_{XTAL32}$  | —                         | 3                         | $\mu$ A |
| 4    | Crystal manufacturer's recommended capacitive load | $C_{L32}$     | See crystal specification | See crystal specification | pF      |
| 5    | Startup Time                                       | $t_{Startup}$ | —                         | 2                         | s       |

- <sup>1</sup>  $I_{xtal32}$  is the oscillator bias current out of the XTAL32 pin with both EXTAL32 and XTAL32 pins grounded.

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**Table 16. 5 V High Frequency (16 MHz) Internal RC Oscillator**

| Spec | Characteristic                                    | Symbol        | Range | Min  | Typ | Max       | Unit |
|------|---|---------------|-------|------|-----|-----------|------|
| 1    | Frequency before trim <sup>1</sup>                | $f_{ut}$      | 35%   | 10.4 | 16  | 21.6      | MHz  |
| 2    | Frequency after loading factory trim <sup>2</sup> | $f_t$         | 5%    | 15.2 | 16  | 16.8      | MHz  |
| 3    | Application trim resolution <sup>3</sup>          | $t_s$         | —     | —    | —   | $\pm 0.5$ | %    |
| 4    | Application frequency trim step <sup>3</sup>      | $f_s$         | —     | —    | 300 | —         | kHz  |
| 5    | Startup Time                                      | $t_{Startup}$ | —     | —    | —   | 500       | ns   |

- <sup>1</sup> Across process, voltage, and temperature.
- <sup>2</sup> Across voltage and temperature.
- <sup>3</sup> Fixed voltage and temperature.

## Electrical Characteristics

Table 17. 5V Low Frequency (128 kHz) Internal RC Oscillator

| Spec | Characteristic                                    | Symbol             | Range | Min   | Typ | Max   | Unit |
|------|---|--------------------|-------|-------|-----|-------|------|
| 1    | Frequency before trim <sup>1</sup>                | F <sub>ut128</sub> | 35%   | 83.2  | 128 | 172.8 | kHz  |
| 2    | Frequency after loading factory trim <sup>2</sup> | F <sub>t128</sub>  | 5%    | 121.6 | 128 | 134.4 | kHz  |
| 3    | Application trim resolution <sup>3</sup>          | T <sub>s128</sub>  | —     | —     | —   | ±2    | %    |
| 4    | Application frequency trim step <sup>3</sup>      | F <sub>s128</sub>  | —     | —     | 1   | —     | kHz  |
| 5    | Startup Time                                      | S <sub>t128</sub>  | —     | —     | —   | 100   | µs   |

<sup>1</sup> Across process, voltage, and temperature.

<sup>2</sup> Across voltage and temperature.

<sup>3</sup> Fixed voltage and temperature.

## 4.10 FMPLL Electrical Characteristics

Table 18. FMPLL Electrical Specifications<sup>1</sup>

| Spec | Characteristic  | Symbol               | Min                               | Max  | Unit                 |
|------|---|----------------------|-----------------------------------|------|----------------------|
| 1    | System Frequency <sup>2</sup>   | f <sub>SYS</sub>     | —                                 | 116  | MHz                  |
| 2    | PLL Reference Frequency Range   | f <sub>REF</sub>     | 4                                 | 40   | MHz                  |
| 3    | PLL Frequency   | f <sub>PLL</sub>     | $\frac{f_{vco(min)}}{(ERFD + 1)}$ |      | MHz                  |
| 4    | Loss of Reference Frequency <sup>3</sup>  | f <sub>LOR</sub>     | 100                               | 2000 | kHz                  |
| 5    | Self Clocked Mode Frequency   | f <sub>SCM</sub>     | 16                                | 64   | MHz                  |
| 6    | PLL Lock Time <sup>4</sup>  | t <sub>LPLL</sub>    | —                                 | 400  | µs                   |
| 7    | Duty Cycle of Reference   | t <sub>DC</sub>      | 40                                | 60   | %                    |
| 8    | Frequency un-LOCK Range   | f <sub>UL</sub>      | -4.0                              | 4.0  | % f <sub>SYS</sub>   |
| 9    | Frequency LOCK Range  | f <sub>LCK</sub>     | -2.0                              | 2.0  | % f <sub>SYS</sub>   |
| 10   | CLKOUT Period Jitter, <sup>5</sup> Measured at f <sub>SYS</sub> Max<br>Cycle-to-cycle Jitter                | C <sub>Jitter</sub>  | -5                                | 5    | %f <sub>SYS</sub>    |
| 11   | CLKOUT Jitter at ≥ 50 µs period   | C <sub>Jitter</sub>  | -0.5                              | 0.5  | %f <sub>CLKOUT</sub> |
| 12   | Peak-to-Peak Frequency Modulation Range Limit <sup>6,7</sup><br>(f <sub>SYS</sub> Max must not be exceeded) | C <sub>mod</sub>     | 0                                 | 4    | %f <sub>SYS</sub>    |
| 13   | FM Depth Tolerance <sup>8</sup>   | C <sub>mod_err</sub> | -0.50                             | 0.50 | %f <sub>SYS</sub>    |
| 14   | VCO Frequency <sup>9</sup>  | f <sub>VCO</sub>     | 192                               | 600  | MHz                  |
| 15   | Modulation Rate Limits <sup>10</sup>  | f <sub>MOD</sub>     | 0.400                             | 1    | MHz                  |

<sup>1</sup> V<sub>DDSYN</sub> = 3.0 V to 3.6 V, V<sub>SS</sub> = V<sub>SSSYN</sub> = 0 V, T<sub>A</sub> = T<sub>L</sub> to T<sub>H</sub>.

- 2 The maximum frequency value is with frequency modulation disabled. If frequency modulation is enabled, the maximum frequency value should be de-rated by the percentage of modulation enabled so that the maximum frequency is not exceeded.
- 3 “Loss of Reference Frequency” is the reference frequency detected internally, which transitions the PLL into self clocked mode.
- 4 This specification applies to the period required for the PLL to re-lock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, lock time will be additive with crystal startup time.
- 5 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of  $C_{jitter} + C_{mod}$ .
- 6 Modulation depth selected must not result in  $f_{PLL}$  value greater than the  $f_{PLL}$  maximum specified value.
- 7 Maximum and minimum variations from programmed modulation depth are 2%, 3%, and 4% peak-to-peak. Use only these settings.
- 8 Depth tolerance is the programmed modulation depth  $\pm 0.25\%$  of  $f_{SYS}$ . Initial design target pending silicon evaluation.
- 9 See the Block Guide for VCO frequency synthesis equations.
- 10 Modulation rates less than 400 kHz will result in exceedingly long FM calibration durations. Modulation rates greater than 1 MHz will result in reduced calibration accuracy.

## 4.11 ADC Electrical Characteristics

Table 19. ADC Conversion Specifications (Operating)

| Spec | Characteristic  | Symbol    | Min             | Max       | Unit |
|------|---|-----------|-----------------|-----------|------|
| 1    | Analog High Reference Voltage   | $V_{RH}$  | $V_{DDA} - 0.5$ | $V_{DDA}$ | V    |
| 2    | Analog Low Reference Voltage  | $V_{RL}$  | 0               | 0.5       | V    |
| 3    | Analog Input Voltage  | $AV_{IN}$ | $V_{RL}$        | $V_{RH}$  | V    |
| 4    | Sampling Frequency  | $F_S$     | —               | 1.53      | MHz  |
| 5    | Maximum ADC Clock Frequency   | $F_{MAX}$ | —               | 60        | MHz  |
| 6    | Sampling Time<br>$V_{DDA} = 3.0\text{ V} - 3.6\text{ V}$<br>$V_{DDA} > 3.6\text{ V} - 5.5\text{ V}$ | $t_s$     | 250<br>125      | —         | ns   |
| 7    | Differential Non Linearity  | DNL       | -1.0            | 1.0       | LSB  |
| 8    | Integral Non Linearity  | INL       | -1.5            | 1.5       | LSB  |
| 9    | Offset Error  | OFS       | -1.0            | 1.0       | LSB  |
| 10   | Gain Error  | GNE       | -2.0            | 2.0       | LSB  |
| 11   | Total Unadjusted Error <sup>1</sup>   | TUE       | -2.0            | 2.0       | LSB  |

<sup>1</sup> TUE assumes no pin activity on pins adjacent to analog channel or output driver activity on corresponding  $V_{DDE}$  segment.

## 4.12 Flash Memory Electrical Characteristics

Table 20. Flash Program and Erase Specifications<sup>1</sup>

| Spec | Characteristic   | Symbol            | Min | Initial Max <sup>2</sup> | Max <sup>3</sup> | Unit          |
|------|--|-------------------|-----|--------------------------|------------------|---------------|
| 1    | Double Word (64 bits) Program Time <sup>4</sup>        | $t_{dwprogram}$   | —   | —                        | 500              | $\mu\text{s}$ |
| 2    | Page (128 bits and 256 bits) Program Time <sup>4</sup> | $t_{pprogram}$    | —   | 160                      | 500              | $\mu\text{s}$ |
| 3    | 16 KB Block Pre-program and Erase Time                 | $t_{16kpperase}$  | —   | 1000                     | 5000             | ms            |
| 4    | 64 KB Block Pre-program and Erase Time                 | $t_{64kpperase}$  | —   | 1800                     | 5000             | ms            |
| 5    | 128 KB Block Pre-program and Erase Time                | $t_{128kpperase}$ | —   | 2600                     | 7500             | ms            |

## Electrical Characteristics

Table 20. Flash Program and Erase Specifications<sup>1</sup> (continued)

| Spec | Characteristic  | Symbol            | Min | Initial Max <sup>2</sup> | Max <sup>3</sup>                | Unit    |
|------|---|-------------------|-----|--------------------------|---------------------------------|---------|
| 6    | 256 KB Block Pre-program and Erase Time   | $t_{256kpperase}$ | —   | 5200                     | 15,000                          | ms      |
| 7    | Wait States Relative to System Frequency <sup>5</sup><br>PFCRP $\eta$ [RWSC] = PFCRP $\eta$ [APC] = 0b000; PFCRP $\eta$ [WWSC] = 0b01<br>PFCRP $\eta$ [RWSC] = PFCRP $\eta$ [APC] = 0b001; PFCRP $\eta$ [WWSC] = 0b01<br>PFCRP $\eta$ [RWSC] = PFCRP $\eta$ [APC] = 0b010; PFCRP $\eta$ [WWSC] = 0b01<br>PFCRP $\eta$ [RWSC] = PFCRP $\eta$ [APC] = 0b011 – 0b111; PFCRP $\eta$ [WWSC] = 0b01 | $t_{wsc}$         | —   | —                        | 30<br>60<br>90<br>$f_{SYS}$ max | MHz     |
| 8    | Recovery Time   | $t_{Recover}$     | —   | —                        | 45                              | $\mu$ s |

<sup>1</sup> Typical program and erase times assume nominal supply values and operation at 25 °C.

<sup>2</sup> Initial factory condition: < 100 program/erase cycles, nominal supply values and operation at 25 °C.

<sup>3</sup> The maximum time is at worst case conditions after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

<sup>4</sup> Actual hardware programming time. This does not include software overhead.

<sup>5</sup> Wait state timing is based on the system clock frequency and thus is same for all masters.

Table 21. Flash EEPROM Module Life (Full Temperature Range)

| Spec | Characteristic   | Symbol    | Min               | Typical <sup>1</sup> | Unit   |
|------|--|-----------|-------------------|----------------------|--------|
| 1    | Number of Program/Erase cycles per block for 16 KB and 64 KB blocks over the operating temperature range ( $T_J$ )   | P/E       | 100,000           | —                    | cycles |
| 2    | Number of Program/Erase cycles per block for 128 KB blocks over the operating temperature range ( $T_J$ )  | P/E       | 1,000             | 100,000              | cycles |
| 3    | Minimum Data Retention at 25 °C ambient temperature <sup>2</sup><br>Blocks with 0–1,000 P/E cycles<br>Blocks with 1,001–10,000 P/E cycles<br>Blocks with 10,001–100,000 P/E cycles | Retention | 20<br>10<br>1 – 5 | —                    | years  |

<sup>1</sup> Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

<sup>2</sup> Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

## 4.13 Pad AC Specifications

Table 22. Pad AC Specifications (5.0 V, 2.5 V)<sup>1</sup>

| Spec | Pad Type <sup>2</sup> | SRC/DSC <sup>3</sup> | Output Delay <sup>4,4</sup> (ns) | Rise/Fall <sup>5,6</sup> (ns) | Load Drive (pF) |
|------|-----------------------|----------------------|----------------------------------|-------------------------------|-----------------|
| 1    | Slow <sup>7</sup>     | 00                   | 318/343                          | 155/173                       | 50              |
|      |                       |                      | 408/431                          | 188/204                       | 200             |
|      |                       | 01                   | 61/67                            | 30/34                         | 50              |
|      |                       |                      | 80/90                            | 38/44                         | 200             |
|      |                       | 11                   | 18/18                            | 10/11                         | 50              |
|      |                       |                      | 27/28                            | 15/17                         | 200             |



Table 22. Pad AC Specifications (5.0 V, 2.5 V)<sup>1</sup> (continued)

| Spec | Pad Type <sup>2</sup> | SRC/DSC <sup>3</sup> | Output Delay <sup>4,4</sup> (ns) | Rise/Fall <sup>5,6</sup> (ns) | Load Drive (pF) |
|------|-----------------------|----------------------|----------------------------------|-------------------------------|-----------------|
| 2    | Medium                | 00                   | 142/186                          | 65/89                         | 50              |
|      |                       |                      | 195/253                          | 91/122                        | 200             |
|      |                       | 01                   | 20/35                            | 8.7/16.6                      | 50              |
|      |                       |                      | 41/64                            | 24/35                         | 200             |
|      |                       | 11                   | 12/11                            | 5.3/5.9                       | 50              |
|      |                       |                      | 32/34                            | 21/23                         | 200             |
| 3    | Fast <sup>8</sup>     | 00                   | 2.7                              | 1.5                           | 10              |
|      |                       | 01                   |                                  |                               | 20              |
|      |                       | 10                   |                                  |                               | 30              |
|      |                       | 11                   |                                  |                               | 50              |
| 4    | Input                 | N/A                  | 1.9/1.9                          | 1.5/1.5                       | 0.5             |

- <sup>1</sup> These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at  $F_{SYS} = 116$  MHz,  $V_{DD} = 1.08 - 1.32$  V,  $V_{DDE} = 1.62 - 1.98$  V,  $V_{DDEH} = 4.5 - 5.5$  V,  $V_{RC33}$  and  $V_{DDPLL} = 3.0 - 3.6$  V,  $T_A = T_L$  to  $T_H$ .
- <sup>2</sup> Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 2.
- <sup>3</sup> SRC/DSC are bitfields in the Pad Configuration Registers. SRC—Slew Rate Control (slow and medium pad types only), DSC—Drive Strength Control (fast pad type only).
- <sup>4</sup> This parameter is supplied for reference and is not guaranteed by design and not tested.
- <sup>5</sup> This parameter is guaranteed by characterization before qualification rather than 100% tested.
- <sup>6</sup> Delay and rise/fall are measured to 20% or 80% of the respective signal.
- <sup>7</sup> Add a maximum of one system clock to the output delay for delay with respect to system clock.
- <sup>8</sup> Output delay is shown in Figure 6. Add a maximum of one system clock to the output delay for delay with respect to system clock.

Table 23. De-rated Pad AC Specifications (3.3 V, 3.3 V)<sup>1</sup>

| Spec | Pad Type <sup>2</sup> | SRC/DSC <sup>3</sup> | Out Delay <sup>4,5</sup> (ns) | Rise/Fall <sup>6</sup> (ns) | Load Drive (pF) |
|------|-----------------------|----------------------|-------------------------------|-----------------------------|-----------------|
| 1    | Slow <sup>7</sup>     | 00                   | 408/431                       | 188/204                     | 50              |
|      |                       |                      | 533/592                       | 250/288                     | 200             |
|      |                       | 01                   | 80/90                         | 38/44                       | 50              |
|      |                       |                      | 146/167                       | 82/96                       | 200             |
|      |                       | 11                   | 27/28                         | 15/17                       | 50              |
|      |                       |                      | 81/92                         | 57/67                       | 200             |
| 2    | Medium                | 00                   | 184/240                       | 79/107                      | 50              |
|      |                       |                      | 253/330                       | 114/153                     | 200             |
|      |                       | 01                   | 28/47                         | 11.8/21.8                   | 50              |
|      |                       |                      | 58/88                         | 34/49                       | 200             |
|      |                       | 11                   | 18/17                         | 7.6/8.9                     | 50              |
|      |                       |                      | 46/51                         | 30/35                       | 200             |

Table 23. De-rated Pad AC Specifications (3.3 V, 3.3 V)<sup>1</sup> (continued)

| Spec | Pad Type <sup>2</sup> | SRC/DSC <sup>3</sup> | Out Delay <sup>4,5</sup><br>(ns) | Rise/Fall <sup>6</sup> ,<br>(ns) | Load Drive<br>(pF) |
|------|-----------------------|----------------------|----------------------------------|----------------------------------|--------------------|
| 3    | Fast <sup>8</sup>     | 00                   | 2.5                              | 1.2                              | 10                 |
|      |                       | 01                   |                                  | 1.2                              | 20                 |
|      |                       | 10                   |                                  | 1.2                              | 30                 |
|      |                       | 11                   |                                  | 1.2                              | 50                 |
| 4    | Input                 | N/A                  | 3/3                              | 1.5/1.5                          | 0.5                |

- <sup>1</sup> These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at  $F_{SYS} = 116 \text{ MHz}$ ,  $V_{DD} = 1.08 - 1.32 \text{ V}$ ,  $V_{DDE} = 3.0 - 3.6 \text{ V}$ ,  $V_{DDEH} = 3.0 - 3.6 \text{ V}$ ,  $V_{RC33}$  and  $V_{DDPLL} = 3.0 - 3.6 \text{ V}$ ,  $T_A = T_L$  to  $T_H$ .
- <sup>2</sup> Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 2.
- <sup>3</sup> SRC/DSC are bitfields in the Pad Configuration Registers. SRC—Slew Rate Control (slow and medium pad types only), DSC—Drive Strength Control (fast pad type only).
- <sup>4</sup> This parameter is supplied for reference and is not guaranteed by design and not tested.
- <sup>5</sup> Delay and rise/fall are measured to 20% or 80% of the respective signal.
- <sup>6</sup> This parameter is guaranteed by characterization before qualification rather than 100% tested.
- <sup>7</sup> Add a maximum of one system clock to the output delay for delay with respect to system clock.
- <sup>8</sup> Output delay is shown in Figure 6. Add a maximum of one system clock to the output delay for delay with respect to system clock.

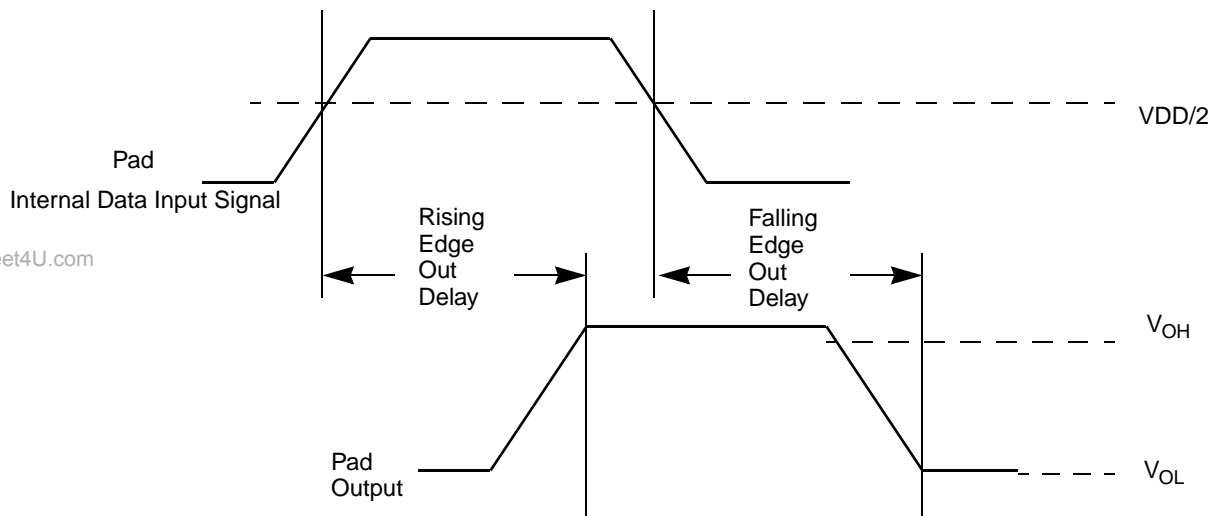


Figure 6. Pad Output Delay

## 4.14 AC Timing

### 4.14.1 Reset and Boot Configuration Pins

Table 24. Reset and Boot Configuration Timing

| Spec | Characteristic                       | Symbol     | Min | Max | Unit    |
|------|--------------------------------------|------------|-----|-----|---------|
| 1    | RESET Pulse Width                    | $t_{RPW}$  | 150 | —   | ns      |
| 2    | BOOTCFG Setup Time after RESET Valid | $t_{RCSU}$ | —   | 100 | $\mu$ s |
| 3    | BOOTCFG Hold Time from RESET Valid   | $t_{RCH}$  | 0   | —   | $\mu$ s |

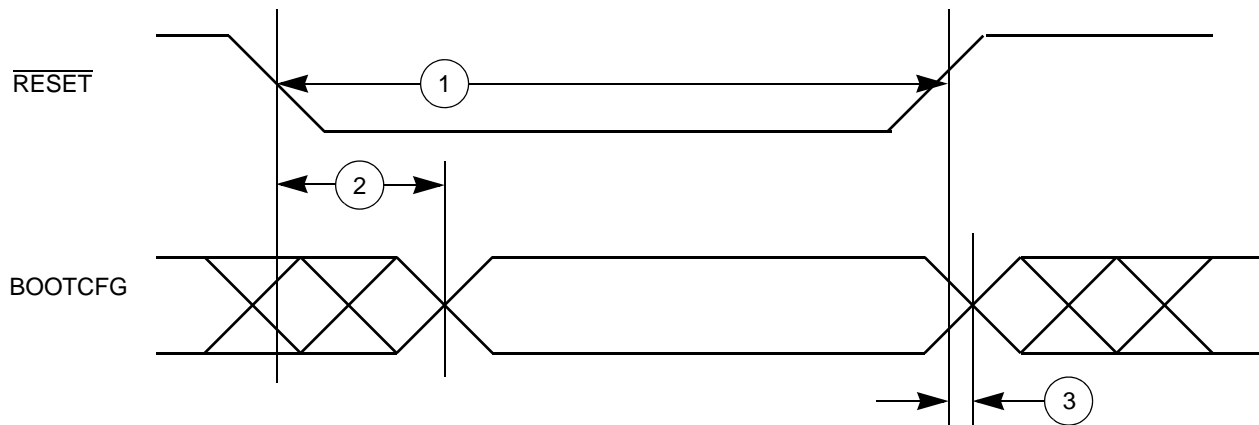


Figure 7. Reset and Boot Configuration Timing

### 4.14.2 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins

Table 25. IRQ/NMI Timing

| Spec | Characteristic                         | Symbol     | Min | Max | Unit      |
|------|--|------------|-----|-----|-----------|
| 1    | IRQ/NMI Pulse Width Low                | $t_{IPWL}$ | 3   | —   | $t_{SYS}$ |
| 2    | IRQ/NMI Pulse Width High               | $T_{IPWH}$ | 3   | —   | $t_{SYS}$ |
| 3    | IRQ/NMI Edge to Edge Time <sup>1</sup> | $t_{CYC}$  | 6   | —   | $t_{SYS}$ |

<sup>1</sup> Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

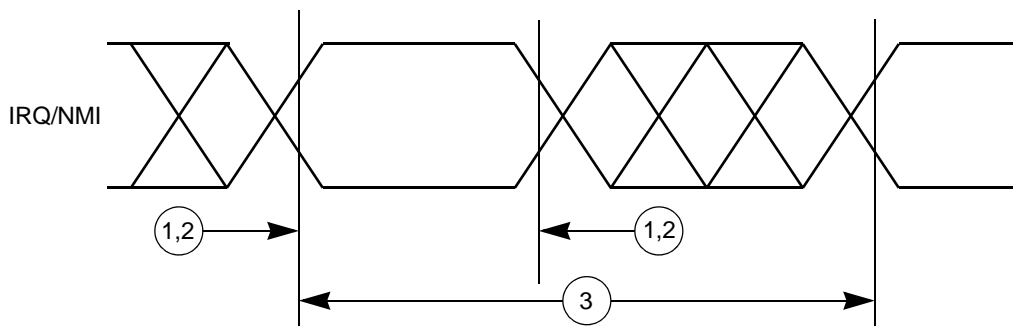


Figure 8. IRQ and NMI Timing

### 4.14.3 JTAG (IEEE 1149.1) Interface

Table 26. JTAG Interface Timing<sup>1</sup>

| Spec | Characteristic   | Symbol               | Min | Max | Unit |
|------|--|----------------------|-----|-----|------|
| 1    | TCK Cycle Time   | $t_{JCYC}$           | 100 | —   | ns   |
| 2    | TCK Clock Pulse Width (Measured at $V_{DDE}/2$ )       | $t_{JDC}$            | 40  | 60  | ns   |
| 3    | TCK Rise and Fall Times (40% – 70%)                    | $t_{TCKRISE}$        | —   | 3   | ns   |
| 4    | TMS, TDI Data Setup Time                               | $t_{TMSS}, t_{TDIS}$ | 5   | —   | ns   |
| 5    | TMS, TDI Data Hold Time                                | $t_{TMSh}, t_{TDIH}$ | 25  | —   | ns   |
| 6    | TCK Low to TDO Data Valid                              | $t_{TDOV}$           | —   | 25  | ns   |
| 7    | TCK Low to TDO Data Invalid                            | $t_{TDOI}$           | 0   | —   | ns   |
| 8    | TCK Low to TDO High Impedance                          | $t_{TDOHZ}$          | —   | 20  | ns   |
| 9    | JCOMP Assertion Time                                   | $t_{JCOMPW}$         | 100 | —   | ns   |
| 10   | JCOMP Setup Time to TCK Low                            | $t_{JCOMP S}$        | 40  | —   | ns   |
| 11   | TCK Falling Edge to Output Valid                       | $t_{BSDV}$           | —   | 50  | ns   |
| 12   | TCK Falling Edge to Output Valid out of High Impedance | $t_{BSDVZ}$          | —   | 50  | ns   |
| 13   | TCK Falling Edge to Output High Impedance              | $t_{BSDHZ}$          | —   | 50  | ns   |
| 14   | Boundary Scan Input Valid to TCK Rising Edge           | $t_{BSDST}$          | 50  | —   | ns   |
| 15   | TCK Rising Edge to Boundary Scan Input Invalid         | $t_{BSDHT}$          | 50  | —   | ns   |

<sup>1</sup> These specifications apply to JTAG boundary scan only. JTAG timing specified at  $V_{DDE} = 3.0 - 5.5 V$ ,  $T_A = T_L$  to  $T_H$ , and  $C_L = 30 pF$  with SRC = 0b11.

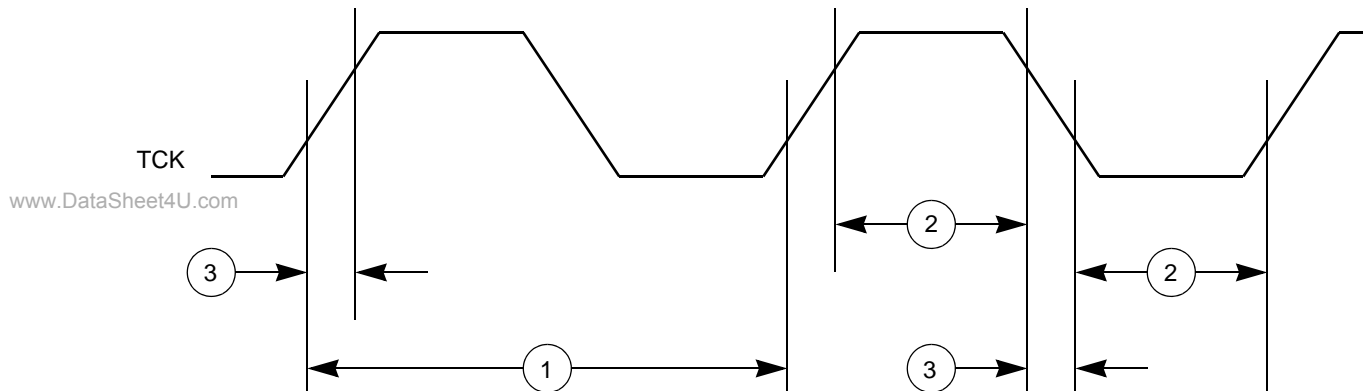


Figure 9. JTAG Test Clock Input Timing

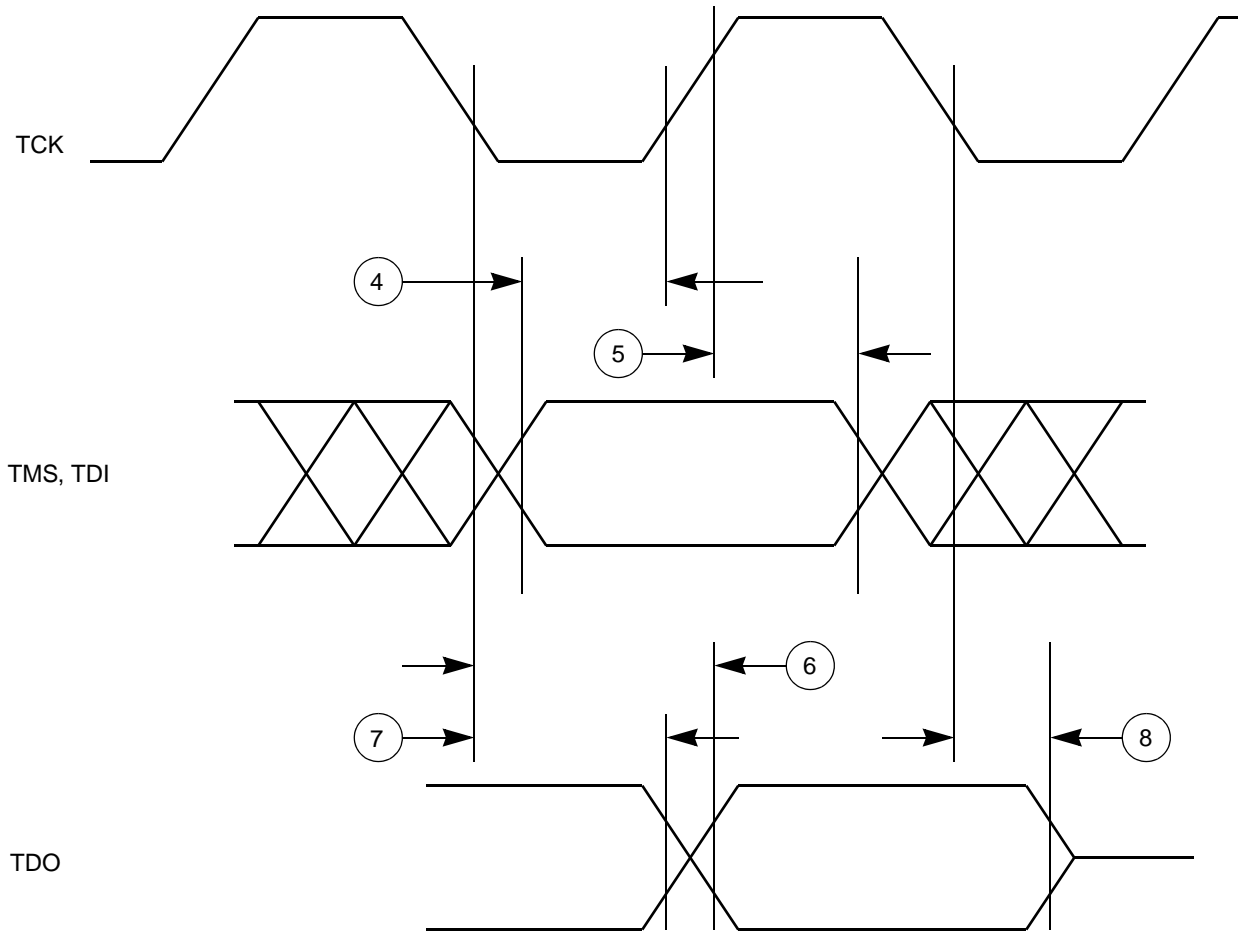


Figure 10. JTAG Test Access Port Timing

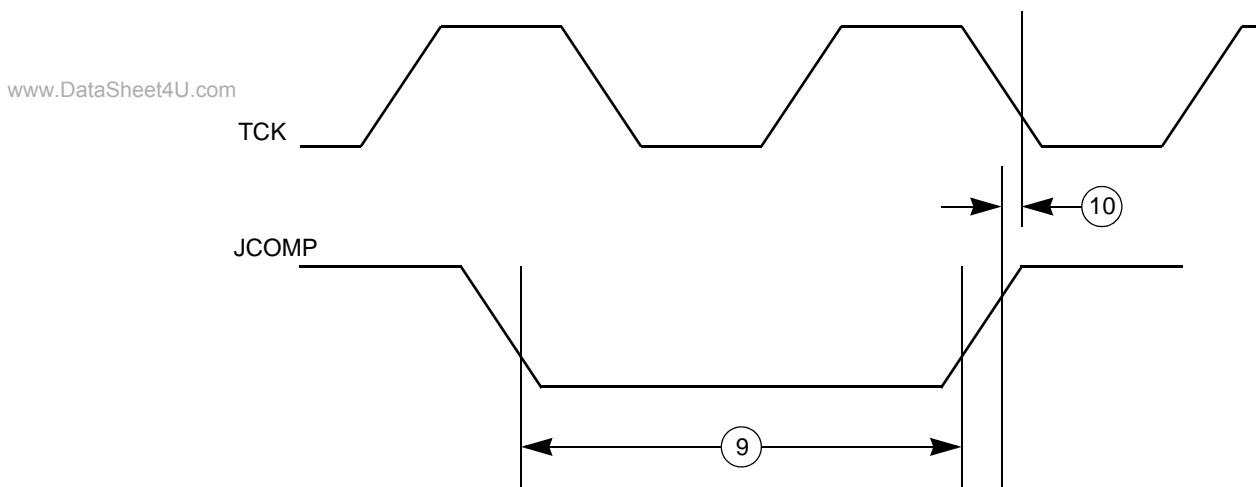


Figure 11. JTAG JCOMP Timing

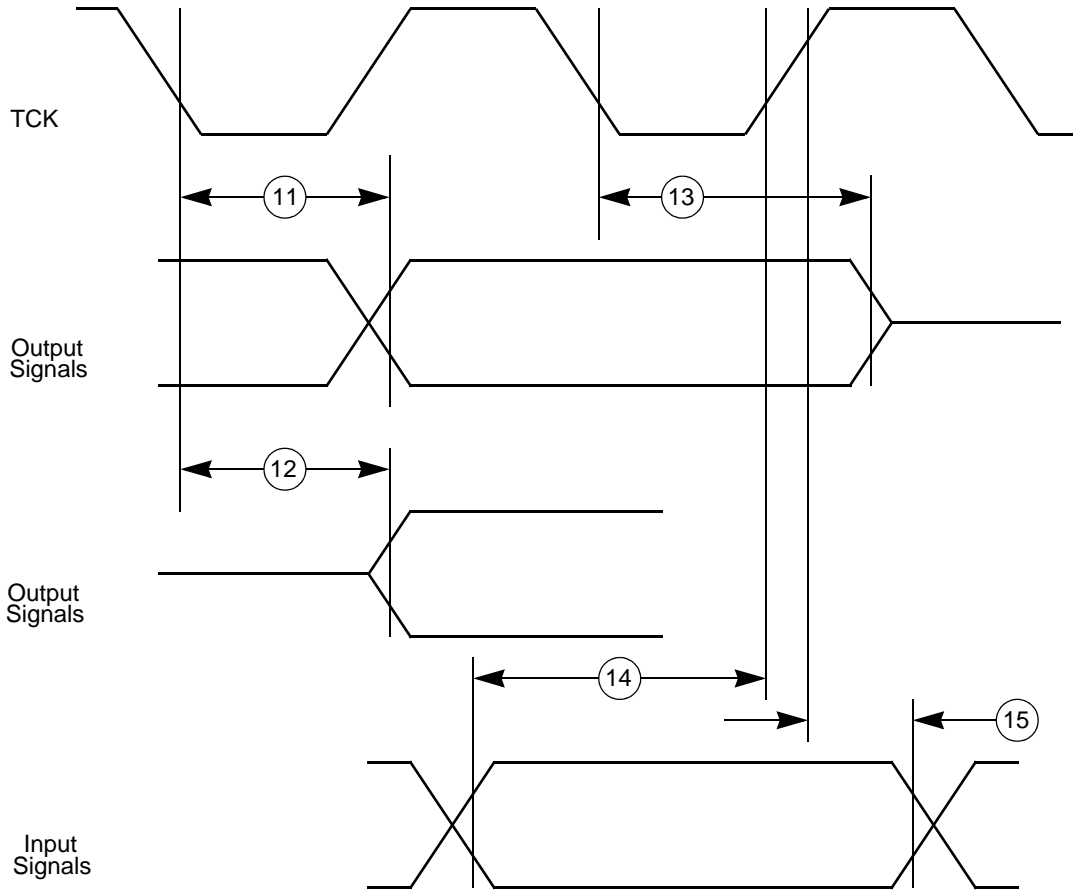


Figure 12. JTAG Boundary Scan Timing

## 4.14.4 Nexus Debug Interface

Table 27. Nexus Debug Port Timing<sup>1</sup>

| Spec | Characteristic   | Symbol                    | Min  | Max  | Unit       |
|------|--|---------------------------|------|------|------------|
| 1    | MCKO Cycle Time  | $t_{MCKO}$                | 15.6 | —    | ns         |
| 2    | MCKO Duty Cycle  | $t_{MDC}$                 | 40   | 60   | %          |
| 3    | MCKO Low to MDO, $\overline{MSEO}$ , $\overline{EVTO}$ Data Valid <sup>2</sup> | $t_{MDOV}$                | -0.1 | 0.25 | $t_{MCKO}$ |
| 4    | $\overline{EVTI}$ Pulse Width  | $t_{EVTIPW}$              | 4.0  | —    | $t_{TCK}$  |
| 5    | $\overline{EVTO}$ Pulse Width  | $t_{EVTOPW}$              | 1    | —    | $t_{MCKO}$ |
| 6    | TCK Cycle Time <sup>3</sup>  | $t_{TCK}$                 | 40   | —    | ns         |
| 7    | TCK Duty Cycle   | $t_{TDC}$                 | 40   | 60   | %          |
| 8    | TDI, TMS Data Setup Time   | $t_{NTDIS}$ , $t_{NTMSS}$ | 8    | —    | ns         |
| 9    | TDI, TMS Data Hold Time  | $t_{NTDIH}$ , $t_{NTMSH}$ | 5    | —    | ns         |
| 10   | TCK Low to TDO Data Valid  | $t_{JOV}$                 | 0    | 25   | ns         |

<sup>1</sup> JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at  $V_{DDE} = 3.0 - 5.5$  V,  $T_A = T_L$  to  $T_H$ , and  $C_L = 30$  pF with SRC = 0b11.

<sup>2</sup> MDO,  $\overline{MSEO}$ , and  $\overline{EVTO}$  data is held valid until next MCKO low cycle.

<sup>3</sup> The system clock frequency needs to be three times faster than the TCK frequency.

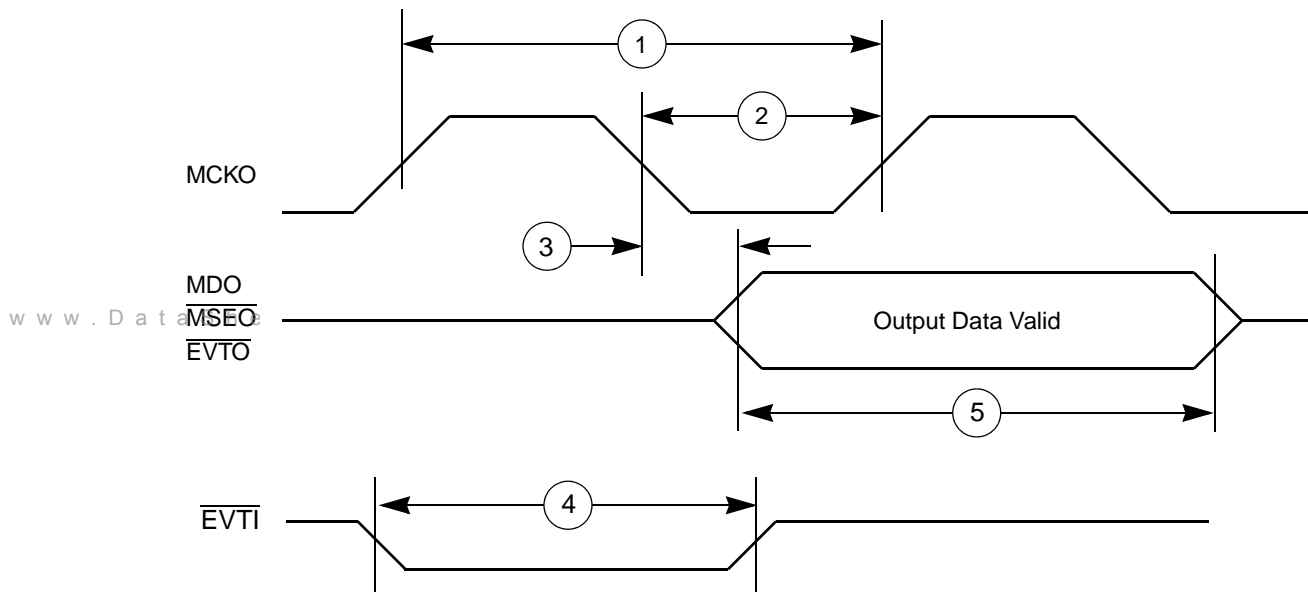
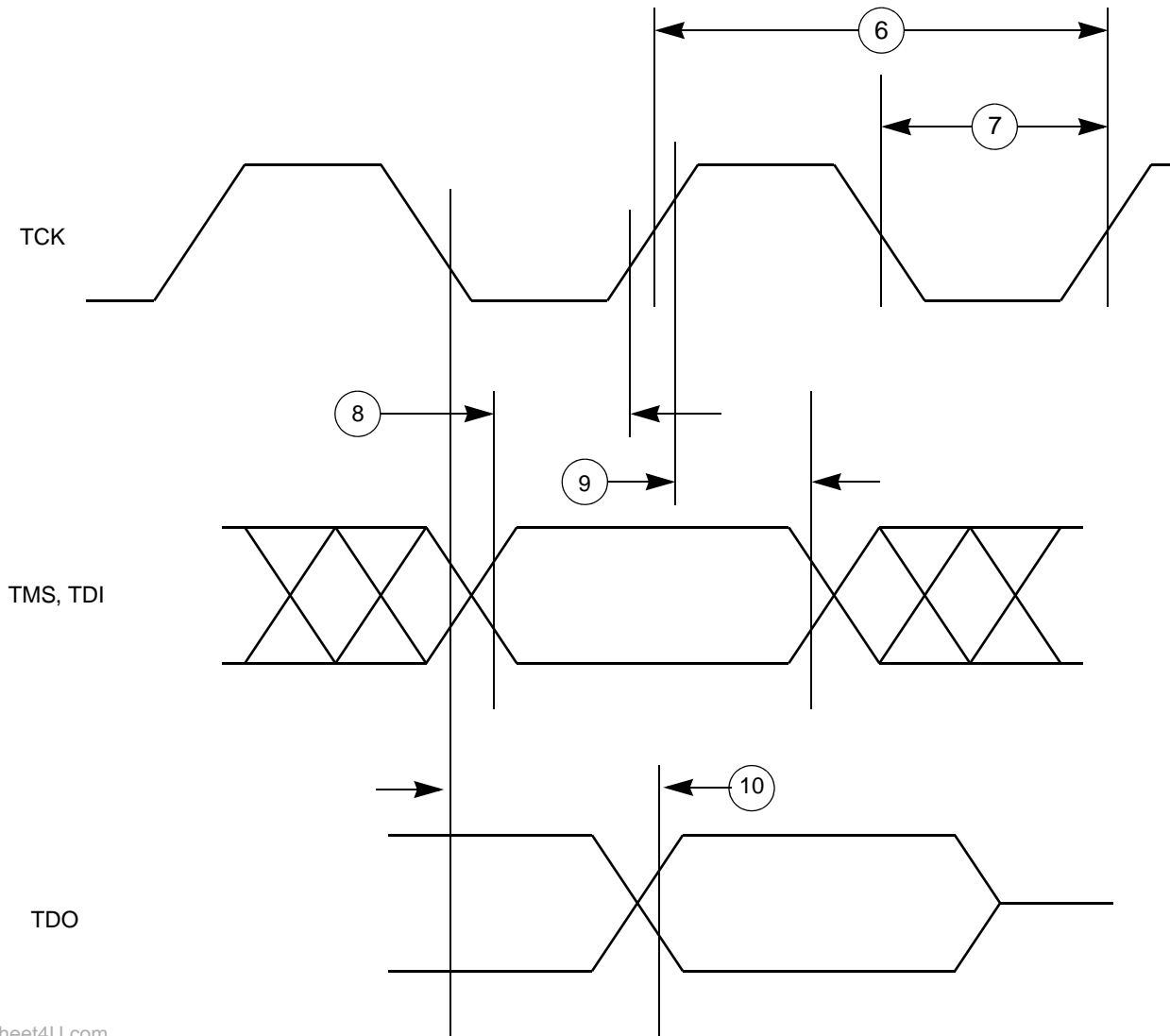


Figure 13. Nexus Output Timing



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Figure 14. Nexus TDI, TMS, TDO Timing



### 4.14.5 Enhanced Modular I/O Subsystem (eMIOS)

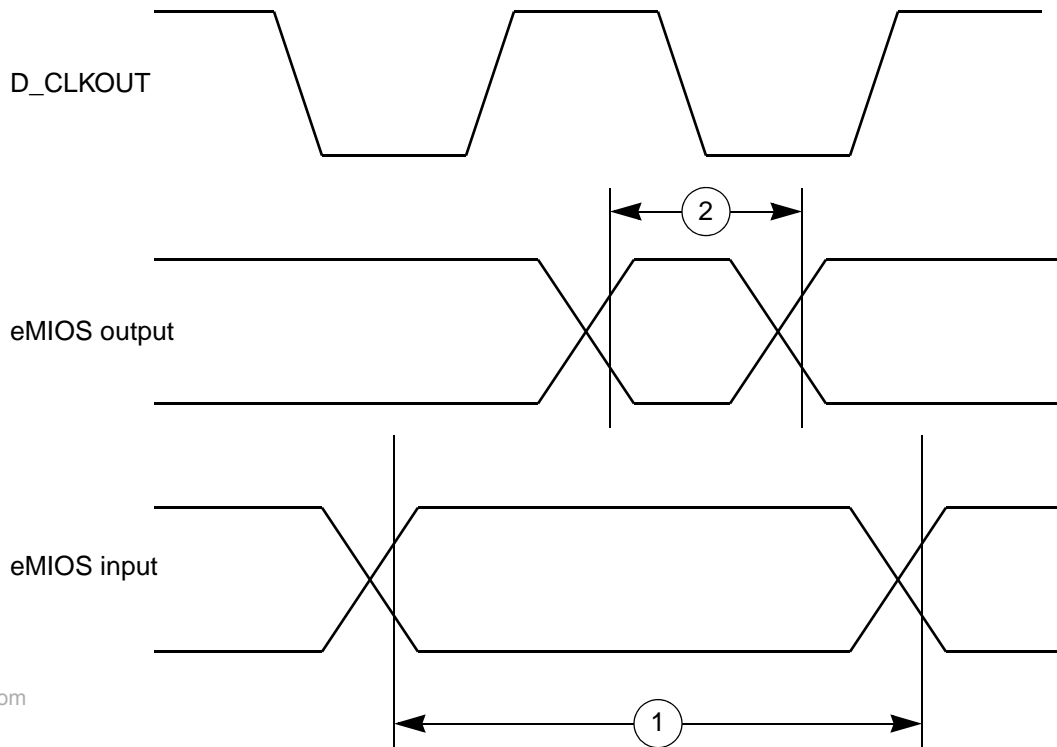
Table 28. eMIOS Timing<sup>1</sup>

| Spec | Characteristic           | Symbol     | Min            | Max | Unit      |
|------|--------------------------|------------|----------------|-----|-----------|
| 1    | eMIOS Input Pulse Width  | $t_{MIPW}$ | 4              | —   | $t_{CYC}$ |
| 2    | eMIOS Output Pulse Width | $t_{MOPW}$ | 1 <sup>2</sup> | —   | $t_{CYC}$ |

<sup>1</sup> eMIOS timing specified at  $V_{DDE} = 3.0 - 5.5 V$ ,  $T_A = T_L$  to  $T_H$ , and  $CL = 30 pF$  with  $SRC = 0b11$ .

<sup>2</sup> This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

Figure 15. eMIOS Timing



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## Electrical Characteristics

## 4.14.6 Deserial Serial Peripheral Interface (DSPI)

Table 29. DSPI Timing

| Spec | Characteristic   | Symbol     | 116 MHz <sup>1</sup> |                      | Unit |
|------|--|------------|----------------------|----------------------|------|
|      |  |            | Min. Value           | Max. Value           |      |
| 1    | DSPI Cycle Time  | $t_{SCK}$  |                      |                      |      |
|      | Master (MTFE = 0)  |            | 100                  | —                    | ns   |
|      | Slave (MTFE = 0)   |            | 100                  | —                    | ns   |
|      | Master (MTFE = 1)  |            | 50                   | —                    | ns   |
|      | Slave (MTFE = 1)   |            | 50                   | —                    | ns   |
| 2    | PCS to SCK Delay <sup>2</sup>  | $t_{CSC}$  | 7                    | —                    | ns   |
| 3    | After SCK Delay <sup>3</sup>   | $t_{ASC}$  | 14                   | —                    | ns   |
| 4    | SCK Duty Cycle   | $t_{SDC}$  | $0.4 \times t_{SCK}$ | $0.6 \times t_{SCK}$ | ns   |
| 5    | Slave Access Time<br>( $\overline{SS}$ active to SOUT valid)                     | $t_A$      | —                    | 25                   | ns   |
| 6    | Slave SOUT Disable Time<br>( $\overline{SS}$ inactive to SOUT High-Z or invalid) | $t_{DIS}$  | —                    | 25                   | ns   |
| 7    | PCSx to $\overline{PCSS}$ time   | $t_{PCSC}$ | 0                    | —                    | ns   |
| 8    | $\overline{PCSS}$ to PCSx time   | $t_{PASC}$ | 0                    | —                    | ns   |
| 9    | Data Setup Time for Inputs   | $t_{SUI}$  |                      |                      |      |
|      | Master (MTFE = 0)  |            | 25                   | —                    | ns   |
|      | Slave  |            | 5                    | —                    | ns   |
|      | Master (MTFE = 1, CPHA = 0) <sup>4</sup>   |            | 10                   | —                    | ns   |
|      | Master (MTFE = 1, CPHA = 1)  |            | 25                   | —                    | ns   |
| 10   | Data Hold Time for Inputs  | $t_{HI}$   |                      |                      |      |
|      | Master (MTFE = 0)  |            | -4                   | —                    | ns   |
|      | Slave  |            | 7                    | —                    | ns   |
|      | Master (MTFE = 1, CPHA = 0) <sup>4</sup>   |            | 12                   | —                    | ns   |
|      | Master (MTFE = 1, CPHA = 1)  |            | -4                   | —                    | ns   |
| 11   | Data Valid (after SCK edge)  | $t_{SUO}$  |                      |                      |      |
|      | Master (MTFE = 0)  |            | —                    | 8                    | ns   |
|      | Slave  |            | —                    | 28                   | ns   |
|      | Master (MTFE = 1, CPHA = 0)  |            | —                    | 15                   | ns   |
|      | Master (MTFE = 1, CPHA = 1)  |            | 8                    | ns                   |      |
| 12   | Data Hold Time for Outputs   | $t_{HO}$   |                      |                      |      |
|      | Master (MTFE = 0)  |            | -7                   | —                    | ns   |
|      | Slave  |            | 2                    | —                    | ns   |
|      | Master (MTFE = 1, CPHA = 0)  |            | 1                    | —                    | ns   |
|      | Master (MTFE = 1, CPHA = 1)  |            | -7                   | —                    | ns   |

<sup>1</sup> 116 MHz timing specified at CL = 50 pF with SRC = 0b11.

<sup>2</sup> The maximum value is programmable in DSPI\_CTARn[PSSCK] and DSPI\_CTARn[CSSCK].

<sup>3</sup> The maximum value is programmable in DSPI\_CTARn[PASC] and DSPI\_CTARn[ASC].

<sup>4</sup> This number is calculated assuming the SMPL\_PT bitfield in DSPI\_MCR is set to 0b10.

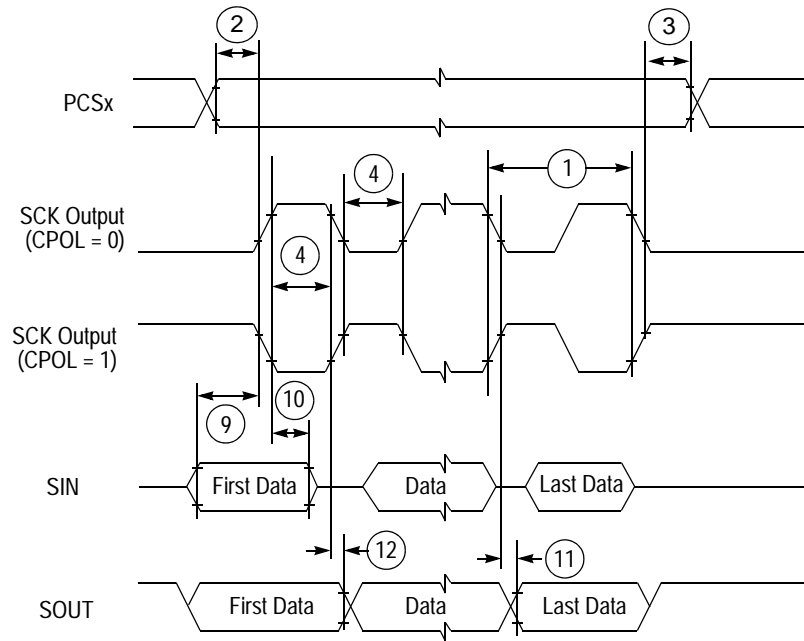


Figure 16. DSPI Classic SPI Timing — Master, CPHA = 0

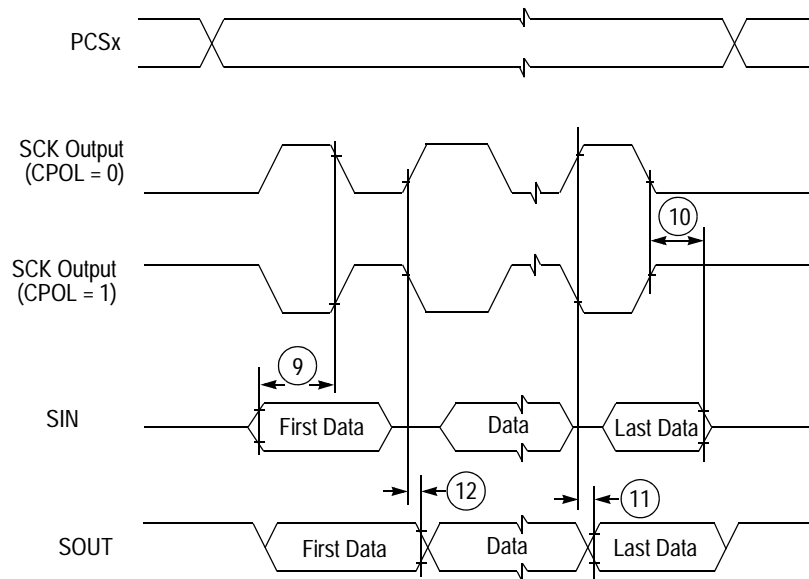


Figure 17. DSPI Classic SPI Timing — Master, CPHA = 1

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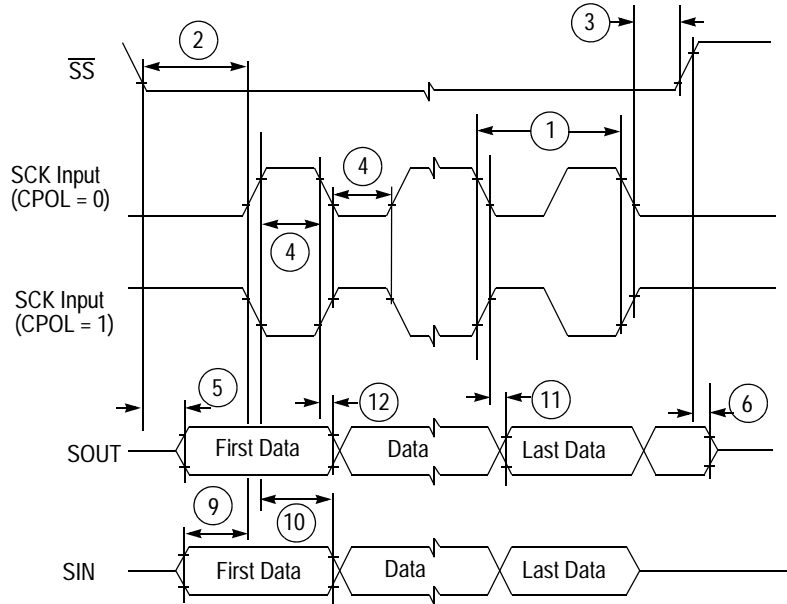


Figure 18. DSPI Classic SPI Timing — Slave, CPHA = 0

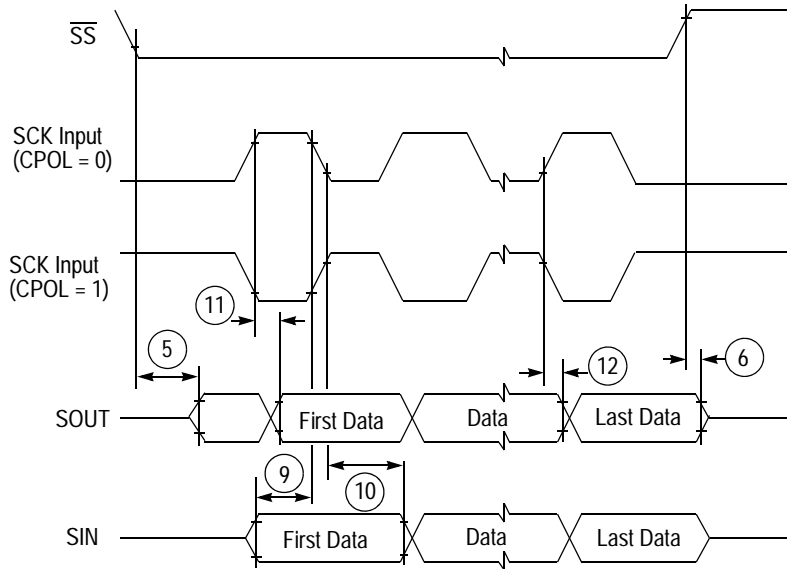


Figure 19. DSPI Classic SPI Timing — Slave, CPHA = 1

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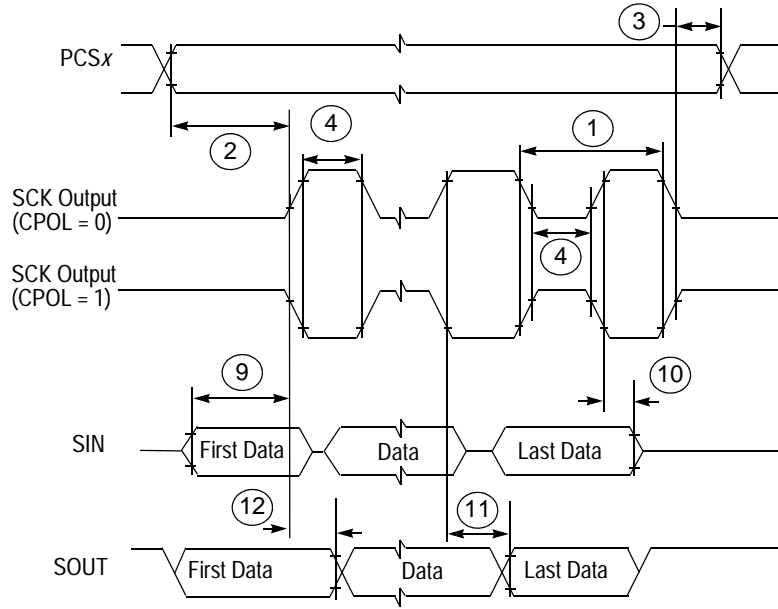


Figure 20. DSPI Modified Transfer Format Timing — Master, CPHA = 0

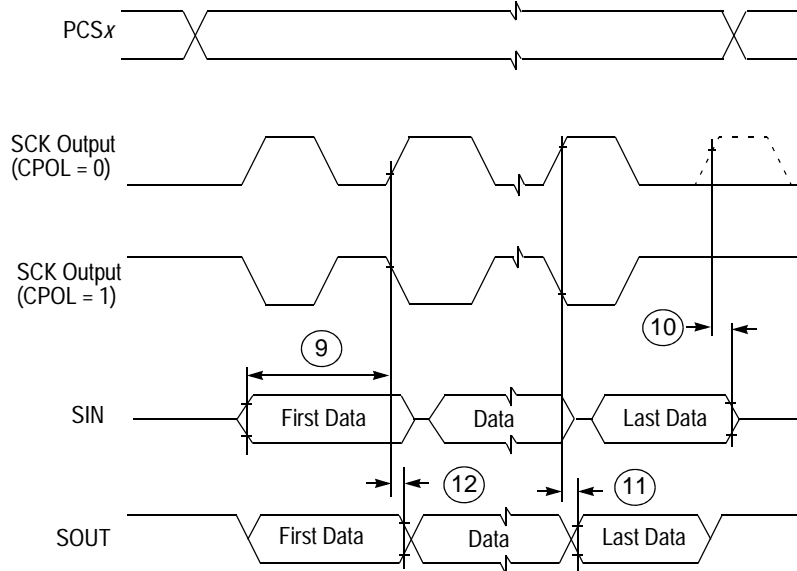


Figure 21. DSPI Modified Transfer Format Timing — Master, CPHA = 1

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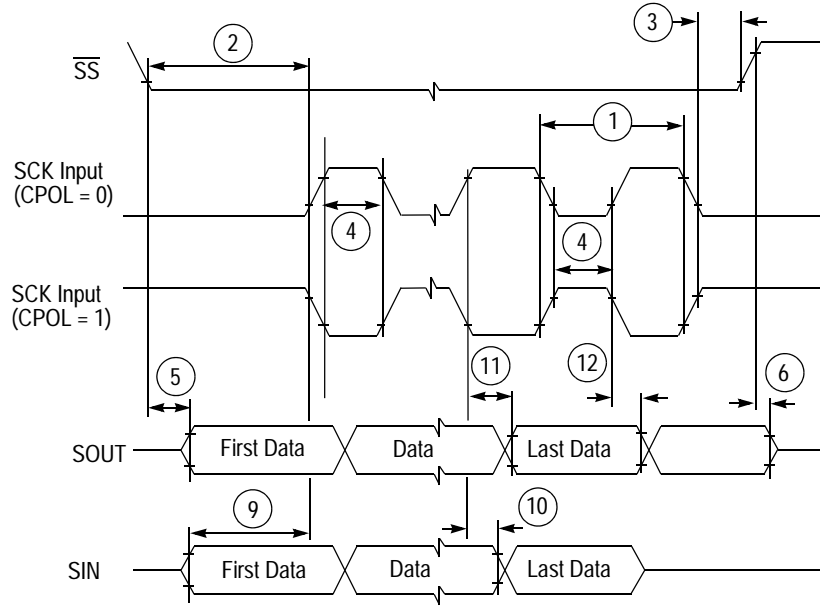


Figure 22. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

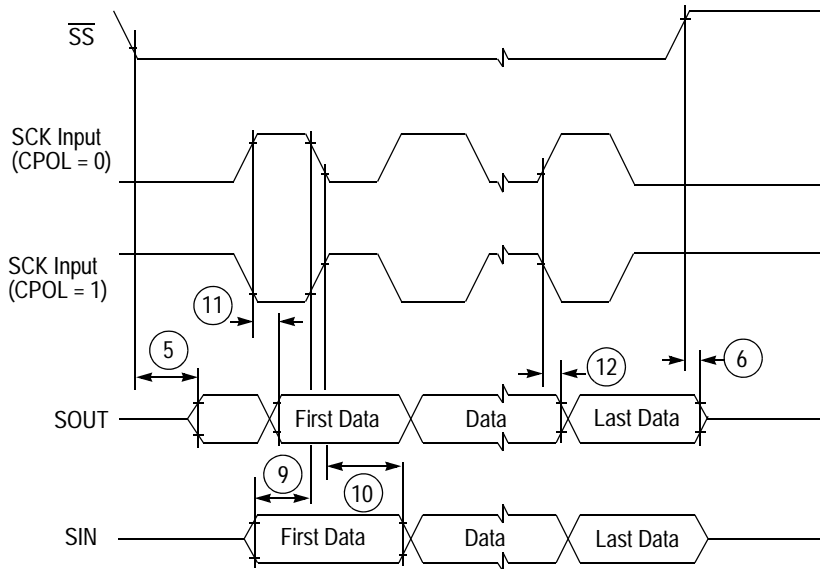


Figure 23. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

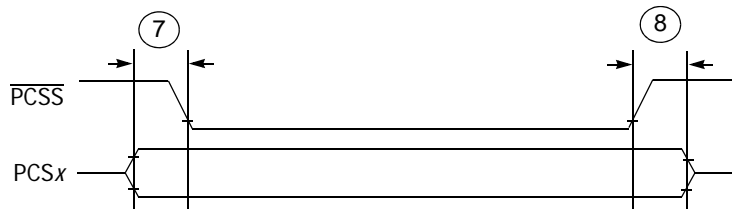


Figure 24. DSPI PCS Strobe ( $\overline{PCSS}$ ) Timing

## 4.14.7 MLB Interface

### 4.14.7.1 Media Local Bus DC Electrical Characteristics

Table 30 provides the DC electrical characteristics for the Media Local Bus interface.

**Table 30. Media Local Bus DC Electrical Characteristics**

| Parameter                   | Symbol   | Min              | Typ | Max     | Unit          | Comments                 |
|-----------------------------|----------|------------------|-----|---------|---------------|--------------------------|
| Maximum Input Voltage       | —        | —                | —   | 3.6     | V             |                          |
| Low Level Input Threshold   | $V_{IL}$ | —                | —   | 0.7     | V             |                          |
| High Level Input Threshold  | $V_{IH}$ | 1.8 <sup>1</sup> | —   | —       | V             |                          |
| Low Level Output Threshold  | $V_{OL}$ | —                | —   | 0.4     | V             | $I_{OL} = 6 \text{ mA}$  |
| High Level Output Threshold | $V_{OH}$ | 2.0              | —   | —       | V             | $I_{OH} = -6 \text{ mA}$ |
| Input Leakage Current       | $I_L$    | —                | —   | $\pm 1$ | $\mu\text{A}$ | $0 < V_{in} < V_{DDE4}$  |

<sup>1</sup> Higher  $V_{IH}$  thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

### 4.14.7.2 Media Local Bus (MLB) AC Electrical Characteristics

Table 31 and Table 32 provide the AC electrical characteristics for the Media Local Bus interface.

**Table 31. MLB Timing for MLB Speed 256 Fs or 512 Fs**

| Spec | Parameter                                   | Symbol      | Min                   | Typ                        | Max                              | Unit   | Comments  |
|------|---|-------------|-----------------------|----------------------------|----------------------------------|--------|---|
| 1    | MLBCLK Operating Frequency <sup>1</sup>     | $f_{mck}$   | 11.264<br>—<br>—<br>— | —<br>12.288<br>24.576<br>— | —<br>—<br>—<br>24.6272<br>25.600 | MHz    | 256 Fs at 44.0 kHz<br>256 Fs at 48.0 kHz<br>512 Fs at 48.0 kHz<br>512 Fs at 48.1 kHz<br>512 Fs PLL unlocked |
| 2    | MLBCLK rise time                            | $t_{mckr}$  | —                     | —                          | 3                                | ns     | $V_{IL}$ to $V_{IH}$  |
| 3    | MLBCLK fall time                            | $t_{mckf}$  | —                     | —                          | 3                                | ns     | $V_{IH}$ to $V_{IL}$  |
| 4    | MLBCLK cycle time                           | $t_{mckc}$  | —                     | 81<br>40                   | —                                | ns     | 256 Fs<br>512 Fs  |
| 5    | MLBCLK low time                             | $t_{mckl}$  | 31.5<br>30            | 37<br>35.5                 | —                                | ns     | 256 Fs<br>256 Fs PLL unlocked   |
|      |   |             | 14.5<br>14            | 17<br>16.5                 | —                                | ns     | 512 Fs<br>512 Fs PLL unlocked   |
| 6    | MLBCLK high time                            | $t_{mckh}$  | 31.5<br>30            | 38<br>36.5                 | —                                | ns     | 256x Fs<br>256 Fs PLL unlocked  |
|      |   |             | 14.5<br>14            | 17<br>16.5                 | —                                | ns     | 512 Fs<br>512 Fs PLL unlocked   |
| 7    | MLBCLK pulse width variation <sup>2</sup>   | $t_{mpwv}$  | —                     | —                          | 2                                | ns p-p |   |
| 8    | MLBSIG/MLBDAT input valid to MLBCLK falling | $t_{dsmcf}$ | 1                     | —                          | —                                | ns     |   |
| 9    | MLBSIG/MLBDAT input hold from MLBCLK low    | $t_{dhmcf}$ | 0                     | —                          | —                                | ns     |   |

## Electrical Characteristics

Table 31. MLB Timing for MLB Speed 256 Fs or 512 Fs (continued)

| Spec | Parameter   | Symbol       | Min | Typ | Max        | Unit | Comments |
|------|---|--------------|-----|-----|------------|------|----------|
| 10   | MLBSIG/MLBDAT output high impedance from MLBCLK low | $t_{mcf dz}$ | 0   | —   | $t_{mckl}$ | ns   |          |
| 11   | Bus Hold time <sup>3</sup>                          | $t_{mdzh}$   | 4   | —   | —          | ns   |          |
| 12   | MLBSIG/MLBDAT output valid from MLBCLK rising       | $t_{mcrdv}$  | —   | —   | 8          | ns   |          |

• Ground = 0.0V  
 • Load Capacitance = 60 pF, SIU\_PCR144–SIU\_PCR146[DSC] = 0b11.  
 • MLB speed of 256 Fs or 512 Fs (Fs = 48 kHz)  
 Unless otherwise noted, all timing parameters are specified from the valid voltage threshold in [Table 30](#).

<sup>1</sup> The Controller can shut off MLBCLK to place MLB in a low-power state.

<sup>2</sup> Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (ns p-p).

<sup>3</sup> The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

Table 32. MLB Timing for MLB Speed 1024 Fs

| Spec | Parameter   | Symbol       | Min                   | Typ                   | Max                         | Unit   | Comments  |
|------|---|--------------|-----------------------|-----------------------|-----------------------------|--------|---|
| 1    | MLBCLK Operating Frequency <sup>1</sup>             | $f_{mck}$    | 45.056<br>—<br>—<br>— | —<br>49.152<br>—<br>— | —<br>—<br>49.2544<br>51.200 | MHz    | 1024 Fs at 44.0 kHz<br>1024 Fs at 48.0 kHz<br>1024 Fs at 48.1 kHz<br>1024 Fs PLL unlocked |
| 2    | MLBCLK rise time                                    | $t_{mckr}$   | —                     | —                     | 1                           | ns     | $V_{IL}$ to $V_{IH}$  |
| 3    | MLBCLK fall time                                    | $t_{mckf}$   | —                     | —                     | 1                           | ns     | $V_{IH}$ to $V_{IL}$  |
| 4    | MLBCLK cycle time                                   | $t_{mckc}$   | —                     | 20.3                  | —                           | ns     | $V_{IL}$ to $V_{IH}$  |
| 5    | MLBCLK low time                                     | $t_{mckl}$   | 6.5<br>6.1            | 7.7<br>7.3            | —                           | ns     | 1024 Fs<br>PLL unlocked   |
| 6    | MLBCLK high time                                    | $t_{mckh}$   | 9.7<br>9.3            | 10.6<br>10.2          | —                           | ns     | 1024 Fs<br>PLL unlocked   |
| 7    | MLBCLK pulse width variation <sup>2</sup>           | $t_{mpwv}$   | —                     | —                     | 0.7                         | ns p-p |   |
| 8    | MLBSIG/MLBDAT input valid to MLBCLK falling         | $t_{dsmcf}$  | 1                     | —                     | —                           | ns     |   |
| 9    | MLBSIG/MLBDAT input hold from MLBCLK low            | $t_{dhmcf}$  | 0                     | —                     | —                           | ns     |   |
| 10   | MLBSIG/MLBDAT output high impedance from MLBCLK low | $t_{mcf dz}$ | 0                     | —                     | $t_{mckl}$                  | ns     |   |
| 11   | Bus Hold time <sup>3</sup>                          | $t_{mdzh}$   | 2                     | —                     | —                           | ns     |   |
| 12   | MLBSIG/MLBDAT output valid from MLBCLK rising       | $t_{mcrdv}$  | —                     | —                     | 7                           | ns     |   |

• Ground = 0.0V  
 • Load Capacitance = 40 pF, SIU\_PCR144–SIU\_PCR146[DSC] = 0b00.  
 • MLB speed = 1024Fs (Fs = 48 kHz)  
 • Unless otherwise noted, timing parameters are specified from the valid voltage threshold in [Table 30](#).



- 1 The Controller can shut off MLBCLK to place MLB in a low-power state.
- 2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (ns p-p).
- 3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

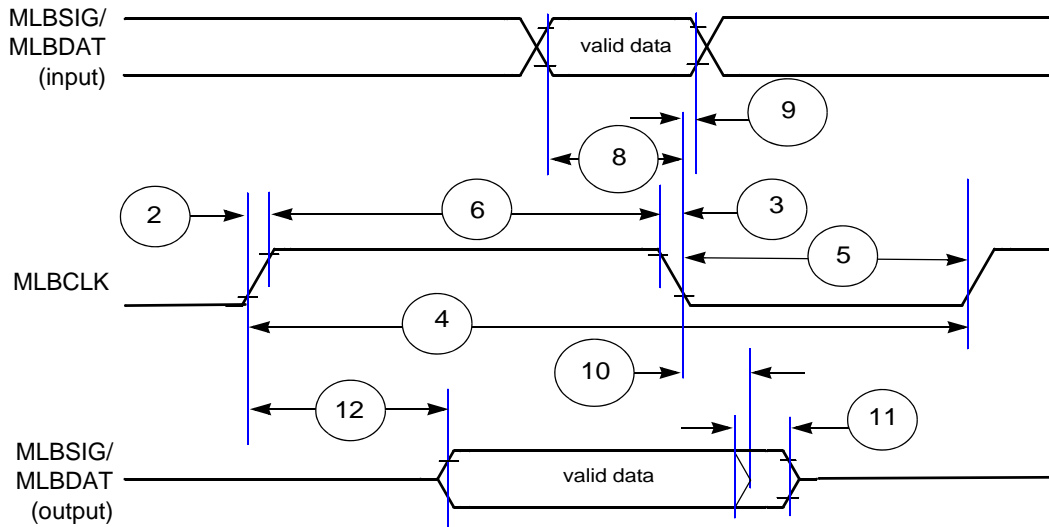


Figure 25. Media Local Bus (MLB) Timing

## 4.14.8 Fast Ethernet Interface

MII signals use CMOS signal levels compatible with devices operating at either 5.0 V or 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

### 4.14.8.1 MII Receive Signal Timing (RXD[3:0], RX\_DV, RX\_ER, and RX\_CLK)

The receiver functions correctly up to a RX\_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX\_CLK frequency.

Table 33. MII Receive Signal Timing

| Spec | Characteristic                         | Min | Max | Unit          |
|------|--|-----|-----|---------------|
| M1   | RXD[3:0], RX_DV, RX_ER to RX_CLK setup | 5   | —   | ns            |
| M2   | RX_CLK to RXD[3:0], RX_DV, RX_ER hold  | 5   | —   | ns            |
| M3   | RX_CLK pulse width high                | 35% | 65% | RX_CLK period |
| M4   | RX_CLK pulse width low                 | 35% | 65% | RX_CLK period |

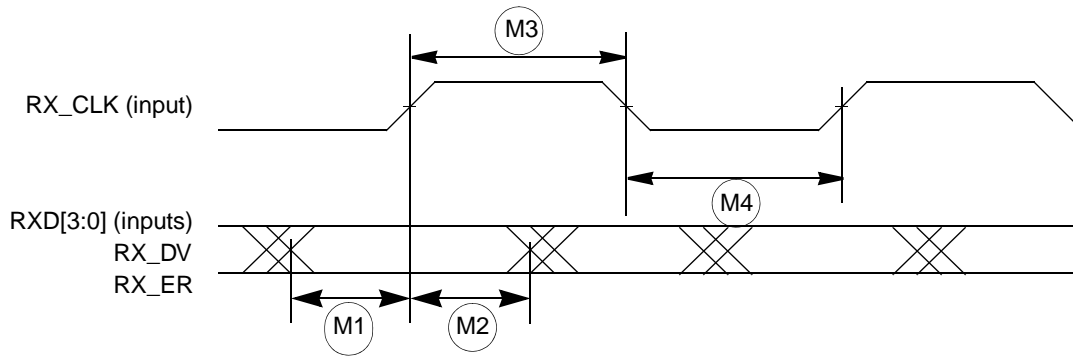


Figure 26. MII Receive Signal Timing Diagram

### 4.14.8.2 MII Transmit Signal Timing (TXD[3:0], TX\_EN, TX\_ER, TX\_CLK)

The transmitter functions correctly up to a TX\_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX\_CLK frequency.

The transmit outputs (TXD[3:0], TX\_EN, TX\_ER) can be programmed to transition from either the rising or falling edge of TX\_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

Table 34. MII Transmit Signal Timing<sup>1</sup>

| Spec | Characteristic                           | Min | Max | Unit          |
|------|--|-----|-----|---------------|
| M5   | TX_CLK to TXD[3:0], TX_EN, TX_ER invalid | 5   | —   | ns            |
| M6   | TX_CLK to TXD[3:0], TX_EN, TX_ER valid   | —   | 25  | ns            |
| M7   | TX_CLK pulse width high                  | 35% | 65% | TX_CLK period |
| M8   | TX_CLK pulse width low                   | 35% | 65% | TX_CLK period |

<sup>1</sup> Output pads configured with SRC = 0b11.

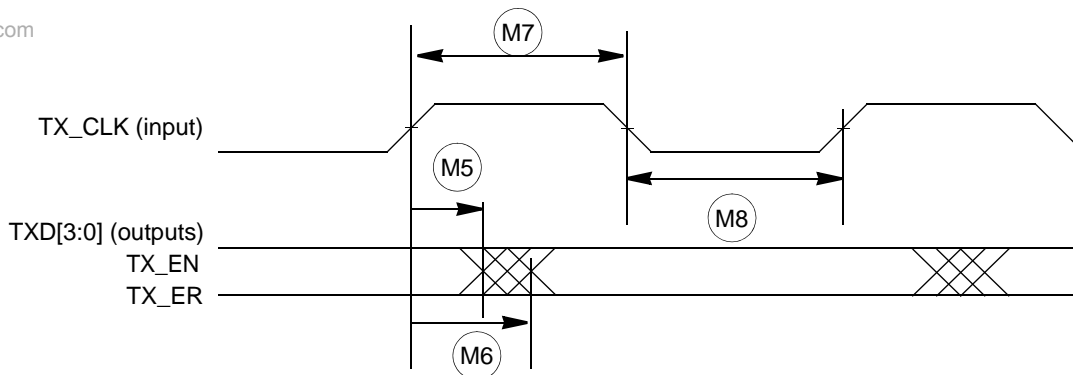


Figure 27. MII Transmit Signal Timing Diagram

### 4.14.8.3 MII Async Inputs Signal Timing (CRS and COL)

Table 35. MII Async Inputs Signal Timing<sup>1</sup>

| Spec | Characteristic               | Min | Max | Unit          |
|------|------------------------------|-----|-----|---------------|
| M9   | CRS, COL minimum pulse width | 1.5 | —   | TX_CLK period |

<sup>1</sup> Output pads configured with SRC = 0b11.

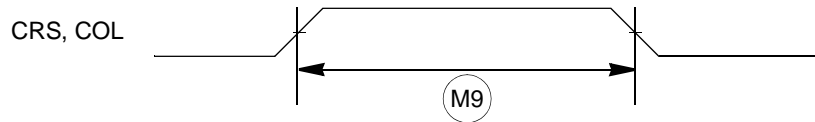


Figure 28. MII Async Inputs Timing Diagram

### 4.14.8.4 MII Serial Management Channel Timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 36. MII Serial Management Channel Timing<sup>1</sup>

| Spec | Characteristic  | Min | Max | Unit       |
|------|---|-----|-----|------------|
| M10  | MDC falling edge to MDIO output invalid (minimum propagation delay) | 0   | —   | ns         |
| M11  | MDC falling edge to MDIO output valid (max prop delay)              | —   | 25  | ns         |
| M12  | MDIO (input) to MDC rising edge setup                               | 10  | —   | ns         |
| M13  | MDIO (input) to MDC rising edge hold                                | 0   | —   | ns         |
| M14  | MDC pulse width high  | 40% | 60% | MDC period |
| M15  | MDC pulse width low   | 40% | 60% | MDC period |

<sup>1</sup> Output pads configured with SRC = 0b11.

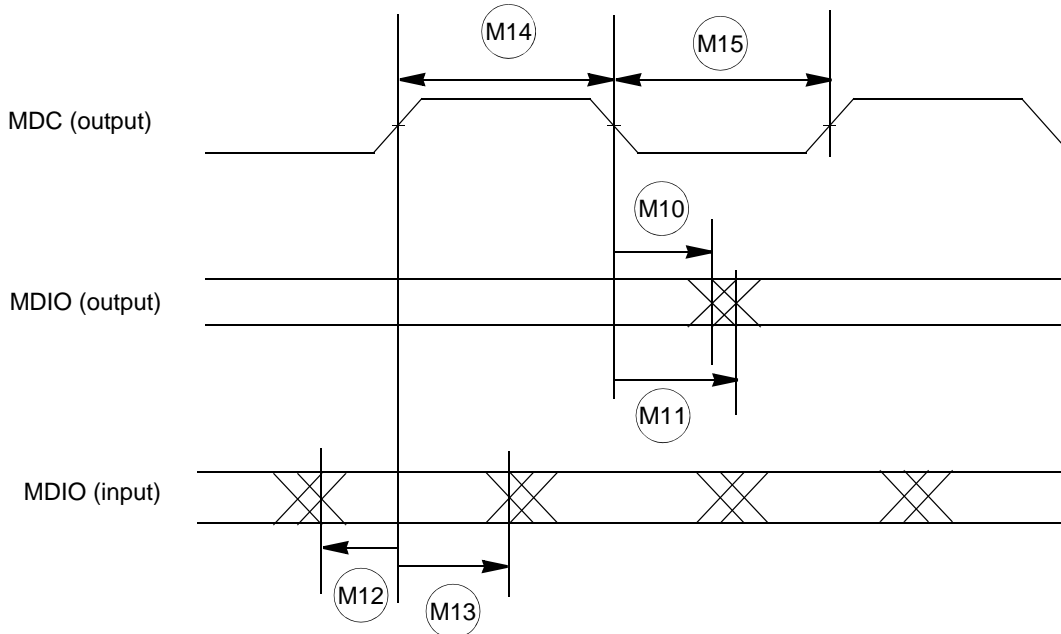


Figure 29. MII Serial Management Channel Timing Diagram

# 5 Package Characteristics

## 5.1 Package Mechanical Data

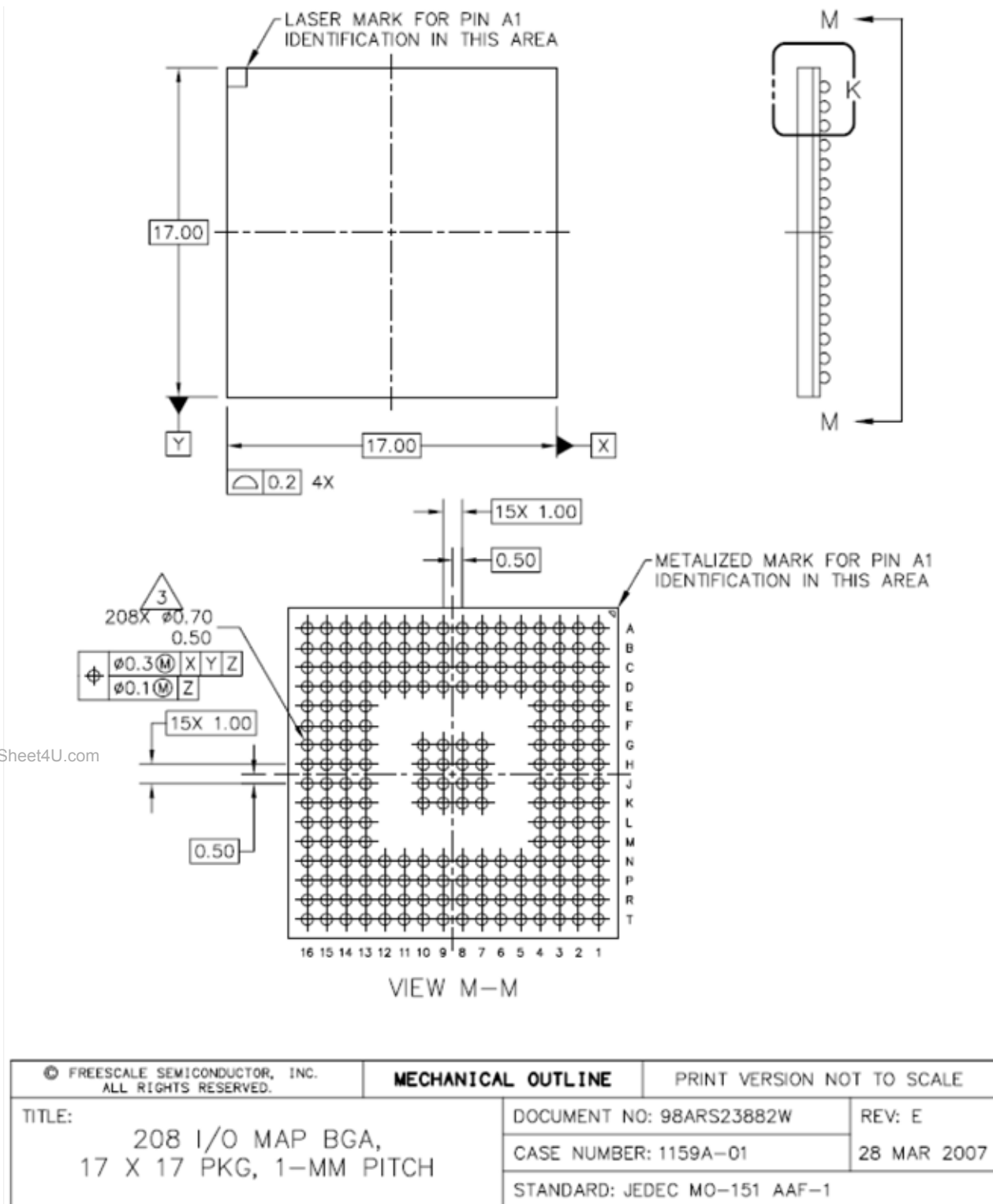
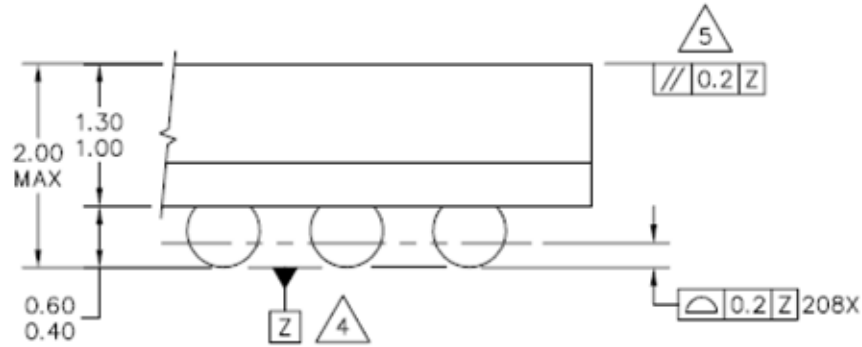


Figure 30. 208 MAPBGA Package Mechanical Drawing

MPC5668x Microcontroller Data Sheet, Rev. 3



DETAIL K  
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. PACKAGE CODE SUMMARY:  
 MAP BGA: 5253  
 MAP BGA PGE DIE: 5371

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|   |  |                              |  |                            |  |
|---|--|------------------------------|--|----------------------------|--|
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| TITLE:<br>208 I/O MAP BGA,<br>17 X 17 PKG, 1-MM PITCH   |  | DOCUMENT NO: 98ARS23882W     |  | REV: E                     |  |
|   |  | CASE NUMBER: 1159A-01        |  | 28 MAR 2007                |  |
|   |  | STANDARD: JEDEC MO-151 AAF-1 |  |                            |  |

Figure 31. 208 MAPBGA Package Detail

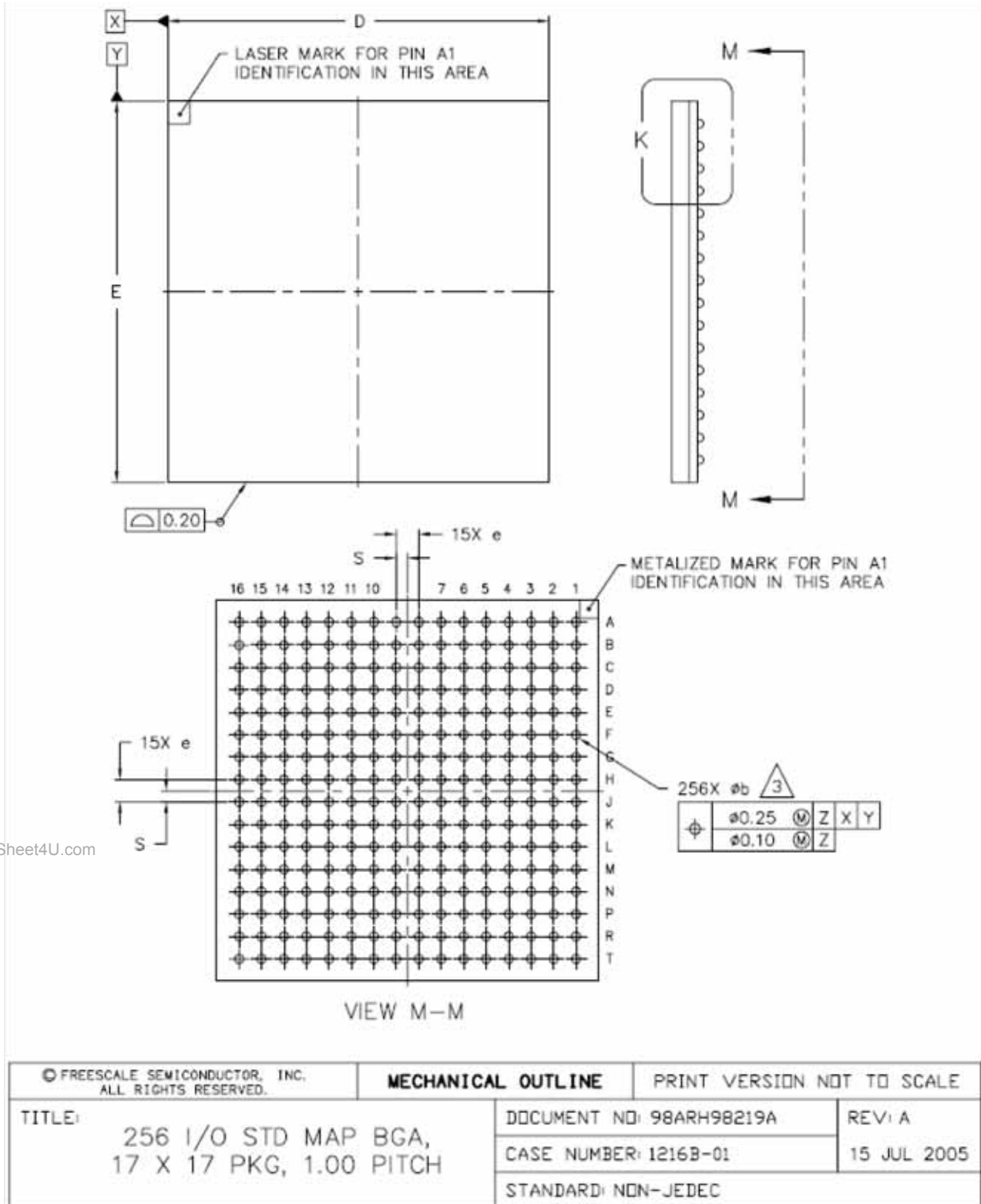
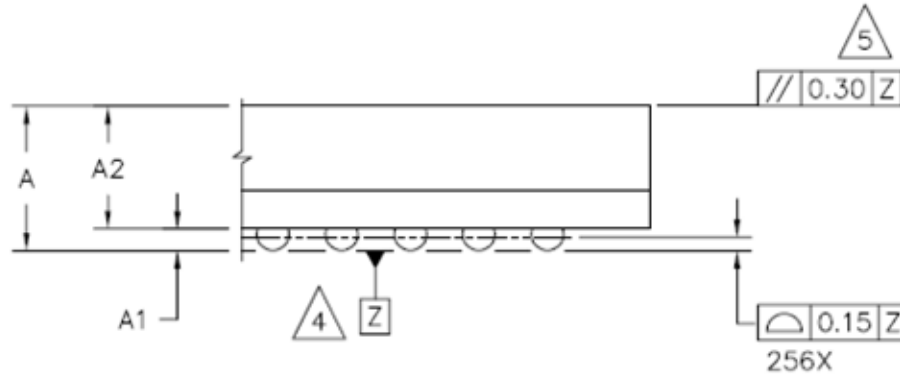


Figure 32. 256 MABGA Package Mechanical Drawing



DETAIL K  
ROTATED 90° CLOCKWISE

| DIM   | MIN       | MAX  | NOTES   |                            |
|---|-----------|------|---|----------------------------|
| A   | 1.25      | 1.60 | 1. DIMENSIONS ARE IN MILLIMETERS.<br>2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.<br>3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.<br>4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.<br>5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE. |                            |
| A1  | 0.27      | 0.47 |   |                            |
| A2  | 1.16 REF  |      |   |                            |
| b   | 0.40      | 0.60 |   |                            |
| D   | 17.00 BSC |      |   |                            |
| E   | 17.00 BSC |      |   |                            |
| e   | 1.00 BSC  |      |   |                            |
| S   | 0.50 BSC  |      |   |                            |
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED. |           |      | <b>MECHANICAL OUTLINE</b>   | PRINT VERSION NOT TO SCALE |
| TITLE: 256 I/O STD MAP BGA,<br>17 X 17 PKG, 1.00 PITCH  |           |      | DOCUMENT NO: 98ARH98219A<br>CASE NUMBER: 1216B-01<br>STANDARD: NON-JEDEC  | REV: A<br>15 JUL 2005      |

Figure 33. 256 MAPBGA Package Detail



## 6 Revision History

Table 37 describes the changes made to this document between revisions.

**Table 37. Revision History**

| Revision | Date           | Description                                    |
|----------|----------------|--|
| 0        | April 2008     | Preliminary release.                           |
| 1        | June 2008      | Initial release: Advance Information.          |
| 2        | Jan 2009       | Release: Advance Information.                  |
| 3        | September 2009 | Release: Advance Information, interim updates. |

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