

**Advance Information**

**MPC7457RXNPNS**  
Rev.2, 10/2003

**MPC7457 Part Number**  
**Specification for the**  
**MPC74x7RXnnnnNx Series**



*Motorola Part  
Numbers Affected:*

*PPC7457RX1000NB*  
*PPC7457RX867NB*  
*PPC7457RX733NB*  
*PPC7457RX600NB*  
*PPC7447RX1000NB*  
*PPC7447RX867NB*  
*MC7447RX1000NB*  
*MC7447RX867NB*  
*MC7447RX733NB*  
*MC7447RX600NB*

This document describes part-number-specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7457 RISC Microprocessor Hardware Specifications* (Order No. MPC7457EC). The MPC7457 and MPC7447 are implementations of the PowerPC™ microprocessor family of reduced instruction set computer (RISC) microprocessors.

Specifications provided in this document supersede those in the *MPC7457 RISC Microprocessor Hardware Specifications*, Rev. 2 or later, for the part numbers listed in Table A only. This document is primarily concerned with the MPC7457; however, unless otherwise noted, all information herein also applies to the MPC7447 part numbers listed in Table A. Specifications not addressed herein are unchanged. Because this document is frequently updated, refer to <http://www.motorola.com/semiconductors> or to your Motorola sales office for the latest version.

Note that headings and table numbers in this document are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification.

Part numbers addressed in this document are listed in Table A.

**Table A. Part Numbers Addressed by this Data Sheet**

Motorola Part Number	Operating Conditions			Significant Differences from Hardware Specification
	CPU Frequency (MHz)	V <sub>DD</sub>	T <sub>j</sub> (°C)	
PPC7457RX1000NB	1000	1.1 V ± 50 mV	0 to 105	Modified core frequency and voltage to reduce power consumption, modified processor bus AC timing.
PPC7447RX1000NB				
MC7447RX1000NB				
PPC7457RX867NB	867			
PPC7447RX867NB				
MC7447RX867NB				
PPC7457RX733NB	733			
MC7447RX733NB				
PPC7457RX600NB	600			
MC7447RX600NB				

**Note:** The P prefix in a Motorola part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

## 1.2 Features

This section summarizes changes to the features of the MPC7457 described in the *MPC7457 RISC Microprocessor Hardware Specifications*.

- Power management
  - 1.1-V processor core

## 1.3 General Parameters

- Core power supply: 1.1 V  $\pm$  50 mV DC nominal

### 1.5.1 DC Electrical Characteristics

Table 4 provides the recommended operating conditions for the MPC7457 part numbers described herein.

**Table 4. Recommended Operating Conditions**

Characteristic	Symbol	Recommended Value	Unit
Core supply voltage	$V_{DD}$	1.1 V $\pm$ 50 mV	V
PLL supply voltage	$AV_{DD}$	1.1 V $\pm$ 50 mV	V

**Note:** These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 7 provides the power consumption for the MPC7457 part numbers described herein.

**Table 7. Power Consumption for MPC7457**

	Processor (CPU) Frequency				Unit	Notes
	600 MHz	733 MHz	867 MHz	1000 MHz		
<b>Full-Power Mode</b>						
Typical	5.3	6.3	7.3	8.3	W	1, 3
Maximum	7.9	9.1	10.3	11.5	W	1, 2
<b>Doze Mode</b>						
Typical	—	—	—	—	W	4
<b>Nap Mode</b>						
Typical	1.3	1.3	1.3	1.3	W	1, 2
<b>Sleep Mode</b>						
Typical	1.2	1.2	1.2	1.2	W	1, 2
<b>Deep Sleep Mode (PLL Disabled)</b>						
Typical	1.1	1.1	1.1	1.1	W	1, 3

**Notes:**

1. These values apply for all valid processor bus and L3 bus ratios. The values do not include I/O supply power ( $OV_{DD}$  and  $GV_{DD}$ ) or PLL supply power ( $AV_{DD}$ ).  $OV_{DD}$  and  $GV_{DD}$  power is system dependent, but is typically <5% of  $V_{DD}$  power. Worst case power consumption for  $AV_{DD}$  < 3 mW.
2. Maximum power is the maximum measured at nominal  $V_{DD}$  and maximum operating junction temperature (see Table 4) while running an entirely cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
3. Typical power is an average value measured at the nominal recommended  $V_{DD}$  (see Table 4) and 65°C while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.
4. Doze mode is not a user-definable state; it is an intermediate state between full-power and either nap or sleep mode. As a result, power consumption for this mode is not tested.

Table 8 provides the clock AC timing specifications for the MPC7457 part numbers described herein.

**Table 8. Clock AC Timing Specifications**

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Maximum Processor Core Frequency								Unit	Notes
		600 MHz		733 MHz		867 MHz		1000 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max		
Processor frequency	$f_{\text{core}}$	500	600	500	733	500	867	500	1000	MHz	1
VCO frequency	$f_{\text{VCO}}$	1000	1200	1000	1466	1000	1733	1000	2000	MHz	1
SYSCLK frequency	$f_{\text{SYSCLK}}$	33	167	33	167	33	167	33	167	MHz	
SYSCLK cycle time	$t_{\text{SYSCLK}}$	6.0	30	6.0	30	6.0	30	6.0	30	ns	

**Note:**

- Caution:** The SYSCLK frequency, PLL\_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL\_CFG[0:4] signal description in Section 1.9.1, "PLL Configuration," for valid PLL\_CFG[0:4] settings.

### 1.5.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7457 part numbers described herein.

**Table 9. Processor Bus AC Timing Specifications <sup>1</sup>**

At recommended operating conditions. See Table 4.

Parameter	Symbol <sup>2</sup>	All Speed Grades		Unit	Notes
		Min	Max		
Input setup times: A[0:35], AP[0:4] D[0:63], DP[0:7] AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], GBL, HIT, TT[0:3], QACK, TA, TBEN, TEA, TS, EXT_QUAL, PMON_IN, SHD[0:1], BMODE[0:1], BMODE[0:1], BVSEL, L3VSEL	t <sub>AVKH</sub> t <sub>DVKH</sub> t <sub>IVKH</sub>  t <sub>MVKH</sub>	2.0 2.0 2.0  2.0	— — —  —	ns	8
Input hold times: A[0:35], AP[0:4] D[0:63], DP[0:7] AACK, ARTRY, BG, CKSTP_IN, DBG, DTI[0:3], GBL, HIT, TT[0:3], QACK, TA, TBEN, TEA, TS, EXT_QUAL, PMON_IN, SHD[0:1] BMODE[0:1], BVSEL, L3VSEL	t <sub>AXKH</sub> t <sub>DXKH</sub> t <sub>IXKH</sub>  t <sub>MXKH</sub>	0 0 0  0	— — —  —	ns	8
Output valid times: A[0:35], AP[0:4] D[0:63], DP[0:7] AACK, ARTRY, BR, CI, CKSTP_IN, DRDY, DTI[0:3], GBL, PMON_OUT, QREQ, TBST, TSIZ[0:2], TT[0:3], TS, SHD[0:1], WT	t <sub>KHAV</sub> t <sub>KHDV</sub> t <sub>KHOV</sub>	— — —	2.0 2.0 2.0	ns	
Output hold times: A[0:35], AP[0:4] D[0:63], DP[0:7] AACK, ARTRY, BR, CI, CKSTP_IN, DRDY, DTI[0:3], GBL, PMON_OUT, QREQ, TBST, TSIZ[0:2], TT[0:3], TS, SHD[0:1], WT	t <sub>KHAX</sub> t <sub>KHDX</sub> t <sub>KHOX</sub>	0.5 0.5 0.5	— — —	ns	
SYSCLK to output enable	t <sub>KHOE</sub>	0.5	—	ns	
SYSCLK to output high impedance (all except TS, ARTRY, SHD0, SHD1)	t <sub>KHOZ</sub>	—	3.5	ns	
SYSCLK to TS high impedance after precharge	t <sub>KHTSPZ</sub>	—	1	t <sub>SYSCLK</sub>	3, 4, 5
Maximum delay to ARTRY/SHD0/SHD1 precharge	t <sub>KHARP</sub>	—	1	t <sub>SYSCLK</sub>	3, 5, 6, 7

**Table 9. Processor Bus AC Timing Specifications <sup>1</sup> (continued)**

At recommended operating conditions. See Table 4.

Parameter	Symbol <sup>2</sup>	All Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}/\overline{\text{SHD0}}/\overline{\text{SHD1}}$ high impedance after precharge	$t_{\text{KHARPZ}}$	—	2	$t_{\text{SYSCLK}}$	3, 5 6, 7

**Notes:**

- All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4 in the *MPC7457 RISC Microprocessor Hardware Specifications*). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- The symbology used for timing specifications herein follows the pattern of  $t_{(\text{signal})(\text{state})(\text{reference})(\text{state})}$  for inputs and  $t_{(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{\text{VKH}}$  symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And  $t_{\text{KHOV}}$  symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
- $t_{\text{SYSCLK}}$  is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
- According to the bus protocol,  $\overline{\text{TS}}$  is driven only by the currently active bus master. It is asserted low then precharged high before returning to high impedance, as shown in Figure 6 in the *MPC7457 RISC Microprocessor Hardware Specifications*. The nominal precharge width for  $\overline{\text{TS}}$  is  $0.5 \times t_{\text{SYSCLK}}$ , that is, less than the minimum  $t_{\text{SYSCLK}}$  period, to ensure that another master asserting  $\overline{\text{TS}}$  on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-impedance behavior is guaranteed by design.
- Guaranteed by design and not tested.
- According to the bus protocol,  $\overline{\text{ARTRY}}$  can be driven by multiple bus masters through the clock period immediately following  $\overline{\text{AACK}}$ . Bus contention is not an issue because any master asserting  $\overline{\text{ARTRY}}$  will be driving it low. Any master asserting it low in the first clock following  $\overline{\text{AACK}}$  will then go to high impedance for one clock before precharging it high during the second cycle after the assertion of  $\overline{\text{AACK}}$ . The nominal precharge width for  $\overline{\text{ARTRY}}$  is  $1.0 t_{\text{SYSCLK}}$ ; that is, it should be high impedance, as shown in Figure 6 in the *MPC7457 RISC Microprocessor Hardware Specifications*, before the first opportunity for another master to assert  $\overline{\text{ARTRY}}$ . Output valid and output hold timing is tested for the signal asserted. The high-impedance behavior is guaranteed by design.
- According to the MPX bus protocol,  $\overline{\text{SHD0}}$  and  $\overline{\text{SHD1}}$  can be driven by multiple bus masters beginning the cycle of  $\overline{\text{TS}}$ . Timing is the same as  $\overline{\text{ARTRY}}$ , that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for  $\overline{\text{SHD0}}$  and  $\overline{\text{SHD1}}$  is  $1.0 t_{\text{SYSCLK}}$ . The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
- $\text{BMODE}[0:1]$  and  $\text{BVSEL}$  are mode select inputs and are sampled before and after  $\overline{\text{HRESET}}$  negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. These inputs must remain stable after the second sample. See Figure 5 in the *MPC7457 RISC Microprocessor Hardware Specifications* for sample timing.

### 1.5.2.3 L3 Clock AC Specifications

Devices described by this part number specification conform to the L3 clock AC timing specifications provided in the *MPC7457 RISC Microprocessor Hardware Specifications*. Refer to the hardware specifications for additional information.

### 1.5.2.4 L3 Bus AC Specifications

Devices described by this part number specification conform to the L3 clock AC timing specifications provided in the *MPC7457 RISC Microprocessor Hardware Specifications*. Refer to the hardware specifications for additional information.



## 1.11 Ordering Information

### 1.11.1 Part Numbers Addressed by This Specification

Table 22 provides the ordering information for the MPC7457 parts described in this document.

Table 22. Part Marking Nomenclature

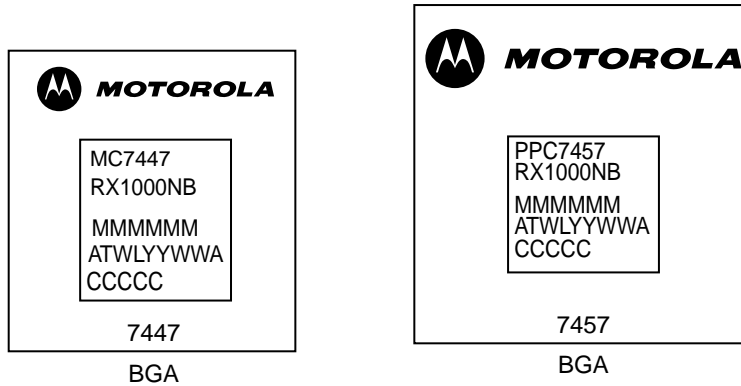
<i>xxx</i>	<i>74x7</i>	<i>RX</i>	<i>nnnn</i>	<i>x</i>	<i>x</i>
Product Code	Part Identifier	Package	Processor Frequency <sup>1</sup>	Application Modifier	Revision Level
PPC <sup>2</sup>	7457	RX = CBGA	1000	N: 1.1 V ± 50 mV 0° to 105°C	B: 1.1: PVR = 8002 0101
			867		
			733		
			600		
	7447		1000		
	867				
	MC		7447		
		867			
		733			
		600			

**Notes:**

1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by other specifications may support other maximum core frequencies.
2. The P prefix in a Motorola part number designates a "Pilot Production Prototype" as defined by Motorola SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

### 1.11.3 Part Marking

Parts are marked as the example shown in Figure 29.



**Notes:**

MMMMMM is the 6-digit mask number.

ATWLYYWWA is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

**Figure 29. Motorola Part Marking for BGA Devices**

# Document Revision History

Table B provides a revision history for this part number specification.

**Table B. Document Revision History**

Rev. No.	Substantive Change(s)
0	Initial release.
0.1	Edited introductory paragraphs to clarify which part numbers are affected by this specification.
1	Corrected product code in part numbers on page 1 and in Table A.
	Updated power consumption specifications in Table 7.
	Corrected product code in Section 1.11 and Table 21.
2	Added "MC7447..." part numbers to reflect qualification status.
	Table 8: Increased maximum system bus frequency ( $f_{SYSCLK}$ ) to 167 MHz.
	Table 9: Corrected numerous errors in lists of pins associated with $t_{KH0V}$ , $t_{KH0X}$ , $t_{IVKH}$ , and $t_{IXKH}$ . Updated (improved) AC timing parameters based on latest characterization data.
	Added 867, 733, and 600 MHz speed grades.
	Removed Tables 10, 13, and 14: devices described by this specification conform to the AC timing found in the MPC7457 hardware specifications.
	Corrected typo in Figure 29: 7447 device was incorrectly marked...RX1000NB.

# Freescale Semiconductor, Inc.

## HOW TO REACH US:

### USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution  
P.O. Box 5405, Denver, Colorado 80217  
1-480-768-2130  
(800) 521-6274

### JAPAN:

Motorola Japan Ltd.  
SPS, Technical Information Center  
3-20-1, Minami-Azabu Minato-ku  
Tokyo 106-8573 Japan  
81-3-3440-3569

### ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.  
Silicon Harbour Centre, 2 Dai King Street  
Tai Po Industrial Estate, Tai Po, N.T., Hong Kong  
852-26668334

### TECHNICAL INFORMATION CENTER:

(800) 521-6274

### HOME PAGE:

[www.motorola.com/semiconductors](http://www.motorola.com/semiconductors)

Information in this document is provided solely to enable system and software implementers to use Motorola products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein.

Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.



Motorola and the Stylized M Logo are registered in the U.S. Patent and Trademark Office. digital dna is a trademark of Motorola, Inc. The described product is a PowerPC microprocessor. The PowerPC name is a trademark of IBM Corp. and used under license. All other product or service names are the property of their respective owners. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

© Motorola, Inc. 2003

MPC7457RXNXPNS

**For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)**