800MHz Low Voltage PECL Clock Synthesizer **MPC9230**

DATA SHEET

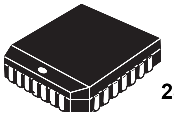
The MPC9230 is a 3.3 V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 50 MHz to 800 MHz(1) and the support of differential PECL output signals the device meets the needs of the most demanding clock applications.

Features

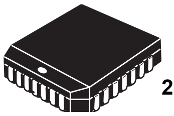
- 50 MHz to 800 MHz(1) synthesized clock output signal
- Differential PECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference clock input
- 3.3 V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 32-lead LQFP and 28-lead PLCC packaging
- 32-lead and 28-lead Pb-free package available
- SiGe Technology
- Ambient temperature range -40°C to +85°C
- Pin and function compatible to the MC12430

MPC9230

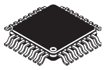
800 MHz LOW VOLTAGE CLOCK SYNTHESIZER



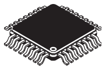
FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776-02



EI SUFFIX
28-LEAD PLCC PACKAGE
Pb-FREE PACKAGE
CASE 776-02



FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-04



AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-04

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator is divided by 16 and then multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1600 MHz.(1) Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL}, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be M/4 times the external input reference frequency. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1600 MHz(1)). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50 Ω to V_{CC} – 2.0 V. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the $\overline{\text{P\_LOAD}}$ input LOW until power becomes valid. On the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs and prevent the LVCMOS compatible control inputs from floating.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output.

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1. The VCO frequency range of 800–1600 MHz is available at an ambient temperature range of 0 to 70°C. At –40 to +85°C, the VCO frequency (output frequency) is limited to max. 1500 MHz (750 MHz).

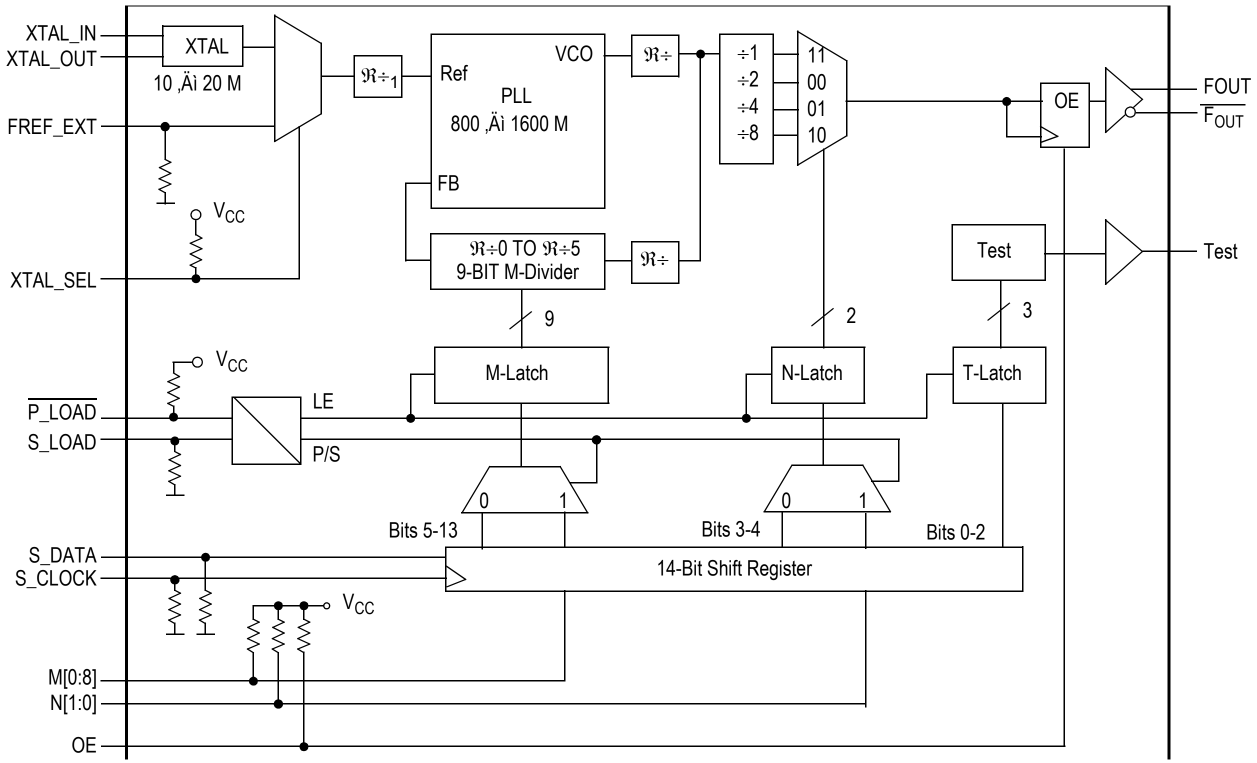


Figure 1. MPC9230 Logic Diagram

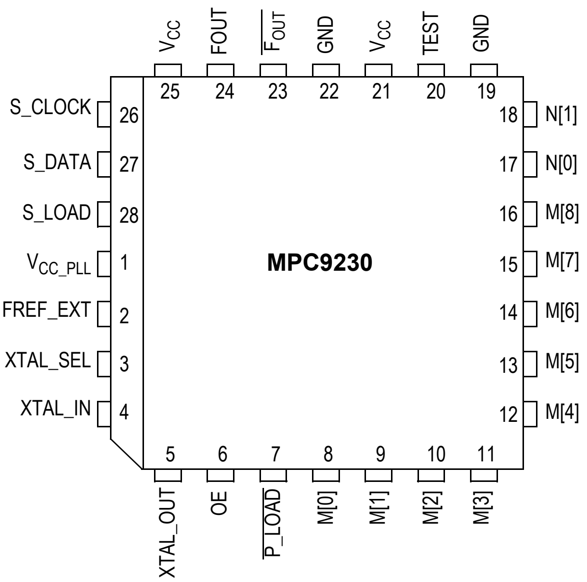


Figure 2. MPC9230 28-Lead PLCC Pinout
(Top View)

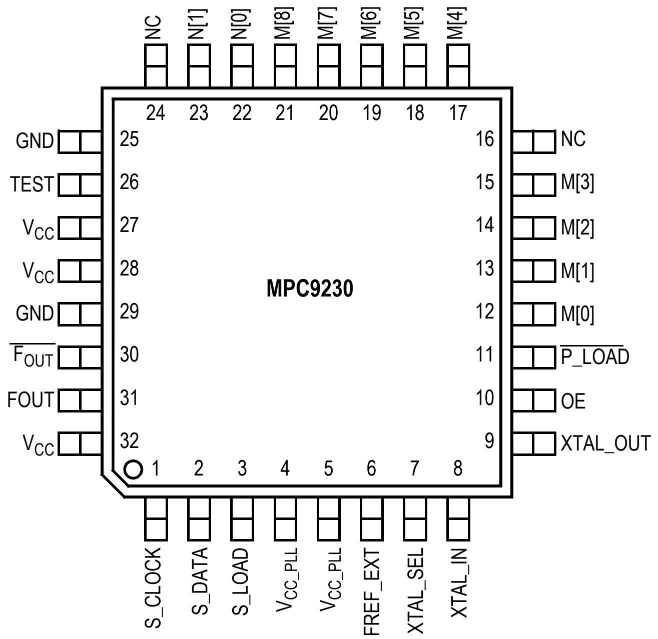


Figure 3. MPC9230 32-Lead Package Pinout
(Top View)

Table 1. Pin Configurations

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface
FREF_EXT	Input	0	LVCMOS	Alternative PLL reference input
F_{OUT}, F_{OUT}	Output		LVPECL	Differential clock output
TEST	Output		LVPECL	Test and device diagnosis output
XTAL_SEL	Input	1	LVCMOS	PLL reference select input
S_LOAD	Input	0	LVCMOS	Serial configuration control input This input controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
P_LOAD	Input	1	LVCMOS	Parallel configuration control input. This input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of P_LOAD. P_LOAD is state sensitive.
S_DATA	Input	0	LVCMOS	Serial configuration data input
S_CLOCK	Input	0	LVCMOS	Serial configuration clock input
M[0:8]	Input	1	LVCMOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of P_LOAD
N[1:0]	Input	1	LVCMOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of P_LOAD
OE	Input	1	LVCMOS	Output enable (active high) The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the F_{OUT} output
GND	Supply		Ground	Negative power supply (GND)
V_{CC}	Supply		V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation
V_{CC_PLL}	Supply		V_{CC}	PLL positive power supply (analog power supply)

Table 2. Output Frequency Range and PLL Post-Divider N

N		Output Division	Output Frequency Range for T_A = 0°C to +70°C	Output Frequency Range for T_A = –40°C to +85°C
1	**0**			
0	0	2	200 – 400 MHz	200 – 375 MHz
0	1	4	100 – 200 MHz	100 – 187.5 MHz
1	0	8	50 – 100 MHz	50 – 93.75 MHz
1	1	1	400 – 800 MHz	400 – 750 MHz

Table 3. Function Table

Input	0	1
XTAL_SEL	FREF_EXT	XTAL interface
OE	Outputs disabled. F_{OUT} is stopped in the logic low state (F_{OUT} = L, F_{OUT} = H)	Outputs enabled

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} - 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 5. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	4.6	V	
V_{IN}	DC Input Voltage	–0.3	$V_{CC} + 0.3$	V	
V_{OUT}	DC Output Voltage	–0.3	$V_{CC} + 0.3$	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs (FREF_EXT, XTAL_SEL, $\overline{\text{P\_LOAD}}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1]. OE)						
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current(1)			±200	μA	$V_{IN} = V_{CC}$ or GND
Differential Clock Output F_{OUT}(2)						
V_{OH}	Output High Voltage	V_{CC}–1.02		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage	V_{CC}–1.95		V_{CC}–1.60	V	LVPECL
Test and Diagnosis Output TEST						
V_{OH}	Output High Voltage	V_{CC}–1.02		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage	V_{CC}–1.95		V_{CC}–1.60	V	LVPECL
Supply Current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current			110	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50 Ω to $V_{TT} = V_{CC} - 2$ V.

Table 7. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs (FREF_EXT, XTAL_SEL, $\overline{\text{P\_LOAD}}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1]. OE)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current(1)			±200	μA	$V_{IN} = V_{CC}$ or GND
Differential Clock Output F_{OUT}(2)						
V_{OH}	Output High Voltage	V_{CC}–1.1		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage	V_{CC}–1.95		V_{CC}–1.65	V	LVPECL
Test and Diagnosis Output TEST						
V_{OH}	Output High Voltage	V_{CC}–1.1		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage	V_{CC}–1.95		V_{CC}–1.65	V	LVPECL
Supply Current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current			110	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50 Ω to $V_{TT} = V_{CC}$ – 2 V.

Table 8. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)**(1)**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal Interface Frequency Range	10		20	MHz	
f_{REF}	FREF_EXT Reference Frequency Range	10		$(f_{VCO,MAX} \div M) \cdot 4$(2)	MHz	
f_{VCO}	VCO Frequency Range(3)	800		1600	MHz	
f_{MAX}	Output Frequency N = 11 (÷1)	400		800	MHz	
	N = 00 (÷2)	200		400	MHz	
	N = 01 (÷4)	100		200	MHz	
	N = 10 (÷8)	50		100	MHz	
f_{S_CLOCK}	Serial Interface Programming Clock Frequency(4)	0		10	MHz	
$t_{P,MIN}$	Minimum Pulse Width (S_LOAD, $\overline{\text{P\_LOAD}}$)	50			ns	
DC	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.05		0.3	ns	20% to 80%
t_S	Setup Time S_DATA to S_CLOCK	20			ns	
	S_CLOCK to S_LOAD	20			ns	
	M, N to $\overline{\text{P\_LOAD}}$	20			ns	
t_H	Hold Time S_DATA to S_CLOCK	20			ns	
	M, N to $\overline{\text{P\_LOAD}}$	20			ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter N = 11 (÷1)		30	80	ps	
	N = 00 (÷2)		35	90	ps	
	N = 01 (÷4)		45	130	ps	
	N = 10 (÷8)		55	160	ps	
$t_{JIT(PER)}$	Period Jitter N = 11 (÷1)		20	60	ps	
	N = 00 (÷2)		25	70	ps	
	N = 01 (÷4)		35	120	ps	
	N = 10 (÷8)		50	140	ps	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. The maximum frequency on FREF_EXT is a function of the max. VCO frequency and the M counter. M should be higher than 160 for stable PLL operation.
3. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot M \div 4$.
4. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See APPLICATIONS INFORMATION for more details.

Table 9. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40°C to +85°C)**(1)**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal Interface Frequency Range	10		20	MHz	
f_{REF}	FREF_EXT Reference Frequency Range	10		$(f_{VCO,MAX} \div M) \cdot 4$(2)	MHz	
f_{VCO}	VCO Frequency Range(3)	800		1500	MHz	
f_{MAX}	Output Frequency N = 11 (÷1) N = 00 (÷2) N = 01 (÷4) N = 10 (÷8)	400 200 100 50		750.00 375.00 187.50 93.75	MHz MHz MHz MHz	
f_{S_CLOCK}	Serial Interface Programming Clock Frequency(4)	0		10	MHz	
$t_{P,MIN}$	Minimum Pulse Width (S_LOAD, $\overline{\text{P\_LOAD}}$)	50			ns	
DC	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.05		0.3	ns	20% to 80%
t_S	Setup Time S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to $\overline{\text{P\_LOAD}}$	20 20 20			ns ns ns	
t_H	Hold Time S_DATA to S_CLOCK M, N to $\overline{\text{P\_LOAD}}$	20 20			ns ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter N = 11 (÷1) N = 00 (÷2) N = 01 (÷4) N = 10 (÷8)		30 35 45 55	80 90 130 160	ps ps ps ps	
$t_{JIT(CC)}$	Period Jitter N = 11 (÷1) N = 00 (÷2) N = 01 (÷4) N = 10 (÷8)		20 25 35 50	60 70 120 140	ps ps ps ps	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to $V_{TT.}$
2. The maximum frequency on FREF_EXT is a function of the max. VCO frequency and the M counter. M should be higher than 160 for stable PLL operation.
3. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot M \div 4$.
4. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See APPLICATIONS INFORMATION for more details.

PROGRAMMING INTERFACE

Programming the MPC9230

Programming the MPC9230 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$F_{OUT} = (f_{XTAL} \div 16) \cdot (4 \cdot M) \div (2 \cdot N) \text{ or} \qquad (1)$$

$$F_{OUT} = (f_{XTAL} \div 8) \cdot M \div N \qquad (2)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback- divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to match the VCO frequency range of 800 to 1600 MHz in order to achieve stable PLL operation:

$$M_{MIN} = 4 \cdot f_{VCO,MIN} \div f_{XTAL} \text{ and} \qquad (3)$$

$$M_{MAX} = 4 \cdot f_{VCO,MAX} \div f_{XTAL} \qquad (4)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M = 200 and M = 400. Table 10 shows the usable VCO frequency and M divider range for other example input frequencies. Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$$F_{OUT} = 2 \cdot M \div N \qquad (5)$$

Table 10. MPC9230 Frequency Operating Range

		VCO frequency for an crystal interface frequency of [MHz]						Output frequency for f_{XTAL}=16 MHz and for N =			
M	**M[8:0]**	**10**	**12**	**14**	**16**	**18**	**20**	**1**	**2**	**4**	**8**
160	010100000						800				
170	010101010						850				
180	010110100					810	900				
190	010111110					855	950				
200	011001000				800	900	1000	400	200	100	50
210	011010010				840	945	1050	420	210	105	52.5
220	011011100				880	990	1100	440	220	110	55
230	011100110			805	920	1035	1150	460	230	115	57.5
240	011110000			840	960	1080	1200	480	240	120	60
250	011111010			875	100	1125	1250	500	250	125	62.5
260	100000100			910	1040	1170	1300	520	260	130	65
270	100001110		810	945	1080	1215	1350	540	270	135	67.5
280	100011000		840	980	1120	1260	1400	560	280	140	70
290	100100010		870	1015	1160	1305	1450	580	290	145	72.5
300	100101100		900	1050	1200	1350	1500	600	300	150	75
310	100110110		930	1085	1240	1395	1550(1)	620	310	155	77.5
320	101000000	800	960	1120	1280	1440	1600(1)	640	320	160	80
330	101001010	825	990	1155	1320	1485		660	330	165	82.5
340	101010100	850	1020	1190	1360	1530(1)		680	340	170	85
350	101011110	875	1050	1225	1400	1575(1)		700	350	175	87.5
360	101101000	900	1080	1260	1440			720	360	180	90
370	101110010	925	1110	1295	1480			740	370	185	92.5
380	101111100	950	1140	1330	1520(1)			760(2)	380(2)	190(2)	95(2)
390	110000110	975	1170	1365	1560(1)			780(2)	390(2)	195(2)	97.5(2)
400	110010000	1000	1200	1400	1600(1)			800(2)	400(2)	200(2)	100(2)
410	110011010	1025	1230	1435							
420	110100100	1050	1260	1470							
430	110101110	1075	1290	1505(1)							
440	110111000	1100	1320	1540(1)							
450	111000010	1125	1350	1575(1)							

1. This VCO frequency is only available at the 0°C to +70°C temperature range.
2. This output frequency is only available at the 0°C to +70°C temperature range.

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 11. Output Frequency Range for f_{XTAL} = 16 MHz

N			F_{OUT}	Output Frequency Range for T_A = 0°C to 70°C	Output Frequency Range for T_A = –40°C to 85°C	F_{OUT} Step
1	0	Value				
0	0	2	M	200 – 400 MHz	200 – 375 MHz	1 MHz
0	1	4	M÷2	100 – 200 MHz	100 – 187.5 MHz	500 kHz
1	0	8	M÷4	50 – 100 MHz	50 – 93.75 MHz	250 kHz
1	1	1	2 · M	400 – 800 MHz	400 – 750 MHz	2 MHz

Example Frequency Calculation for an 16 MHz Input Frequency

If an output frequency of 131 MHz was desired, the following steps would be taken to identify the appropriate M and N values. According to Table 11, 131 MHz falls in the frequency set by a value of 4, so N[1:0] = 01. For N = 4, the output frequency is F_{OUT} = M ÷ 2 and M = F_{OUT} x 2. Therefore M = 2 x 131 = 262, so M[8:0] = 010000011. Following this procedure a user can generate any whole frequency between 50 MHz and 800 MHz. Note than for N > 2 fractional values of can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to:

$$f_{STEP} = f_{XTAL} \div 8 \div N$$

APPLICATIONS INFORMATION

Using the Parallel and Serial Interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{\text{P\_LOAD}}$ signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the $\overline{\text{P\_LOAD}}$ signal is LOW, the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the F_{OUT} output pair. To use the serial port, the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the $\overline{\text{P\_LOAD}}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MPC9230 synthesizer. M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the Test and Diagnosis Output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents F_{OUT}, the LVPECL compatible TEST output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis. The T2, T1 and T0 control bits are preset to '000' when $\overline{\text{P\_LOAD}}$ is LOW so that the LVPECL compatible F_{OUT} outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin. Most of the signals available on the TEST output pin are useful only for performance verification of the MPC9230 itself; however, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC9230 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the F_{OUT} differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving F_{OUT} directly gives the user more control on the test clocks sent through the clock tree. Table 12 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level, the input frequency is limited to 200 MHz. This means the fastest the F_{OUT} pin can be toggled via the S_CLOCK is 50 MHz as the divide ratio of the Post-PLL divider is 4 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 12. Test and Debug Configuration for TEST

T[2:0]			TEST Output
T2	T1	T0	
0	0	0	14-bit shift register out[1]
0	0	1	Logic 1
0	1	0	f_{XTAL} ÷ 16
0	1	1	M-Counter out
1	0	0	F_{OUT}
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	F_{OUT} ÷ 4

1. Clocked out at this rate of S_CLOCK.

Table 13. Debug Configuration for PLL Bypass[1]

Output	Configuration
F_{OUT}	S_CLOCK ÷ N
TEST	M-Counter out[2]

1. T[2:0]=110. AC specifications do not apply in PLL bypass mode.
2. Clocked out at the rate of S_CLOCK÷(2·N).

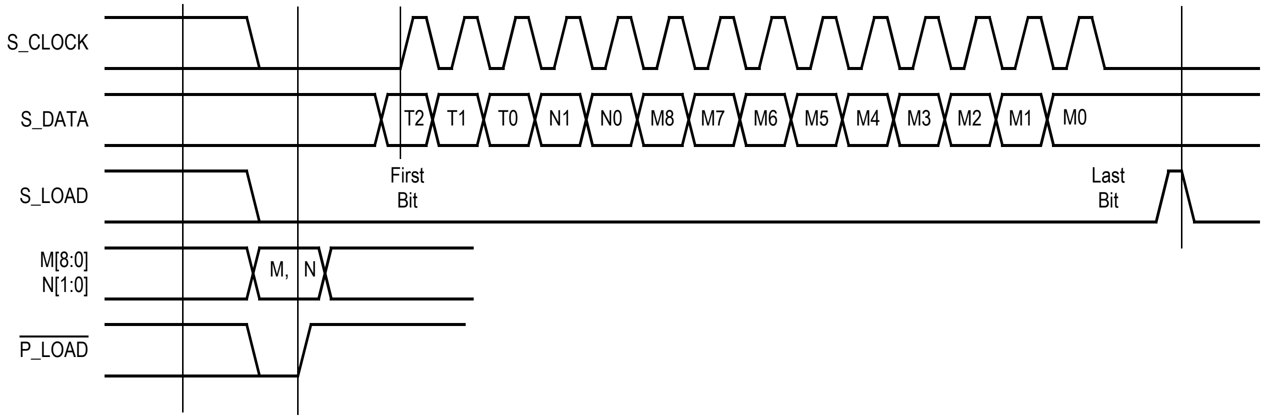


Figure 4. Serial Interface Timing Diagram

Power Supply Filtering

The MPC9230 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} pin impacts the device characteristics. The MPC9230 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient; however, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9230. Figure 5 illustrates a typical power supply filter scheme. The MPC9230 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the MPC9230 pin of the MPC9230. From the data sheet, the V_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is maximum 20 mA, assuming that a minimum of 2.835 V must be maintained on the V_{CC_PLL} pin. The resistor shown in Figure 5 must have a resistance of 10–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 µH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the V_{CC_PLL} pin, a low DC resistance inductor is required (less than 15 Ω).

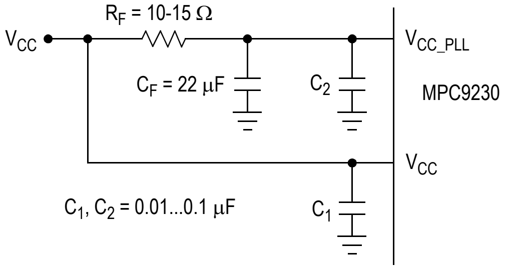


Figure 5. V_{CC_PLL} Power Supply Filter

Layout Recommendations

The MPC9230 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MPC9230. There exists many different potential board layouts, and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC9230 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not reintroduce all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided, and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit, and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal, as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Although the MPC9230 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

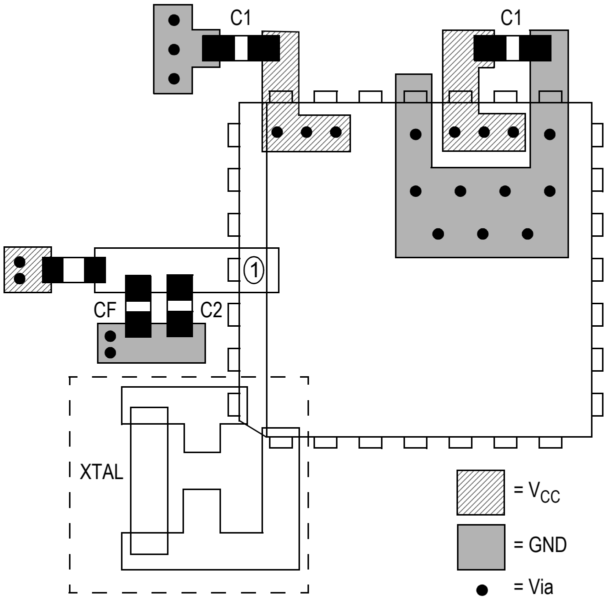


Figure 6. PCB Board Layout Recommendation for the PLCC28 Package

Using the On-Board Crystal Oscillator

The MPC9230 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on-chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the MPC9230 as possible to avoid any board level parasitics. To facilitate co-location, surface mount crystals are recommended but not required. Because the series resonant design is affected by capacitive loading on the XTAL terminals, loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance, it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required, it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1 KΩ.

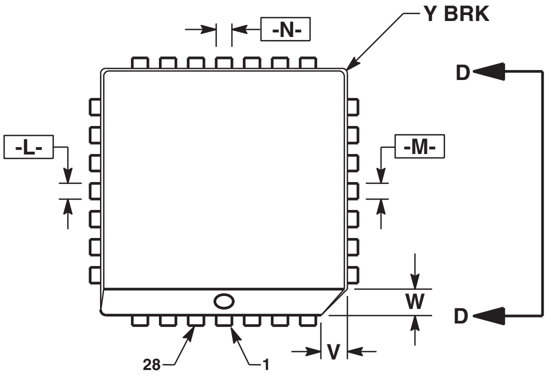
The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately, most crystals are characterized in a parallel resonant mode. Fortunately, there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result, a parallel resonant crystal can be used with the MPC9230 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified; a few hundred ppm translates to kHz inaccuracies. In a general, computer application at this level of inaccuracy is immaterial. Table 14 below specifies the performance requirements of the crystals to be used with the MPC9230.

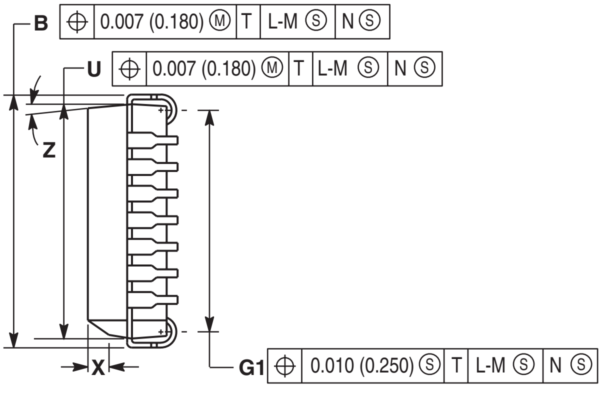
Table 14. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance(1)
Frequency Tolerance	±75 ppm at 25°C
Frequency/Temperature Stability	±150 pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7 pF
Equivalent Series Resistance (ESR)	50 to 80 Ω
Correlation Drive Level	100 μΩ
Aging	5 ppm/Yr (First 3 Years)

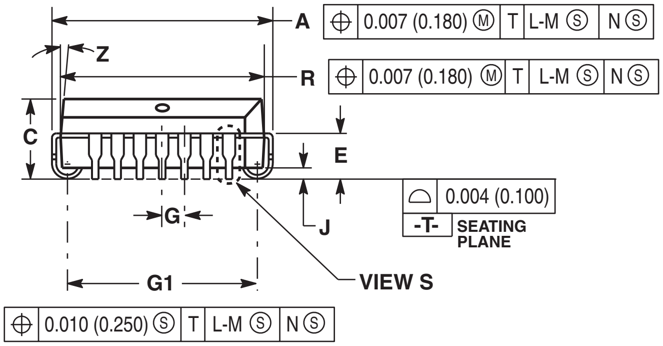
1. See accompanying text for series versus parallel resonant discussion.

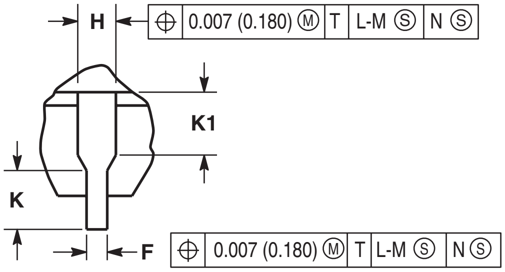
PACKAGE DIMENSIONS





VIEW D-D





VIEW S

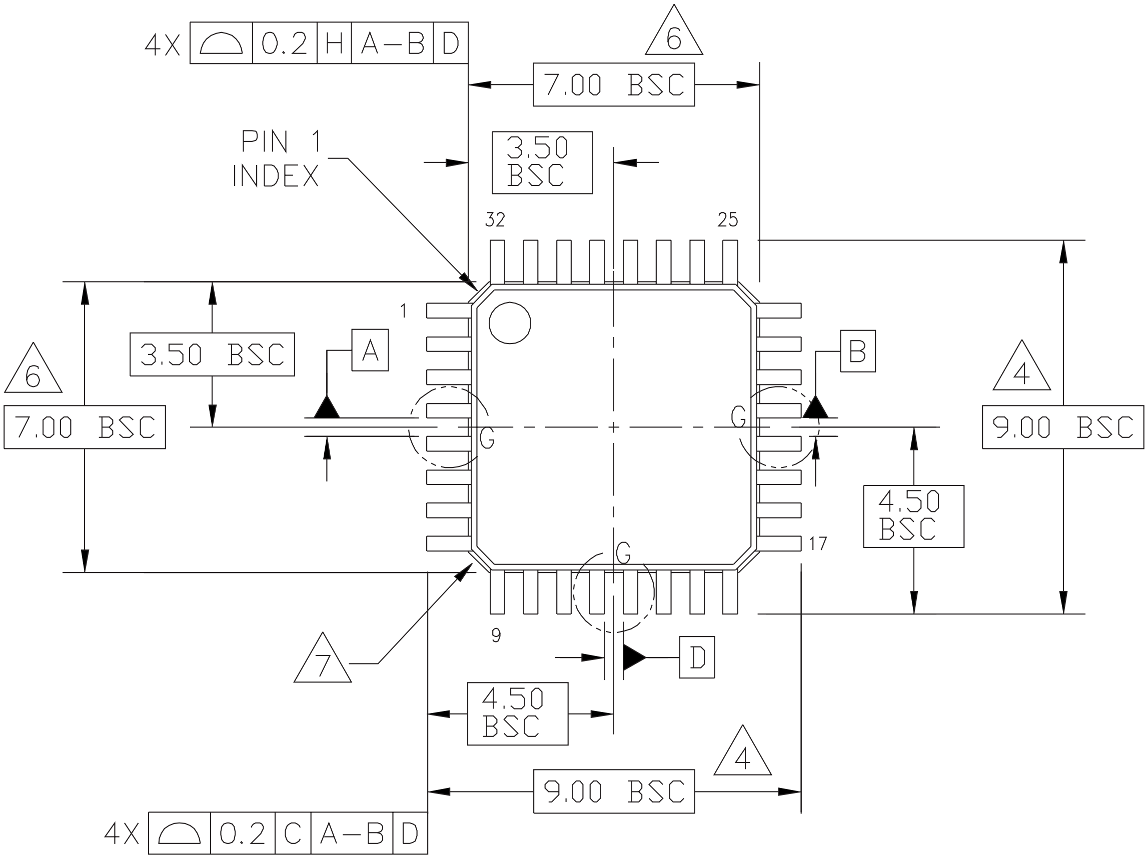
NOTES:

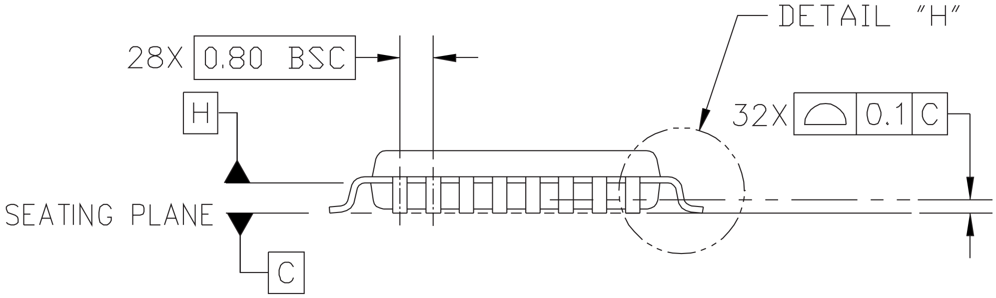
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXISTS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DEMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASITC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

28-LEAD PLCC PACKAGE

PACKAGE DIMENSIONS





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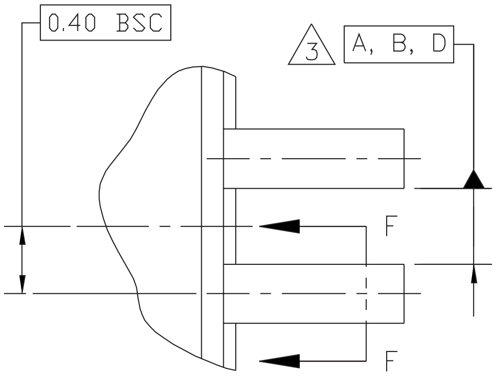
TITLE:	DOCUMENT NO: 98ASH70029A		REV: C
LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	CASE NUMBER: 873A-04		01 APR 2005
	STANDARD: JEDEC MS-026 BBA		

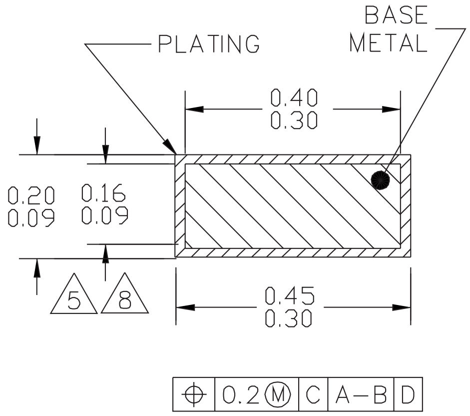
PAGE 1 OF 3

CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE

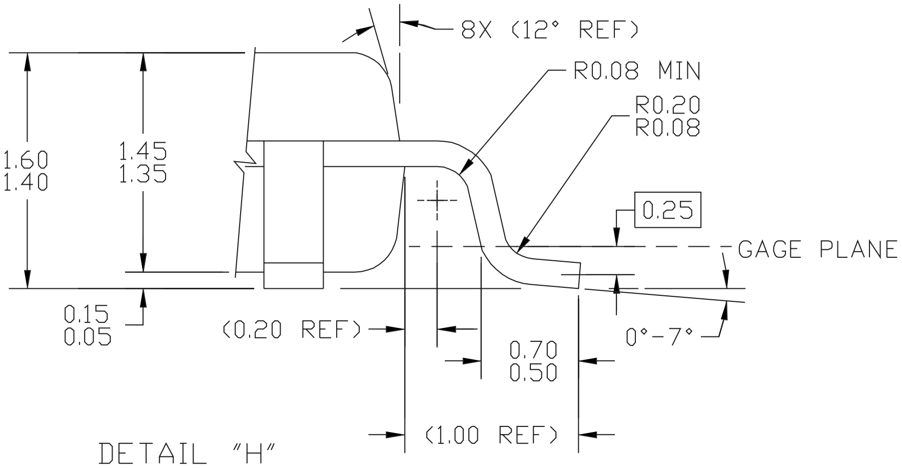
PACKAGE DIMENSIONS



DETAIL G



SECTION F-F
ROTATED 90°CW
32 PLACES



DETAIL "H"

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PAGE 2 OF 3

CASE 873A-04
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PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

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