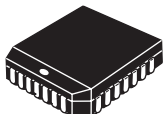
900MHz, Low Voltage, LVPECL Clock Syntheesizer

MPC92439

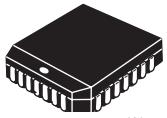
DATA SHEET

The MPC92439 is a 3.3 V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 3.125 MHz to 900 MHz and the support of differential LVPECL output signals the device meets the needs of the most demanding clock applications.

900MHZ LOW VOLTAGE CLOCK SYNTHESIZER



FN SUFFIX(1)
28-LEAD PLCC PACKAGE
CASE 776-02



EI SUFFIX(2)
28-LEAD PLCC PACKAGE
CASE 776-02

FA SUFFIX(1)
32-LEAD LQFP PACKAGE
CASE 873A-03

AC SUFFIX(2)
32-LEAD LQFP PACKAGE
CASE 873A-03

K SUFFIX
32-LEAD VFQFN PACKAGE
Pb-FREE PACKAGE

PROPOSED

Notes:
(1) FN, FA suffix: leaded terminations
(2) EI, AC suffix: lead-free, RoHS-compliant, EPP

ORDERING INFORMATION

Device	Package
MPC92439EI	PLCC-28 (Pb-Free)
MPC92439FA	LQFP-32
MPC92439AC	LQFP-32 (Pb-Free)
MPC92439KLF	VFQFN-32 (Pb-Free)

PROPOSED

Features

- 3.125 MHz to 900 MHz synthesized clock output signal
- Differential LVPECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference input
- 3.3V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 28-PLCC and 32-LQFP packaging
- 28-Lead and 32-lead Pb-free packages available
- SiGe Technology
- Ambient temperature range 0°C to + 70°C
- Pin and function compatible to the MC12439 and MPC9239

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator or external reference clock signal is multiplied by the PLL. The VCO within the PLL operates over a range of 400 to 900 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL}, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (400 to 900 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50Ω to V_{CC} – 2.0V. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the P_LOAD input LOW until power becomes valid. On the LOW-to-HIGH transition of P_LOAD, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating. The serial interface centers on a twelve bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See PROGRAMMING INTERFACE for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output. The PWR_DOWN pin, when asserted, will synchronously divide the FOUT by 16. The power down sequence is clocked by the PLL reference clock, thereby causing the frequency reduction to happen relatively slowly. Upon de-assertion of the PWR_DOWN pin, the FOUT input will step back up to its programmed frequency in four discrete increments.

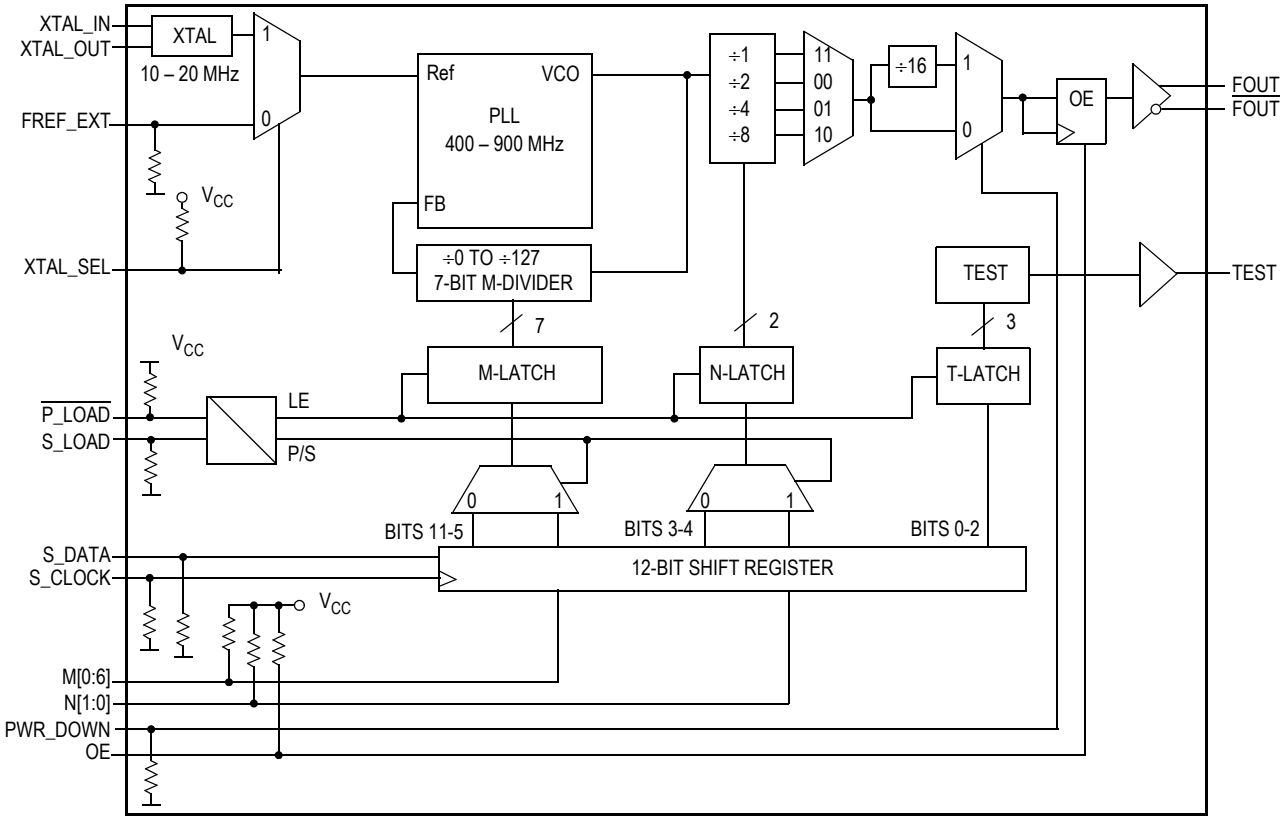


Figure 1. MPC92439 Logic Diagram

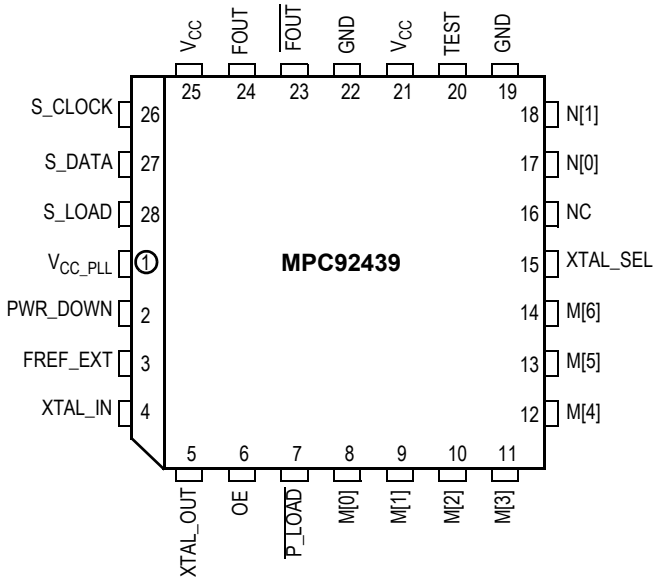


Figure 2. MPC92439 28-Lead PLCC Pinout
(Top View)

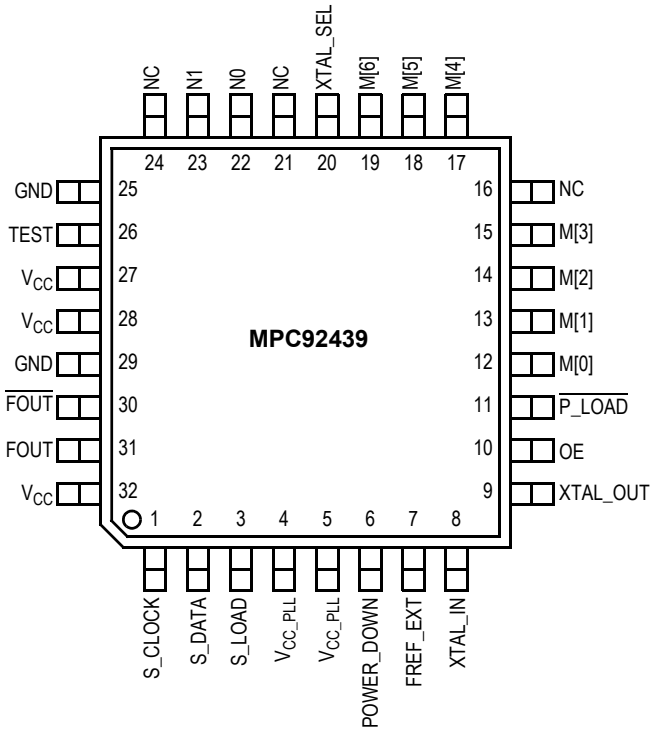


Figure 3. MPC92439 32-Lead Package Pinout
(Top View)

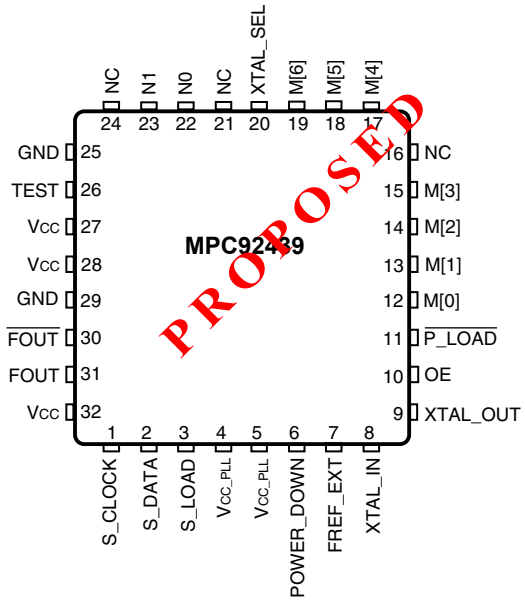


Figure 4. 32-Lead VFQFN Package Pinout (Top View)

Table 1. Pin Configurations

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT		6	Analog	Crystal oscillator interface
FREF_EXT	Input	0	LVCMOS	Alternative PLL reference input
FOUT, $\overline{\text{FOUT}}$	Output		LVPECL	Differential clock output
TEST	Output		LVCMOS	Test and device diagnosis output
XTAL_SEL	Input	1	LVCMOS	PLL reference select input
PWR_DOWN	Input	0	LVCMOS	Configuration input for power down mode. Assertion (deassertion) of power down will decrease (increase) the output frequency by a ratio of 16 in 4 discrete steps. PWR_DOWN assertion (deassertion) is synchronous to the input reference clock.
S_LOAD	Input	0	LVCMOS	Serial configuration control input. This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
P_LOAD	Input	1	LVCMOS	Parallel configuration control input. this input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of $\overline{\text{P\_LOAD}}$. $\overline{\text{P\_LOAD}}$ is state sensitive.
S_DATA	Input	0	LVCMOS	Serial configuration data input.
S_CLOCK	Input	0	LVCMOS	Serial configuration clock input.
M[0:6]	Input	1	LVCMOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$.
N[1:0]	Input	1	LVCMOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$.
OE	Input	1	LVCMOS	Output enable (active high) The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the FOUT output. OE = L low stops FOUT in the logic low state (FOUT = L, $\overline{\text{FOUT}}$ = H).
GND	Supply		Ground	Negative power supply (GND).
V_{CC}	Supply		V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation.
V_{CC_PLL}	Supply		V_{CC}	PLL positive power supply (analog power supply).
NC				Do not connect

Table 2. Output Frequency Range and PLL Post-Divider N

PWR_DOWN	N		VCO Output Frequency Division	FOUT Frequency Range
	1	0		
0	0	0	2	200 - 450 MHz
0	0	1	4	100 -225 MHz
0	1	0	8	50-112.5 MHz
0	1	1	1	400-900 MHz
1	0	0	32	12.5-28.125 MHz
1	0	1	64	6.25-14.0625 MHz
1	1	0	128	3.125-7.03125 MHz
1	1	1	16	25-56.25 MHz

Table 3. Function Table

Input	0	1
XTAL_SEL	FREF_EXT	XTAL interface
OE	Outputs disabled, FOUT is stopped in the logic low state (FOUT = L, $\overline{FOUT}$ = H)	Outputs enabled
PWR_DOWN	Output divider ÷ 1	Output divider ÷ 16

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multi-layer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
	Thermal Resistance Junction to Ambient 32 VFQFN	2.5	1	0		meters per second
	PROPOSED	43.0	37.6	33.7	°C/W	
θ_{JC}	LQFP 32 Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 5. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	4.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs (FREF_EXT, POWER_DOWN, XTAL_SEL, P_LOAD, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1]. OE)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current(1)			±200	µA	V_{IN} = V_{CC} or GND
Differential Clock Output F_{OUT}(2)						
V_{OH}	Output High Voltage	V_{CC}–1.02		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage	V_{CC}–1.95		V_{CC}–1.60	V	LVPECL
Test and Diagnosis Output TEST						
V_{OH}	Output High Voltage	2.0			V	I_{OH} = –0.8 mA
V_{OL}	Output Low Voltage			0.55	V	I_{OL} = 0.8 mA
Supply Current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current		62	110	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50Ω to V_{TT} = V_{CC} – 2V.

Table 7. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)**(1)**

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal interface frequency range		10		20	MHz	
f_{VCO}	VCO frequency range(2)		400		900	MHz	
f_{MAX}	Output Frequency	N = 11 (÷1) N = 00 (÷2) N = 01 (÷4) N = 10 (÷8)	400 200 100 50		900 450 225 112.5	MHz MHz MHz MHz	PWR_DOWN = 0
f_{S_CLOCK}	Serial Interface Programming Clock Frequency(3)		0		10	MHz	
$t_{P,MIN}$	Minimum Pulse Width	(S-LOAD, P_LOAD)	50			ns	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.05		0.3	ns	20% to 80%
t_S	Setup Time	S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20 20 20			ns ns ns	
t_S	Hold Time	S_DATA to S_CLOCK M, N to P_LOAD	20 20			ns ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter (RMS 1σ)(4)	N=11 (÷1) N=00 (÷2) N=01 (÷4) N=10 (÷8)			12 25 55 65	ps	
$t_{JIT(CC)}$	Period jitter (RMS 1σ)(5)	N=11 (÷1) N=00 (÷2) N=01 (÷4) N=10 (÷8)			13 23 36 40		
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot M$
3. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See APPLICATIONS INFORMATION for more details.
4. Maximum cycle jitter measured at the lowest VCO frequency. Figure 5 shows the cycle jitter vs. frequency characteristics
5. Maximum period jitter measured at the lowest VCO frequency. Figure 6 shows the period jitter vs. frequency characteristics

Table 8. MPC92439 Frequency Operating Range (in MHz)

		VCO frequency for an crystal interface frequency of						Output frequency for f_{XTAL}=16 MHz and for N =			
M	**M[6:0]**	**10**	**12**	**14**	**16**	**18**	**20**	**1**	**2**	**4**	**8**
20	0010100						400				
21	0010101						420				
22	0010110						440				
23	0010111					414	460				
24	0011000					432	480				
25	0011001				400	450	500	400	200	100	50
26	0011010				416	468	520	416	208	104	52
27	0011011				432	486	540	432	216	108	54
28	0011100				448	504	560	448	224	112	56
29	0011101			406	464	522	580	464	232	116	58
30	0011110			420	480	540	600	480	240	120	60
31	0011111			434	496	558	620	496	248	124	62
32	0100000			448	512	576	640	512	256	128	64
33	0100001			462	528	594	660	528	264	132	66
34	0100010		408	476	544	612	680	544	272	136	68
35	0100011		420	490	560	630	700	560	280	140	70
36	0100100		432	504	576	648	720	576	288	144	72
37	0100101		444	518	592	666	740	592	296	148	74
38	0100110		456	532	608	684	760	608	304	152	76
39	0100111		468	546	624	702	780	624	312	156	78
40	0101000	400	480	560	640	720	800	640	320	160	80
41	0101001	410	492	574	656	738	820	656	328	164	82
42	0101010	420	504	588	672	756	840	672	336	168	84
43	0101011	430	516	602	688	774	860	688	344	172	86
44	0101100	440	528	616	704	792	880	704	352	176	88
45	0101101	450	540	630	720	810	900	720	360	180	90
46	0101110	460	552	644	736	828		736	368	184	92
47	0101111	470	564	658	752	846		752	376	188	94
48	0110000	480	576	672	768	864		768	384	192	96
49	0110001	490	588	684	784	882		784	392	196	98
50	0110010	500	600	700	800	900		800	400	200	100
51	0110011	510	612	714	816			816	408	204	102
52	0110100	520	624	728	832			832	416	208	104
53	0110101	530	636	742	848			848	424	212	106
54	0110110	540	648	756	864			864	432	216	108
55	0110111	550	660	770	880			880	440	220	110
56	0111000	560	672	784	896			896	448	224	112
57	0111001	570	684	798							
58	0111010	580	696	812							
59	0111011	590	708	826							
60	0111100	600	720	840							
61	0111101	610	732	854							
62	0111110	620	744	868							
63	0111111	630	756	882							
64	1000000	640	768	896							
...		...	...	...							

PROGRAMMING INTERFACE

Programming the MPC92439

Programming the MPC92439 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$f_{OUT} = f_{XTAL} \cdot M \div N \quad (1)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to match the VCO frequency range of 400 to 900 MHz in order to achieve stable PLL operation:

$$M_{MIN} = f_{VCO,MIN} \div (f_{XTAL}) \text{ and} \quad (2)$$

$$M_{MAX} = f_{VCO,MAX} \div (f_{XTAL}) \quad (3)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M = 25 and M = 56. Table 8 shows the usable VCO frequency and M divider range for other example input frequencies. Assuming that a 16 MHz input frequency is used, equation (1) reduces to:

$$f_{OUT} = 16\ M \div N \quad (4)$$

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 9. Output Frequency Range for f_{XTAL} = 16 MHz

N			F_{OUT}	F_{OUT} Range	F_{OUT} Step
1	0	Value			
0	0	2	8·M	200-450 MHz	8 MHz
0	1	4	4·M	100-225 MHz	4 MHz
1	0	8	2·M	50-112.5 MHz	2 MHz
1	1	1	16·M	400-900 MHz	16 MHz

Example Calculation for an 16 MHz Input Frequency

For example, if an output frequency of 384 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 384 MHz falls within the frequency range set by an N value of 2, so N[1:0]=00. For N = 2, FOUT = 8·M and M = FOUT÷8. Therefore, M = 384 ÷ 8 = 48, so M[6:0] = 0110000. Following this procedure a user can generate any whole frequency between 50 MHz and 900 MHz. The size of the programmable frequency steps will be equal to:

$$f_{STEP} = f_{XTAL} \div N \quad (5)$$

APPLICATIONS INFORMATION

Jitter Performance of the MPC92439

Figure 5 and Figure 6 illustrate the RMS jitter performance of the MPC92439 across its specified VCO frequency range. The cycle-to-cycle and period jitter is a function of the VCO frequency and the output divider N. The general trend is that as the output frequency increases (higher VCO frequency and lower N-divider) the MPC92439 output jitter decreases. Optimum jitter performance can be achieved at higher VCO and output frequencies. The maximum cycle-to-cycle and period jitter published in Table 7 correspond to the jitter performance at the lowest VCO frequency limit).

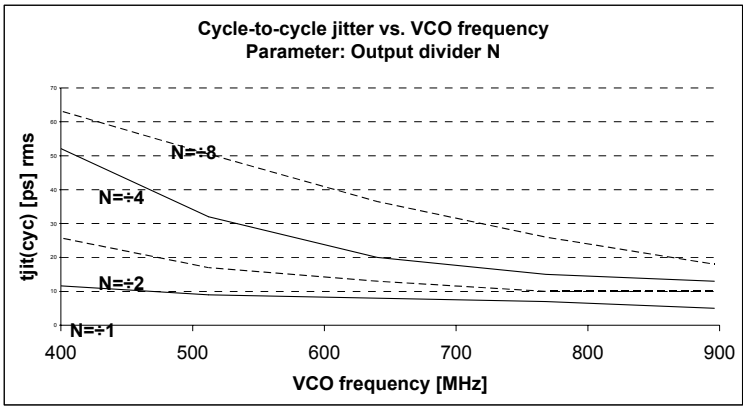


Figure 5. MPC92439 Cycle-to-cycle Jitter

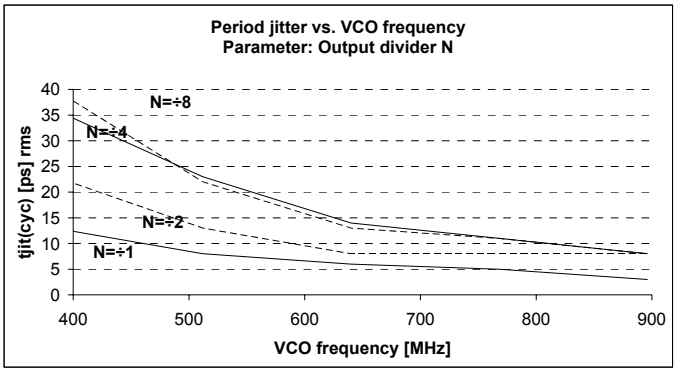


Figure 6. MPC92439 Period Jitter

Using the Parallel and Serial Interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW to HIGH transition will latch the information present on the M[6:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW the input latches will be transparent and any changes on the M[6:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 12 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two, and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M6). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW

transition on the S_LOAD input will latch the new divide values into the counters. Figure 7 illustrates the timing diagram for both a parallel and a serial load of the MPC92439 synthesizer.

M[6:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the Test and Diagnosis Output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the LVCMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis.

The T2, T1 and T0 control bits are preset to '000' when $\overline{\text{P\_LOAD}}$ is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MPC92439 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC92439 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clocktree shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 100 MHz as the divide ratio of the Post-PLL divider is 2 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 10. Test and Debug Configuration for TEST

T[2:0]			TEST Output
T2	T1	T0	
0	0	0	12-bit shift register out(1)
0	0	1	Logic 1
0	1	0	$f_{XTAL} \div 2$
0	1	1	M-Counter out
1	0	0	FOUT
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	FOUT ÷ 4

1. Clocked out at the rate of S_CLOCK\

Table 11. Debug Configuration for PLL Bypass(1)

Output	Configuration
FOUT	S_CLOCK ÷ N
TEST	M-Counter out(2)

1. T[2:0] = 110. AC specifications do not apply in PLL bypass mode
2. Clocked out at the rate of S_CLOCK ÷ (2·N)

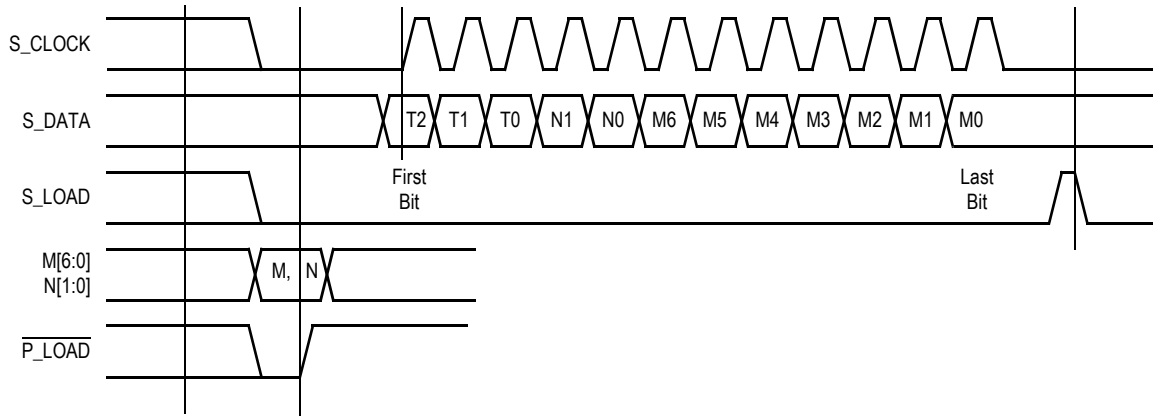


Figure 7. Serial Interface Timing Diagram

Power Supply Filtering

The MPC92439 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} pin impacts the device characteristics. The MPC92439 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC92439. Figure 8 illustrates a typical power supply filter scheme. The MPC92439 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between

the V_{CC} supply and the MPC92439 pin of the MPC92439. From the data sheet, the V_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is maximum 20 mA, assuming that a minimum of 2.835 V must be maintained on the V_{CC_PLL} pin. The resistor shown in Figure 8 must have a resistance of 10–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 µH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the V_{CC_PLL} pin, a low DC resistance inductor is required (less than 15 Ω).

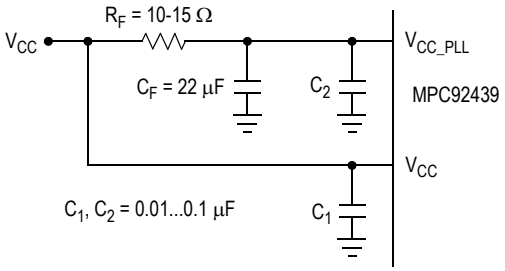


Figure 8. V_{CC_PLL} Power Supply Filter

Layout Recommendations

The MPC92439 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 9 shows a representative board layout for the MPC92439. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 9 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC92439 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Although the MPC92439 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

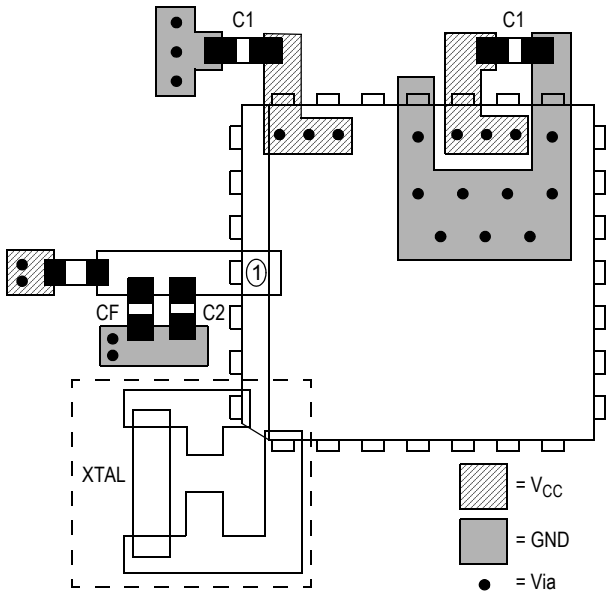


Figure 9. PCB Board Layout Recommendation for the PLCC28 Package

The On-Chip Crystal Oscillator

The MPC92439 features an integrated on-chip crystal oscillator to minimize system implementation cost. The integrated oscillator is a Pierce-type that uses the crystal in its parallel resonance mode. It is recommended to use a 10 to 20 MHz crystal with a load specification of C_L = 10 pF. Crystals with a load specification of C_L = 20 pF may be used at the expense of an slightly higher frequency than specified for the crystal. Externally connected capacitors on both the XTAL_IN and XTAL_OUT pins are not required but can be used to fine-tune the crystal frequency as desired.

The crystal, the trace and optional capacitors should be placed on the board as close as possible to the MPC92439 XTAL_IN and XTAL_OUT pins to reduce crosstalk of active signals into the oscillator. Short and wide traces further reduce parasitic inductance and resistance. It is further recommended to guard the crystal circuit by placing a ground ring around the traces and oscillator components. See Table 12 for recommended crystal specifications.

Table 12. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance Mode	Parallel
Crystal Frequency	10 - 20 MHz
Shunt Capacitance C_0	5 - 7 pF
Load Capacitance C_L	10 pF
Equivalent Series Resistance ESR	20–60 Ω

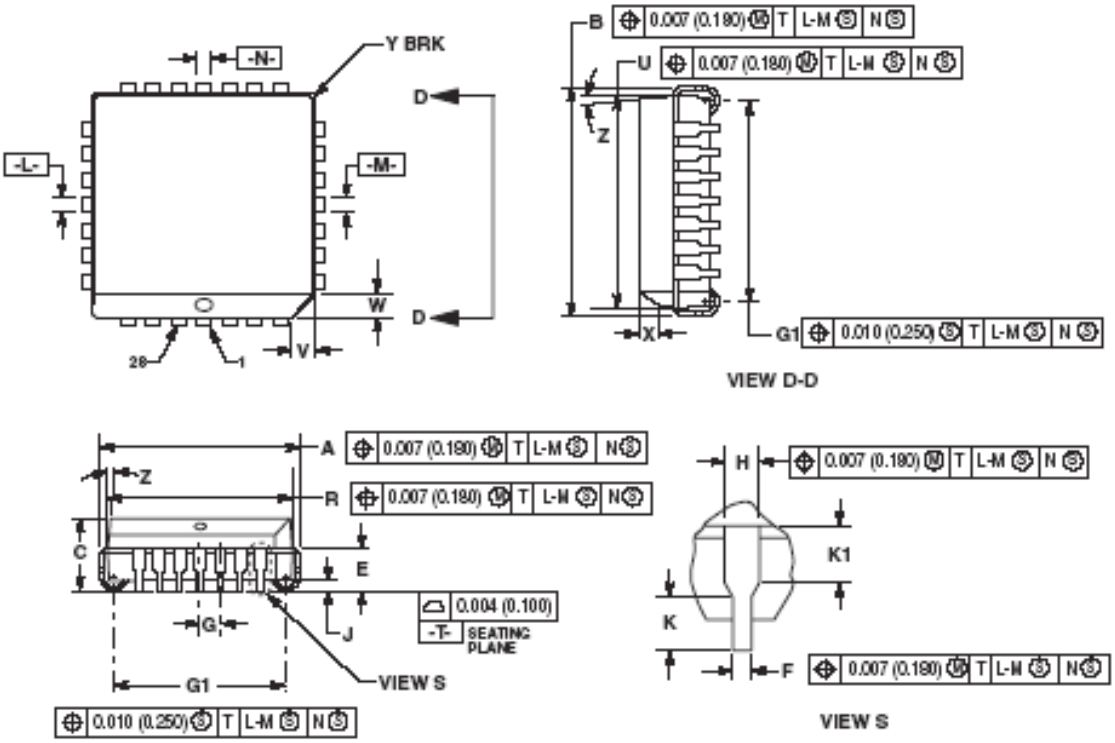
As an alternative to parallel resonance mode crystals, the oscillator also works with crystals specified in the series resonance mode. With series resonance crystals, the oscillator frequency and the synthesized output frequency of the MPC92439 will be a approximately 350-400 ppm higher than using crystals specified for parallel frequency mode. This is applicable to applications using the MPC92439 in sockets designed for the pin and function compatible MC12439 synthesizer, which has an oscillator using the crystal in its series resonance mode.Table 13 shows the recommended specifications for series resonance mode crystals

Table 13. Alternative Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance Mode	Series
Crystal Frequency	10 - 20 MHz
Shunt Capacitance C_0	5 - 7 pF
Equivalent Series Resistance ESR	50–80 Ω

Package Outline and Package Dimensions

PACKAGE DIMENSIONS

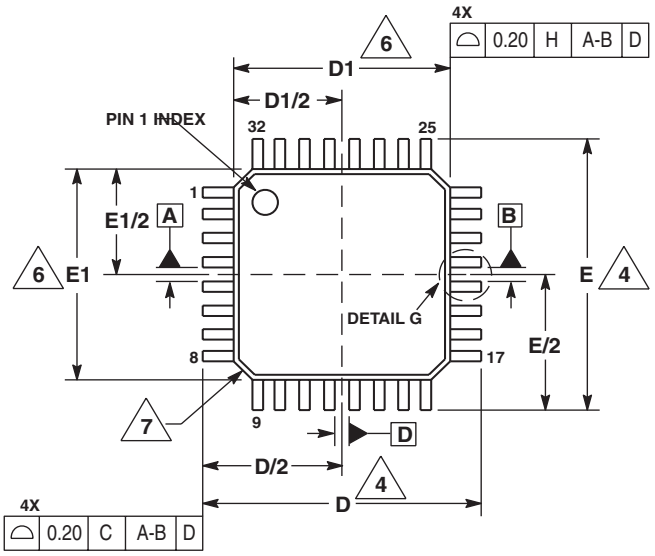


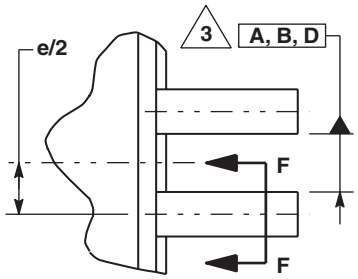
NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXISTS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

CASE 776-02
ISSUE D
PLCC PLASTIC PACKAGE

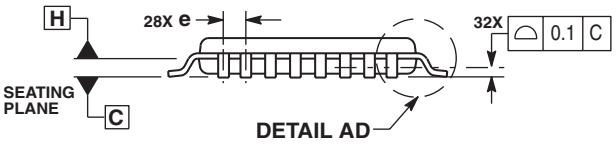
PACKAGE DIMENSIONS

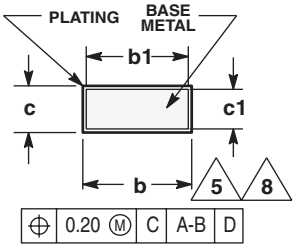




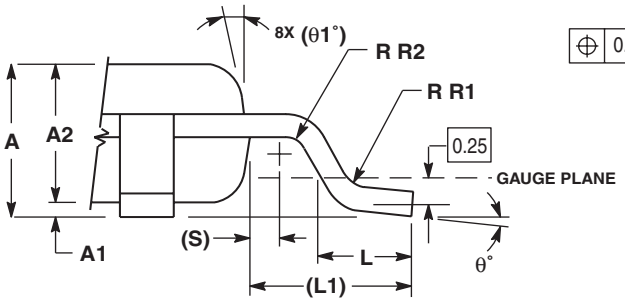
DETAIL G

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.





SECTION F-F

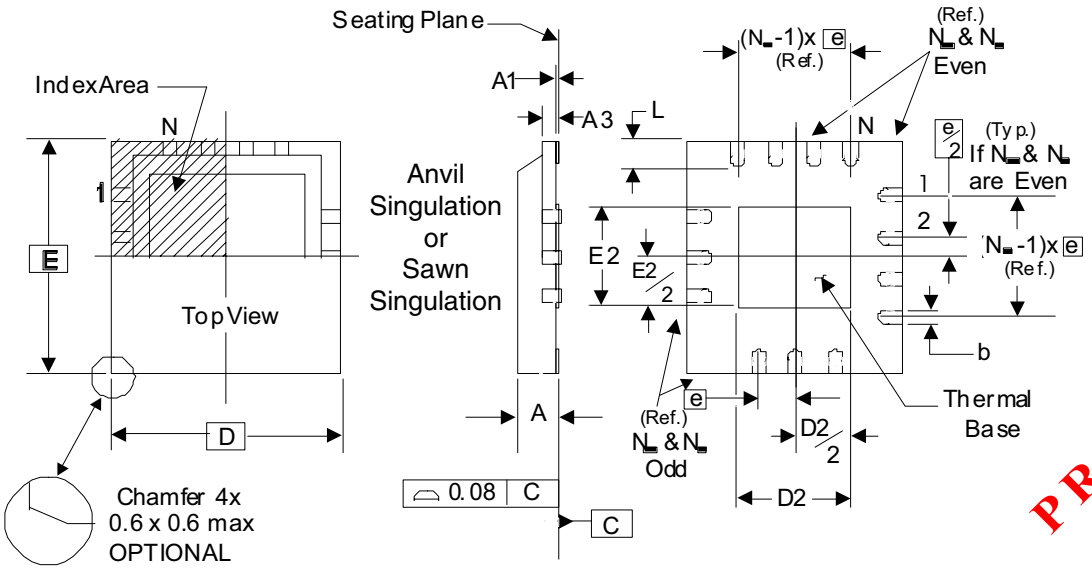


DETAIL AD

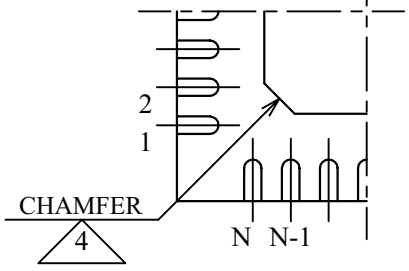
	MILLIMETERS	
DIM	MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
q	0°	7°
q1	12 REF	
R1	0.08	0.20
R2	0.08	---
S	0.20 REF	

CASE 873A-03
ISSUE B
LQFP PLASTIC PACKAGE

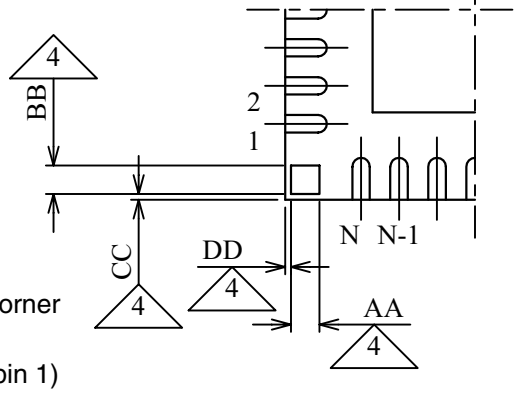
Package Outline - K Suffix for 32 Lead VFQFN



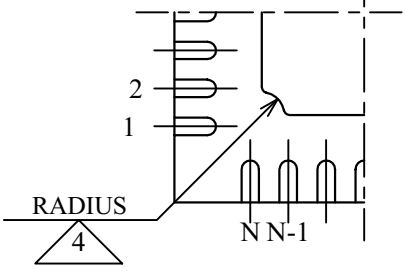
Bottom View w/Type A ID



Bottom View w/Type B ID



Bottom View w/Type C ID



There are 3 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type B: Dummy pad between pin 1 and N.
3. Type C: Mouse bite on the paddle (near pin 1)

Table 14. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

PROPOSED

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 14.

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