Order Number: MPC9330/D
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Product Preview

3.3V/2.5V 1:6 LVCMOS PLL Clock Generator

MPC9330

3.3V/2.5V 1:6 LVCMOS PLL CLOCK GENERATOR

FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A

The MPC9330 is a 3.3V or 2.5V compatible, 1:6 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance telecomm, networking and computing applications. With output frequencies up to 200 MHz and output skews less than 150 ps[1] the device meets the needs of the most demanding clock applications. The MPC9330 is specified for the extended temperature range of –40°C to +85°C.

Features

- 1:6 PLL based low-voltage clock generator
- 2.5V or 3.3V power supply
- Generates clock signals up to 200 MHz
- Maximum output skew of 150 ps[1]
- On-chip crystal oscillator clock reference
- Alternative LVCMOS PLL reference clock input
- Internal and external PLL feedback
- PLL multiplies the reference clock by 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3 or x/4
- Supports zero-delay operation in external feedback mode
- Synchronous output clock stop in logic low eliminates output runt pulses
- Power_down feature reduces output clock frequency
- Drives up to 12 clock lines
- 32 lead LQFP packaging
- Ambient temperature range –40°C to +85°C
- Pin and function compatible to the MPC930

Functional Description

The MPC9330 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9330 requires either the selection of internal PLL feedback or the connection of one of the device outputs to the feedback input to close the PLL feedback path in external feedback mode. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. In external PLL feedback configuration and with the available post-PLL dividers (divide-by-2, divide-by-4 and divide-by-6), the internal VCO of the MPC9330 is running at either 4x, 8x, 12x, 16x or 24x of the reference clock frequency. In internal feedback configuration (divide-by-16) the internal VCO is running 16x of the reference frequency. The frequency of the QA, QB, QC output banks is a division of the VCO frequency and can be configured independently for each output bank using the FSELA, FSELB and FSELC pins, respectively. The available output to input frequency ratios are 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3 or x/4.

The REF_SEL pin selects the internal crystal oscillator or the LVCMOS compatible input as the reference clock signal. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The outputs can be disabled (high-impedance) by deasserting the $\overline{\text{OE/MR}}$ pin. In the PLL configuration with external feedback selected, deasserting OE/MR causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Asserting OE/MR will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation. The MPC9330 output clock stop control allows the outputs to start and stop synchronously in the logic low state, without the potential generation of runt pulses.

The MPC9330 is fully 2.5V and 3.3V compatible and requires no external loop filter components. All inputs (except XTAL) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9330 outputs can drive one or two traces giving the devices an effective fanout of 1:12. The device is packaged in a 7x7 mm[2] 32-lead LQFP package.

1. Design target, pending final characterization.

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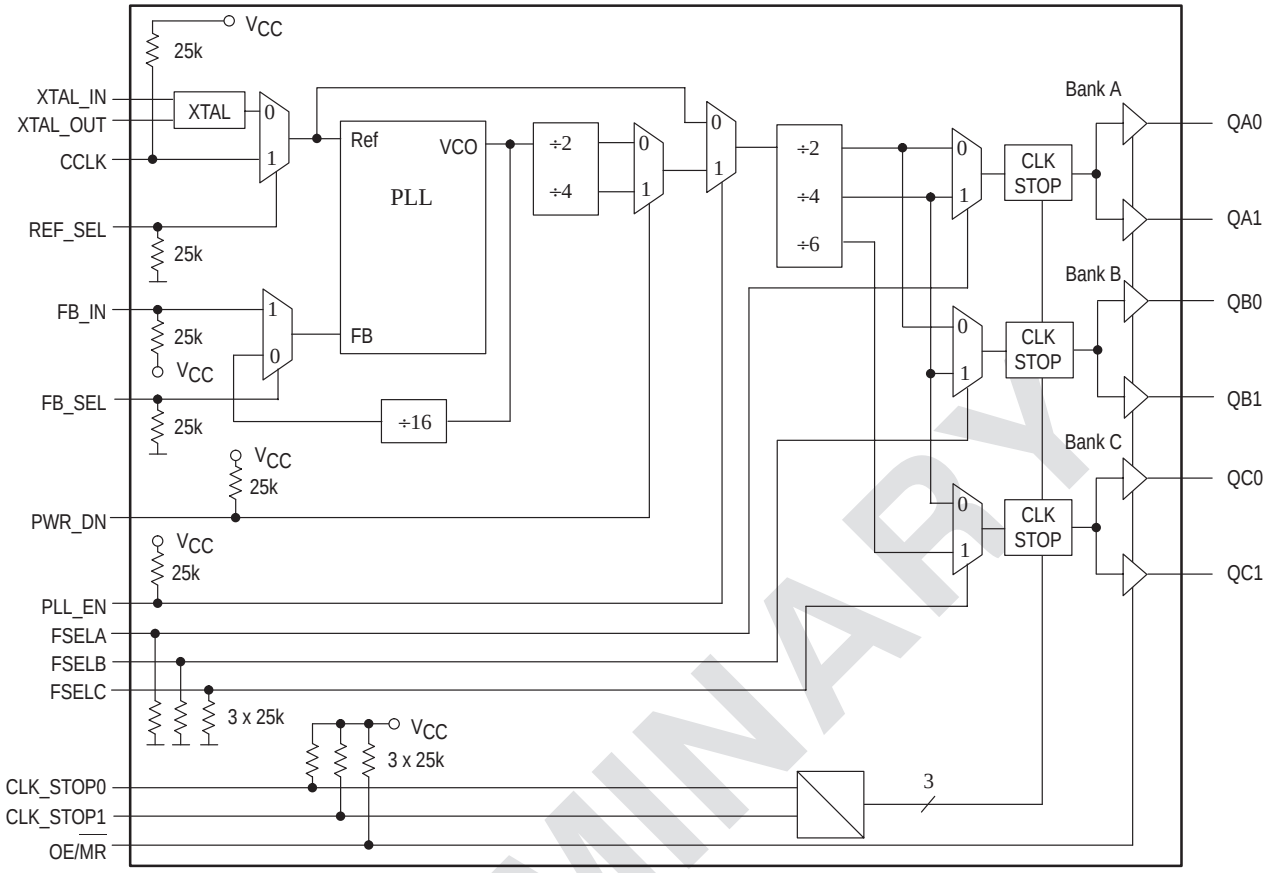
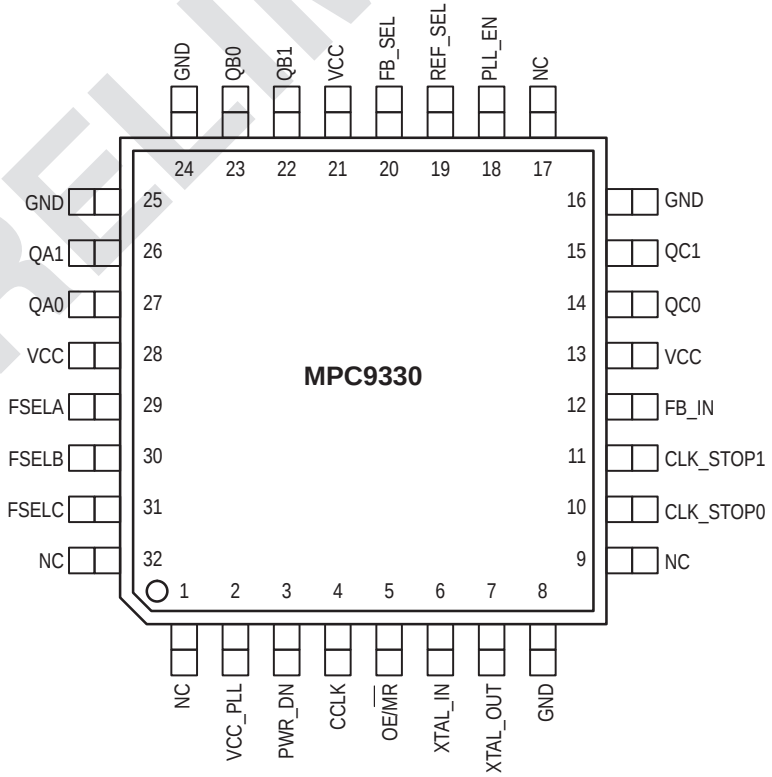


Figure 1. MPC9330 Logic Diagram



The MPC9330 requires an external RC filter for the analog power supply pin VCC_PLL. Please see application section for details.

Figure 2. MPC9330 32–Lead Package Pinout (Top View)

Table 1: PIN CONFIGURATION

Pin	I/O	Type	Function
CCLK	Input	LVCMOS	PLL reference clock signal
XTAL_IN, XTAL_OUT	Input	Analog	Crystal oscillator interface
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to an output
FB_SEL	Input	LVCMOS	Feedback select
REF_SEL	Input	LVCMOS	Reference clock select
PWR_DN	Input	LVCMOS	Output frequency and power down select
FSELA	Input	LVCMOS	Frequency divider select for bank A outputs
FSELB	Input	LVCMOS	Frequency divider select for bank B outputs
FSELC	Input	LVCMOS	Frequency divider select for bank C outputs
PLL_EN	Input	LVCMOS	PLL enable/disable
CLK_STOP0-1	Input	LVCMOS	Clock output enable/disable
$\overline{OE}/MR$	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
QA0-1, QB0-1, QC0-1	Output	LVCMOS	Clock outputs
GND	Supply	Ground	Negative power supply
VCC_PLL	Supply	VCC	PLL positive power supply (analog power supply). The MPC9330 requires an external RC filter for the analog power supply pin V_{CC_PLL}. Please see applications section for details.
VCC	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation

Table 2: FUNCTION TABLE

Control	Default	0	1
REF_SEL	0	The crystal oscillator output is the PLL reference clock	CCLK is the PLL reference clock
FB_SEL	0	Internal PLL feedback of 16. $f_{VCO} = 16 * f_{ref}$	External feedback. Zero-delay operation enabled for CCLK as reference clock
PLL_EN	1	Test mode with PLL disabled. The reference clock is substituted for the internal VCO output. MPC9330 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
PWR_DN	1	VCO ÷ 2 (High output frequency range)	VCO ÷ 4 (Low output frequency range)
FSELA	0	Output divider ÷ 2	Output divider ÷ 4
FSELB	0	Output divider ÷ 2	Output divider ÷ 4
FSELC	0	Output divider ÷ 4	Output divider ÷ 6
CLK_STOP[0:1]	11	See Table 3	
$\overline{OE}/MR$	1	Outputs disabled (high-impedance state) and reset of the device. During reset in external feedback configuration, the PLL feedback loop is open. The VCO is tied to its lowest frequency. The MPC9330 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLK). Reset does not affect PLL lock in internal feedback configuration.	Outputs enabled (active)
PWR_DN, FSELA, FSELB and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 1 to Table 3 for supported frequency ranges and output to input frequency ratios.			

Table 3: CLOCK OUTPUT SYNCHRONOUS DISABLE (CLK_STOP) FUNCTION TABLE[a]

CLK_STOP0	CLK_STOP1	QA[0:1]	QB[0:1]	QC[0:1]
0	0	Active	Stopped in logic L state	Stopped in logic L state
0	1	Active	Stopped in logic L state	Active
1	0	Stopped in logic L state	Stopped in logic L state	Active
1	1	Active	Active	Active

a. Output operation for $\overline{OE}/MR$=1 (outputs enabled). $\overline{OE}/MR$=1=0 will high-impedance tristate all outputs independend on CLK_STOP[0:1]

Table 4: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch–Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5: ABSOLUTE MAXIMUM RATINGS[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6: DC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-24 mA[a]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL}= 24 mA I_{OL}= 12 mA
Z_{OUT}	Output Impedance		14 - 17		Ω	
I_{IN}	Input Current[b]			±200	µA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		3.0	5.0	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

a. The MPC9330 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

b. Inputs have pull–down resistors affecting the input current.

Table 7: AC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = –40°C to 85°C)[a] [b]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency[c]	÷ 4 feedback[d]	50		100	MHz	PLL locked
	PLL mode, external feedback	÷ 8 feedback	25		50	MHz	
		÷ 12 feedback	16.67		33.3	MHz	
		÷ 16 feedback	12.5		25	MHz	
		÷ 24 feedback	8.33		16.67	MHz	
	PLL mode, internal feedback	⟨÷ 16 feedback)	12.5		25	MHz	
	Input Reference Frequency in PLL bypass mode[e]				TBD	MHz	
f_{VCO}	VCO Lock Frequency Range[f]		200		400	MHz	
f_{XTAL}	Crystal Interface Frequency Range[g]		10		20	MHz	
f_{MAX}	Output Frequency	÷ 4 output	50		100	MHz	PLL locked
		÷ 8 output	25		50	MHz	
		÷ 12 output	16.67		33.3	MHz	
		÷ 16 output	12.5		25	MHz	
		÷ 24 output	8.33		16.67	MHz	
f_{refDC}	Reference Input Duty Cycle		40		60	%	
t_r, t_f	CCLK Input Rise/Fall Time				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)	CCLK or PCLK to FB_IN		±100		ps	FB_SEL=1 & PLL locked
$t_{sk(o)}$	Output-to-Output Skew[h]				150	ps	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter	RMS (1σ)[i]		TBD		ps	
$t_{JIT(PER)}$	Period Jitter	RMS (1σ)		TBD		ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1σ)		TBD		ps	
BW	PLL closed loop bandwidth[j]	÷ 4 feedback			TBD	kHz	
	PLL mode, external feedback	÷ 8 feedback			TBD	kHz	
		÷ 12 feedback			TBD	kHz	
		÷ 16 feedback			TBD	kHz	
		÷ 24 feedback			TBD	kHz	
t_{LOCK}	Maximum PLL Lock Time			10		ms	

a. All AC characteristics are design targets and subject to change upon device characterization.
b. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
c. PLL mode requires PLL_EN = 0 to enable the PLL.
d. ÷4 feedback (FB) can be accomplished by setting PWR_DN = 0 and the connection of one ÷2 output to FB_IN. See Table 1 to Table 3 for other feedback configurations.
e. In bypass mode, the MPC9330 divides the input reference clock.
f. The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
g. The usable crystal frequency range depends on the VCO lock frequency and the PLL feedback ratio.
h. See application section for part–to–part skew calculation.
i. See application section for a jitter calculation for other confidence factors than 1 σ.
j. –3 dB point of PLL transfer characteristics.

Table 8: DC CHARACTERISTICS (V_{CC} = 2.5V ± 5%, T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	–0.3		0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.8			V	I_{OH}=-15 mA[a]
V_{OL}	Output Low Voltage			0.6	V	I_{OL}= 15 mA
Z_{OUT}	Output Impedance		17 - 20		Ω	
I_{IN}	Input Current			±200	µA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

a. The MPC9330 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

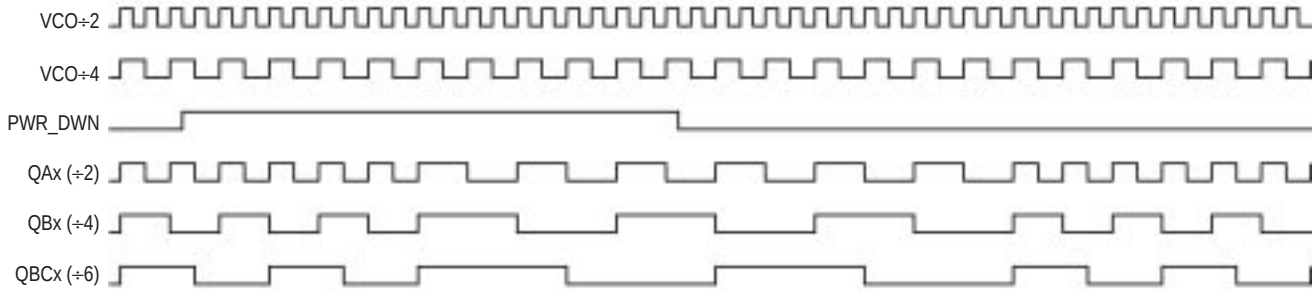
Table 9: AC CHARACTERISTICS (V_{CC} = 2.5V ± 5%, T_A = –40°C to 85°C)[a b]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency[c]	÷ 4 feedback[d]	50		100	MHz	PLL locked
	PLL mode, external feedback	÷ 8 feedback	25		50	MHz	
		÷ 12 feedback	16.67		33.3	MHz	
		÷ 16 feedback	12.5		25	MHz	
		÷ 24 feedback	8.33		16.67	MHz	
	PLL mode, internal feedback	⟨÷ 16 feedback)	12.5		25	MHz	
	Input Reference Frequency in PLL bypass mode[e]				TBD		
f_{VCO}	VCO Lock Frequency Range[f]		200		400	MHz	
f_{XTAL}	Crystal Interface Frequency Range[g]		10		20	MHz	
f_{MAX}	Output Frequency	÷ 4 output[g]	50		100	MHz	PLL locked
		÷ 8 output	25		50	MHz	
		÷ 12 output	16.67		33.3	MHz	
		÷ 16 output	12.5		25	MHz	
		÷ 24 output	8.33		16.67	MHz	
f_{refDC}	Reference Input Duty Cycle		40		60	%	
t_r, t_f	CCLK Input Rise/Fall Time				1.0	ns	0.7 to 1.7V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)	CCLK or PCLK to FB_IN		±100		ps	FB_SEL=1 & PLL locked
$t_{sk(o)}$	Output-to-Output Skew[h]				150	ps	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8V
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter	RMS (1σ)[i]		TBD		ps	
$t_{JIT(PER)}$	Period Jitter	RMS (1σ)		TBD		ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1σ)		TBD		ps	
BW	PLL closed loop bandwidth[j]	÷ 4 feedback			TBD	kHz	
		÷ 8 feedback			TBD	kHz	
		÷ 12 feedback			TBD	kHz	
		÷ 16 feedback			TBD	kHz	
		÷ 24 feedback			TBD	kHz	
t_{LOCK}	Maximum PLL Lock Time			10		ms	

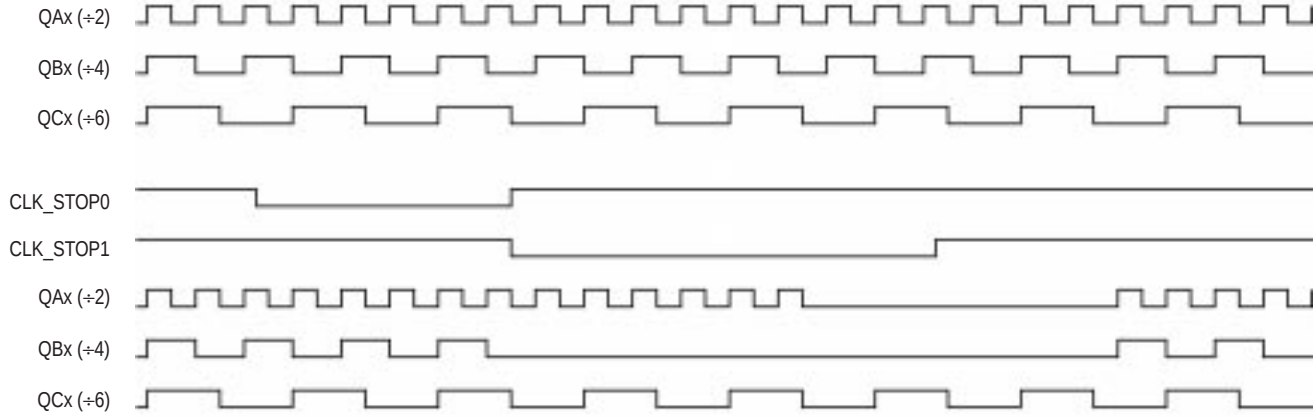
a. All AC characteristics are design targets and subject to change upon device characterization.
b. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
c. PLL mode requires PLL_EN = 0 to enable the PLL.
d. ÷4 feedback (FB) can be accomplished by setting PWR_DN = 0 and the connection of one ÷2 output to FB_IN. See Table 1 to Table 3 for other feedback configurations.
e. In bypass mode, the MPC9330 divides the input reference clock.
f. The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
g. The usable crystal frequency range depends on the VCO lock frequency and the PLL feedback ratio.
h. See application section for part–to–part skew calculation.
i. See application section for a jitter calculation for other confidence factors than 1 σ.
j. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Output power down (PWR_DN) timing diagram



Output clock stop (CLK_STOP) timing diagram



Programming the MPC9330

The MPC9330 supports output clock frequencies from 6.67 to 200 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 400 MHz for stable and optimal operation. The FSELA, FSELB, FSELC and PWR_DN pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:4, 1:3, 1:2, 1:1, 2:3, 4:3 and 3:2. Tables 10 through 12 illustrate the various output configurations and frequency ratios supported by the MPC9330.

Table 10: MPC9330 Example Configurations (Internal Feedback: FB_SEL = 0)

fref[a] [MHz]	PWR_DN	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
10.0-25.0	0	0	0	0	fref · 4 (40-100 MHz)	fref · 4 (40-100 MHz)	fref · 2 (20-50 MHz)
	0	0	0	1	fref · 4 (40-100 MHz)	fref · 4 (40-100 MHz)	fref ·4÷3 (13.3-33.3 MHz)
	0	0	1	0	fref · 4 (40-100 MHz)	fref · 2 (20-50 MHz)	fref · 2 (20-50 MHz)
	0	0	1	1	fref · 4 (40-100 MHz)	fref · 2 (20-50 MHz)	fref ·4÷3 (13.3-33.3 MHz)
	0	1	0	0	fref · 2 (20-50 MHz)	fref · 4 (40-100 MHz)	fref · 2 (20-50 MHz)
	0	1	0	1	fref · 2 (20-50 MHz)	fref · 4 (40-100 MHz)	fref ·4÷3 (13.3-33.3 MHz)
	0	1	1	0	fref · 2 (20-50 MHz)	fref · 2 (20-50 MHz)	fref · 2 (20-50 MHz)
	0	1	1	1	fref · 2 (20-50 MHz)	fref · 2 (20-50 MHz)	fref ·4÷3 (13.3-33.3 MHz)
	1	0	0	0	fref · 2 (20-50 MHz)	fref · 2 (20-50 MHz)	fref (10-25 MHz)
	1	0	0	1	fref · 2 (20-50 MHz)	fref · 2 (20-50 MHz)	fref ·2÷3 (6.67-16.67 MHz)
	1	0	1	0	fref · 2 (20-50 MHz)	fref (10-25 MHz)	fref (10-25 MHz)
	1	0	1	1	fref · 2 (20-50 MHz)	fref (10-25 MHz)	fref ·2÷3 (6.67-16.67 MHz)
	1	1	0	0	fref (10-25 MHz)	fref · 2 (20-50 MHz)	fref (10-25 MHz)
	1	1	0	1	fref (10-25 MHz)	fref · 2 (20-50 MHz)	fref ·2÷3 (6.67-16.67 MHz)
	1	1	1	0	fref (10-25 MHz)	fref (10-25 MHz)	fref (10-25 MHz)
	1	1	1	1	fref (10-25 MHz)	fref (10-25 MHz)	fref ·2÷3 (6.67-16.67 MHz)

a. fref is the input clock reference frequency (CCLK or XTAL)

Table 11: MPC9330 Example Configurations (External Feedback and PWR_DN = 0)

PLL Feedback	fref[a] [MHz]	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 4[b]	40-100	0	0	0	fref (40-100 MHz)	fref (40-100 MHz)	fref÷2 (20-50 MHz)
		0	0	1	fref (40-100 MHz)	fref (40-100 MHz)	fref÷3 (13.3-33.3MHz)
		0	1	0	fref (40-100 MHz)	fref÷2 (20-50 MHz)	fref÷2 (20-50 MHz)
		0	1	1	fref (40-100 MHz)	fref÷2 (20-50 MHz)	fref÷3 (13.3-33.3MHz)
VCO ÷ 8[c]	20-50	1	0	0	fref (20-50 MHz)	fref ·2 (40-100 MHz)	fref (20-50 MHz)
		1	0	1	fref (20-50 MHz)	fref ·2 (40-100 MHz)	fref ·2÷3 (13.3-33.3 MHz)
		1	1	0	fref (20-50 MHz)	fref (20-50 MHz)	fref (20-50 MHz)
		1	1	1	fref (20-50 MHz)	fref (20-50 MHz)	fref ·2÷3 (13.3-33.3 MHz)
VCO ÷ 12[d]	13.3-33.3	0	0	1	fref ·3 (40-100 MHz)	fref ·3 (40-100 MHz)	fref (13.3-33.3 MHz)
		0	1	1	fref ·3 (40-100 MHz)	fref ·3÷2 (20-50 MHz)	fref (13.3-33.3 MHz)
		1	0	1	fref ·3÷2 (20-50 MHz)	fref ·3 (40-100 MHz)	fref (13.3-33.3 MHz)
		1	1	1	fref ·3÷2 (20-50 MHz)	fref ·3÷2 (20-50 MHz)	fref (13.3-33.3 MHz)

a. fref is the input clock reference frequency (CCLK or XTAL)
b. QAx connected to FB_IN and FSELA=0, PWR_DN=0
c. QAx connected to FB_IN and FSELA=1, PWR_DN=0
d. QCx connected to FB_IN and FSELC=1, PWR_DN=0

Table 12: MPC9330 Example Configurations (External Feedback and PWR_DN = 1)

PLL Feedback	fref[a] [MHz]	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 16[b]	10-25	1	0	0	fref (10-25 MHz)	fref ·2 (20-50 MHz)	fref (10-25 MHz)
		1	0	1	fref (10-25 MHz)	fref ·2 (20-50 MHz)	fref ·2÷3 (6.6-16.6 MHz)
		1	1	0	fref (10-25 MHz)	fref (10-25 MHz)	fref (10-25 MHz)
		1	1	1	fref (10-25 MHz)	fref (10-25 MHz)	fref ·2÷3 (6.6-16.6 MHz)
VCO ÷ 24[c]	6.67-16.67	0	0	1	fref ·3 (20-50 MHz)	fref ·3 (20-50 MHz)	fref (6.67-16.67 MHz)
		0	1	1	fref ·3 (20-50 MHz)	fref ·3÷2 (10-25 MHz)	fref (6.67-16.67 MHz)
		1	0	1	fref ·3÷2 (10-25 MHz)	fref ·3 (20-50 MHz)	fref (6.67-16.67 MHz)
		1	1	1	fref ·3÷2 (10-25 MHz)	fref ·3÷2 (10-25 MHz)	fref (6.67-16.67 MHz)

a. fref is the input clock reference frequency (CCLK or XTAL)
b. QAx connected to FB_IN and FSELA=1, PWR_DN=1
c. QCx connected to FB_IN and FSELC=1, PWR_DN=1

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9330 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9330 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9330. Figure 3. illustrates a typical power supply filter scheme. The MPC9330 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CC_PLL} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V (V_{CC}=3.3V or V_{CC}=2.5V) must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 3. "V_{CC_PLL} Power Supply Filter" must have a resistance of 270Ω (V_{CC}=3.3V) or 9-10Ω (V_{CC}=2.5V) to meet the voltage drop criteria.

R_F = 270Ω for V_{CC} = 3.3V
R_F = 9–10Ω for V_{CC} = 2.5V

C_F = 1 µF for V_{CC} = 3.3V
C_F = 22 µF for V_{CC} = 2.5V

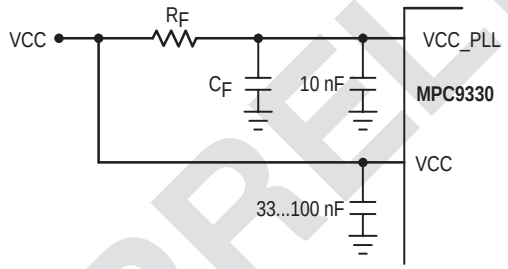


Figure 3. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3. "V_{CC_PLL} Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9330 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9330 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9330 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4. "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9330 clock driver is effectively doubled due to its capability to drive multiple lines.

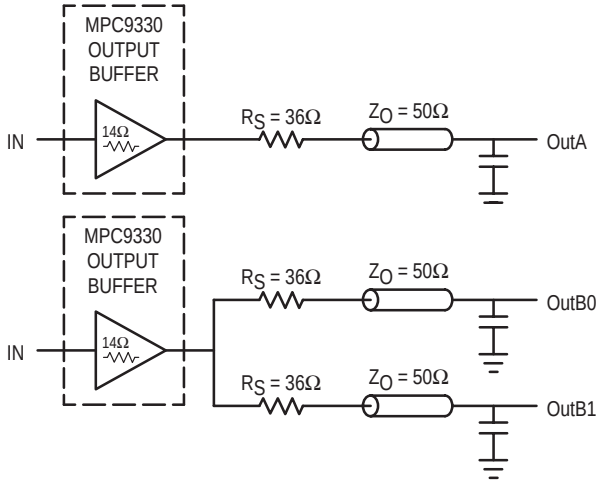


Figure 4. Single versus Dual Transmission Lines

The waveform plots in Figure 5. "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9330 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9330. The output waveform in Figure 5. "Single

versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \,||\, 50\Omega$$
$$R_S = 36\Omega \,||\, 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 (25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification.

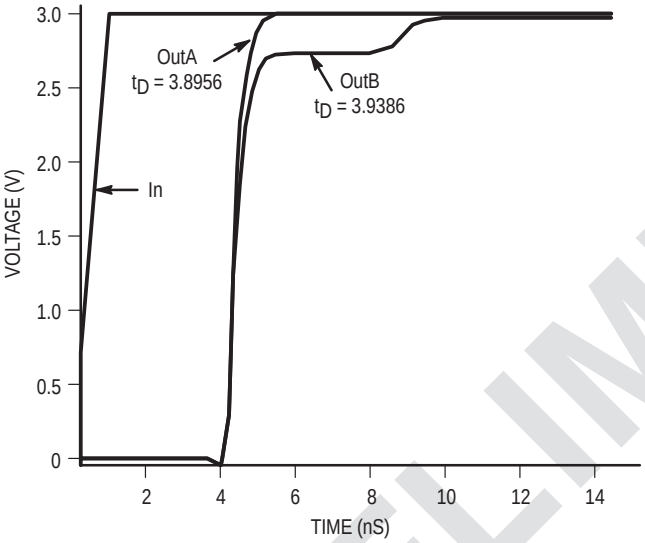
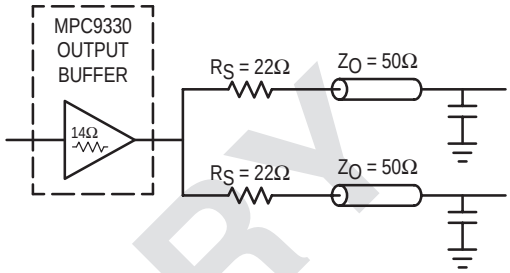


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6. "Optimized Dual Line Termination" should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\Omega + 22\Omega \,||\, 22\Omega = 50\Omega \,||\, 50\Omega$
$25\Omega = 25\Omega$

Figure 6. Optimized Dual Line Termination

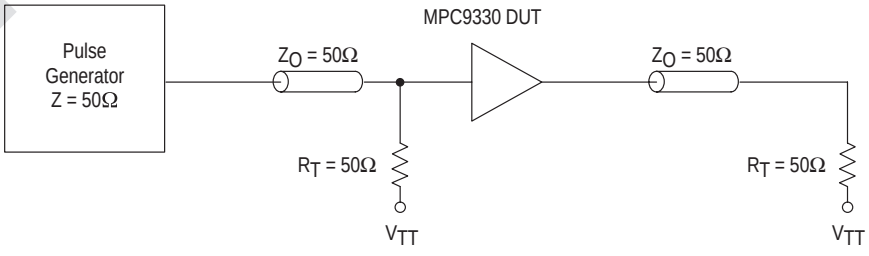
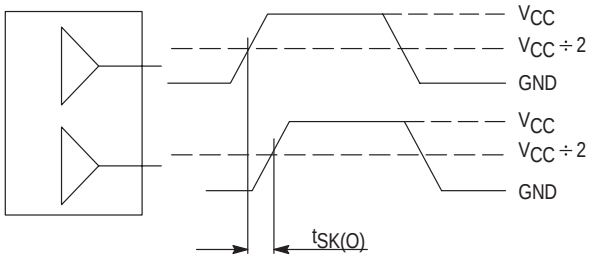


Figure 7. CCLK MPC9330 AC test reference for V_{CC} = 3.3V and V_{CC} = 2.5V



The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 8. Output–to–output Skew $t_{SK(O)}$

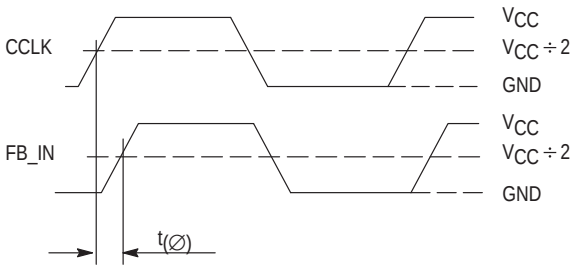
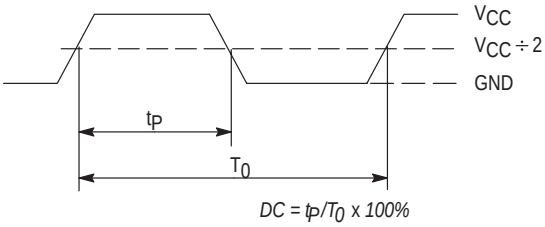
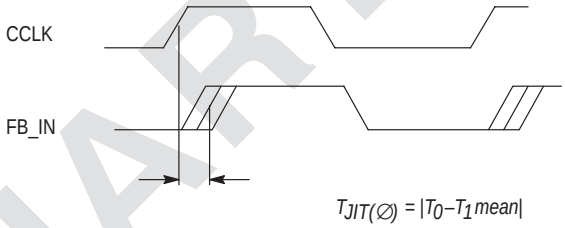


Figure 9. Propagation delay ($t_{(\varnothing)}$, static phase offset) test reference



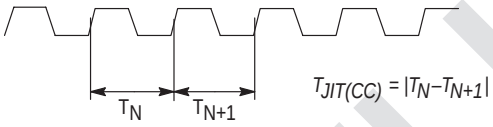
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 10. Output Duty Cycle (DC)



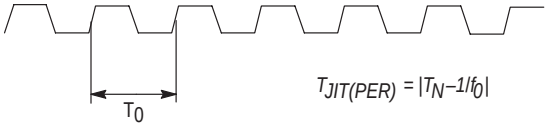
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 11. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 12. Cycle–to–cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 13. Period Jitter

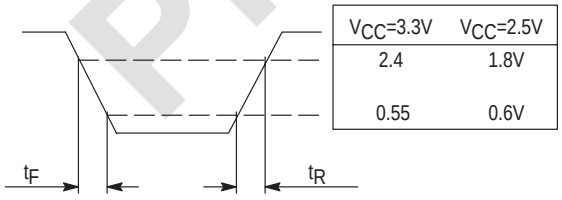
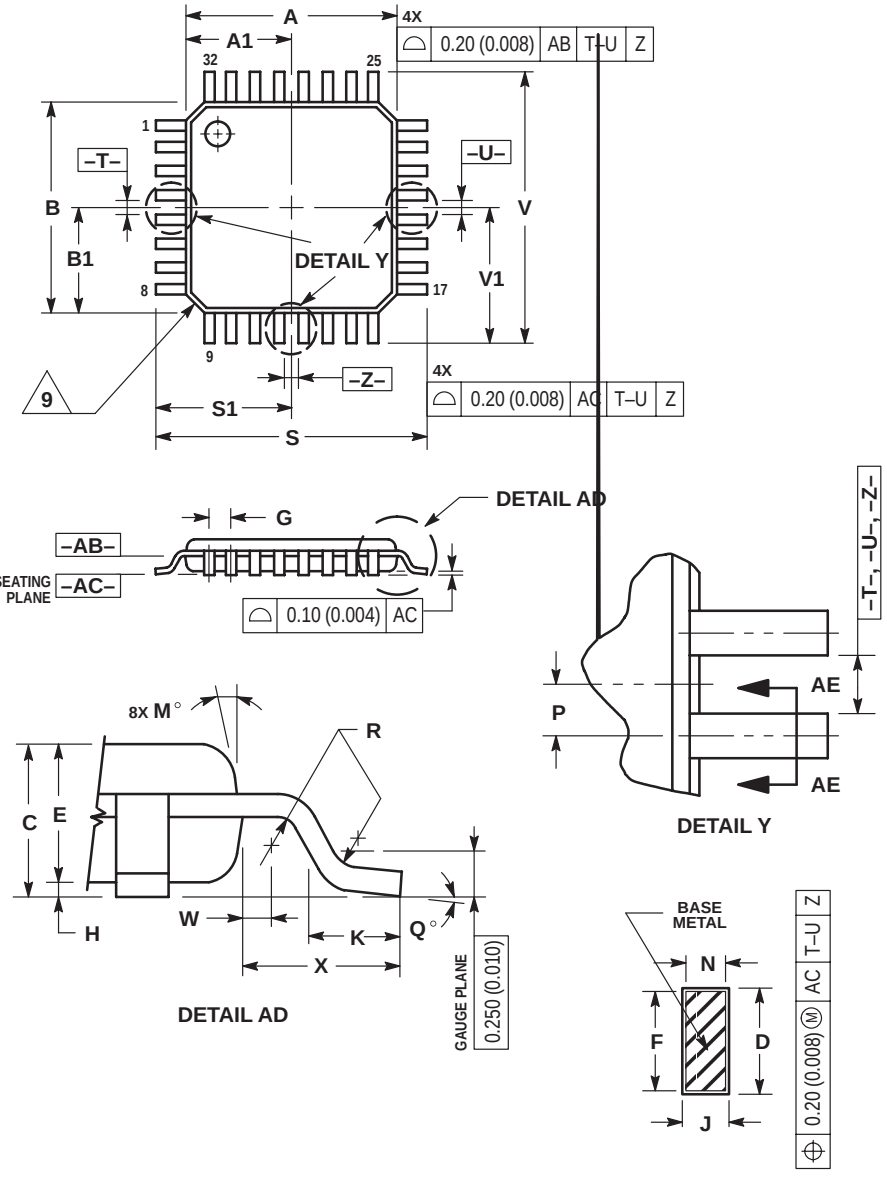


Figure 14. Output Transition Time Test Reference

OUTLINE DIMENSIONS

FA SUFFIX
LQFP PACKAGE
CASE 873A-02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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