



## MPD8020

### CMOS/DMOS Semicustom High-Voltage Array

#### Summary Information\*—Not Recommended for New Designs

### General Description

The Micrel MPD8020 is a *Smart Power* Application Specific Integrated Circuit (ASIC). The MPD8020 features an array of low-voltage CMOS analog and digital circuits and high-voltage DMOS power transistors on a monolithic integrated circuit. The MPD8020 provides the customer a proprietary design with size, reliability, performance advantages.

### Quick Turnaround

Prepared wafers can be held prior to the final process (metallization) where the customer's unique interconnect pattern is applied. This speeds turnaround by allowing many of the fabrication steps to be completed before the final design is finished.

### Voltage Ratings

The MPD8020's logic and analog circuitry operate from a single +5V to +15V supply. The high-voltage section operates from +20V to +100V. An optional internal charge pump, plus two external components, can drive the internal N-channel DMOS FET gates approximately 15V higher than the high-voltage supply as required by high-side switch applications.

### Fabrication Process

The MPD8020 CMOS/DMOS Semicustom High-Voltage Array uses Micrel's proprietary process which combines TTL/CMOS compatible high-speed CMOS logic, CMOS analog, bipolar analog, and high-voltage DMOS power devices in single IC.

### Package Options

- Dice
- 16-pin to 48-pin plastic DIPs
- 16-pin to 48-pin ceramic DIPs
- Ceramic LCCs
- PLCCs
- Surface mount packages
- Fused-lead PLCCs and DIPs
- Custom packages

### Support

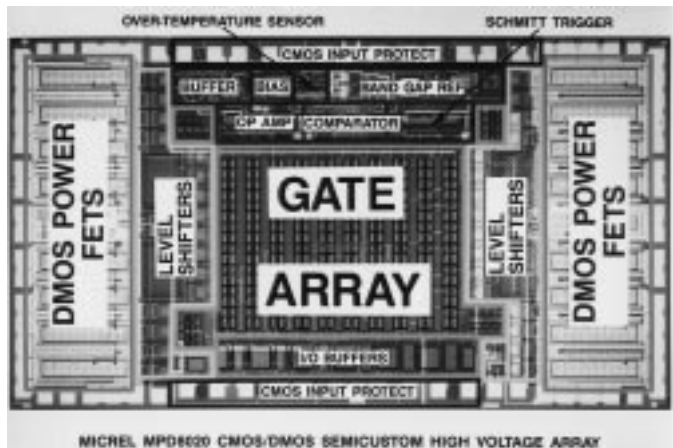
The MPD8020 is supported from concept to packaged ICs by Micrel's designers, CAD systems, CAE simulations (including SPICE, HILO, TIMVER), and an experienced fabrication and test group.

### Features

- Sixteen 100V, 200mA, 10 $\Omega$ , N-channel, DMOS power FETs with fully floating gates, drains, and sources
- DMOS can be paralleled for 100V, 3.2A, 0.625 $\Omega$ , single, half-bridge, full-bridge, or bilateral switches
- 200 uncommitted CMOS gates array
- Twelve TTL/CMOS I/O buffers
- Three op amp/comparator/Schmitt trigger circuits
- One unity-gain analog buffer
- 1.25V/2.5V bandgap reference
- Overtemperature sensor
- Charge pump (drives high-side switch gates above  $V_{DD}$ )
- Sixteen medium-current, current-sink drivers
- Sixteen high-voltage, level-shifting, high-side drivers
- Separate analog- and digital-ground pads
- Numerous logic, high-voltage,  $V_{CC}$ , and  $V_{DD}$  pads
- Resistors, capacitors, and a zener diode
- Military temperature specifications available
- Military, commercial, and power packages

### Applications

- Switch-mode regulators
- Motor control
- Bilateral analog switch
- High-voltage switch
- Relay and solenoid driver
- Smart switch with bus decoder
- Half- or full-bridge driver
- 3-phase driver
- Lamp driver
- Differential line driver
- Automotive switch
- Printer solenoid driver
- High-voltage display driver



MPD8020 CMOS/DMOS/Bipolar Semicustom Array

\* Contact Micrel for more information.

Patents 4,951,101; 4,979,001

## Available Macro Cells

- 16 fully floating 100V, 200mA, 10 $\Omega$  vertical-DMOS FETs
- 16 high-voltage 100V P- and N-channel level shifters (configured from 32 cross coupled 20mA to 50mA P- and N-channel pairs)
- 200 CMOS gates in an uncommitted gate array
  - over 30 pre-designed logic “templates” of shift registers, decoders, flip-flops, NAND gates, NOR gates, etc.
  - general purpose op amps, comparators, and Schmitt triggers, implemented in the gate array
- 12 TTL/CMOS I/O buffers
- 16 logic drivers (with logic enable) for bottom-side DMOS drive
- 3 configurable op amp/comparator/Schmitt trigger cells configurable as:
  - ground or  $V_{CC}$  sensing amplifiers or comparators
  - folded cascode high-performance amplifiers
  - NPN input amplifiers
  - programmable bandwidth/power consumption amplifiers
- Unity-gain buffer with adaptive bias (to drive large loads with minimum quiescent current)
- 1.25V bandgap reference plus multiple programmable outputs up to  $V_{CC}$
- Overtemperature protection circuit with programmable temperature trip points and hysteresis
- Master bias programming circuit for all the linears
- High-voltage  $V^{++}$  “doubler” for N-channel gate drive above the +100V  $V_{DD}$  supply
- Low-voltage ( $V_{CC}$ ) pass regulator to drive a local low-voltage analog and digital power supply from the high-voltage supply.
- Multiple current mirrors both at high (100V) and low (15V) levels
- Floating zener clamps, avalanche zeners, references and Schottky diodes
- Diffusion, diffusion P-well, pinched and poly resistors
- 40pF of on-chip capacitance
- Isolated PNP and NPN transistors

## Design Resources and Requirements

### Supplied by Micrel

- MPD8020 CMOS/DMOS Semicustom High-Voltage Array data sheet
- MPD8020 Kit Part #1 (Analog SSI and MSI Circuits)
  - 40-pin DIP kit parts with 11 commonly used analog circuits
  - Kit Part #1 data sheet with specification and application hints
- MPD8020 Kit Part #2 (Digital SSI and MSI Circuits)
  - 40-pin DIP kit parts with 8 revealing digital circuits for checking speed and digital timing characteristics (also some analog circuits implemented in the gate array)
  - Kit Part #2 data sheet with specification and application hints
- Highly experienced design and applications engineers on call to discuss how to optimize a complex analog, digital, and power circuit on one I.C.

### Requirements by Micrel

- System block diagram with basic I/O specifications, or...
- Schematic of circuit implemented with analog, digital, and discrete power transistors plus the I/O specification, or...
- Breadboard using Micrel kit parts plus “glue” logic and I/O specification, or...
- Spice and Hi-Low netlists or other compatible computer generated description and I/O specifications.

## Typical Semicustom Design Cycle

The typical design cycle follows exploratory discussions and contract initiation.

Week	Activity
2	Specification and customer interface
8	Design and customer interface
12	Electrical and layout computerized checks
14	Mask generation
16	Apply ASIC masks to preprocessed wafers
17	Wafer test
19	Packaged test units
20	Final test, QA and ship 25 units