

MPF970 MPF971

CASE 29-02, STYLE 5
TO-92 (TO-226AA)

JFET
SWITCHING

P-CHANNEL — DEPLETION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Reverse Gate-Source Voltage	V_{GSR}	30	Vdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation (at $T_A = 25^\circ\text{C}$ Derate above 25°C)	P_D	350 2.8	mW mW/ $^\circ\text{C}$
Storage Channel Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Temperature Range	$T_{channel}$	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Gate-Source Breakdown Voltage ($I_G = 1.0 \mu\text{Adc}$, $V_{DS} = 0$)	$V_{(BR)GSS}$	30	—	—	Vdc
Gate Reverse Current ($V_{GS} = 15 \text{ Vdc}$, $V_{DS} = 0$) ($V_{GS} = 15 \text{ Vdc}$, $V_{DS} = 0$, $T_A = 150^\circ\text{C}$)	I_{GSS}	— —	— —	1.0 1.0	nAdc μAdc
Drain-Cutoff Current ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 12 \text{ Vdc}$) ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 12 \text{ Vdc}$, $T_A = 150^\circ\text{C}$) ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 7.0 \text{ Vdc}$) ($V_{DS} = 15 \text{ Vdc}$, $V_{GS} = 7.0 \text{ Vdc}$, $T_A = 150^\circ\text{C}$)	$I_{D(off)}$	— — — —	— — — —	10 10 10 10	nAdc μAdc nAdc μAdc
Gate Source Cutoff Voltage ($V_{DS} = 15 \text{ Vdc}$, $I_D = 10 \text{ nAdc}$)	$V_{GS(off)}$	5.0 1.0	— —	12 7.0	Vdc

ON CHARACTERISTICS

Zero-Gate-Voltage Drain Current(1) ($V_{DS} = 20 \text{ Vdc}$, $V_{GS} = 0$)	I_{DSS}	15 2.0	— —	100 50	mAdc
Drain-Source On-Voltage ($I_D = 10 \text{ mAdc}$, $V_{GS} = 0$) ($I_D = 1.5 \text{ mAdc}$, $V_{GS} = 0$)	$V_{DS(on)}$	— —	— —	1.5 1.5	Vdc
Static Drain-Source On Resistance ($I_D = 1.0 \text{ mAdc}$, $V_{GS} = 0$)	$r_{DS(on)}$	— —	— —	100 250	Ohms

SMALL-SIGNAL CHARACTERISTICS

Drain-Source "ON" Resistance ($V_{GS} = 0$, $I_D = 0$, $f = 1.0 \text{ kHz}$)	$r_{ds(on)}$	— —	— —	100 250	Ohms
Input Capacitance ($V_{GS} = 12 \text{ Vdc}$, $V_{DS} = 0$, $f = 1.0 \text{ MHz}$) ($V_{GS} = 7.0 \text{ Vdc}$, $V_{DS} = 0$, $f = 1.0 \text{ MHz}$)	C_{iss}	— —	— —	12 12	pF
Reverse Transfer Capacitance ($V_{GS} = 12 \text{ Vdc}$, $V_{DS} = 0$, $f = 1.0 \text{ MHz}$) ($V_{GS} = 7.0 \text{ Vdc}$, $V_{DS} = 0$, $f = 1.0 \text{ MHz}$)	C_{rss}	— —	— —	5.0 5.0	pF

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ELECTRICAL CHARACTERISTICS (continued) ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (See Figure 6, $R_K = 0$) (1)					
Rise Time ($I_{D(on)} = 10\text{ mAdc}$, $V_{GS(off)} = 12\text{ Vdc}$) ($I_{D(on)} = 1.5\text{ mAdc}$, $V_{GS(off)} = 7.0\text{ Vdc}$)	t_r	—	2.0 3.0	5.0 5.0	ns
Fall Time ($I_{D(on)} = 10\text{ mAdc}$, $V_{GS(off)} = 12\text{ Vdc}$) ($I_{D(on)} = 1.5\text{ mAdc}$, $V_{GS(off)} = 7.0\text{ Vdc}$)	t_f	—	9.0 68	15 80	ns
Turn-On Time ($I_{D(on)} = 10\text{ mAdc}$, $V_{GS(off)} = 12\text{ Vdc}$) ($I_{D(on)} = 1.5\text{ mAdc}$, $V_{GS(off)} = 7.0\text{ Vdc}$)	t_{on}	—	3.5 5.0	8.0 10	ns
Turn-Off Time ($I_{D(on)} = 10\text{ mAdc}$, $V_{GS(off)} = 12\text{ Vdc}$) ($I_{D(on)} = 1.5\text{ mAdc}$, $V_{GS(off)} = 7.0\text{ Vdc}$)	t_{off}	—	13 88	25 120	ns

(1) Pulse Test: Pulse Width $\leq 100\text{ }\mu\text{s}$, Duty Cycle $\leq 1.0\%$.

FIGURE 1 – EFFECT OF I_{DSS} ON DRAIN-SOURCE RESISTANCE AND GATE-SOURCE VOLTAGE

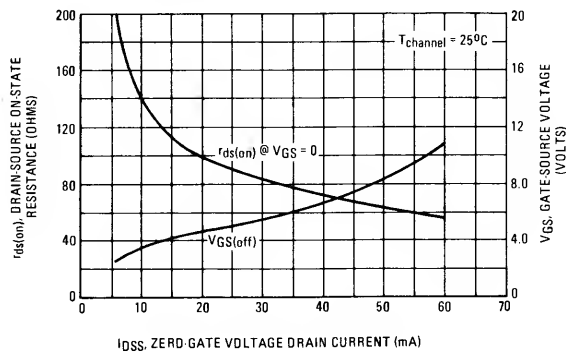


FIGURE 2 – TURN-ON DELAY TIME

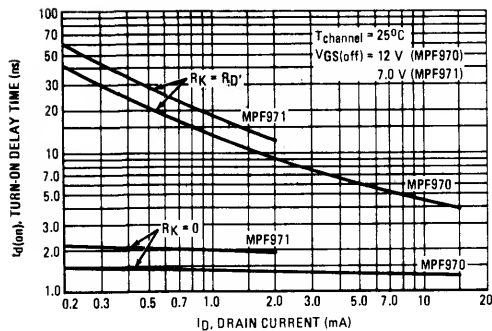
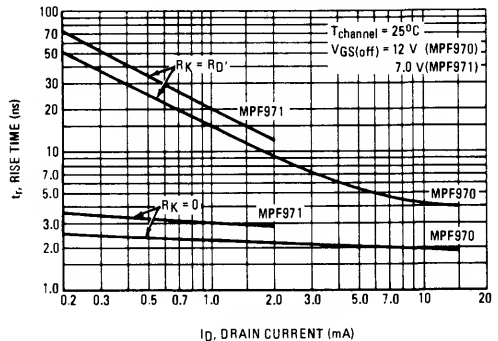


FIGURE 3 – RISE TIME



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FIGURE 4 – TURN-OFF DELAY TIME

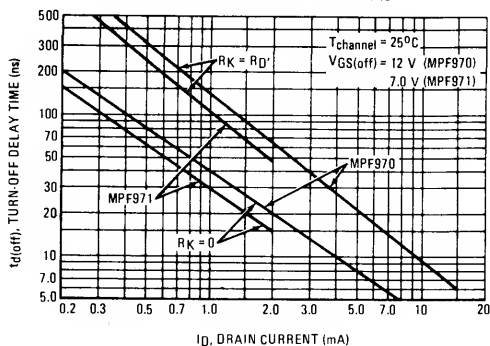


FIGURE 5 – FALL TIME

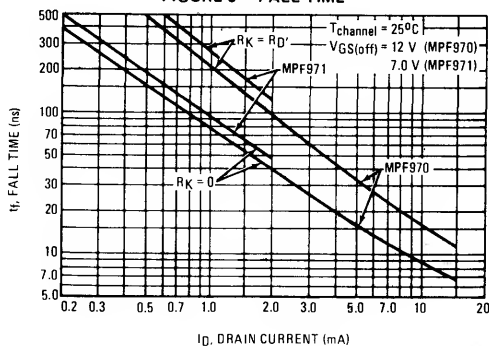
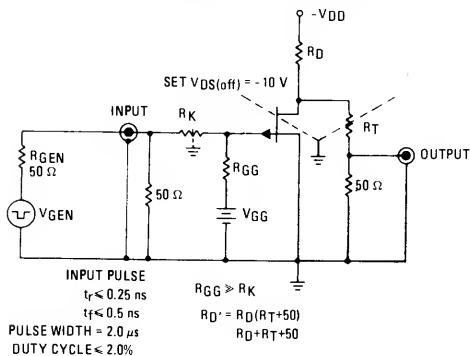


FIGURE 6 – SWITCHING TIME TEST CIRCUIT



NOTE 1

The switching characteristics shown above were measured using a test circuit similar to Figure 6. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ($+V_{GG}$). The Drain-Source Voltage (V_{DS}) is slightly lower than Drain Supply Voltage (V_{DD}) due to the voltage divider. Thus Reverse Transfer Capacitance (C_{rss}) or Gate-Drain Capacitance (C_{gd}) is charged to $V_{GG} + V_{DS}$.

During the turn-on interval, Gate-Source Capacitance (C_{gs}) discharges through the series combination of R_{GEN} and R_K . C_{gd} must discharge to $V_{DS(on)}$ through R_G and R_K in series with the parallel combination of effective load impedance (R_D') and Drain-Source Resistance (r_{ds}). During the turn-off, this charge flow is reversed.

Predicting turn-on time is somewhat difficult as the channel resistance r_{ds} is a function of the gate-source voltage. While C_{gs} discharges, V_{GS} approaches zero and r_{ds} decreases. Since C_{gd} discharges through r_{ds} , turn-on time is non-linear. During turn-off, the situation is reversed with r_{ds} increasing as C_{gd} charges.

The above switching curves show two impedance conditions; 1) R_K is equal to R_D , which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2) $R_K = 0$ (low impedance) the driving source impedance is that of the generator.

FIGURE 7 – TYPICAL FORWARD TRANSFER ADMITTANCE

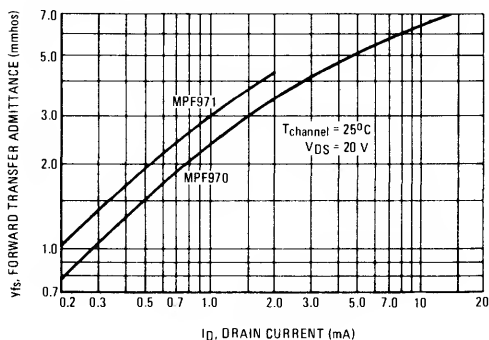


FIGURE 8 – TYPICAL CAPACITANCE

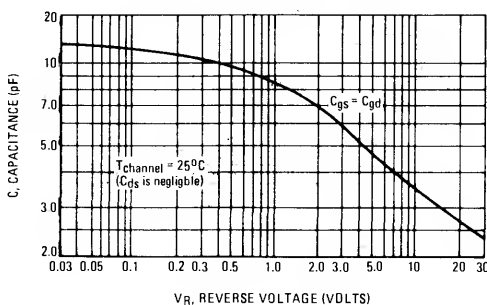


FIGURE 9 – EFFECT OF GATE-SOURCE VOLTAGE ON DRAIN-SOURCE RESISTANCE

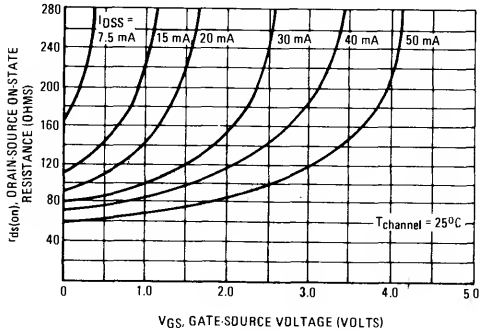


FIGURE 10 – EFFECT OF TEMPERATURE ON DRAIN-SOURCE ON STATE RESISTANCE

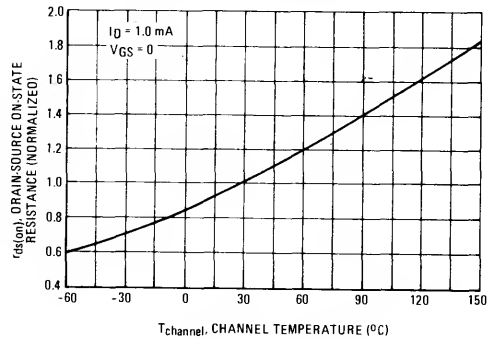


FIGURE 11 – LOW FREQUENCY CIRCUIT MODEL

