



# Quad 2-Input OR Gate

**ELECTRICALLY TESTED PER:**  
MPG 1664 (-30°C to +85°C)

- $P_D = 240$  mW typ/pkg
- $t_{pd} = 0.9$  ns typ (510 ohm load)  
= 1.1 ns typ (50 ohm load)
- Full Load Current,  $I_L = -25$  mAdc max

ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage ( $V_{CC} = 0$ )	$V_{CC}$	-8.0	0	Vdc
Base Input Voltage ( $V_{CC} = 0$ )	$V_{IN}$	0	$V_{EE}$	Vdc
Output Source Current Continuous	$I_O$		< 40	mAdc
Storage Temperature Range	$T_{stg}$	-55	+125	°C
Operating Temperature Range	$T_A$	-30	+85	°C

### PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
$V_{CC1}$	1	5	GND
AOUT	2	6	51 $\Omega$ to $V_{TT}$
BOUT	3	7	51 $\Omega$ to $V_{TT}$
A <sub>IN1</sub>	4	8	GND
A <sub>IN2</sub>	5	9	OPEN
B <sub>IN1</sub>	6	10	GND
B <sub>IN2</sub>	7	11	OPEN
VEE	8	12	VEE
N.C.	9	13	OPEN
C <sub>IN1</sub>	10	14	GND
C <sub>IN2</sub>	11	15	OPEN
D <sub>IN1</sub>	12	16	GND
D <sub>IN2</sub>	13	1	OPEN
C <sub>OUT</sub>	14	2	51 $\Omega$ to $V_{TT}$
D <sub>OUT</sub>	15	3	51 $\Omega$ to $V_{TT}$
$V_{CC2}$	16	4	GND

**BURN - IN CONDITIONS:**  
 $V_{TT} = -2.0$  V MAX /  $-2.2$  V MIN  
 $V_{EE} = -5.7$  V MAX /  $-5.2$  V MIN

**Military 1664**

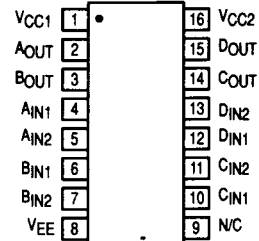


### AVAILABLE AS

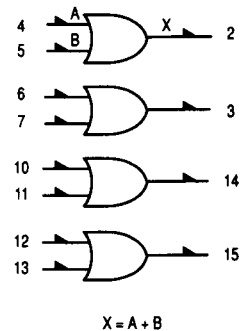
- 1) JAN: N/A
  - 2) SMD: N/A
  - 3) 883: N/A
  - 4) 1664/BXA \*
- X = CASE OUTLINE AS FOLLOWS:**

**PACKAGE: CERDIP: E**  
**CERFLAT: F**

\* 883 Processing (Non-Compliant)



### LOGIC DIAGRAM



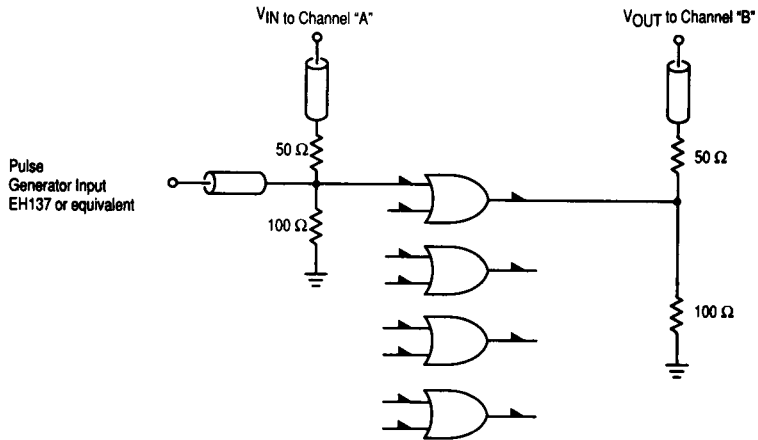


Figure 1. Test Circuit

## NOTES

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1. Coaxial cables (Equal lengths, typ 2 places) to scope.
2.  $t_r = t_f = 1.5 \text{ ns} \pm 0.2 \text{ ns}$ .
3. PRR = 20 MHz, 50% duty cycle.
4. Unused outputs connected to a 50 Ω resistor to ground.

Temp.	25°C	85°C	-30°C
$V_{ILL}$	0.31 V	0.337 V	0.285 V
$V_{IHH}$	1.11 V	1.185 V	1.041 V

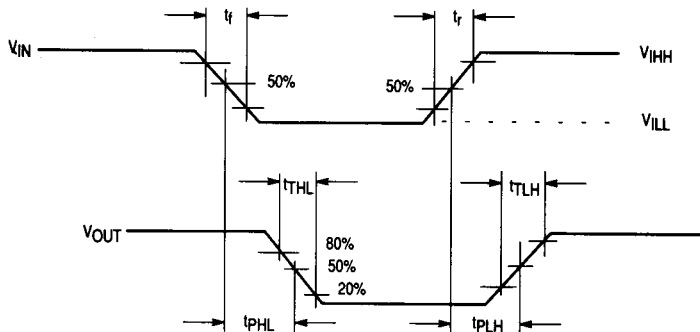


Figure 2. Test Circuit Waveforms

# 1664 QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IHA</sub>	V <sub>ILA</sub>	V <sub>EE</sub>	V <sub>EEA</sub>
T <sub>A</sub> = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2
T <sub>A</sub> = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2
T <sub>A</sub> = -30 °C	-0.875	-1.89	-1.160	-1.515	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
		+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments V <sub>CC</sub> = 0.0 V, Output Load = 50 Ω to - 2.0 V					
		Subgroup 1 Min	Subgroup 1 Max	Subgroup 2 Min	Subgroup 2 Max	Subgroup 3 Min	Subgroup 3 Max		V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IHA</sub>	V <sub>ILA</sub>	V <sub>CC</sub>	V <sub>EE</sub>
	<b>Functional Parameters:</b>													
V <sub>OH</sub>	High Output Voltage	-0.96	-0.81	-0.89	-0.7	-1.045	-0.875	V	4 - 7, 10 - 13			1, 16	8	2, 3, 14, 15
V <sub>OL</sub>	Low Output Voltage	-1.85	-1.62	-1.83	-1.575	-1.89	-1.65	V		4 - 7, 10 - 13		1, 16	8	2, 3, 14, 15
V <sub>OHA</sub>	High Output Voltage	-0.98	-0.81	-0.91	-0.7	-1.065	-0.875	V		4 - 7, 10 - 13		1, 16	8	2, 3, 14, 15
V <sub>OLA</sub>	Low Output Voltage	-1.85	-1.60	-1.83	-1.555	-1.89	-1.63	V			4 - 7, 10 - 13	1, 16	8	2, 3, 14, 15
I <sub>EE</sub>	Power Supply Drain Current	-56						mA				1, 16	8	8
I <sub>INH</sub>	Input Current High		350					µA	4 - 7, 10 - 13			1, 16	8	4 - 7, 10 - 13
I <sub>INL</sub>	Input Current Low	0.5						µA		4 - 7, 10 - 13		1, 16	8	4 - 7, 10 - 13

# 1664 QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)							
	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IHA</sub>	V <sub>ILA</sub>	V <sub>EE</sub>	V <sub>EEL</sub>	V <sub>CC</sub>	V <sub>CEL</sub>
T <sub>A</sub> = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2	+2.0	+2.0
T <sub>A</sub> = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2	+2.0	+2.0
T <sub>A</sub> = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2	+2.0	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
		+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND				
		Subgroup 9	Subgroup 10	Subgroup 11	Subgroup 12	Subgroup 13	Subgroup 14						
t <sub>TLH</sub>	Rise Time	2.1	2.3	2.2	2.2	ns	V <sub>IN</sub>	V <sub>OUT</sub>	V <sub>CC</sub>	V <sub>EEA</sub>	P.U.T.		
t <sub>THL</sub>	Fall Time	2.1	2.3	2.2	2.2	ns	5, 6, 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15		
t <sub>PHL</sub>	Propagation Delay High to Low	0.6	1.7	0.6	1.9	0.6	1.8	ns	5, 6, 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t <sub>PLH</sub>	Propagation Delay Low to High	0.6	1.5	0.6	1.7	0.6	1.6	ns	5, 6, 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15



PACKAGE OUTLINE DIMENSIONS (continued)

**P SUFFIX  
PLASTIC PACKAGE  
CASE 646-06**

NOTE 1

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.29	1.01	0.015	0.039

NOTES:  
 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.  
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.  
 3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.  
 4. ROUNDED CORNERS OPTIONAL.

**P SUFFIX  
PLASTIC PACKAGE  
CASE 648-08**

SEATING PLANE

±0.25 (0.010) T A

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.  
 3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.  
 4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.  
 5. ROUNDED CORNERS OPTIONAL.

**P SUFFIX  
PLASTIC PACKAGE  
CASE 649-03**

**(PW SUFFIX  
FOR MC10H181  
ONLY)**

SEATING PLANE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	10°		10°	
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:  
 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.  
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

**F SUFFIX  
CERAMIC PACKAGE  
CASE 650-05**

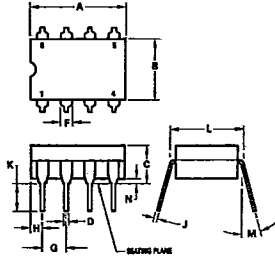
SEATING PLANE

±0.13 (0.005) T A B

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.90	0.370	0.390
B	6.73	6.80	0.265	0.269
C	1.53	2.15	0.060	0.085
D	0.38	0.48	0.014	0.019
G	1.27 BSC		0.050 BSC	
H	0.64	0.01	0.025	0.040
J	0.11	0.17	0.004	0.007
K	6.35	9.39	0.250	0.370
L	18.93	—	0.745	—
N	—	0.50	—	0.020

NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.  
 3. DIMENSION "A" AND "B" ALLOW FOR LID MISALIGNMENT, AND GLASS MENISCUS.  
 4. DIMENSION "H" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.  
 5. LEAD NUMBER 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.  
 6. DIMENSION "J" INCLUDES SOLDER LEAD FINISH.  
 7. LEAD NUMBERS SHOWN FOR REFERENCE ONLY.

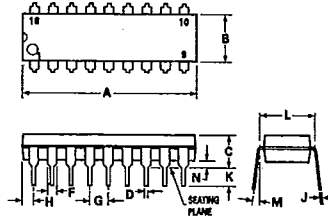
**L SUFFIX  
CERAMIC PACKAGE  
CASE 693-02**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.91	10.92	0.350	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	2.18	4.08	0.125	0.160
L	7.37	7.87	0.290	0.310
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

- NOTES:  
 1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.  
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

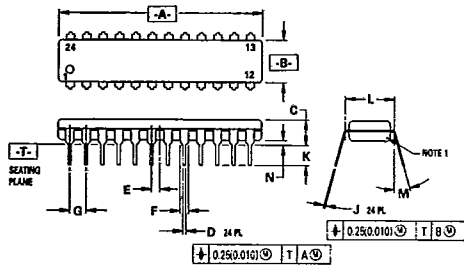
**P SUFFIX  
PLASTIC PACKAGE  
CASE 707-02**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

- NOTES:  
 1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.  
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.  
 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

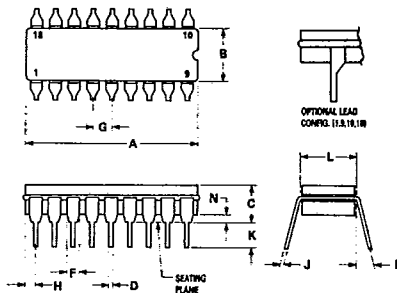
**P SUFFIX  
PLASTIC PACKAGE  
CASE 724-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.68	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

- NOTES:  
 1. CHAMFERED CONTOUR OPTIONAL.  
 2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.  
 3. DIMENSIONS AND TOLERANCES PER ANSI Y14.34, 1982.  
 4. CONTROLLING DIMENSION: INCH.

**L SUFFIX  
CERAMIC PACKAGE  
CASE 726-04**



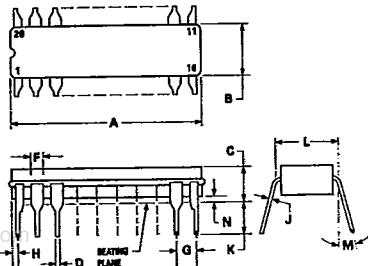
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

- NOTES:  
 1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.  
 2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.  
 3. DIM "A" & "B" INCLUDES MENISCUS.  
 4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

PACKAGE OUTLINE DIMENSIONS (continued)

1

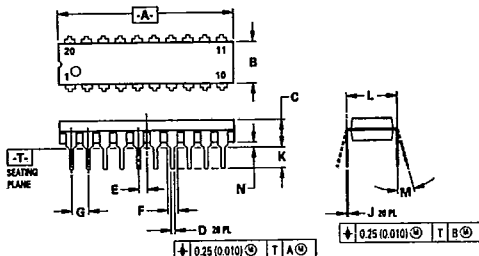
**L SUFFIX  
CERAMIC PACKAGE  
CASE 732-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.80	7.43	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

- NOTES:  
 1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.  
 2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.  
 3. DIM A AND B INCLUDES MENISCUS.

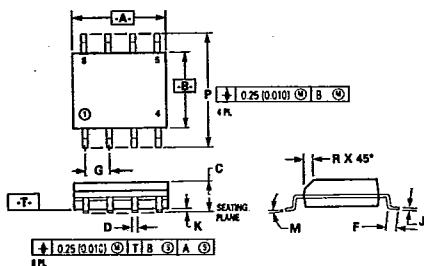
**P SUFFIX  
PLASTIC PACKAGE  
CASE 738-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.55	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.38	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.  
 3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.  
 4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

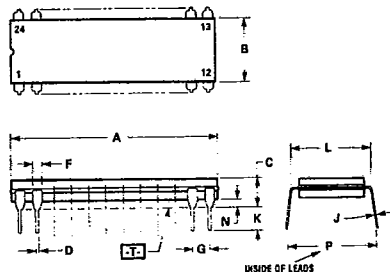
**D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.90	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.015	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- NOTES:  
 1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.  
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 3. CONTROLLING DIM: MILLIMETER.  
 4. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.  
 5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

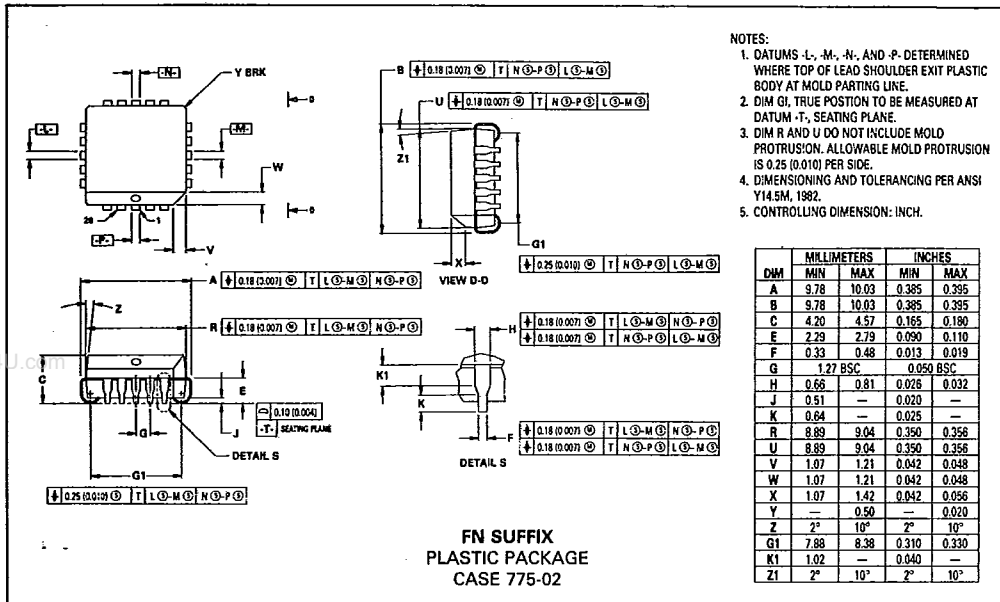
**L SUFFIX  
CERAMIC PACKAGE  
CASE 758-01**



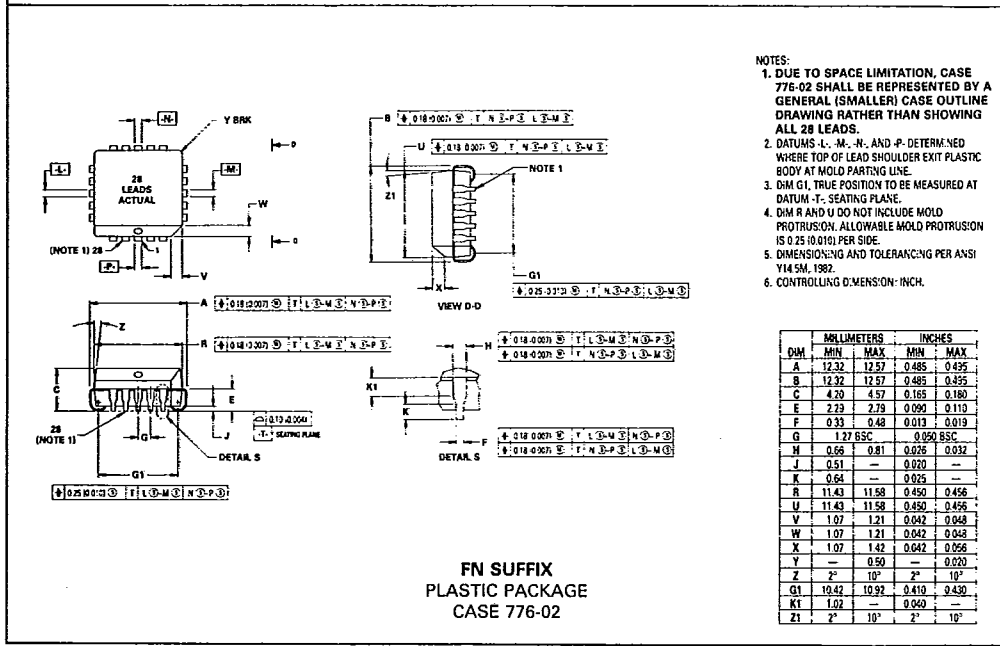
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.64	1.240	1.285
B	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.97	0.045	0.062
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
P	9.14	10.16	0.360	0.400

- NOTES:  
 1. DIMENSION A IS DATUM.  
 2. POSITIONAL TOLERANCE FOR LEADS: 24 PLACES  
 $\pm 0.25(0.010) \text{ } \textcircled{T} \text{ } \textcircled{A} \text{ } \textcircled{B}$   
 3.  $\textcircled{T}$  IS SEATING PLANE.  
 4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.  
 5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.





- NOTES:
- DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
  - DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
  - DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
  - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.



- NOTES:
- DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.
  - DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
  - DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
  - DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
  - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.

# MECL Logic Surface Mount

## WHY SURFACE MOUNT?

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

## MECL AVAILABILITY IN SURFACE MOUNT

Motorola is now offering MECL 10K and MECL 10KH in the PLCC (Plastic Leaded Chip Carrier) packages.

MECL in PLCC may be ordered in conventional plastic rails or on Tape and Reel. Refer to the Tape and Reel section for ordering details.

## TAPE AND REEL

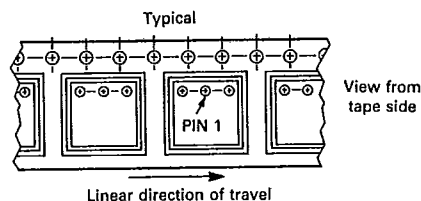
Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. The packaging fully conforms to

the latest EIA RS-481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.

## GENERAL INFORMATION

- Reel Size 13 inch (330 mm) Suffix: R2
- Tape Width 16 mm
- Units/Reel 1000

## MECHANICAL POLARIZATION



## ORDERING INFORMATION

- Minimum Lot Size/Device Type = 3000 Pieces.
- No Partial Reel Counts Available.
- To order devices which are to be delivered in Tape and Reel, add the appropriate suffix to the device number being ordered.

### EXAMPLE:

#### ORDERING CODE

- MC10100FN
- MC10100FNR2
- MC10H100FN
- MC10H100FNR2
- MC12015D
- MC12015DR2

#### SHIPMENT METHOD

- Magazines (Rails)
- 13 inch Tape and Reel
- Magazines (Rails)
- 13 inch Tape and Reel
- Magazines (Rails)
- 13 inch Tape and Reel

## DUAL-IN-LINE PACKAGE TO PLCC PIN CONVERSION DATA

The following tables give the equivalent I/O pinouts of Dual-In-Line (DIL) packages and Plastic Leaded Chip Carrier (PLCC) packages.

### Conversion Tables

16 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
20 PIN PLCC	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

20 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

24 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
28 PIN PLCC	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28