MPQ2022A

40V, 300mA Dual-Channel LDO with Serial Digital Interface and ADC for Digital Diagnosis and Protection, AEC-Q100 Qualified

DESCRIPTION

The MPQ2022A is a dual-channel, low-dropout (LDO) regulator with a serial digital interface and one-time programmable (OTP) memory. The device provides phantom power to low-noise amplifiers (LNAs) for active antennas in automotive systems, and can work in cold-crank (4.5V) up to load-dump (40V) input voltage (V_{IN}) conditions.

The MPQ2022A delivers up to 300mA per channel with excellent load and line regulation. The low, 35µA quiescent current (I_Q) makes the device well-suited for power supplies that are always turned on.

The MPQ2022A's dual LDO outputs are configurable via the serial digital interface. The output voltage (V_{OUTx}, where x = 1 or 2) can be set between 1V and 13.6V. The various parameters can be adapted by writing the settings in the device.

During bench evaluations, different configurations can be easily obtained via the serial digital interface, instead of reworking external components. Once the optimal settings have been set, the multi-page OTP can permanently store the settings.

The MPQ2022A is available in a QFN-16 (4mmx4mm) package with wettable flanks.

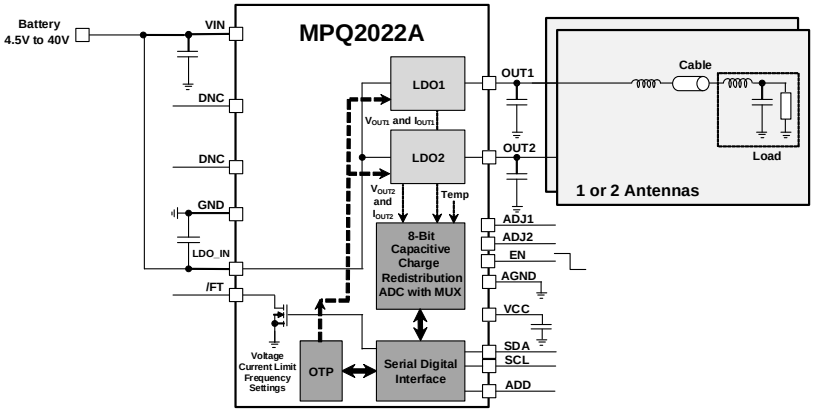
FEATURES

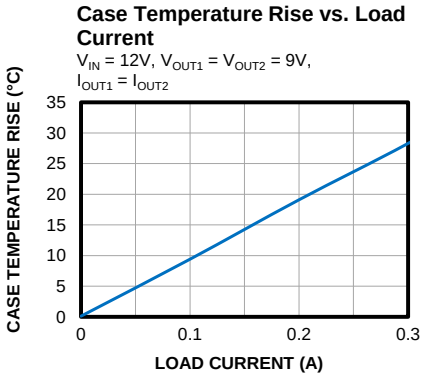
- Powerful Digital Capabilities:
  - No External Resistor Network for Output Voltage (V_{OUT}) Settings
  - Configurable, Dual Low-Dropout (LDO) Regulators:
    - 300mA Continuous Output Current (I_{OUTx}) Per Channel
    - 1V to 13.6V V_{OUTx} Range
    - Over-Temperature Protection
  - Serial Digital Interface
  - Analog-to-Digital Converter (ADC) for LDO Output Voltages and Load Currents
  - Multi-Page One-Time Programmable (OTP) Memory
- Designed for Automotive Applications:
  - Available in AEC-Q100 Grade 1
- Additional Features:
  - Wide 4.5V to 40V Input Voltage (V_{IN}) Range
  - Low, 35µA Quiescent Current (I_Q)
  - Soft-Start (SS) Feature for All Regulator Outputs
  - LDO Short-to-Battery Detection
  - Open-Load Detection
  - Available in a QFN-16 (4mmx4mm) Package
  - Available with Wettable Flank Package

APPLICATIONS

- Automotive Antenna Phantom Power
- Automotive Cameras
- Automotive Advanced Driver-Assistance Systems (ADAS) with Functional Safety and ASIL Requirements

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MPQ2022AGRE-xxxx-AEC1**	QFN-16 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ2022AGRE-xxxx-AEC1-Z).

** "xxxx" is the configuration code identifier for the register settings stored in the OTP register. Each "x" can be a hexadecimal value between 0 and F. The default code is "-0000." Contact an MPS FAE to create this unique number.

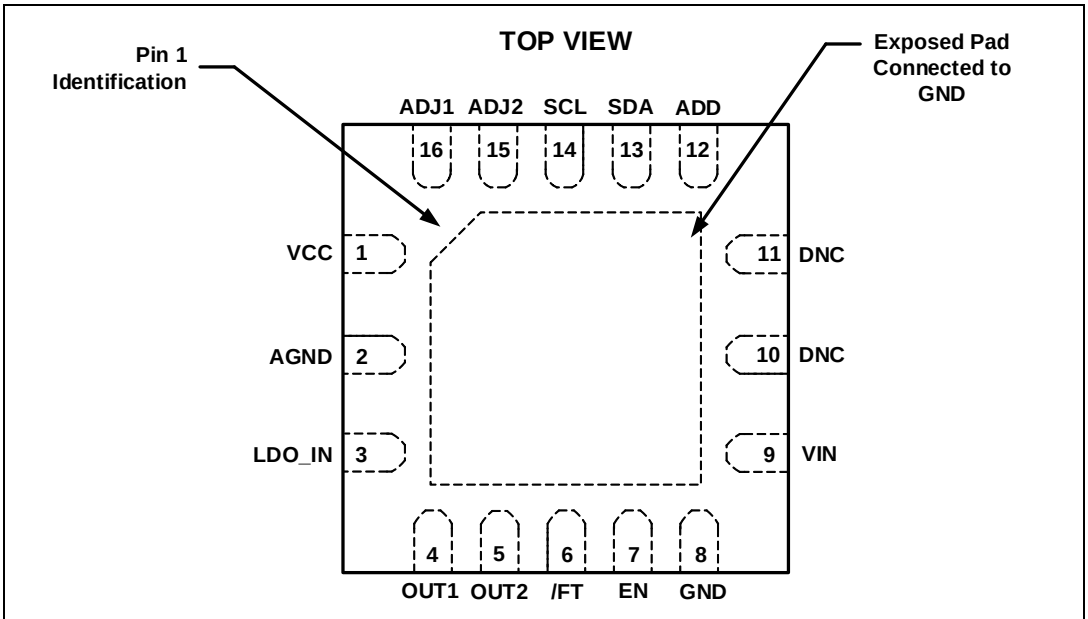
*** Moisture Sensitivity Level Rating

TOP MARKING

MPSYWW
M2022A
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M2022A: Part number
LLLLLL: Lot number
E: Wettable Flank

PACKAGE REFERENCE



QFN-16 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VCC	**Bias supply.** The VCC pin is a 5V, internal regulator output that supplies power to the serial digital interface, internal control circuit, and gate drivers. Connect an external, low-ESR decoupling capacitor from VCC to ground, placed closed to VCC. A 1µF to 10µF ceramic capacitor is recommended.
2	AGND	**Analog ground.** The AGND pin is the ground for the internal logic and signal control blocks.
3	LDO_IN	**Supply input of the dual LDOs.** Connect the LDO_IN pin to VIN. In addition, connect a 1µF to 10µF ceramic capacitor from LDO_IN to ground.
4	OUT1	**LDO1 output.** For stability, place a low-value ceramic capacitor at the OUT1 pin to act as an output capacitor. A 10µF ceramic capacitor is recommended for most applications.
5	OUT2	**LDO2 output.** For stability, place a low-value ceramic capacitor at the OUT2 pin to act as an output capacitor. A 10µF ceramic capacitor is recommended for most applications.
6	/FT	**Fault pin output.** The /FT pin is an open-drain status pin. Connect /FT to a ≤5V voltage source via a resistor (e.g. 100kΩ). If not used, float /FT or connect it to ground.
7	EN	**Enable.** Pull the EN pin below the 2.2V falling threshold to shut down the chip. Pull EN above the 2.4V rising threshold to enable the chip. EN can be connected to VIN via a pull-up resistor (e.g. 100kΩ) to enable the chip. Float EN to disable the chip. EN also has an internal, 3.3MΩ pull-down resistor.
8	GND	**Power ground.** The GND pin is the reference ground for the regulated output voltage (V_{OUT}). For optimal thermal results, connect GND to larger copper areas.
9	VIN	**Input supply.** The VIN pin supplies power to the internal control circuitry. Connect VIN to the LDO_IN pin. In addition, place a decoupling capacitor connected to ground as close as possible to VIN.
10, 11	DNC	**Do not connect.** Reserved for factory functions. It is recommended to float the DNC pin.
12	ADD	**Address setting for the serial digital interface.** Connect a resistor from the ADD pin to ground to set the serial digital interface address. If not used, float the ADD pin.
13	SDA	**Serial digital interface data.** The SDA pin is an open-drain port. An external pull-up resistor is required to connect SDA to the serial digital interface bus's supply rail. If SDA is not used, it is recommended to connect the SDA pin to VCC via a resistor (e.g. 100kΩ).
14	SCL	**Serial digital interface clock.** The SCL pin is an open-drain port. An external pull-up resistor is required to connect SCL to the serial digital interface bus's supply rail. If SCL is not used, it is recommended to connect the pin to VCC via a resistor (e.g. 100kΩ).
15	ADJ2	**LDO2 reference voltage input.** In tracking mode for the LDO2 output voltage (V_{OUT2}), connect the ADJ2 pin directly to the voltage reference, or use a voltage divider for lower output values. If ADJ2 is not used, float this pin or connect it to ground.
16	ADJ1	**LDO1 reference voltage input.** In tracking mode for the LDO1 output voltage (V_{OUT1}), connect the ADJ1 pin directly to the voltage reference, or use a voltage divider for lower output values. If ADJ1 is not used, float this pin or connect it to ground.
-	Exposed Pad	**Exposed thermal power pad.** Connect the exposed pad (EP) to the ground plane for optimal heat dissipation. Do not use EP as the primary electrical ground connection.

ABSOLUTE MAXIMUM RATINGS (1)

VIN, SW, FB, LDO_IN.....
.....-0.3V to +45V
OUT1, OUT2.....-0.3V to +18V
All other pins .....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2) (6)
QFN-16 (4mmx4mm)..... 4W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM)
VCC to VIN ..... Class 1C (3)
Other pins .....Class 2 (3)
Charged device model (CDM) ..... Class C2b (4)

Recommended Operating Conditions

Input voltage (V_{IN}) .....4.5V to 40V
Output voltage (V_{OUT1}, V_{OUT2}) .....1V to 13.6V
Load current (I_{OUT1}, I_{OUT2}) 300mA
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-16 (4mmx4mm)
JESD51-5/7……..40.4….6...°C/W (5)
EVQ2022A-R-00A…….31….5.5..°C/W (6)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on JESD51-5/7, a 4-layer PCB, where a thermal via array is placed under the exposed pad. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-5/7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from junction-to-case bottom.
6) Measured on the EVQ2022A-R-00A, a 4-layer, 2oz PCB (8.8cmx8.8cm). The θ_{JC} value shows the thermal resistance from junction-to-case top.

ELECTRICAL CHARACTERISTICS

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Voltage and Current Parameters						
Input voltage	V_{IN}		4.5		40	V
Quiescent supply current	I_Q	LDO enabled, V_{OUT1} = V_{OUT2} = 9V, ADC disabled, no load, T_J = 25°C		35		µA
		LDO enabled, V_{OUT1} = V_{OUT2} = 9V, ADC disabled, no load, T_J = -40°C to +150°C			135	µA
Shutdown supply current	I_{SD}	V_{EN} = 0V			5	µA
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_VTH\_R}$			4.2		V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_VTH\_F}$			3.8		V
Thermal Shutdown and Over-Temperature Protection						
Thermal shutdown (7)	T_{SD}	Rising T_J		170		°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			20		°C
/FT						
/FT sink current capacity	V_{FT_SINK}	Sink 4mA			300	mV
/FT delay time	t_{FT_DELAY}	Rising edge		40		µs
		Falling edge		40		µs
/FT leakage current	I_{FT_LKG}			10	100	nA
Enable (EN)						
EN rising threshold	$V_{EN\_VTH\_R}$	Level-sensitive input	2.1	2.4	2.7	V
EN falling threshold	$V_{EN\_VTH\_F}$	Level-sensitive input	1.9	2.2	2.5	V
EN hysteresis threshold	V_{EN_HYS}			200		mV
EN input current	I_{EN}	V_{EN} = 2V		0.6	1.2	µA
Internal VCC						
VCC regulator	V_{CC}	I_{CC} = 0mA	4.8	5	5.2	V
Fault Detection						
Start-up short-to-battery detection window	t_{BLK_RC}	Default setting, register 0x0F, bits[7:6] = 00		15		ms
		Register 0x0F, bits[7:6] = 01		7		ms
		Register 0x0F, bits[7:6] = 10		3		ms
		Register 0x0F, bits[7:6] = 11		1		ms
Short-to-battery threshold	V_{STB}	V_{OUT} - V_{IN}, check during start-up sequence		-80	-10	mV
Dual Linear Regulator (LDO1 and LDO2)						
Regulated output range	V_{OUT1}, V_{OUT2}	Configurable range	1		13.6	V
		Default setting		9		V
Output voltage accuracy	ACC_{VOUT1}, ACC_{VOUT2}	Default setting, V_{OUT1}, V_{OUT2} = 9V, T_J = 25°C	-2		+2	%
		Default setting, V_{OUT1}, V_{OUT2} = 9V, T_J = -40°C to +150°C	-3		+3	%
		V_{OUT1}, V_{OUT2} = 1V to 13.6V, T_J = 25°C	-3		+3	%
		V_{OUT1}, V_{OUT2} = 1V to 13.6V, T_J = -40°C to +150°C	-4		+4	%

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Line regulation	dV_{ALINE}	V_{IN} = 15V to 40V, 5mA load current, V_{OUT} = 9V,	-10	1	+10	mV
Load regulation	dV_{ALOAD}	I_{LOAD} = 5mA to 300mA, V_{OUT} = 9V, T_J = 25°C		30	50	mV
Power supply rejection ratio (7)	PSRR	I_{LOAD} = 100mA at 100Hz, V_{OUT} = 9V		60		dB
Dropout voltage	$V_{DROPOUT}$	I_{LOAD} = 100mA, measured between LDO_IN and OUTx, I_{OUT1} = no load and I_{OUT2} = 100mA or I_{OUT2} = no load and I_{OUT1} = 100mA, T_J = 25°C		250	400	mV
		I_{LOAD} = 100mA, measured between LDO_IN and OUTx, I_{OUT1} = no load and I_{OUT2} = 100mA or I_{OUT2} = no load and I_{OUT1} = 100mA, T_J = -40°C to +150°C			700	
Over-current limit	I_{LDO_LIMIT}	Configurable range	100		500	mA
		Default value		400		mA
Current limit accuracy	ACC_{ILDO_LIMIT}	LDO_IN - OUTx > $V_{DROPOUT}$, 500mA ≥ I_{LDO_LIMIT} > 200mA, T_J = 25°C	-10		+10	%
		LDO_IN - OUTx > $V_{DROPOUT}$, 500mA ≥ I_{LDO_LIMIT} > 200mA, T_J = -40°C to +150°C	-15		+15	
		LDO_IN - OUTx > $V_{DROPOUT}$, 100mA ≤ I_{LDO_LIMIT} ≤ 200mA, T_J = 25°C	-15		+15	
		LDO_IN - OUTx > $V_{DROPOUT}$, 100mA ≤ I_{LDO_LIMIT} ≤ 200mA, T_J = -40°C to +150°C	-20		+20	

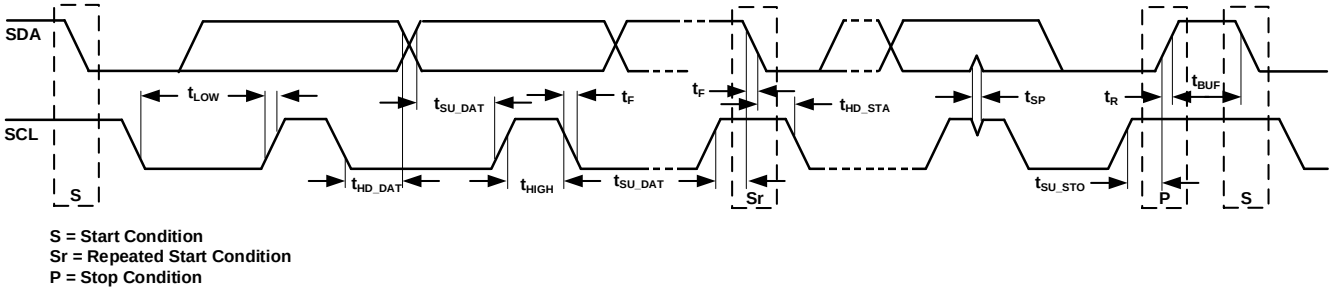
Note:

7) Not tested in production. Guaranteed by design and characterization.

SERIAL DIGITAL INTERFACE PORT SIGNAL CHARACTERISTICS

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Serial Digital Interface Specifications						
Input logic low	V_{IL}		0		0.4	V
Input logic high	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data set-up time	t_{SU_DAT}		100			ns
Data hold time	t_{HD_DAT}		0		0.9	µs
Set-up time for a repeated start condition	t_{SU_STA}		0.6			µs
Hold time for a start condition	t_{HD_STA}		0.6			µs
Bus free time between a start and stop condition	t_{BUF}		1.3			µs
Set-up time for a stop condition	t_{SU_STO}		0.6			µs
SCL and SDA rise time	t_R		20 + 0.1 x C_B		120	ns
SCL and SDA fall time	t_F		20 + 0.1 x C_B		120	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF



S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

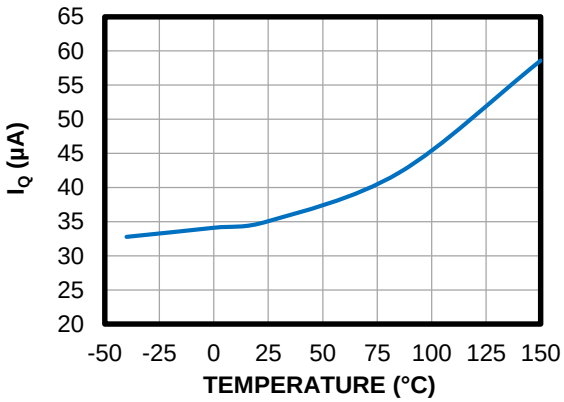
Figure 1: Serial Digital Interface-Compatible Interface Timing Diagram

TYPICAL CHARACTERISTICS

C_{IN} = 10µF, C_{OUT1}, C_{OUT2} = 10µF, V_{IN} = 13.5V, V_{OUT1}, V_{OUT2} = 9V, V_{EN} = 3V, T_A = 25°C, unless otherwise noted.

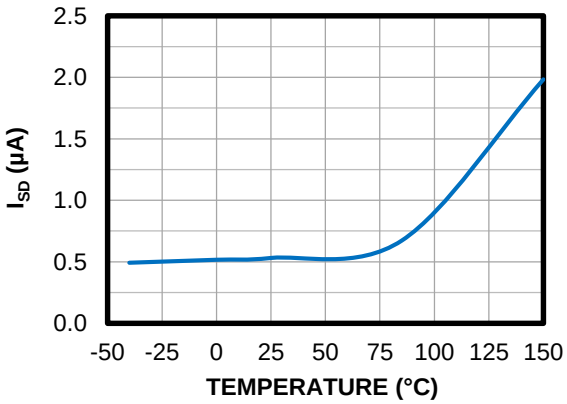
I_Q vs. Temperature

No load

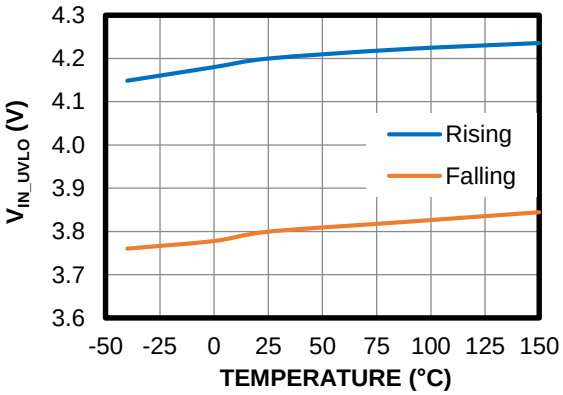


I_{SD} vs. Temperature

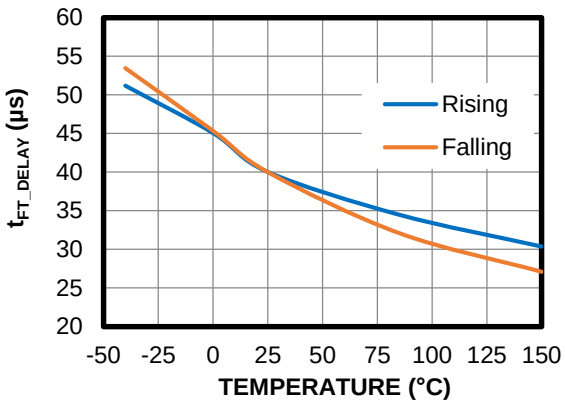
V_{IN} = 13.5V, V_{EN} = 0V



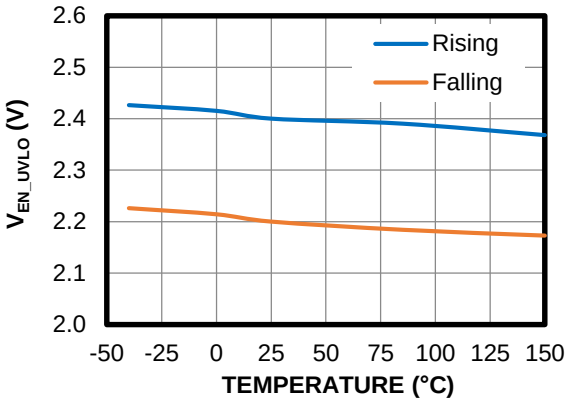
V_{IN} UVLO Threshold vs. Temperature



/FT Delay Time vs. Temperature

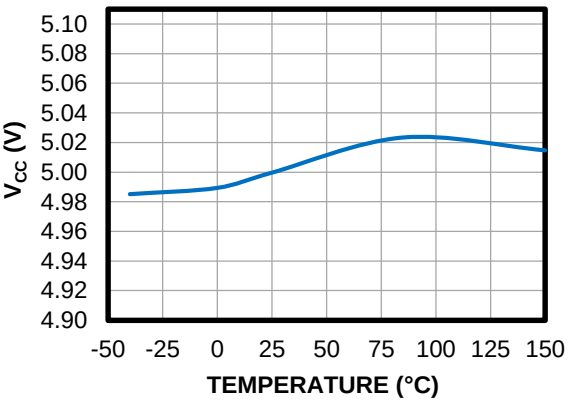


EN UVLO Threshold vs. Temperature



V_{CC} vs. Temperature

V_{IN} = 13.5V

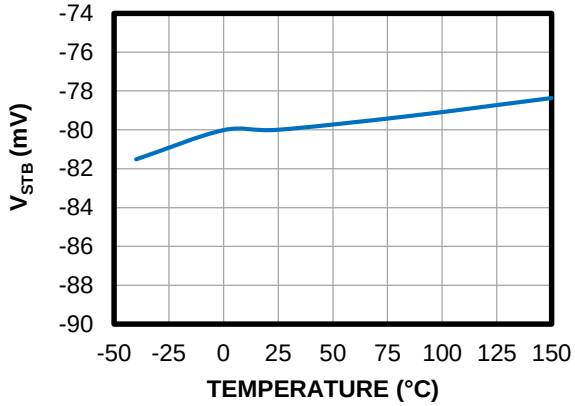


TYPICAL CHARACTERISTICS *(continued)*

C_{IN} = 10µF, C_{OUT1}, C_{OUT2} = 10µF, V_{IN} = 13.5V, V_{OUT1}, V_{OUT2} = 9V, V_{EN} = 3V, T_A = 25°C, unless otherwise noted.

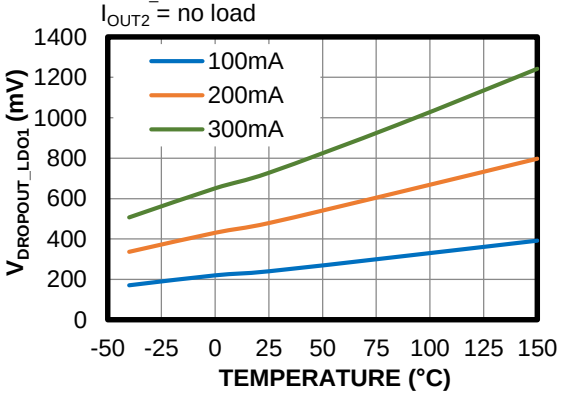
Short-to-Battery Threshold vs. Temperature

V_{OUT} - V_{IN}, check during start-up sequence



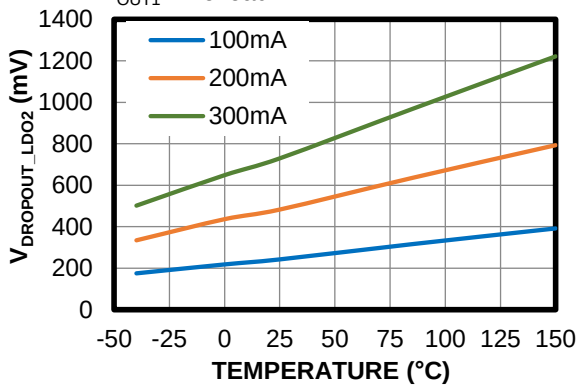
LDO1 Dropout Voltage vs. Ambient Temperature

V_{LDO_IN} = V_{OUT1} = V_{OUT2}, I_{OUT1} = load, I_{OUT2} = no load



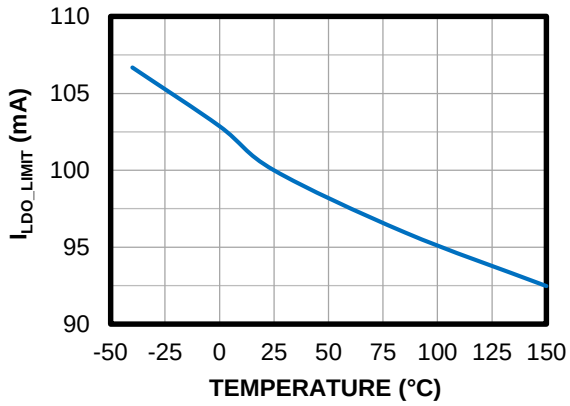
LDO2 Dropout Voltage vs. Ambient Temperature

V_{LDO_IN} = V_{OUT1} = V_{OUT2}, I_{OUT2} = load, I_{OUT1} = no load



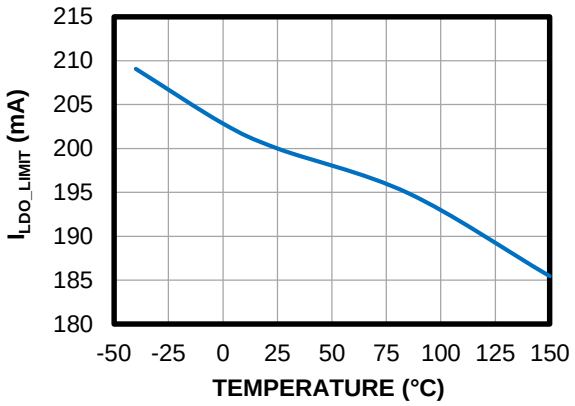
LDO Current Limit vs. Temperature

LDO current limit = 100mA



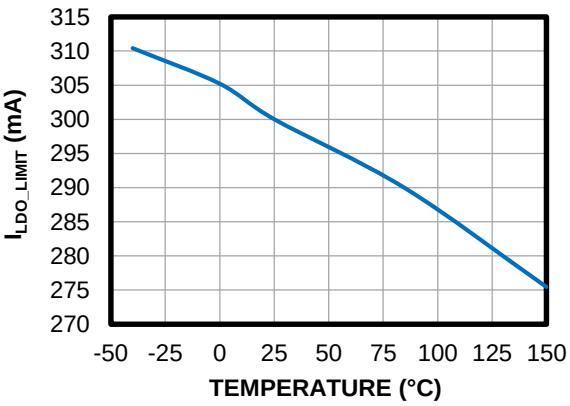
LDO Current Limit vs. Temperature

LDO current limit = 200mA



LDO Current Limit vs. Temperature

LDO current limit = 300mA

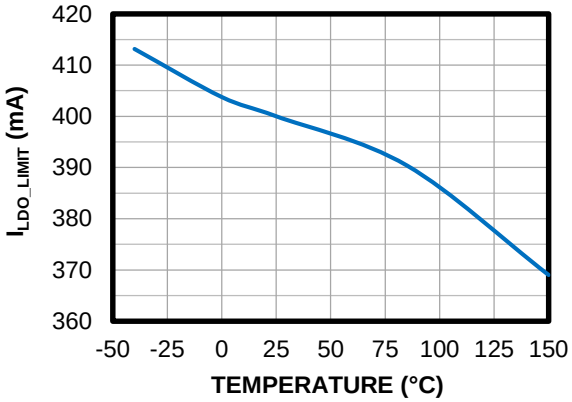


TYPICAL CHARACTERISTICS *(continued)*

C_{IN} = 10µF, C_{OUT1}, C_{OUT2} = 10µF, V_{IN} = 13.5V, V_{OUT1}, V_{OUT2} = 9V, V_{EN} = 3V, T_A = 25°C, unless otherwise noted.

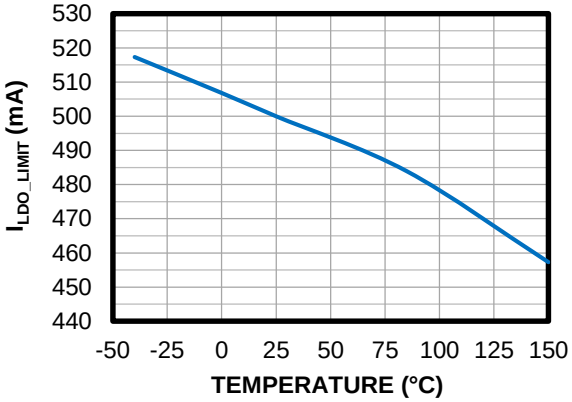
LDO Current Limit vs. Temperature

LDO current limit = 400mA



LDO Current Limit vs. Temperature

LDO current limit = 500mA

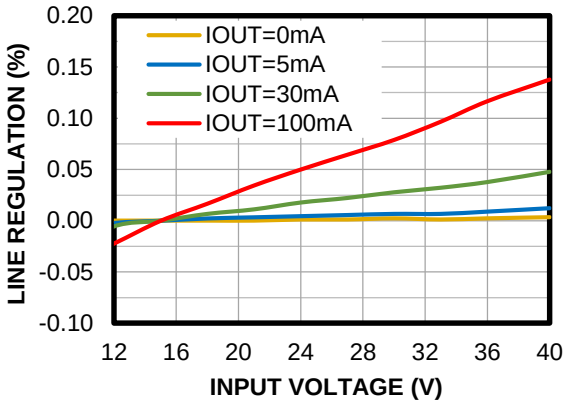


TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 10µF, C_{OUT1}, C_{OUT2} = 10µF, V_{IN} = 13.5V, V_{OUT1}, V_{OUT2} = 9V, V_{EN} = 3V, T_A = 25°C, unless otherwise noted.

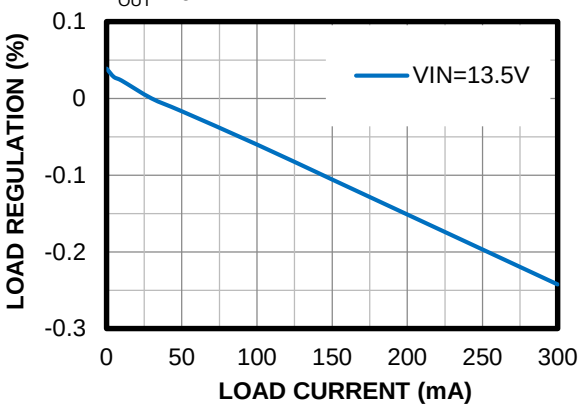
LDO Line Regulation

V_{OUT} = 9V



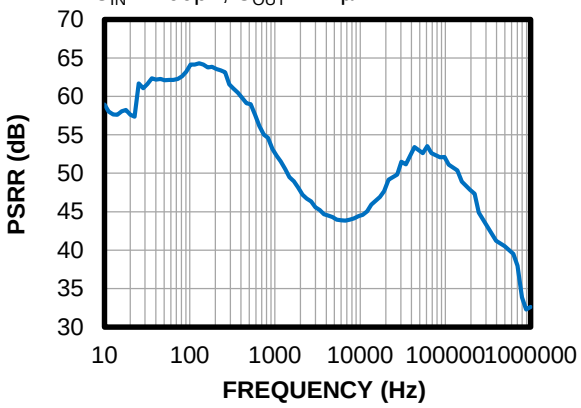
LDO Load Regulation

V_{OUT} = 9V



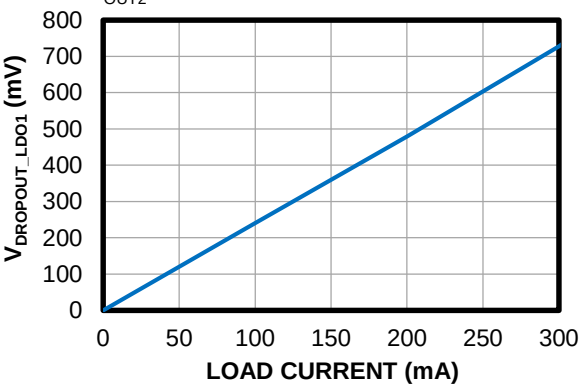
PSRR

V_{IN} = 13.5V, V_{OUT} = 9V, I_{OUT} = 5mA,
C_{IN} = 100pF, C_{OUT} = 22µF



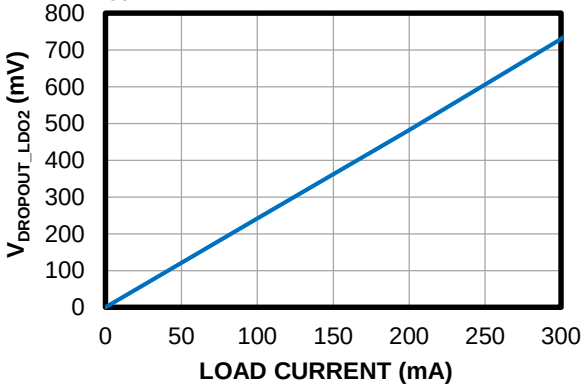
LDO1 Dropout Voltage vs. Load Current

V_{LDO_IN} = V_{OUT1} = V_{OUT2}, I_{OUT1} = load,
I_{OUT2} = no load



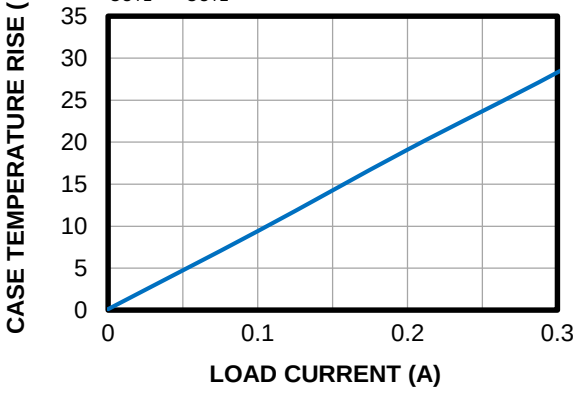
LDO2 Dropout Voltage vs. Load Current

V_{LDO_IN} = V_{OUT1} = V_{OUT2}, I_{OUT2} = load,
I_{OUT1} = no load



Case Temperature Rise vs. Load Current

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = 9V,
I_{OUT1} = I_{OUT2}

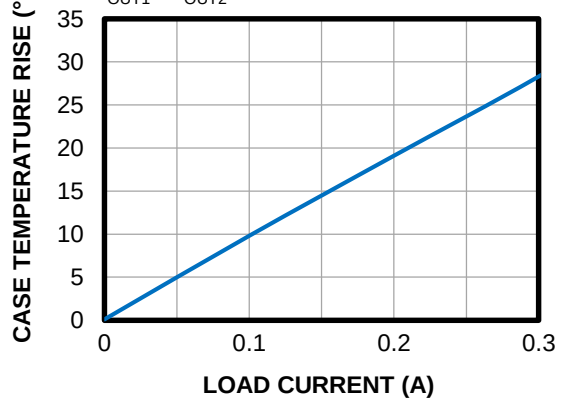


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF, C_{OUT1}, C_{OUT2} = 10µF, V_{IN} = 13.5V, V_{OUT1}, V_{OUT2} = 9V, V_{EN} = 3V, T_A = 25°C, unless otherwise noted.

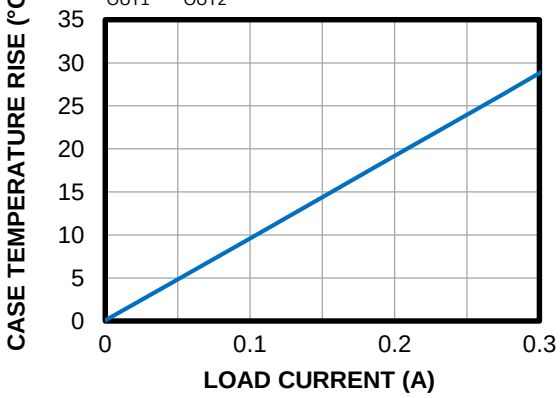
Case Temperature Rise vs. Load Current

V_{IN} = 8V, V_{OUT1} = V_{OUT2} = 5V, I_{OUT1} = I_{OUT2}



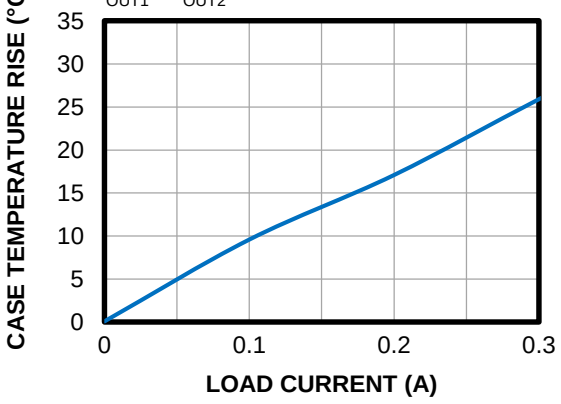
Case Temperature Rise vs. Load Current

V_{IN} = 15V, V_{OUT1} = V_{OUT2} = 12V, I_{OUT1} = I_{OUT2}



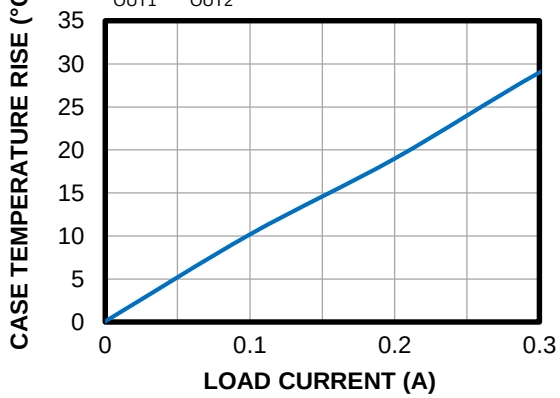
Case Temperature Rise vs. Load Current

V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 3.3V, I_{OUT1} = I_{OUT2}



Case Temperature Rise vs. Load Current

V_{IN} = 16.5V, V_{OUT1} = V_{OUT2} = 13.6V, I_{OUT1} = I_{OUT2}

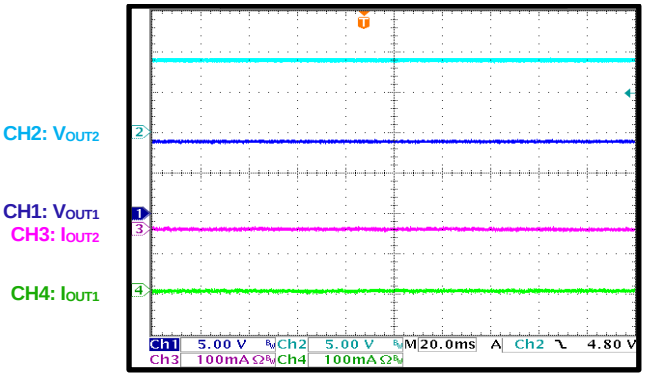


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF, C_{OUT1}, C_{OUT2} = 10µF, V_{IN} = 13.5V, V_{OUT1}, V_{OUT2} = 9V, V_{EN} = 3V, T_A = 25°C, unless otherwise noted.

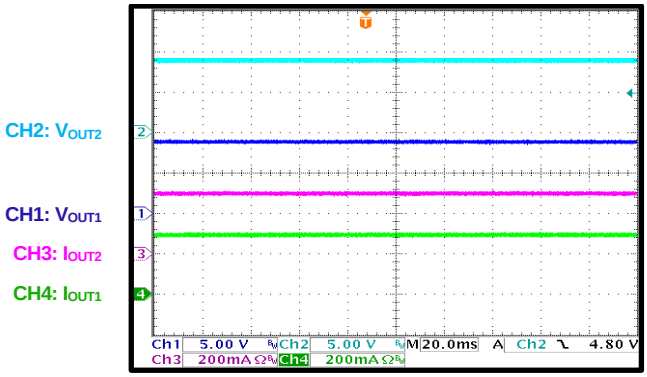
Steady State

I_{OUT1} = I_{OUT2} = 0A



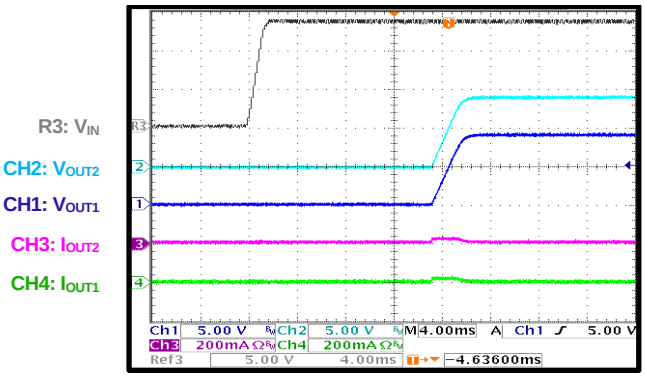
Steady State

I_{OUT1} = I_{OUT2} = 0.3A



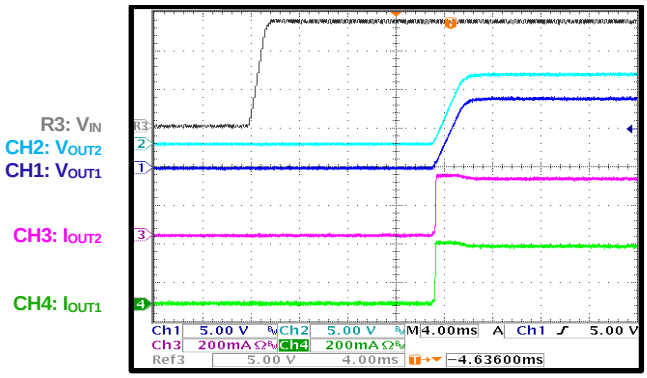
Start-Up through VIN

I_{OUT1} = I_{OUT2} = 0A



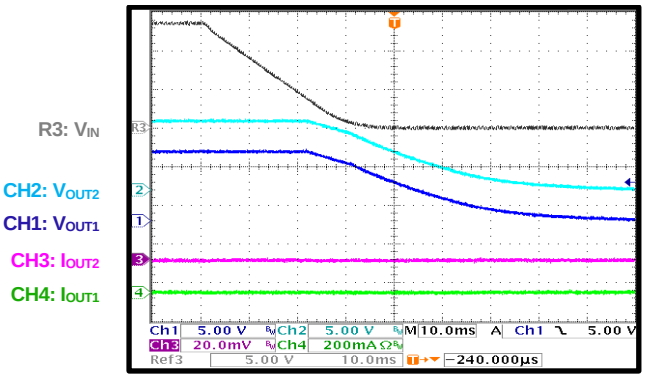
Start-Up through VIN

I_{OUT1} = I_{OUT2} = 0.3A



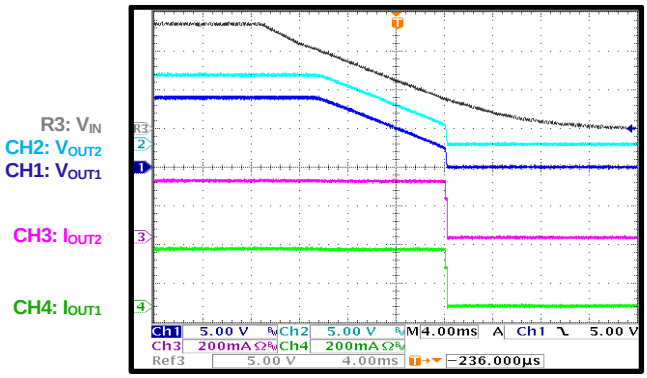
Shutdown through VIN

I_{OUT1} = I_{OUT2} = 0A



Shutdown through VIN

I_{OUT1} = I_{OUT2} = 0.3A

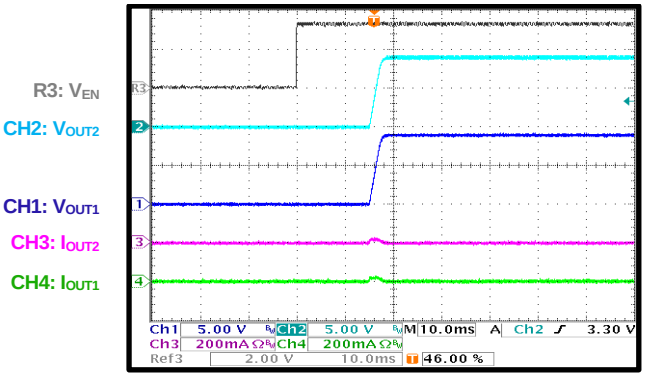


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF, C_{OUT1}, C_{OUT2} = 10µF, V_{IN} = 13.5V, V_{OUT1}, V_{OUT2} = 9V, V_{EN} = 3V, T_A = 25°C, unless otherwise noted.

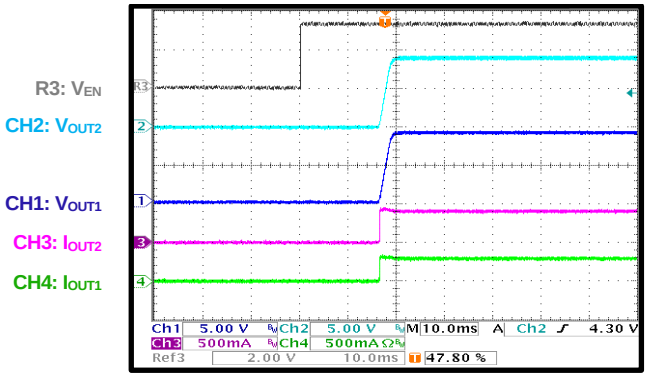
Start-Up through EN

I_{OUT1} = I_{OUT2} = 0A



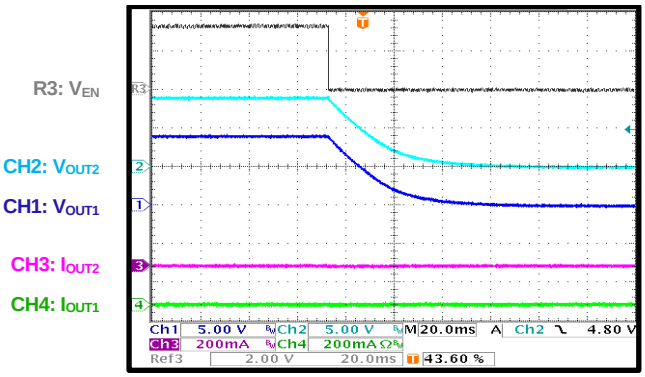
Start-Up through EN

I_{OUT1} = I_{OUT2} = 0.3A



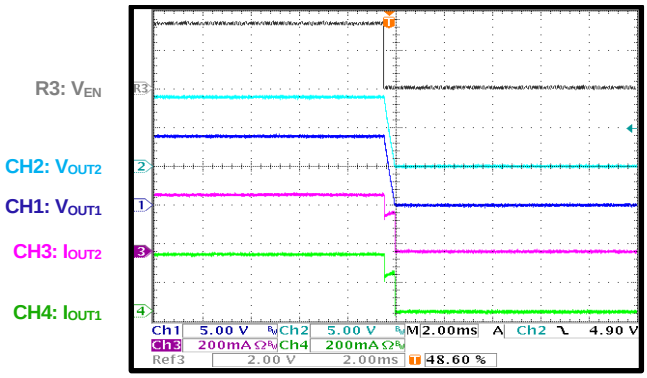
Shutdown through EN

I_{OUT1} = I_{OUT2} = 0A



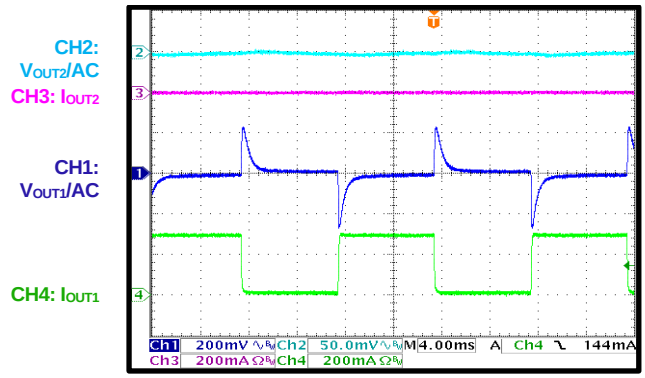
Shutdown through EN

I_{OUT1} = I_{OUT2} = 0.3A



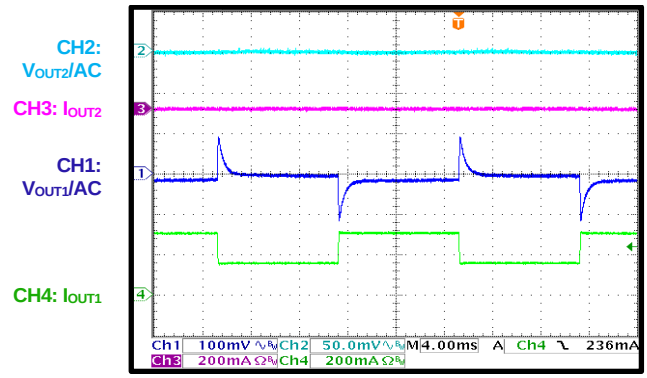
Load Transient

I_{OUT1} = 8mA to 300mA, 1.6A/µs, I_{OUT2} = 0A



Load Transient

I_{OUT1} = 150mA to 300mA, 1.6A/µs, I_{OUT2} = 0A

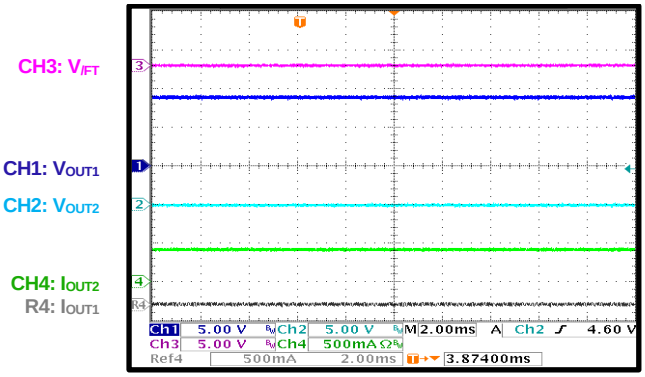


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF, C_{OUT1}, C_{OUT2} = 10µF, V_{IN} = 13.5V, V_{OUT1}, V_{OUT2} = 9V, V_{EN} = 3V, T_A = 25°C, unless otherwise noted.

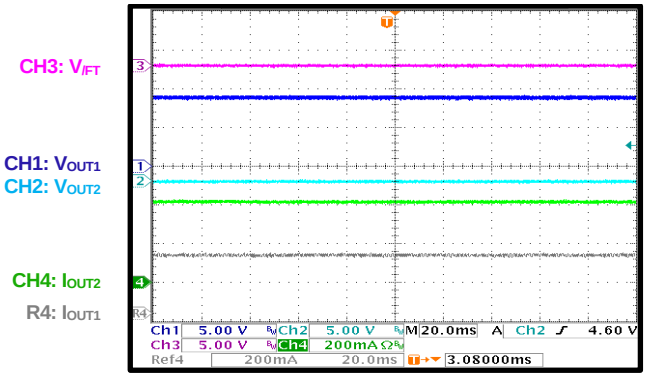
SCP Steady State

I_{OUT1} = 0A, V_{OUT2} short to circuit



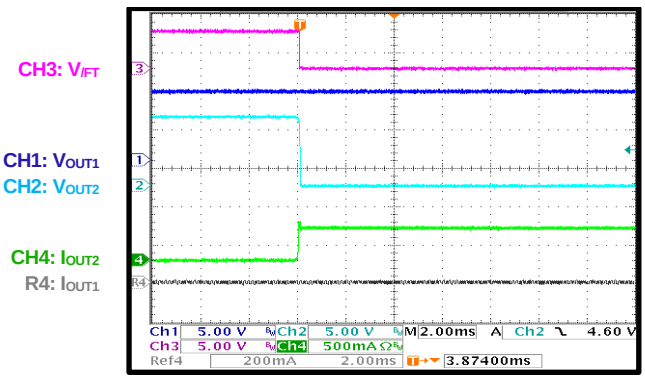
SCP Steady State

I_{OUT1} = 0.3A, V_{OUT2} short to circuit



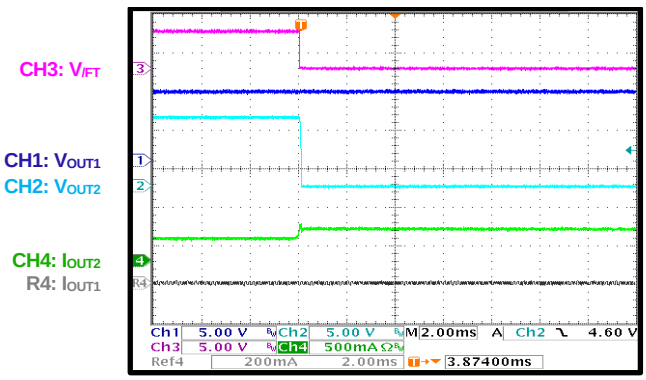
SCP Entry

I_{OUT1} = I_{OUT2} = 0A, V_{OUT2} short to circuit



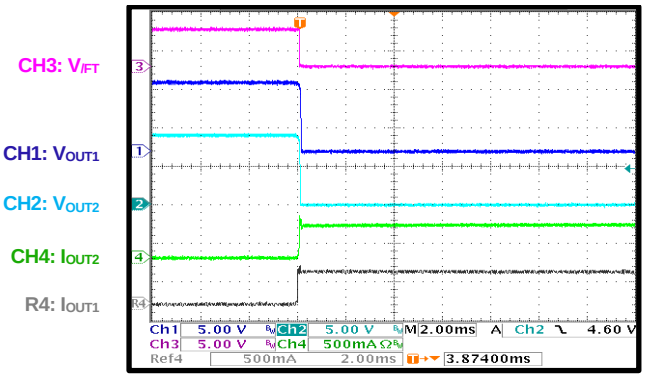
SCP Entry

I_{OUT1} = 0.3A, I_{OUT2} = 0A, V_{OUT2} short to circuit



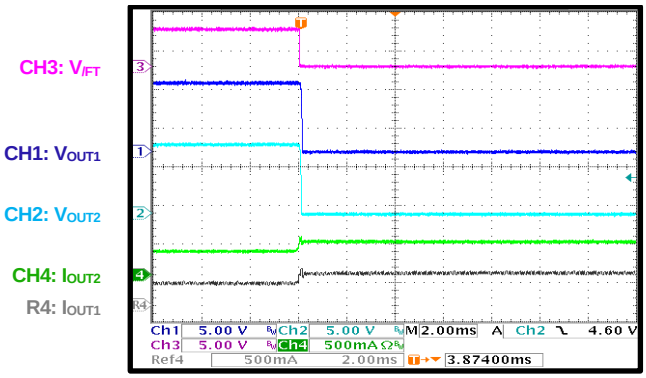
SCP Entry

I_{OUT1} = I_{OUT2} = 0A, V_{OUT1} and V_{OUT2} short to circuit



SCP Entry

I_{OUT1} = I_{OUT2} = 0.3A, V_{OUT1} and V_{OUT2} short to circuit

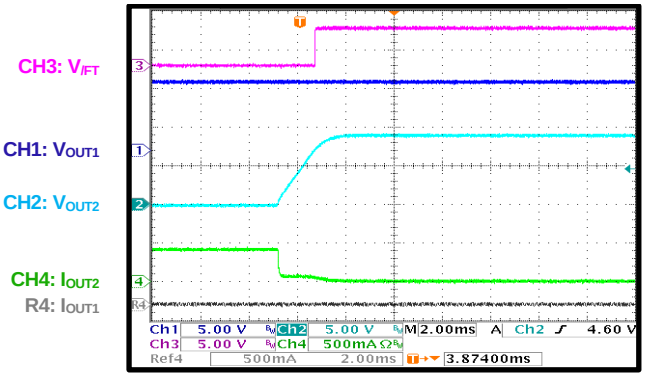


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF, C_{OUT1}, C_{OUT2} = 10µF, V_{IN} = 13.5V, V_{OUT1}, V_{OUT2} = 9V, V_{EN} = 3V, T_A = 25°C, unless otherwise noted.

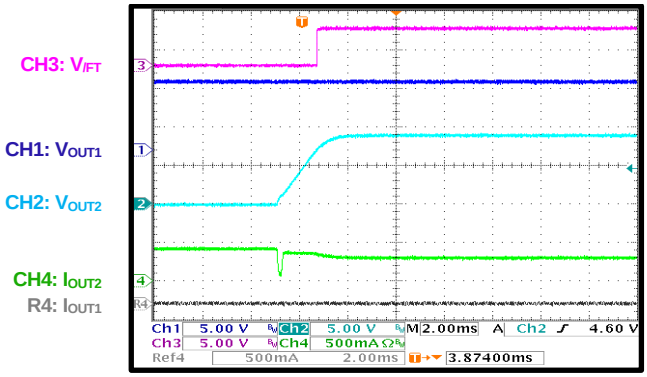
SCP Recovery

I_{OUT1} = 0A, short circuit to I_{OUT2} = 0A



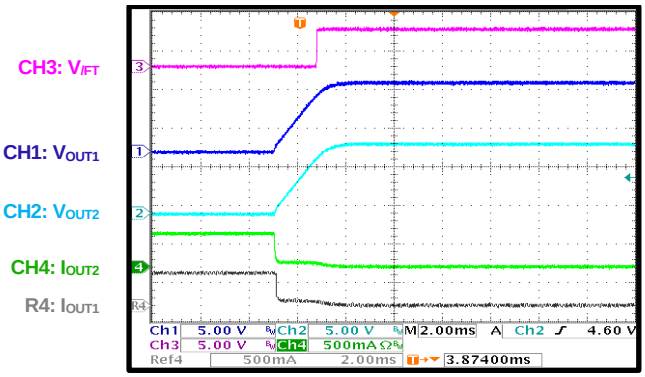
SCP Recovery

I_{OUT1} = 0A, short circuit to I_{OUT2} = 0.3A



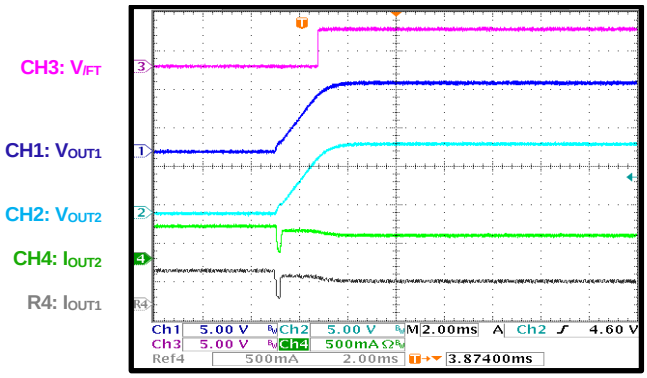
SCP Recovery

Short circuit to I_{OUT1} = I_{OUT2} = 0A



SCP Recovery

Short circuit to I_{OUT1} = I_{OUT2} = 0.3A



FUNCTIONAL BLOCK DIAGRAM

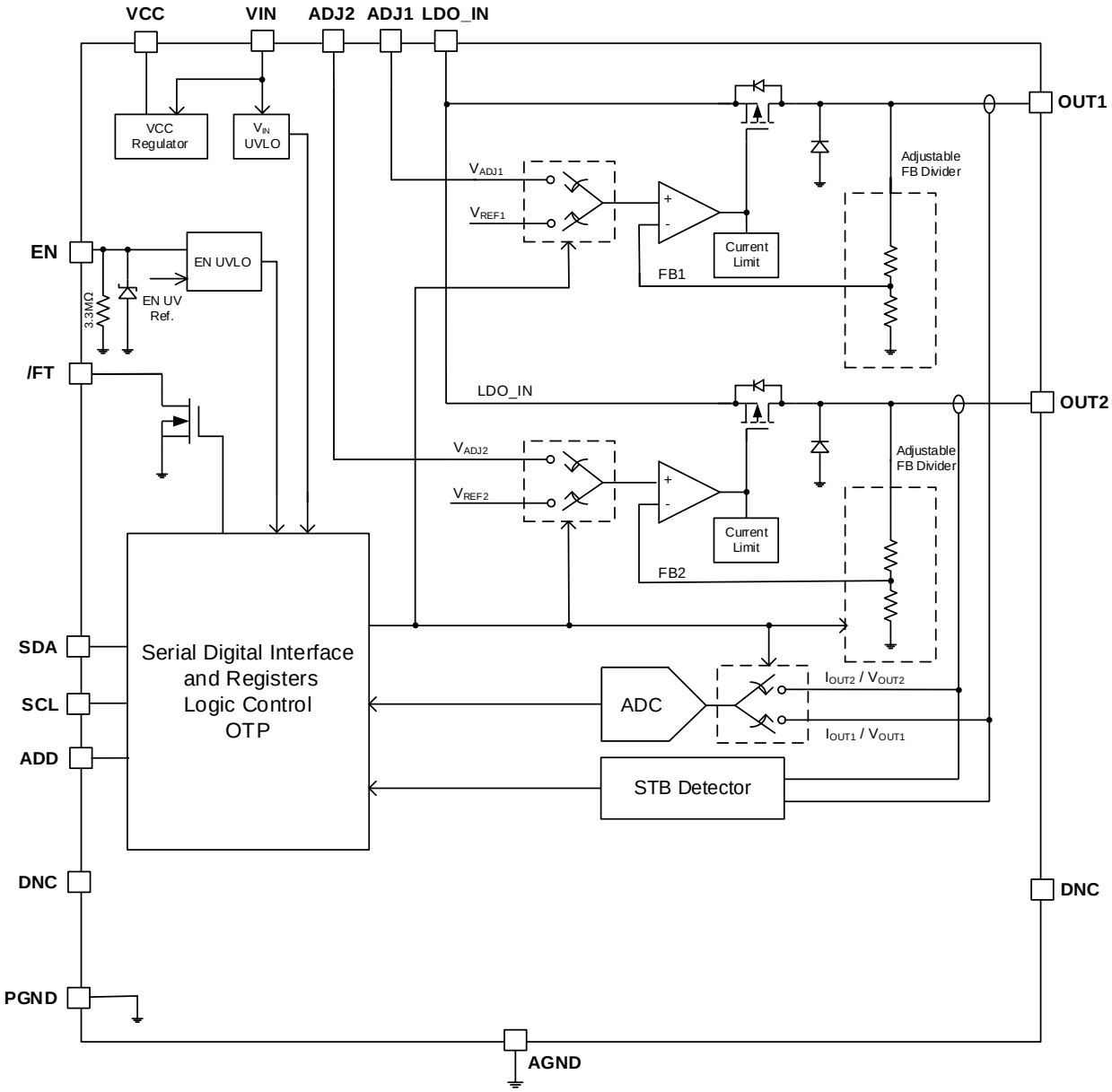


Figure 2: Functional Block Diagram

TIMING SEQUENCES

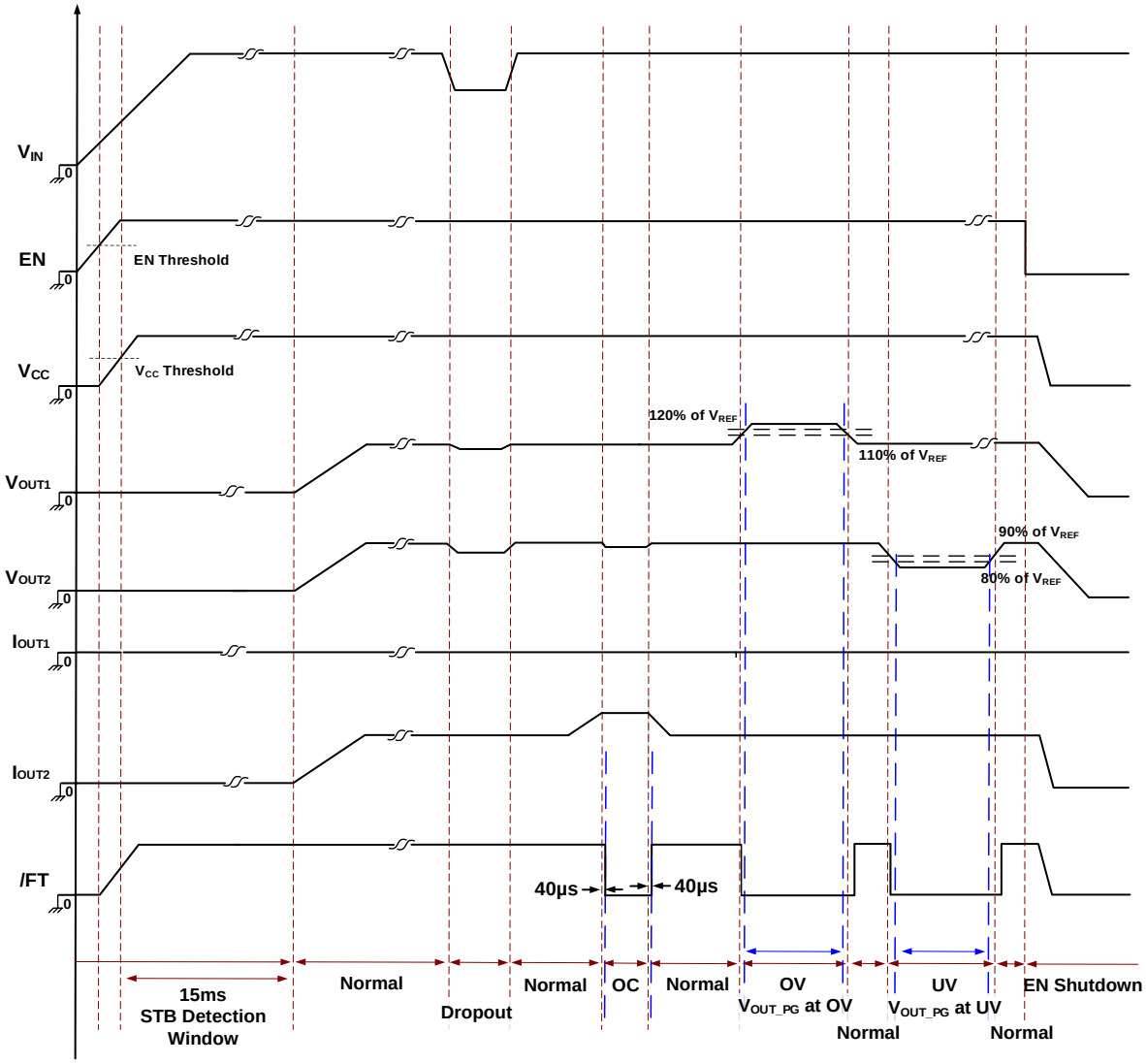


Figure 3: Timing Sequence

TIMING SEQUENCES *(continued)*

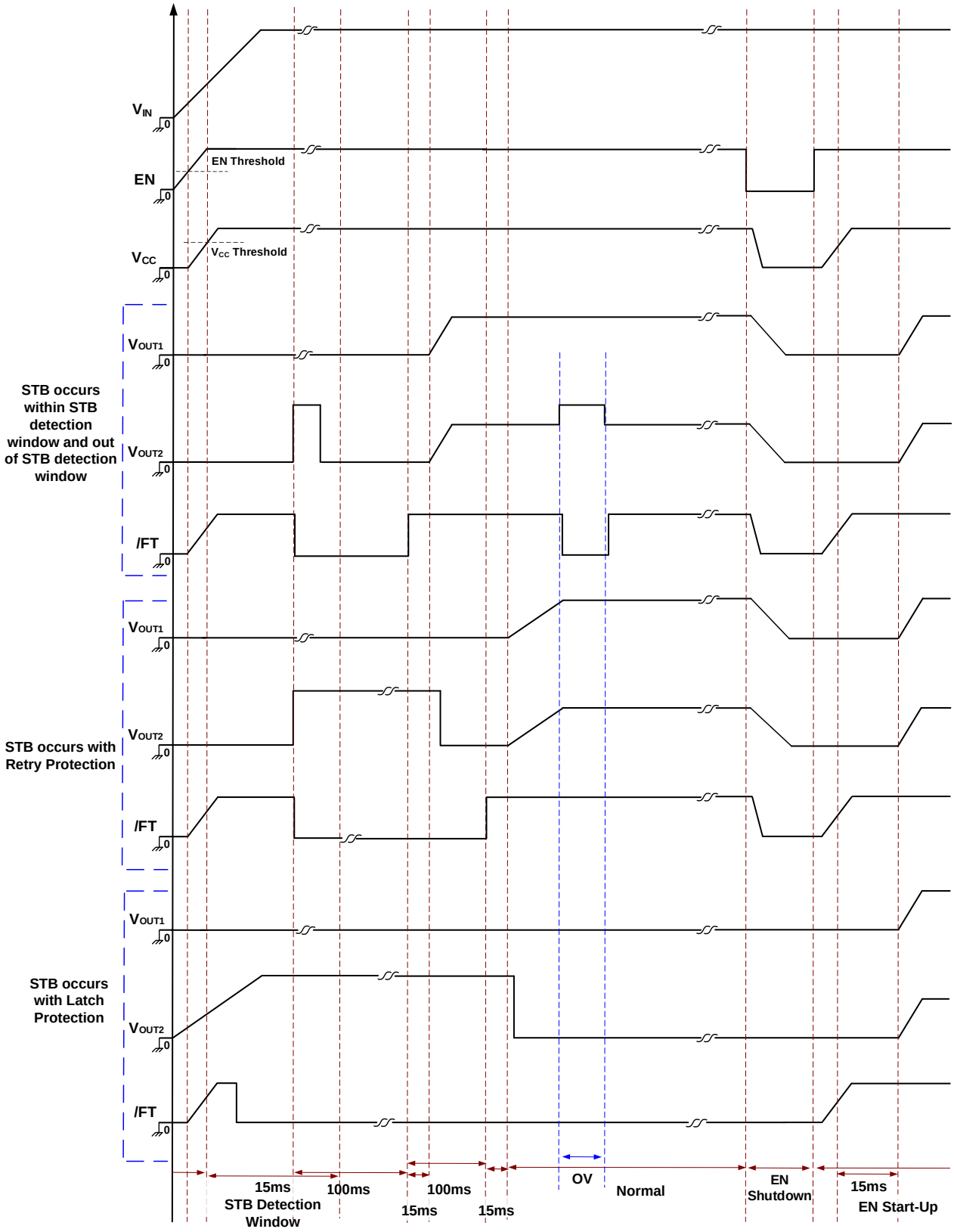


Figure 4: STB Timing Sequence

OPERATION

The MPQ2022A is a dual phantom antenna linear regulator with a serial digital interface. The device supplies power to systems with high-voltage batteries. It features a wide 4.5V to 40V input voltage (V_{IN}) range, low dropout (LDO) voltage, and a low quiescent supply current.

The two adjustable-output LDOs (LDO1 and LDO2) are supplied from LDO_IN and have outputs that are adjustable via the serial digital interface, from 1V to 13.6V with 200mV/step, or from 1V to 7.3V with 100mV/step.

The regulator's output current (I_{OUTx}, where x = 1 or 2) is limited internally, and the device is protected against short-circuit, over-current (OC), and over-temperature (OT) conditions. The dual LDOs' peak I_{OUTx} limit range can be configured to be between 100mA and 500mA via the serial digital interface.

If the junction temperature (T_J) is too high, the thermal sensor sends a signal to the control logic that shuts down the IC. The IC restarts when the temperature has sufficiently cooled.

The maximum power I_{OUTx} is a function of the package's maximum power dissipation for a given temperature. The maximum power dissipation is dependent on the thermal resistance of the case and the circuit board, the temperature difference between the die junction and the ambient air, and the airflow rate. GND and the exposed pad must be connected to the ground plane for proper dissipation.

Fault Indicator and Diagnostics

The MPQ2022A provides full diagnostics for different fault conditions. The device monitors the load current via an internal sense resistor to protect against OC and short-circuit conditions. In addition, the device also detects output over-voltage (OV) and under-voltage (UV) conditions, and provides short-to-battery protection, thermal shutdown, and open load.

The /FT pin pulls high during normal operation. Any fault or warning pulls this pin down to indicate a fault status (see Table 1). If the fault or warning is removed, /FT is pulled high. /FT is an open drain of a MOSFET. It should be connected to a ≤5V voltage source via a resistor (e.g. 100kΩ).

The MPQ2022A has dedicated register bits that serve as fault flags and indicate the device's status for system diagnostics. See the Register Map section on page 27 for more details.

Table 1: Fault Indicator

Fault	Registers Fault Flag	/FT Indication	Fault Actions
Thermal	Yes	Yes	If register 0x04, bit[0] = 0b, latch-off mode If register 0x04, bit[0] = 1b, hiccup mode
Short to battery	Yes	Yes	If register 0x04, bit[0] = 0b, latch-off mode If register 0x04 bit[0] = 1b, hiccup mode
LDO OC	Yes	Yes	No action. The chip continues operating until thermal shutdown occurs.
LDO OV	Yes	Yes	No action. The chip continues operating with the OV status.
LDO UV	Yes	Yes	No action. The chip continues operating with the UV status.
LDO OL	Yes	Yes	No action. The chip continues operating with the OL status.

Fault Handling

After a thermal shutdown or short-to-battery fault occurs, the device operates based on the corresponding fault mode set via register 0x04, bit[0]. There are two operating schemes: hiccup mode and latch-off mode.

In hiccup mode, the chip attempts to restart the converter. After the converter completely shuts down, a fault recovery timer starts. After a 100ms delay time, the converter attempts to soft start (SS) automatically.

If the fault condition is not removed, the converter reinitiates the fault protection and repeats the auto-recovery process in hiccup

Latch-off mode stops the converter until the power is cycled on the input supply or EN. The part restarts in normal mode, which includes a 15ms blank time (based on register 0x0F, bits[7:6]).

Short-Circuit and Over-Current (OC) Conditions

The current limit of each LDO channel is configured via the serial digital interface to protect the device during short-circuit or OC conditions. When either LDO's I_{OUTx} reaches its internal threshold, the LDO's I_{OUTx} is limited, and a dedicated bit in the register is set to indicate the fault. /FT is asserted low as well, but the output is not disabled.

/FT and the status of the internal register diagnostic bits is monitored by the external microcontroller unit (MCU), and the channel experiencing the short-circuit or OC condition is disabled by the MCU by setting the dedicated register bits via the serial digital interface. If a severe condition occurs, the MCU can shut down the part by pulling the EN pin low.

If this condition persists, thermal shutdown can occur, and then both outputs are disabled.

Short-to-Battery (STB) Detection

The LDO output pins can be shorted to the battery due to a system fault. Each LDO channel detects this failure by comparing the corresponding voltage at the OUT1, OUT2, and VIN pins before the device's internal switches turn on.

An adjustable blank time asserts each time the device is enabled and both VIN and EN exceed their rising thresholds, or the device recovers from thermal shutdown or hiccup mode. The blank time can be adjusted between 1ms and 15ms (based on register 0x0F, bits[7:6]), where 15ms is the default value.

Short-to-battery detection occurs during this adjustable blank time. If the device detects the short-to-battery fault, both dual LDO switches latch off or enter hiccup mode (based on register 0x04, bit[0]), /FT asserts low and the dedicated bits in the register are set to indicate the fault channel. After the short-to-battery fault is removed, the device can recover to normal operation automatically if hiccup mode is selected. If latch-off mode is selected, the device can recover to normal operation by cycling the power on VIN or EN to reset VCC.

mode. If the fault condition is removed once SS ends and the converter operates normally for a consecutive 80µs, then the fault status resets.

Thermal Shutdown

Thermal shutdown circuitry protects the device from overheating. If T_J exceeds 170°C (typical), the switch turns off immediately. Once the temperature drops by approximately 20°C (typical), the switch turns on again.

Integrated Inductive Clamp

During output shutdown, the cable inductance continues to source the current from the device's output. The device integrates an inductive clamp to help dissipate the inductive energy stored in the cable. An internal diode is connected between the OUT1, OUT2, and GND pins with a 300mA DC current capability for inductive clamp protection. Connect an additional diode for higher currents.

VCC Regulator

During normal operation, a LDO regulator outputs a nominal 5V VCC supply from VIN. This supplies power to all control blocks and the serial digital interface block. Add a 1µF to 10µF, low-ESR ceramic capacitor to act as the bypass capacitor from VCC to GND.

VCC has an internal under-voltage lockout (UVLO) block. The chip shuts down when V_{CC} drops below its 2.4V falling threshold, and starts up again when V_{CC} exceeds its 2.6V rising threshold. The part resets to the one-time programmable (OTP) memory value when V_{CC} falls to 2.4V.

Input Under-Voltage Lockout (UVLO)

V_{IN} has an internally fixed UVLO threshold. UVLO activates when V_{IN} on the VIN pin drops below its 3.8V falling threshold, and ensures the regulator is not latched to an unknown state when the input supply voltage is low. If V_{IN} has a negative transient that drops below the UVLO threshold and then recovers, the regulator shuts down. Once V_{IN} exceeds the 4.2V UVLO rising threshold, the regulator starts up with a normal start-up sequence.

Enable (EN)

The EN pin enables and disables the entire device. Pull EN below the 2.2V falling threshold to shut down the chip. Pull EN above the 2.4V rising threshold to enable the chip.

Separate, dedicated register bits enable the software of LDO1 and LDO2, respectively.

The physical EN pin has a higher priority than the software enable function. This means pulling EN low turns off the part, regardless of the values set via register 0x04, bit[4].

Adjustable LDO Output Voltage

The dual LDOs' output voltages (V_{OUT1} and V_{OUT2}) can be adjusted between 1V and 13.6V via the serial digital interface. V_{OUT1} and V_{OUT2} can also be adjusted by tracking the external voltages on the ADJ1 and ADJ2 pins.

This external voltage tracking mode is enabled via the serial digital interface. If this mode is enabled, V_{OUT1} and V_{OUT2} are equal to the voltage at ADJ1 and ADJ2, respectively. The applied voltage range on ADJ1 and ADJ2 is 3V to 13V. To track higher voltages, a resistor divider can scale down the voltage level.

Note that when external voltage tracking mode is enabled, /FT pin indication and LDO output OV, UV, and power good (PG) indication in the serial digital interface registers are invalid. /FT remains high.

The dual LDOs cannot be used in parallel.

LDO Output Voltage and Current Monitor

The MPQ2022A's dedicated analog-to-digital converter (ADC) block monitors the dual LDOs' output voltages and load currents. The ADC can be enabled via the serial digital interface. Read registers 0x05 to 0x08 to monitor the LDO1 and LDO2 output voltages and load currents.

Note that the ADC block does not provide fault diagnostics.

Open Load Detection

The MPQ2022A provides open-load detection. If this function is enabled and the load drops below the open-load falling threshold, the MPQ2022A considers the load system to be in an open-load state, and then /FT pulls down.

When the load exceeds the open-load rising threshold, the chip is not in an open-load state, and /FT is pulled high.

The open-load function does not work when it is disabled. By default, the open-load function is disabled. Contact an MPS FAE for more details.

Note that open load detection is achieved through an internal current comparator instead of through ADC block sampling.

Multi-Page One-Time Programmable (OTP) Memory

The MPQ2022A features 2 pages of OTP memory to permanently store the desired settings.

A differential OTP cell is used instead of a single-ended cell for long-term reliability. Data is stored on two floating gate avalanche injection metal oxide semiconductors (FAMOS), and output comparators are used for differential reading.

The first page of the multi-page OTP memory is already configured based on the custom codes.

Once the device is enabled, the default values on the first page set the control parameters in the registers. If there is data on other pages of the OTP memory, the newest setting is identified by an internal indicator to the write registers. See the Register Map section on page 27 for more details.

SERIAL DIGITAL INTERFACE

Serial Digital Interface Description

The two-wire, bidirectional serial digital interface consists of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. A master device is connected to the line to generate the SCL signal and device address and arrange the communication sequence. The MPQ2022A interface is a serial digital interface slave that supports fast mode (400kHz), adding flexibility to the power supply solution. V_{OUTx}, the transition slew rate, and additional parameters can be instantaneously controlled via the serial digital interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the clock's high period. The data line's high or low state can only change when the clock signal on the SCL line is low (see Figure 5).

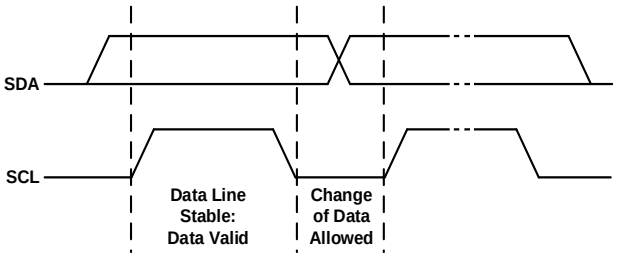


Figure 5: Bit Transfer on the Serial Digital Interface Bus

Start and Stop Conditions

The start and stop conditions are signaled by the master device, which signifies the beginning and end of the serial digital interface transfer. The start (S) command is defined as the SDA signal transitioning from high to low while the SCL is high. The stop (P) command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 6).

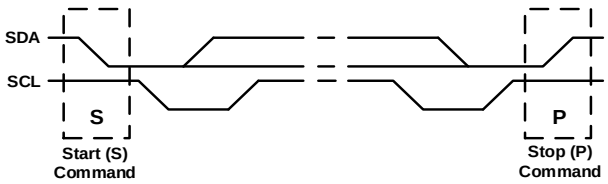


Figure 6: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is considered busy after the start command. The bus is considered free again after a minimum of 4.7µs after the stop command. The bus remains busy if a repeated start (Sr) command is generated instead of a stop command. The start and repeated start commands are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable and low during the clock pulse's high period.

Figure 7 shows the format for data transfers. After the start command, a slave address is sent. This address is 7 bits long, followed by an eighth data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop command, which is generated by the master. If the master wants to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

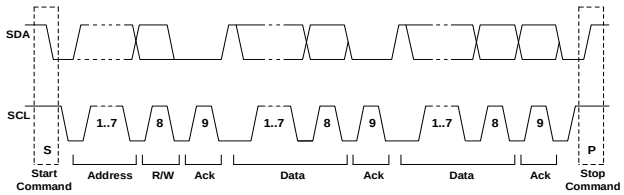


Figure 7: A Complete Data Transfer

Packet Error Checking (PEC)

The packet error checking (PEC) mechanism improves communication reliability and robustness. When applicable, PEC is implemented by appending a packet error code at the end of each message transfer.

PEC is a CRC-8 error-checking byte, calculated on all the message bytes (including addresses and read/write bits). PEC is appended to the message by the device that supplied the last data byte.

Write Sequence

Figure 8 shows a typical write sequence, which requires a master's start command, a valid slave address, a register index byte, a corresponding data byte, and ends with a PEC for a single data update.

After receiving each byte, the MPQ2022A acknowledges by pulling the SDA line low during a single clock pulse's high period. A valid serial digital interface address selects the MPQ2022A. The MPQ2022A performs an update on the LSB byte's falling edge.

The PEC byte in a write sequence can be calculated with CRC-8, and requires the slave address, register index, and data to make the calculation. CRC-8 can be calculated with Equation (1):

$$CRC\text{-}8 = 1 + X + X^2 + X^8 \quad (1)$$

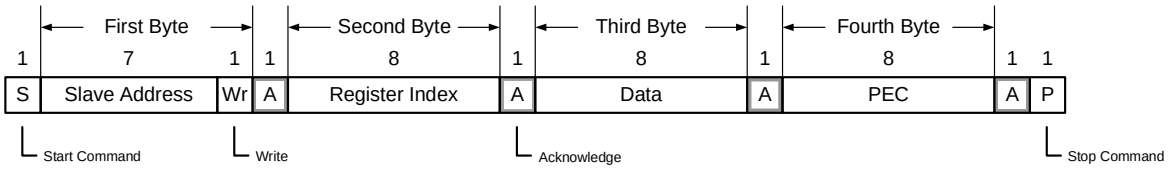


Figure 8: Write Sequence

Read Sequence

Figure 9 shows a typical read sequence, which is five bytes long. It starts with the master's start command, then a valid slave address, followed by a register index byte. Unlike a write sequence, the master sends a start command again. The bus direction then turns around with the re-broadcast of the slave address, with bit[1] indicating a read cycle. The following fourth byte contains the data being returned by the MPQ2022A. This byte value in the data byte reflects the value of the register index being queried before. Finally, the MPQ2022A sends a PEC byte to end the read sequence.

The PEC byte in a read sequence can be calculated with CRC-8, and requires the slave address, register index, slave address, and data to make the calculation. See Equation (1) in the Write Sequence section to calculate CRC-8.

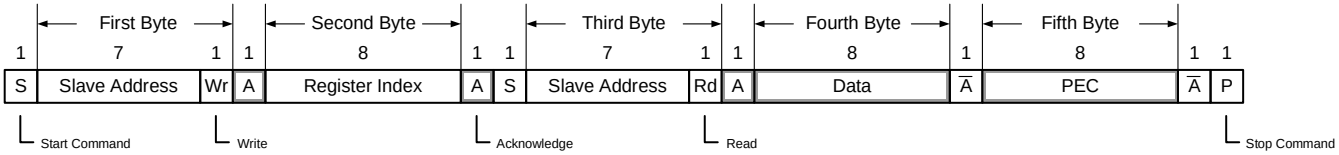


Figure 9: Read Sequence

Serial Digital Interface Update Sequence

The MPQ2022A requires a start command, a valid serial digital interface address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPQ2022A acknowledges by pulling the SDA line low during a single clock pulse's high period. A valid serial digital interface address selects the MPQ2022A. The MPQ2022A performs an update on the LSB byte's falling edge.

Serial Digital Interface Chip Address

The ADD pin configures the serial digital interface address by adjusting the resistance that is connected between ADD and ground. A 10μA current flows from ADD and generates a voltage on the ADD resistor. The MPQ2022A supports 7 addresses, for up to 7 voltage rails, by detecting the different voltages on ADD. Table 2 on page 26 shows the resistances for different serial digital interface addresses. The resistor's tolerance should not exceed 1% of the recommended resistance.

When the master sends the address as an 8-bit value, the 7-bit address should be followed by 0 or 1 to indicate a write or read operation, respectively.

Table 2: Serial Digital Interface Address

Address	Resistor (kΩ)	Minimum ADD Voltage (mV)	Typical ADD Voltage (mV)	Maximum ADD Voltage (mV)	Min (µA)	Typical ADD Current (µA)	Max (µA)
21h	0 (1%)	0	0	40	9.5	10	10.5
22h	6.98 (1%)	40	70	100			
23h	15 (1%)	100	150	200			
24h	30 (1%)	200	300	400			
25h	54.9 (1%)	400	550	700			
26h	95.3 (1%)	700	950	1200			
27h	>130 (1%) or floating	1200	-	-			

REGISTER MAP

Register Short Name	R/W	Add	Default (8)	D7	D6	D5	D4	D3	D2	D1	D0
Device Status and Diagnostics											
DEV_REV	R	0x00	00h	SILLICON_INFO							
DEV_STAT	R	0x01	00h	RSV (9)	LDO_1 _ACTIVE	LDO_2 _ACTIVE	VOUT1_ PG	VOUT2_ _PG	FT_ ASSERT	SDI_ ERR	POR
ERR_ FLAG_1	R	0x02	00h	VOUT_ 1_OV	VOUT_ 1_UV	VOUT_ 2_OV	VOUT_2 _UV	RSV (9)	RSV (9)	LDO_ 1_STB	LDO_ 2_STB
ERR_ FLAG_2	R	0x03	00h	LDO_ 1_OC	LDO_ 2_OC	RSV (9)	OT	LDO_ 1_OL	LDO_ 2_OL	RSV (9)	RSV (9)
DEV_CTRL	W/R	0x04	61h	RSV (9)	LDO_ 1_EN	LDO_2 _EN	SHUT DOWN	ADC-EN	SOFT_ RST	RSV (9)	FAULT_ HANDLE
Monitoring											
MON _VOUT_1	R	0x05	00h	VOUT1_MON							
MON _VOUT_2	R	0x06	00h	VOUT2_MON							
MON _IOUT_1	R	0x07	00h	IOUT1_MON							
MON _IOUT_2	R	0x08	00h	IOUT2_MON							
Power Management											
SET_ VOUT_1	W/R	0x09	68h	FAULT_ CLEAR	VOUT1_ STEP	VOUT1_SET					
SET_ VOUT_2	W/R	0x0A	68h	POWER_ _SEQ	VOUT2_ STEP	VOUT2_SET					
RSVD	W/R	0x0B	78h	RSV (9)							
RSVD	W/R	0x0C	4Ch	RSV (9)							
SET_PG_ UVOV	W/R	0x0D	00h	VOUT1_ OV_THR	VOUT1_ UV_THR	VOUT2_ OV_THR	VOUT2_ UV_THR	VOUT1_ PG_ H_THR	VOUT1_ PG_ L_THR	VOUT2_ PG_ H_THR	VOUT2_ PG_ L_THR
SET_IOUT_ LIM_1	W/R	0x0E	10h	LDO1_ TRC	LDO2_ TRC	RSV (9)	IOUT_1_OC_THR				
SET_IOUT_ LIM_2	W/R	0x0F	10h	STB_DETECTION_ WINDOW		OC_MIN	IOUT_2_OC_THR				

Notes:

8) The default values for the MPQ2022A-0000 registers. The default value can be redefined if the OTP function is available.
9) This bit is not defined and is reserved for future use.

REGISTER DESCRIPTION

DEV_REV (0x00)

Access: Read-only

POR/Soft Reset Value: 00000000

The DEV_REV command returns the device revision and information.

Bits	Name	Description
D[7:0]	SILICON_ INFORMATION	Returns the silicon information.

DEV_STAT (0x01)

Access: Read-only

POR/Soft Reset Value: 00000000

The DEV_STAT command returns the device status.

Bits	Name	Description
D[7]	RESERVED	Reserved. Always reads as 0.
D[6]	LDO_1_ACTIVE	0: LDO1 is not active 1: LDO1 is active
D[5]	LDO_2_ACTIVE	0: LDO2 is not active 1: LDO2 is active
D[4]	VOUT1_PG	0: The LDO1's output voltage (V_{OUT1}) is not within its power good (PG) range 1: V_{OUT1} is within its PG range
D[3]	VOUT2_PG	0: The LDO2's output voltage (V_{OUT2}) is not within its PG range 1: V_{OUT2} is within its PG range
D[2]	FT_ASSERT	0: /FT is not asserting 1: /FT is asserting (active low)
D[1]	SDI_ERR	0: No serial digital interface communication error has occurred 1: A serial digital interface communication error has occurred Note that if the SDI_ERR bit occurs, the chip can be read but not written.
D[0]	POR	0: No power-on reset (POR) event has occurred 1: A POR event has occurred and finished

ERR_FLAG_1 (0x02)

Access: Read-only

POR/Soft Reset Value: 00000000

The ERR_FLAG_1 command returns device error flags for over-voltage (OV) and under-voltage (UV) conditions.

Bits	Name	Description
D[7]	VOUT_1_OV	0: Clears to 0 when there is no over-voltage (OV) condition on OUT1 1: An OV condition has been detected on OUT1
D[6]	VOUT_1_UV	0: Clears to 0 when there is no under-voltage (UV) condition on OUT1 1: A UV condition has been detected on OUT1
D[5]	VOUT_2_OV	0: Clears to 0 when there is no OV condition on OUT2 1: An OV condition has been detected on OUT2
D[4]	VOUT_2_UV	0: Clears to 0 when there is no UV condition on OUT2 1: A UV condition has been detected on OUT2

D[3]	RESERVED	Reserved. Always reads as 0.
D[2]	RESERVED	Reserved. Always reads as 0.
D[1]	LDO_1_STB	0: Clears to 0 when no short-to-battery condition has been detected on LDO1 1: A short-to-battery condition has been detected on LDO1
D[0]	LDO_2_STB	0: Clears to 0 when no short-to-battery condition has been detected on LDO2 1: A short-to-battery condition has been detected on LDO2

ERR_FLAG_2 (0x03)

Access: Read-only

POR/Soft Reset Value: 00000000

The ERR_FLAG_2 command returns device error flags for over-current (OC) and over-temperature (OT) conditions.

Bits	Name	Description
D[7]	LDO_1_OC	0: Clears to 0 when no over-current (OC) condition has been detected on OUT1 1: An OC condition has been detected on OUT1
D[6]	LDO_2_OC	0: Clears to 0 when no OC condition has been detected on OUT2 1: An OC condition has been detected on OUT2
D[5]	RESERVED	Reserved. Always reads as 0.
D[4]	OT	0: Clears to 0 when no over-temperature (OT) condition has been detected 1: An OT condition has been detected
D[3]	LDO_1_OL	0: Clears to 0 when no open-load condition has been detected on OUT1 1: An open-load condition has been detected on OUT1 Note that the LDO_1_OL bit is only valid when the open-load function is enabled.
D[2]	LDO_2_OL	0: Clears to 0 when no open-load condition has been detected on OUT2 1: An open-load condition has been detected on OUT2 Note that the LDO_2_OL bit is only valid when the open-load function is enabled.
D[1:0]	RESERVED	Reserved. Always reads as 0.

DEV_CTRL (0x04)

Access: R/W

POR/Soft Reset Value: 01100001

The DEV_CTRL command controls the device.

Bits	Name	Description
D[7]	RESERVED	Reserved. Always reads as 0.
D[6]	LDO_1_EN	0: LDO1 is disabled 1: LDO1 is enabled
D[5]	LDO_2_EN	0: LDO2 is disabled 1: LDO2 is enabled
D[4]	SHUTDOWN	0: Turns on the device if the EN pin voltage (V_{EN}) exceeds the EN rising threshold ($V_{EN\_VTH\_R}$) 1: The device is forced to shut down
D[3]	ADC-EN	0: The analog-to-digital converter (ADC) is disabled 1: The ADC is enabled
D[2]	SOFT_RST	0: No soft reset has been requested 1: A soft reset has been requested. The device returns to the state of the one-time programmable (OTP) memory code
D[1]	RESERVED	Reserved. Always reads as 0.

D[0]	FAULT_HANDLE	0: Latch-off mode 1: Hiccup mode with a 100ms blank time

MON_VOUT_1 (0x05)

Access: Read-only

POR/Soft Reset Value: 00000000

The MON_VOUT_1 command returns the monitored LDO1 output voltage (V_{OUT1_MON}).

Bits	Name	Description
D[7:0]	VOUT1_MON	Records the monitored V_{OUT1} (V_{OUT1_MON}) by the ADC. This value refreshes each time it is read. 1 least significant bit (LSB) = 55mV. V_{OUT1_MON} can be calculated with the following equation: V_{OUT1_MON} = D[7:0] x 55mV For example, if bits[7:0] = $(10100100)_2$, this is $(164)_{10}$, and V_{OUT1} = 164 x 55mV = 9.02V.

MON_VOUT_2 (0x06)

Access: Read-only

POR/Soft Reset Value: 00000000

The MON_VOUT_2 command returns the monitored LDO2 output voltage (V_{OUT2_MON}).

Bits	Name	Description
D[7:0]	VOUT2_MON	Records the monitored V_{OUT2} (V_{OUT2_MON}) by the ADC. This value refreshes each time it is read. 1LSB = 55mV. V_{OUT2_MON} can be calculated with the following equation: V_{OUT2_MON} = D[7:0] x 55mV For example, if bits[7:0] = $(10100100)_2$, this is $(164)_{10}$, and V_{OUT2} = 164 x 55mV = 9.02V.

MON_IOUT_1 (0x07)

Access: Read-only

POR/Soft Reset Value: 00000000

The MON_IOUT_1 command returns the monitored LDO1 output current (I_{OUT1_MON}).

Bits	Name	Description
D[7:0]	IOUT1_MON	Records the monitored I_{OUT1} (I_{OUT1_MON}) by the ADC. This value refreshes each time it is read. 1LSB = 1.2mA. I_{OUT1_MON} can be calculated with the following equation: I_{OUT1_MON} = D[7:0] x 1.2mA For example, if bits[7:0] = $(11111010)_2$, this is equal to $(250)_{10}$, and I_{OUT1} = 250 x 1.2mA = 300mA.

MON_IOUT_2 (0x08)

Access: Read-only

POR/Soft Reset Value: 00000000

The MON_IOUT_2 command returns the monitored LDO2 output current (I_{OUT2_MON}).

Bits	Name	Description
D[7:0]	IOUT2_MON	Records the monitored I_{OUT2} (I_{OUT2_MON}) by the ADC. This value refreshes each time it is read. 1LSB = 1.2mA. I_{OUT2_MON} can be calculated with the following equation: I_{OUT2_MON} = D[7:0] x 1.2mA For example, if bits[7:0] = $(11111010)_2$, this is equal to $(250)_{10}$, and I_{OUT2} = 250 x 1.2mA = 300mA.

SET_VOUT_1 (0x09)

Access: R/W

POR/Soft Reset Value: 01101000

The SET_VOUT_1 command sets the LDO1 output voltage (V_{OUT1}).

Bits	Name	Description
D[7]	FAULT_CLEAR	0: No action (default) 1: Clears all fault flags and de-asserts /FT. For example, if the SDI_ERR bit occurs, set bit[7] = 1, then the chip can be written again.
D[6]	VOUT1_STEP	Sets the V_{OUT1} step. This bit is set to 1 by default. 0: 100mV 1: 200mV
D[5:0]	VOUT1_SET	Sets V_{OUT1}, calculated with the following equation: V_{OUT1} = 1V + VOUT1_SET x VOUT1_STEP If the default is bits[5:0] = $(101000)_2$, which is $(40)_{10}$, then the default V_{OUT1} = 1V + 40 x 200mV = 9V.

SET_VOUT_2 (0x0A)

Access: R/W

POR/Soft Reset Value: 01101000

The SET_VOUT_2 command sets the LDO2 output voltage (V_{OUT2}).

Bits	Name	Description
D[7]	POWER_SEQ	0: OUT1 and OUT2 are powered simultaneously 1: OUT2 is delayed by 100ms
D[6]	VOUT2_STEP	Sets the V_{OUT2} step. This bit is set to 1 by default. 0: 100mV 1: 200mV
D[5:0]	VOUT2_SET	Sets V_{OUT2}, calculated with the following equation: V_{OUT2} = 1V + VOUT2_SET x VOUT2_STEP If the default is bits[5:0] = $(101000)_2$, which is $(40)_{10}$, then the default V_{OUT2} = 1V + 40 x 200mV = 9V

RESERVED (0x0B)

Access: R/W

POR/Soft Reset Value: 01111000

Bits	Name	Description
D[7:0]	RESERVED	Reserved. Always reads as 0.

RESERVED (0x0C)

Access: R/W

POR/Soft Reset Value: 01001100

Bits	Name	Description
D[7:0]	RESERVED	Reserved. Always reads as 0.

SET_PG_UVOV (0x0D)

Access: R/W

POR/Soft Reset Value: 00000000

The SET_PG_UVOV command sets the power good (PG) and LDO under-voltage (UV) and over-voltage (OV) settings.

Bits	Name	Description
D[7]	VOUT1_OV_THR	0: The V_{OUT1} OV threshold is 115% of the set V_{OUT1} 1: The V_{OUT1} OV threshold is 120% of the set V_{OUT1}
D[6]	VOUT1_UV_THR	0: The V_{OUT1} UV threshold is 75% of the set V_{OUT1} 1: The V_{OUT1} UV threshold is 80% of the set V_{OUT1}
D[5]	VOUT2_OV_THR	0: The V_{OUT2} OV threshold is 115% of the set V_{OUT2} 1: The V_{OUT2} OV threshold is 120% of the set V_{OUT2}
D[4]	VOUT2_UV_THR	0: The V_{OUT2} UV threshold is 75% of the set V_{OUT2} 1: The V_{OUT2} UV threshold is 80% of the set V_{OUT2}
D[3]	VOUT1_PG_H_THR	0: The OUT1 PG threshold's upper boundary is 105% of the set voltage 1: The OUT1 PG threshold's upper boundary is 110% of the set voltage
D[2]	VOUT1_PG_L_THR	0: The OUT1 PG threshold's lower boundary is 90% of the set voltage 1: The OUT1 PG threshold's lower boundary is 95% of the set voltage
D[1]	VOUT2_PG_H_THR	0: The OUT2 PG threshold's upper boundary is 105% of the set voltage 1: The OUT2 PG threshold's upper boundary is 110% of the set voltage
D[0]	VOUT2_PG_L_THR	0: The OUT2 PG threshold's lower boundary is 90% of the set voltage 1: The OUT2 PG threshold's lower boundary is 95% of the set voltage

SET_IOUT_LIM_1 (0x0E)

Access: R/W

POR/Soft Reset Value: 00010000

The SET_IOUT_LIM_1 command sets the LDO1 current limit threshold (I_{LIMIT1}).

Bits	Name	Description
D[7]	LDO1-TRC	0: Disables LDO1 tracking mode 1: Enables LDO1 tracking mode
D[6]	LDO2-TRC	0: Disables LDO2 tracking mode 1: Enables LDO2 tracking mode
D[5]	RESERVED	Reserved. Always reads as 0.
D[4:0]	IOUT_1_OC_THR	Sets the OUT1 OC threshold (I_{LIMIT1}), where 1LSB = 6.25mA. I_{LIMIT1} can be calculated with the following equation: I_{LIMIT1} = D[4:0] x 6.25mA + OC_MIN OC_MIN is set by register 0x0F, bit[5]. The default bits[4:0] = $(10000)_2$, which is equal to $(16)_{10}$, and I_{LIMIT1} = 16 x 6.25 + 300 = 400mA

SET_IOUT_LIM_2 (0x0F)

Access: R/W

POR/Soft Reset Value: 00010000

The SET_IOUT_LIM_2 command sets the LDO2 current limit threshold (I_{LIMIT1}).

Bits	Name	Description
D[7:6]	STB_DETECTION_WINDOW	00: 15ms 01: 7ms 10: 3ms 11: 1ms
D[5]	OC_MIN	Sets the minimum OC threshold for LDO1 and LDO2. The default value is 300mA. 0: 300mA 1: 100mA
D[4:0]	IOUT_2_OC_THR	Sets the OUT2 OC threshold (I_{LIMIT2}), where 1LSB = 6.25mA. I_{LIMIT2} can be calculated with the following equation: I_{LIMIT2} = D[4:0] x 6.25mA + OC_MIN OC_MIN is set by register 0x0F, bit[5]. The default bits[4:0] = $(10000)_2$, which is equal to $(16)_{10}$, and I_{LIMIT2} = 16 x 6.25 + 300 = 400mA

APPLICATION INFORMATION

Figure 10 shows the MPQ2022A's typical application circuit.

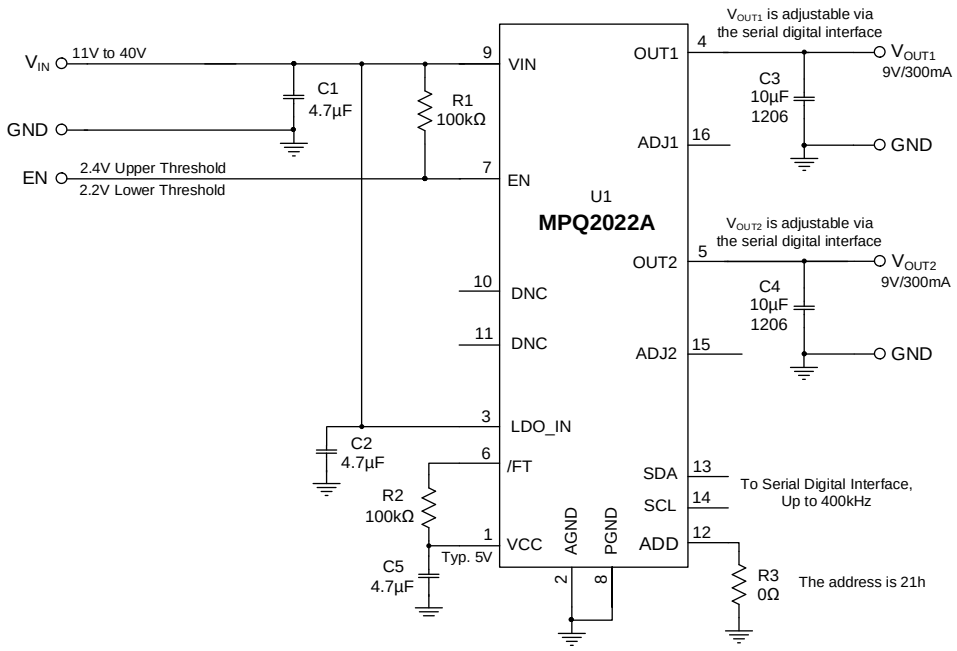


Figure 10: Typical Application Circuit (V_{OUT1} = 9V, V_{OUT2} = 9V)

Table 3 shows the design guide index. See Figure 10 for more details.

Table 3: Design Guide Index

Pin #	Name	Components	Design Guide Index
1	VCC	C5	Internal VCC (VCC, Pin 1)
2	AGND	-	GND Connection (PGND, Pin 8; AGND, Pin 2)
3	LDO_IN	C2	Selecting Input Capacitors for the Dual LDOs (LDO_IN, Pin 3)
4	OUT1	C3	Selecting Output Capacitors for LDO1 (OUT1, Pin 4)
5	OUT2	C4	Selecting Output Capacitors for LDO2 (OUT5, Pin 5)
6	/FT	R2	Fault Indictor (/FT, Pin 6)
7	EN	R1	Enable (EN, Pin 7)
8	GND	-	GND Connection (PGND, Pin 8; AGND, Pin 2)
9	VIN	C1	Selecting Input Capacitors (VIN, Pin 9)
10, 11	DNC	-	Do Not Connect (DNC, Pin 10 and Pin 11)
12	ADD	R3	Selecting the Resistor for the Serial Digital Interface Address (ADD, Pin 12)
13	SDA	-	Serial Digital Interface (SDA, Pin 13; SCL, Pin 14)
14	SCL	-	Serial Digital Interface (SDA, Pin 13; SCL, Pin 14)
15, 16	ADJ2, AD1	-	Setting the Reference Voltage Input for the Dual LDOs (ADJ2, Pin 15; ADJ1, Pin 16)

Internal VCC (VCC, Pin 1)

The VCC capacitor (C5) should be between 1µF and 10µF. A 4.7µF ceramic capacitor is generally recommended.

All the control blocks and the serial digital interface block are powered by the internal regulator. This regulator uses V_{IN} as its input and operates across the full V_{IN} range.

In latch-off mode, V_{CC} should drop below its falling threshold before start-up to prevent a failed start-up. It is not recommended for V_{CC} to supply power to the external circuits. If V_{CC} is below its UVLO threshold, do not use the serial digital interface.

Selecting the Input Capacitor for the Dual LDOs (LDO_IN, Pin 3)

For efficient operation, place a 1µF to 10µF ceramic capacitor with X5R or X7R dielectrics between the LDO_IN pin and ground. Larger-value capacitors improve line transient response.

Selecting the Output Capacitor for the Dual LDOs (OUT1, Pin 4; OUT2, Pin 5)

For stable operation, use a 4.7µF to 22µF ceramic capacitor with X5R or X7R dielectrics. Larger-value capacitors improve load transient response and reduce noise. Output capacitors of other dielectric types may be used, but they are not recommended as their capacitance can deviate significantly from their rated value across different temperatures.

Setting the Dual LDOs' Output Voltages (V_{OUT1} and V_{OUT2})

The MPQ2022A does not require an external resistor to set V_{OUTx}. The OTP registers 0x09 and 0x0A set the dual LDOs' V_{OUTx} (see the Register Map section on page 27).

V_{OUT1} and V_{OUT2} are configured via registers 0x09 and 0x0A, and can be adjusted between 1V and 13.6V with 200mV/step, or between 1V and 7.3V with 100mV/step. Using registers 0x09 and 0x0A, V_{OUTx} can be calculated with Equation (2):

$$V_{OUTx} = D[5:0] \times Step + 1V \quad (2)$$

For example, if register 0x09, bits[7:0] is set to 68h, the step is 200mV. Then the LDO V_{OUTx} = 1V + 40 x 0.2V = 9V.

When the difference between the LDO input voltage (V_{LDO_IN}) and V_{OUTx} is below the dropout voltage ($V_{DROPOUT}$), the part enters dropout mode, and LDO's current limit drops by 15%. The difference between V_{LDO_IN} and V_{OUTx} must remain above 1.5V when designing the circuit.

Fault Indictor (/FT, Pin 6)

The /FT pin resistance (R_{FT}), denoted by R2, is recommended to be about 100kΩ.

/FT is connected to an internal MOSFET's open drain. For fault indication, /FT should be connected to a ≤5V voltage via an external pull-up resistor.

If not used, float /FT or connect it to ground.

Enable (EN, Pin 7)

The EN pin can enable and disable the entire device. Pull EN below the 2.2V falling threshold to shut down the chip. Pull EN above the 2.4V rising threshold to enable the chip.

Separate, dedicated register bits enable the software of LDO1 and LDO2, respectively. The physical EN pin has a higher priority than the software enable function.

Since EN has a 3.3MΩ pull-down resistor, float EN to shut down the chip. EN can be connected to a high-voltage bus (e.g. the VIN pin) via a pull-up resistor. In this scenario, it is recommended to use a 100kΩ pull-up resistor.

The MPQ2022A has an internal, fixed UVLO threshold. In the normal input range, the rising threshold is 4.2V, and the falling threshold is 3.8V. For applications that require a higher UVLO threshold, place an external resistor between VIN and EN to raise the equivalent UVLO threshold (see Figure 11).

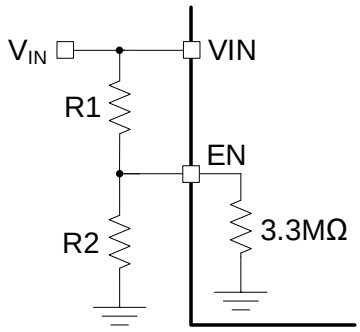


Figure 11: Adjustable UVLO through EN Divider

The UVLO rising threshold ($V_{IN\_UVLO\_VTH\_R}$) can be calculated with Equation (3):

$$V_{IN\_UVLO\_VTH\_R} = (1+\frac{R1}{R2 \,||\, 3.3M\Omega}) \times V_{EN\_VTH\_R} \quad (3)$$

Where $V_{EN\_VTH\_R}$ is 2.4V.

The UVLO falling threshold ($V_{IN\_UVLO\_VTH\_F}$) can be calculated with Equation (4):

$$V_{IN\_UVLO\_VTH\_F} = (1+\frac{R1}{R2 \,||\, 3.3M\Omega}) \times V_{EN\_VTH\_F} \quad (4)$$

Where $V_{EN\_VTH\_F}$ is 2.2V.

To quickly turn EN on and off, the EN off time must be longer than 500µs.

Selecting the Input Capacitor (VIN, Pin 9)

Use a low-ESR capacitor exceeding 4.7µF to minimize the IC noise. Ceramic capacitors are recommended, but tantalum or low-ESR electrolytic capacitors are also sufficient.

To ensure stable operation, place the input capacitor as close to the IC as possible. As an alternative, place a small, high-quality, 0.1µF ceramic capacitor close to the IC, and place the larger-value capacitor further away. If using the latter technique, use either tantalum- or electrolytic-type capacitors for the larger-value capacitor. Place all ceramic capacitors close to the MPQ2022A.

Do Not Connect (DNC, Pin 10 and Pin 11)

Do not connect. The DNC pins are reserved for factory functions. It is recommended to float DNC.

Selecting the Resistor for the Serial Digital Interface Address (ADD, Pin 12)

The MPQ2022A supports 7 addresses, for up to 7 voltage rails, by detecting the different voltages on the ADD pin. Table 2 on page 26 shows the resistances for different serial digital interface addresses. The resistor's tolerance should not exceed 1% of the recommended resistance.

Serial Digital Interface (SDA, Pin 13; SCL, Pin 14)

The MPQ2022A's interface is a serial digital interface slave that supports fast mode (400kHz), which adds flexibility to the power supply solution. See the Serial Digital Interface section on page 24 for more details.

If the serial digital interface is not used, it is recommended to connect these pins to the VCC pin via a resistor (e.g. 100kΩ).

Setting the Reference Voltage Input for the Dual LDOs (ADJ1, Pin 15; ADJ2, Pin 16)

External voltage tracking mode is enabled via the serial digital interface. If enabled, V_{OUT1} and V_{OUT2} are equal to the voltages at ADJ1 and ADJ2, respectively. For stable operation, use a 10nF to 100nF ceramic capacitor with X5R or X7R dielectrics.

If ADJ1 and ADJ2 are not used, it is recommended to float these pins or connect them to GND.

GND Connection (AGND, Pin 2; GND, Pin 8)

See the PCB Layout Guidelines section on page 37 for more details.

External Reverse Voltage Protection

In some situations (e.g. a backup battery is connected as the MPQ2022A's load), V_{OUTx} may be pulled up while V_{IN} is pulled to ground, pulled to some intermediate voltage, or is floated. Thus, V_{OUT} exceeds V_{IN}. Since the MPQ2022A's P-channel MOSFET pass element has a body diode, the current is conducted from the output to input and is not internally limited. The body diode's maximum I_{OUT} is 1A. The unlimited body diode's reverse current may exceed 1A, which results in the device being damaged. To avoid this scenario, it is recommended to place an external diode at the input (see Figure 12). The diode's recommended parameter is 40V/2A.

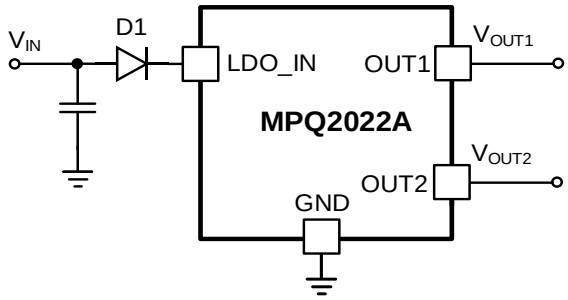


Figure 12: External Reverse Voltage Protection

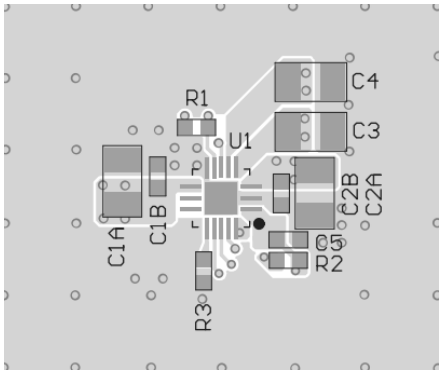
PCB Layout Guidelines [10]

Efficient PCB layout (especially for the input capacitor and output capacitor) is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 13 and follow the guidelines below:

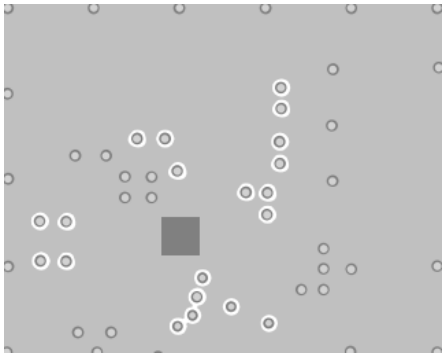
1. Place the input capacitor as close to the VIN and GND pins as possible.
2. Use a large ground plane to connect directly to PGND.
3. If the bottom layer is a ground plane, add vias near PGND.
4. Ensure that the high-current paths (e.g. PGND and LDO_IN) have short, direct, and wide traces.
5. To minimize high frequency, place the ceramic input capacitor, especially the small package size (0603), input/output bypass capacitor, as close to the VIN, LDO_IN, and PGND pins as possible.
6. Keep the connections between the input capacitor, VIN, and LDO_IN as short and wide as possible.
7. Place the VCC capacitor as close to the VCC and AGND pins as possible.
8. Use multiple vias to connect the power planes to the internal layers.

Note:

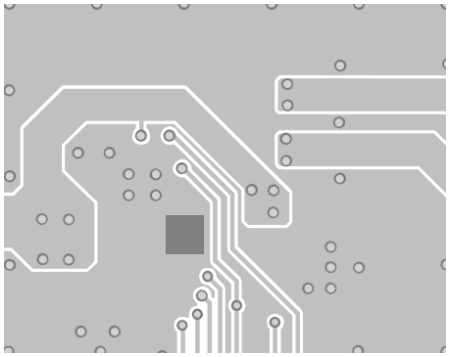
10) The recommended PCB layout is based on Figure 14 on page 38.



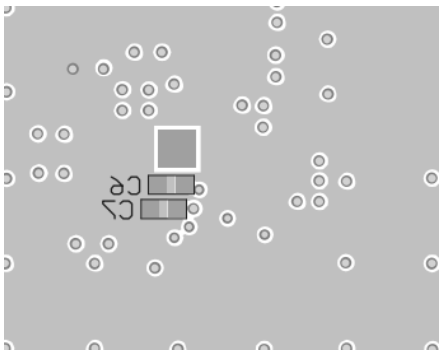
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 13: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

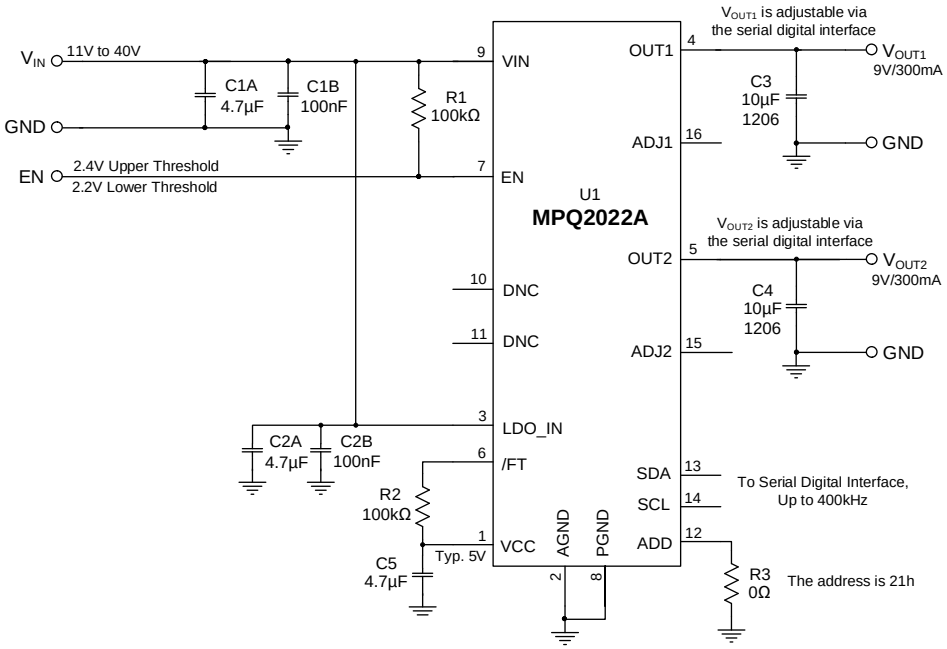
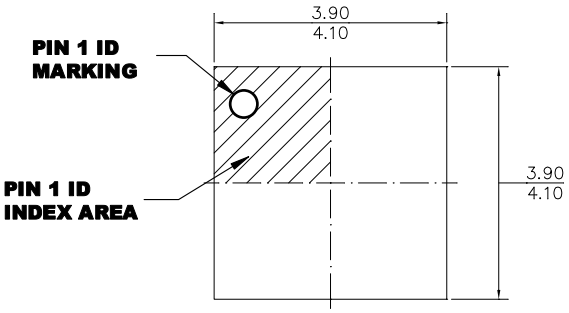


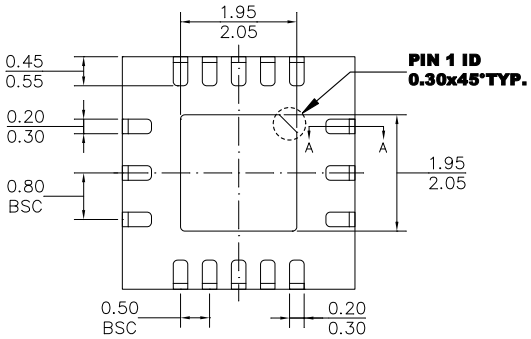
Figure 14: Typical Application Circuit (V_{OUT1} = 9V, V_{OUT2} = 9V)

PACKAGE INFORMATION

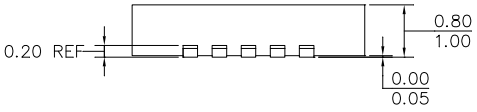
QFN-16 (4mmx4mm)
Wettable Flank



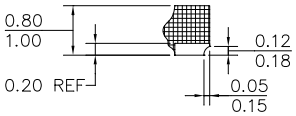
TOP VIEW



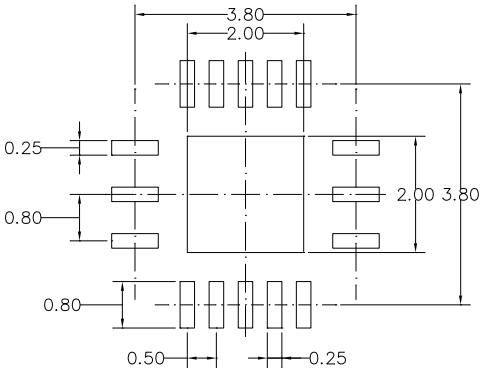
BOTTOM VIEW



SIDE VIEW



SECTION A-A

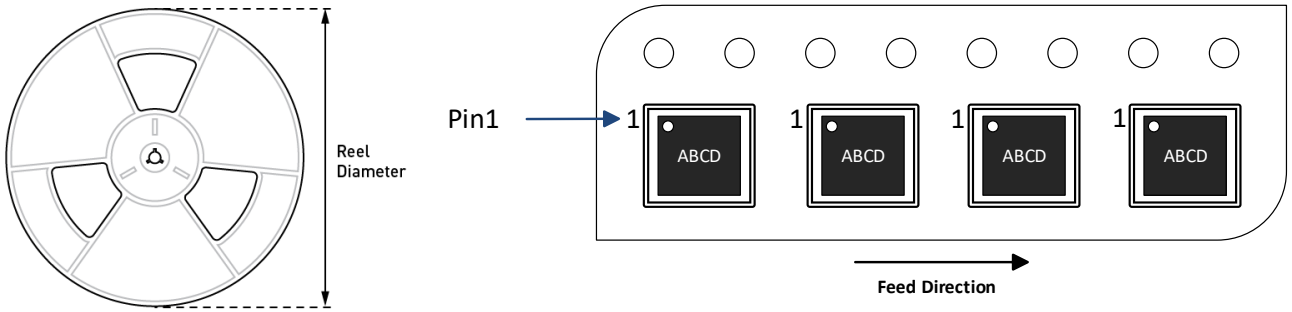


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING REFERENCE TO JEDEC MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2022AGRE-xxxx-AEC1-Z	QFN-16 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	06/26/2023	Initial Release	-