



# MPQ2177

5.5V, 1A, 2.4MHz, Synchronous  
Step-Down Converter with Power Good  
and Soft Start, AEC-Q100 Qualified

## DESCRIPTION

The MPQ2177 is a monolithic, step-down, switch-mode converter with built-in internal power MOSFETs. It achieves 1A of continuous output current across a 2.5V to 5.5V input voltage ( $V_{IN}$ ) range, with excellent load and line regulation. The output voltage ( $V_{OUT}$ ) can be regulated to as low as 0.6V.

The constant-on-time (COT) control scheme provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MPQ2177 is ideal for a wide range of applications, including automotive infotainment systems, clusters, and telematics.

The MPQ2177 requires a minimal number of readily available, standard external components, and is available in an ultra-small QFN-8 (1.5mmx2mm) package.

## FEATURES

### Designed for Automotive Applications

- Wide 2.5V to 5.5V Operating  $V_{IN}$  Range
- Up to 1A Output Current
- 1% FB Accuracy
- Junction Temperature Operation from -40°C to +150°C

### High Performance for Improved Thermals

- 75mΩ and 45mΩ Internal Power MOSFETs

### Optimized for EMC/EMI

- 2.4MHz Switching Frequency
- Forced Continuous Conduction Mode (CCM) across the Full Load Range
- MeshConnect™ Flip-Chip Package

### Optimized for Board Size and BOM

- Built-In Internal Power MOSFETs
- Integrated Compensation Network
- Fixed Output Options

### Additional Features

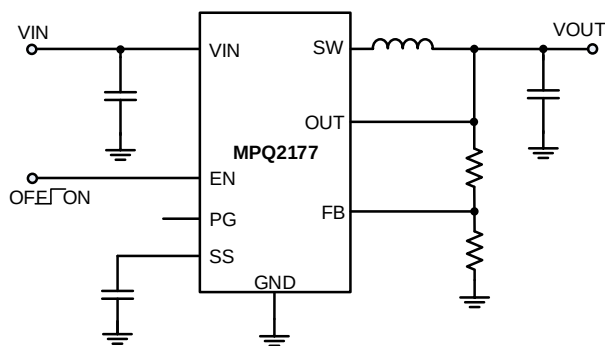
- EN for Power Sequencing
- Power Good (PG)
- 100% Duty On
- External Soft Start (SS) Control
- Output Discharge
- Output Over Voltage Protection (Vo OVP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Available in a QFN-8 (1.5mmx2mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade 1

## APPLICATIONS

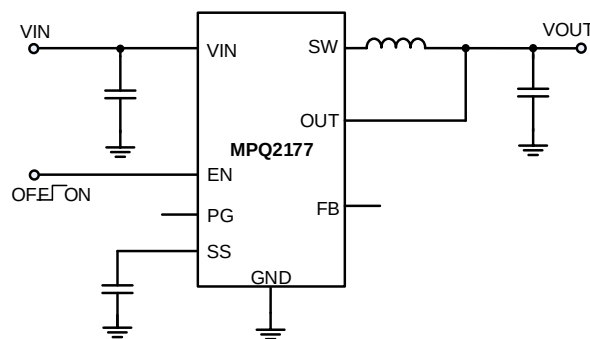
- Automotive Infotainment
- Camera Modules
- Key Fobs
- Automotive Clusters
- Automotive Telematics
- Industrial Supplies
- Battery-Powered Devices

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

## TYPICAL APPLICATION



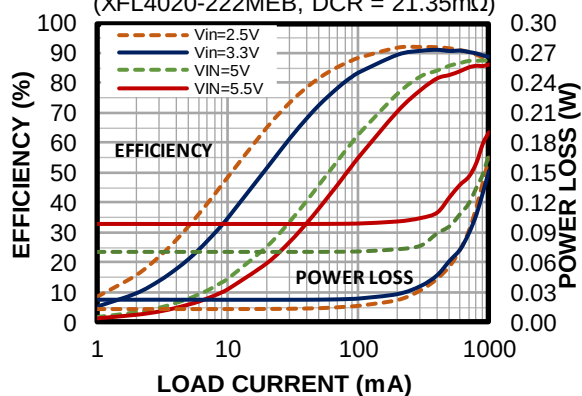
Adjustable Output Version



Fixed Output Version

### Efficiency vs. Load Current vs. Power Loss

$V_{OUT} = 1.2V$ ,  $L = 2.2\mu H$ ,  
(XFL4020-222MEB, DCR = 21.35m $\Omega$ )



## ORDERING INFORMATION

| Part Number*           | Package           | Top Marking | MSL Rating** |
|------------------------|-------------------|-------------|--------------|
| MPQ2177GQHE***         | QFN-8 (1.5mmx2mm) | See Below   | 1            |
| MPQ2177GQHE-AEC1***    |                   |             |              |
| MPQ2177GQHE-12-AEC1*** |                   |             |              |
| MPQ2177GQHE-18-AEC1*** |                   |             |              |

\* For Tape & Reel, add suffix -Z (e.g. MPQ2177GQHE-AEC1-Z).

\*\* Moisture Sensitivity Level Rating

\*\*\* Wettable flank

## TOP MARKING

—  
KR  
LL

KR: Product code of MPQ2177GQHE and MPQ2177GQHE-AEC1

LL: Lot number

—  
LG  
LL

LG: Product code of MPQ2177GQHE-12-AEC1

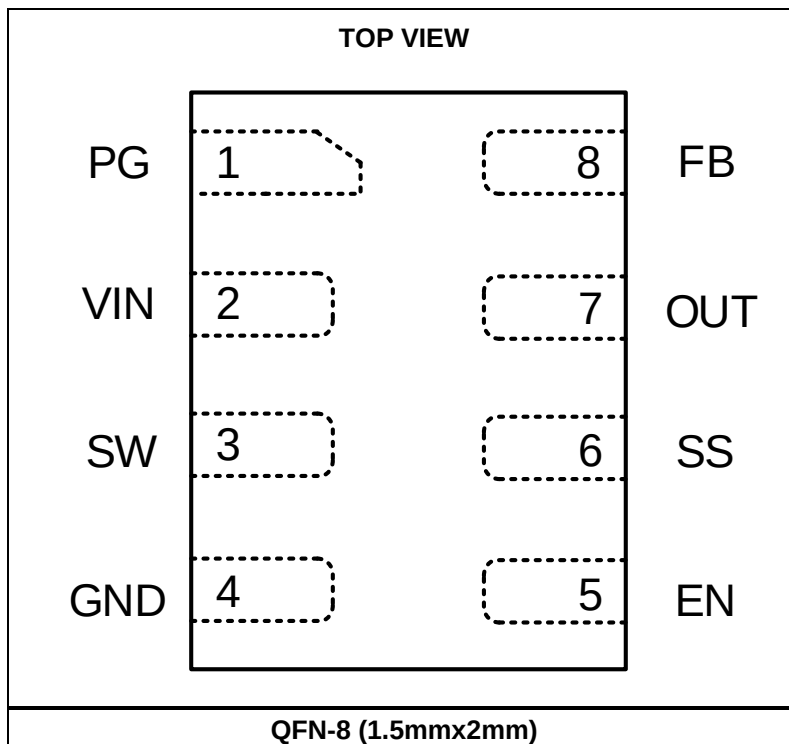
LL: Lot number

—  
LH  
LL

LH: Product code of MPQ2177GQHE-18-AEC1

LL: Lot number

# PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin # | Name | Description                                                                                                                                                                                                                                                                                       |
|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | PG   | <b>Power good indicator.</b> The output of this pin is an open drain. Connect PG to a voltage source using an external resistor. PG is pulled high when $V_{FB}$ exceeds 90% of $V_{REF}$ ; PG is pulled low to GND if $V_{FB}$ drops below 85% of $V_{REF}$ . Float this pin if not used.        |
| 2     | VIN  | <b>Supply voltage.</b> The MPQ2177 operates from a 2.5V to 5.5V input. A decoupling capacitor is required to prevent large voltage spikes from appearing at the input.                                                                                                                            |
| 3     | SW   | <b>Output switching node.</b> SW is the drain of the internal, high-side P-channel MOSFET. Connect the inductor to SW to complete the converter.                                                                                                                                                  |
| 4     | GND  | <b>Ground.</b>                                                                                                                                                                                                                                                                                    |
| 5     | EN   | <b>On/off control.</b> Pull EN below the falling threshold (0.65V) to shut down the chip. Pull EN above the rising threshold (0.9V) to enable the chip. There is an internal 2M $\Omega$ resistor from EN pin to ground.                                                                          |
| 6     | SS   | <b>Soft start.</b> Connect a capacitor across SS and GND to set the soft-start time ( $t_{SS}$ ) to avoid start-up inrush current. The minimum recommended soft-start capacitance ( $C_{SS}$ ) is 1nF.                                                                                            |
| 7     | OUT  | <b>Output voltage.</b> The OUT pin is output voltage ( $V_{OUT}$ ) for the power rail and input sense. Connect the load to this pin. An output capacitor is required to decrease the output voltage ripple.                                                                                       |
| 8     | FB   | <b>Feedback pin.</b> An external resistor divider from the output to GND, tapped to the FB pin. The FB voltage ( $V_{FB}$ ) is compared to the internal 0.6V reference voltage ( $V_{REF}$ ) to set the regulation voltage. For the fixed output version of the MPQ2177, this pin can be floated. |

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

All pins ..... -0.3V to +6.5V  
 Junction temperature ..... 150°C  
 Lead temperature ..... 260°C  
 Continuous power dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(2)</sup> <sup>(4)</sup>  
 ..... 2.2W  
 Storage temperature ..... -65°C to +150°C

## ESD Ratings

Human body model (HBM) .....  $\pm 2000\text{V}$   
 Charged device model (CDM) .....  $\pm 750\text{V}$

## Recommended Operating Conditions

Supply voltage ( $V_{IN}$ ) ..... 2.5V to 5.5V  
 Output voltage ( $V_{OUT}$ ) ..... 0.6V to  $V_{IN} - 0.5\text{V}$   
 Operating junction temp ( $T_J$ ) .... -40°C to +150°C

## Thermal Resistance

 $\theta_{JA}$   $\theta_{JC}$ 

QFN-8 (1.5mmx2mm)

JESD51-7 <sup>(3)</sup> ..... 130 ..... 25 ..... °C/W

EVQ2177-LE-00A <sup>(4)</sup> ..... 59 ..... 14 ..... °C/W

### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
- Measured on EVQ2177-LE-00A, 2oz per layer, 6.3cmx6.3cm, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical value tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                           | Symbol         | Condition                                                                                                      | Min   | Typ  | Max   | Units      |
|-----------------------------------------------------|----------------|----------------------------------------------------------------------------------------------------------------|-------|------|-------|------------|
| $V_{IN}$ range                                      |                |                                                                                                                | 2.5   |      | 5.5   | V          |
| Under-voltage lockout (UVLO) rising threshold       |                |                                                                                                                |       | 2.3  | 2.45  | V          |
| UVLO threshold hysteresis                           |                |                                                                                                                |       | 200  |       | mV         |
| Shutdown supply current                             |                | $V_{EN} = 0V$ , $T_J = 25^{\circ}C$                                                                            |       | 0.01 | 1     | $\mu A$    |
|                                                     |                | $V_{EN} = 0V$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$ <sup>(6)</sup>                                         |       |      | 3     | $\mu A$    |
|                                                     |                | $V_{EN} = 0V$ , $T_J = -40^{\circ}C$ to $+150^{\circ}C$                                                        |       |      | 20    | $\mu A$    |
| Quiescent supply current                            |                | $V_{EN} = 2V$ , $V_{FB} = 0.63V$ , $V_{IN} = 3.6V$ , $T_J = 25^{\circ}C$                                       |       | 460  | 650   | $\mu A$    |
| Feedback voltage                                    | $V_{FB}$       | $T_J = 25^{\circ}C$                                                                                            | 594   | 600  | 606   | mV         |
|                                                     |                | $T_J = -40^{\circ}C$ to $+150^{\circ}C$                                                                        | 591   | 600  | 609   |            |
| Feedback current                                    | $I_{FB}$       | $V_{FB} = 0.63V$ , adjustable output                                                                           |       | 50   | 100   | nA         |
|                                                     |                | $V_{FB} = 0.63V$ , 1.2V fixed output                                                                           |       | 3    | 8     | $\mu A$    |
|                                                     |                | $V_{FB} = 0.63V$ , 1.8V fixed output                                                                           |       | 5    | 10    | $\mu A$    |
| Output regulation voltage (fixed output version)    | $V_{OUT\_REG}$ | 1.2V fixed output                                                                                              | 1.176 | 1.2  | 1.224 | V          |
|                                                     |                | 1.8V fixed output                                                                                              | 1.764 | 1.8  | 1.836 | V          |
| P-channel MOSFET on resistance                      | $R_{DS(ON)_P}$ | $V_{IN} = 5V$                                                                                                  |       | 75   | 110   | m $\Omega$ |
| N-channel MOSFET on resistance                      | $R_{DS(ON)_N}$ | $V_{IN} = 5V$                                                                                                  |       | 45   | 70    | m $\Omega$ |
| Switch leakage                                      |                | $V_{EN} = 0V$ , $V_{IN} = 6V$ , $V_{SW} = 0V$ or $6V$ , $T_J = 25^{\circ}C$                                    |       | 0    | 1     | $\mu A$    |
|                                                     |                | $V_{EN} = 0V$ , $V_{IN} = 6V$ , $V_{SW} = 0V$ or $6V$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$ <sup>(6)</sup> |       |      | 30    | $\mu A$    |
| Switching frequency                                 | $f_{SW}$       | $V_{IN} = 5V$ , $V_{OUT} = 1.2V$ , CCM                                                                         | 2000  | 2400 | 2640  | kHz        |
| Minimum on time <sup>(6)</sup>                      | $t_{MIN\_ON}$  | $V_{IN} = 5V$                                                                                                  |       | 50   |       | ns         |
| Minimum off time <sup>(6)</sup>                     | $t_{MIN\_OFF}$ | $V_{IN} = 5V$                                                                                                  |       | 80   |       | ns         |
| P-channel MOSFET peak current limit                 |                |                                                                                                                | 1.6   | 2.5  | 3.4   | A          |
| N-channel MOSFET valley current limit               |                |                                                                                                                | 0.4   | 1    | 1.6   | A          |
| Soft-start current                                  | $I_{SS\_ON}$   |                                                                                                                | 1.5   | 3    | 4.5   | $\mu A$    |
| Maximum duty cycle                                  |                |                                                                                                                |       | 100  |       | %          |
| Power good (PG) under-voltage (UV) rising threshold |                | FB rising edge                                                                                                 | 87    | 90   | 93    | %          |
| PG UV falling threshold                             |                | FB falling edge                                                                                                | 82    | 85   | 88    | %          |
| PG delay                                            | $t_{PGD}$      | PG rising/falling edge                                                                                         |       | 80   |       | $\mu s$    |

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical value tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                  | Symbol         | Condition                        | Min | Typ  | Max | Units       |
|--------------------------------------------|----------------|----------------------------------|-----|------|-----|-------------|
| PG sink current capability                 | $V_{PG\_L}$    | Sink 1mA                         |     |      | 0.4 | V           |
| PG logic high voltage                      | $V_{PG\_H}$    | $V_{IN} = 5V$ , $V_{FB} = 0.6V$  | 4.9 |      |     | V           |
| Self-bias PG <sup>(5)</sup>                |                |                                  |     |      | 0.7 | V           |
| PG leakage current/logic high              |                | 5V logic high                    |     |      | 100 | nA          |
| EN turn-on delay                           |                | EN on to SW active               |     | 100  |     | $\mu s$     |
| EN turn-off delay                          |                | EN off to when switching stops   |     | 30   |     | $\mu s$     |
| EN input logic low voltage                 |                |                                  | 0.4 | 0.65 |     | V           |
| EN input logic high voltage                |                |                                  |     | 0.9  | 1.2 | V           |
| EN pull-down resistor                      |                |                                  |     | 2    |     | M $\Omega$  |
| Output discharge resistor                  | $R_{DIS}$      | $V_{EN} = 0V$ , $V_{OUT} = 1.2V$ |     | 150  |     | $\Omega$    |
| EN input current                           |                | $V_{EN} = 2V$                    |     | 1.2  |     | $\mu A$     |
|                                            |                | $V_{EN} = 0V$                    |     | 0    |     | $\mu A$     |
| Output over-voltage (OV) rising threshold  | $V_{OVP}$      |                                  | 110 | 115  | 120 | % $V_{FB}$  |
| Output OV hysteresis                       | $V_{OVP\_HYS}$ |                                  |     | 10   |     | % $V_{FB}$  |
| Output OV delay                            |                |                                  |     | 2    |     | $\mu s$     |
| Low-side current limit                     |                | Current flow from SW to GND      |     | 1.2  |     | A           |
| Absolute $V_{IN}$ OVP                      |                | After $V_{OUT}$ OVP enable       |     | 6.1  |     | V           |
| Absolute $V_{IN}$ OVP hysteresis           |                |                                  |     | 160  |     | mV          |
| Thermal shutdown <sup>(6)</sup>            |                |                                  |     | 170  |     | $^{\circ}C$ |
| Thermal shutdown hysteresis <sup>(6)</sup> |                |                                  |     | 20   |     | $^{\circ}C$ |

### Notes:

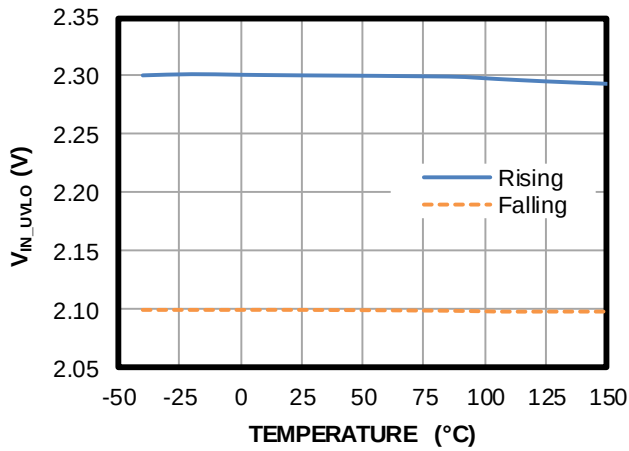
5)  $V_{IN} = 0V$ ,  $EN = 0V$ , PG pulled up to 3V to 5.5V with a 100k $\Omega$  resistor.

6) Guaranteed by design and bench characterization. Not tested in production.

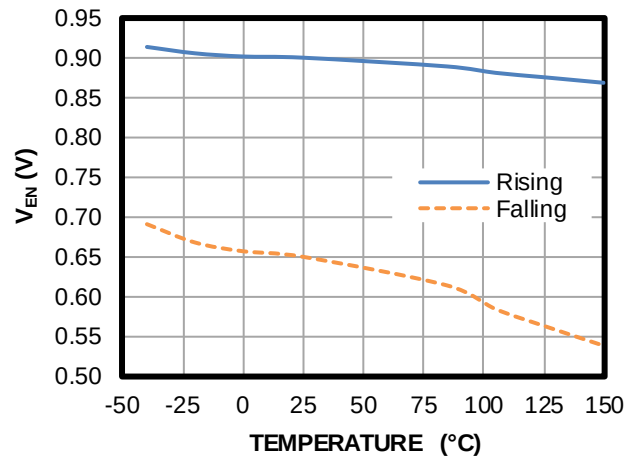
# TYPICAL CHARACTERISTICS

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

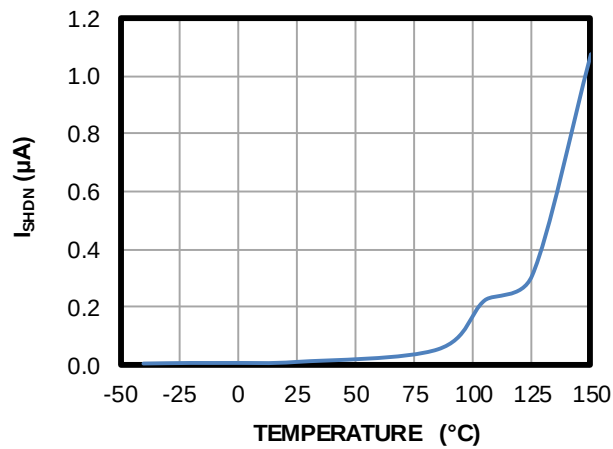
## $V_{IN}$ UVLO Threshold vs. Temperature



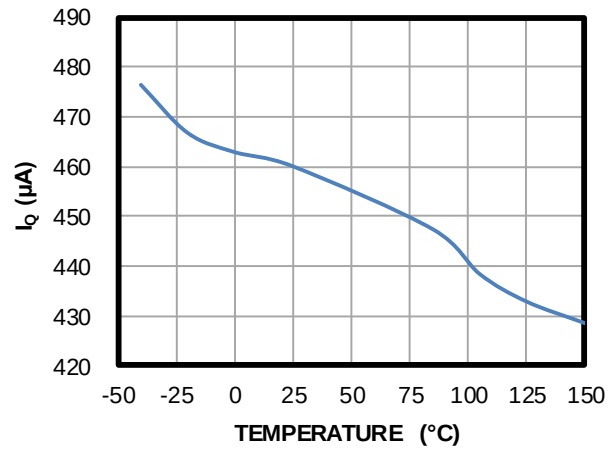
## EN Rising and Falling Threshold vs. Temperature



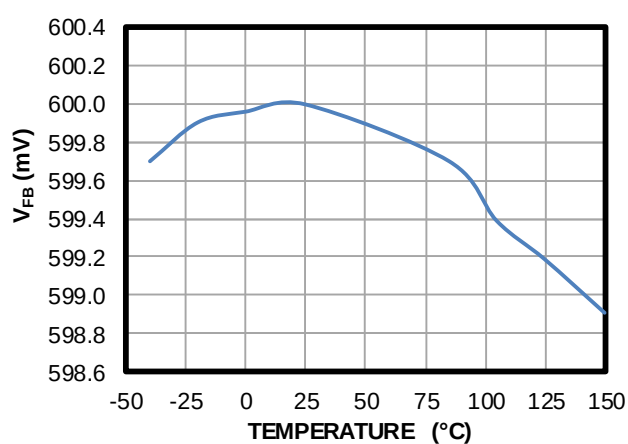
## Shutdown Current vs. Temperature



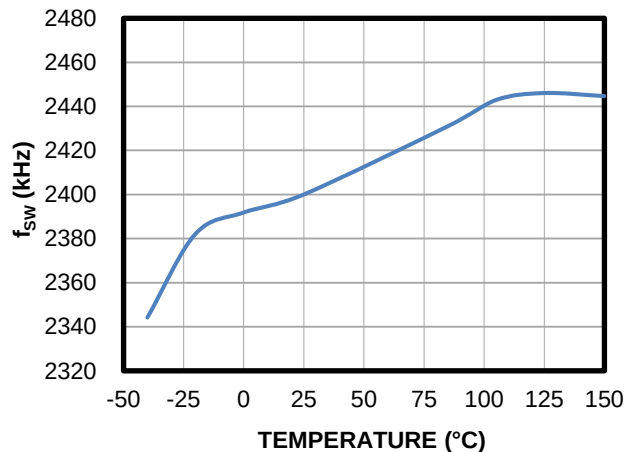
## Quiescent Current vs. Temperature



## $V_{FB}$ vs. Temperature



## Switching Frequency vs. Temperature

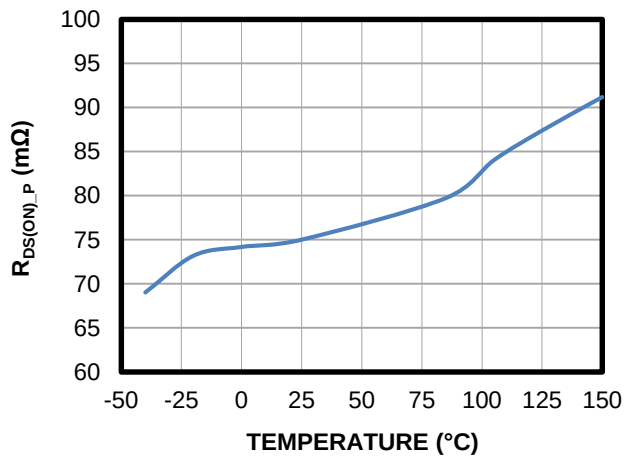




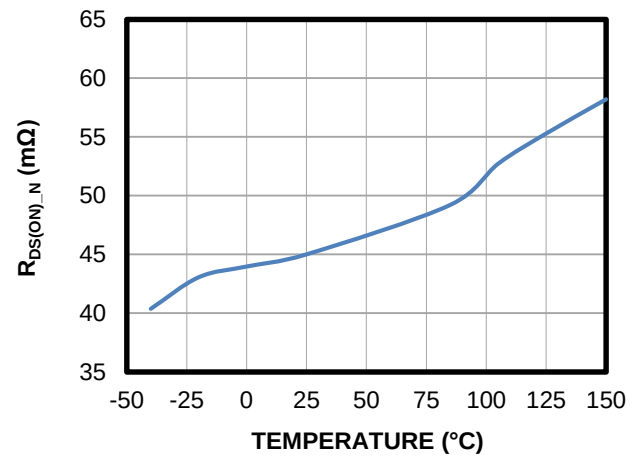
# TYPICAL CHARACTERISTICS (continued)

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

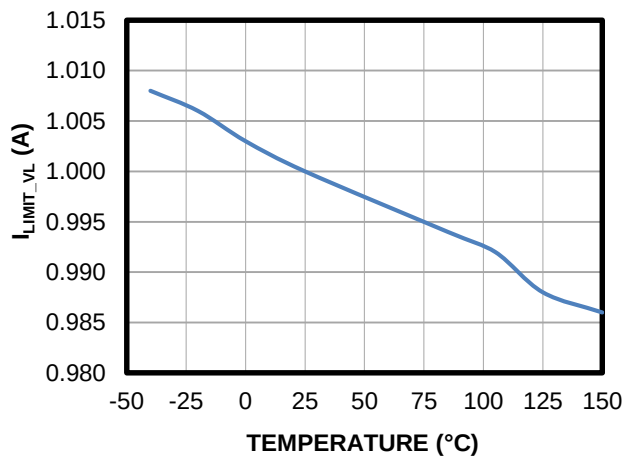
$R_{DS(ON)_P}$  vs. Temperature



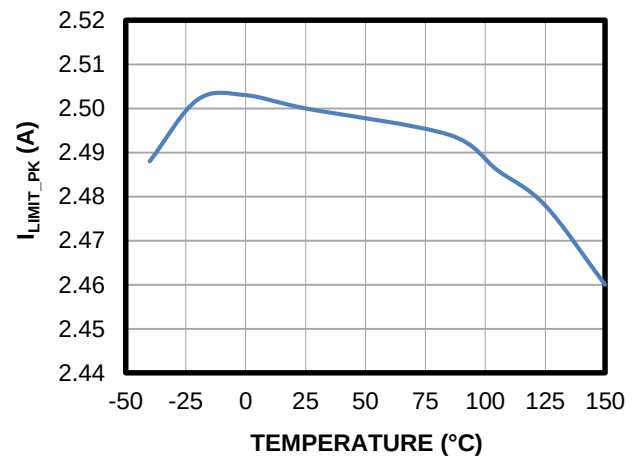
$R_{DS(ON)_N}$  vs. Temperature



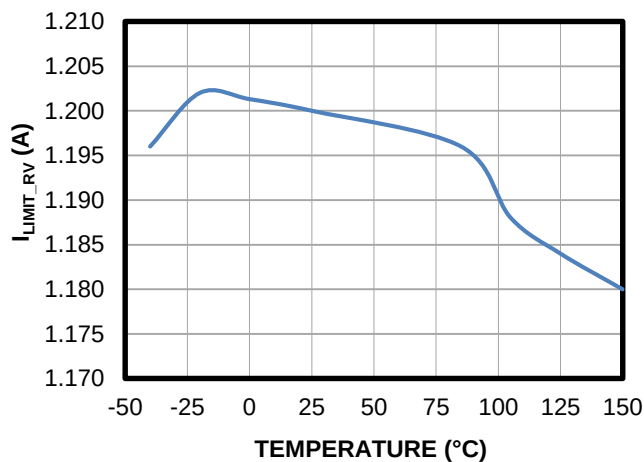
N-Channel MOSFET Valley Current Limit vs. Temperature



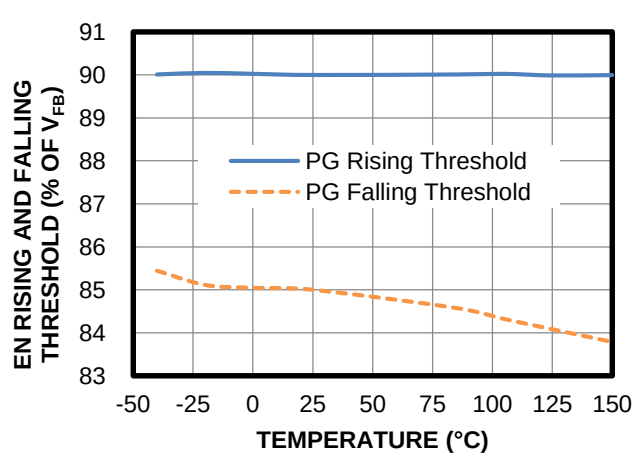
P-Channel MOSFET Peak Current Limit vs. Temperature



Low-Side Reverse Current Limit vs. Temperature



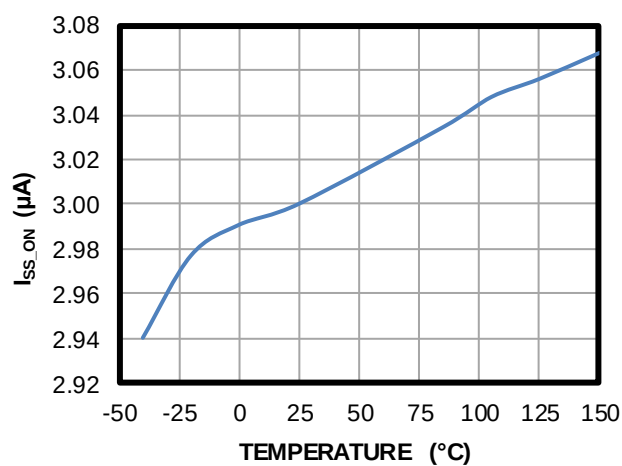
PG Rising and Falling Threshold vs. Temperature



# TYPICAL CHARACTERISTICS *(continued)*

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

Soft-Start Current vs. Temperature

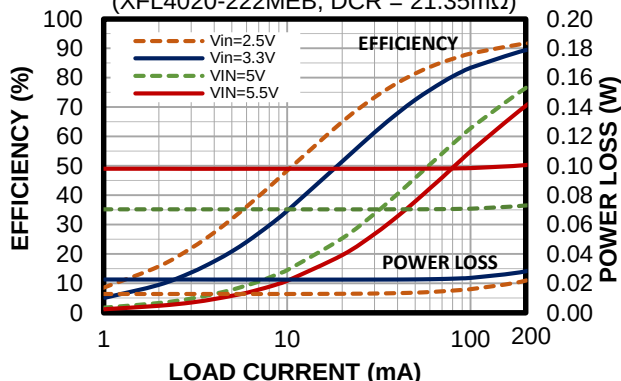


# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

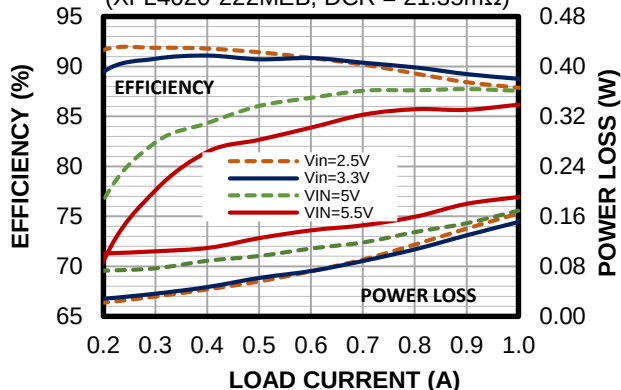
**Efficiency vs. Load Current vs. Power Loss**

$V_{OUT} = 1.2V$ ,  $L = 2.2\mu H$ ,  
(XFL4020-222MEB, DCR = 21.35m $\Omega$ )



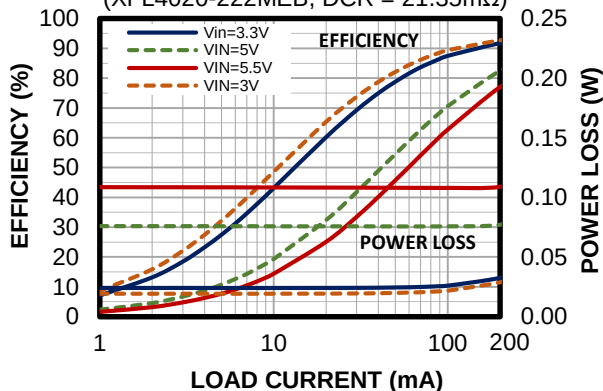
**Efficiency vs. Load Current vs. Power Loss**

$V_{OUT} = 1.2V$ ,  $L = 2.2\mu H$ ,  
(XFL4020-222MEB, DCR = 21.35m $\Omega$ )



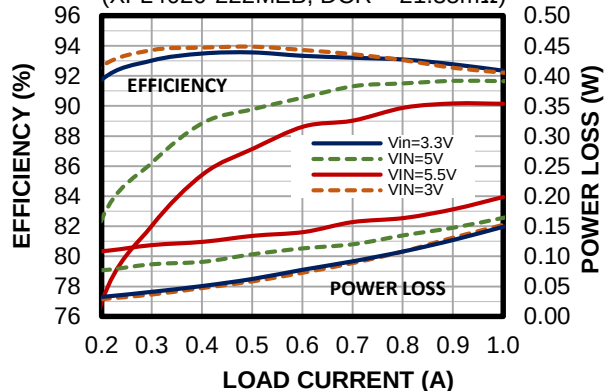
**Efficiency vs. Load Current vs. Power Loss**

$V_{OUT} = 1.8V$ ,  $L = 2.2\mu H$ ,  
(XFL4020-222MEB, DCR = 21.35m $\Omega$ )



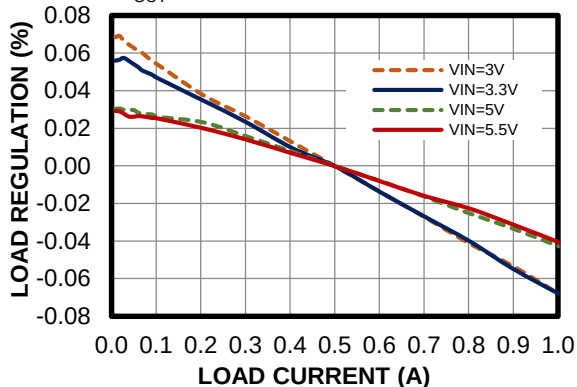
**Efficiency vs. Load Current vs. Power Loss**

$V_{OUT} = 1.8V$ ,  $L = 2.2\mu H$ ,  
(XFL4020-222MEB, DCR = 21.35m $\Omega$ )



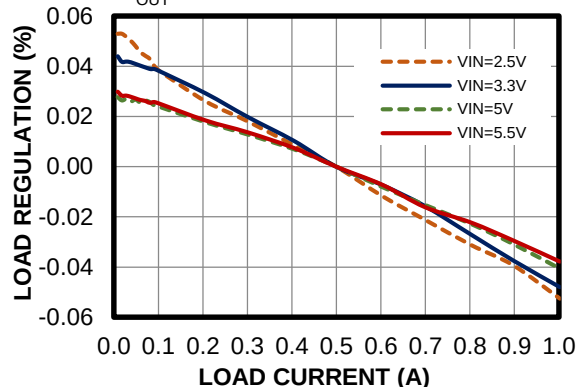
**Load Regulation**

$V_{OUT} = 1.8V$



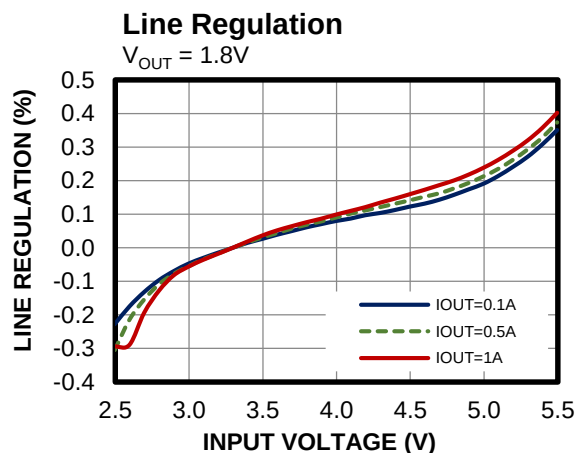
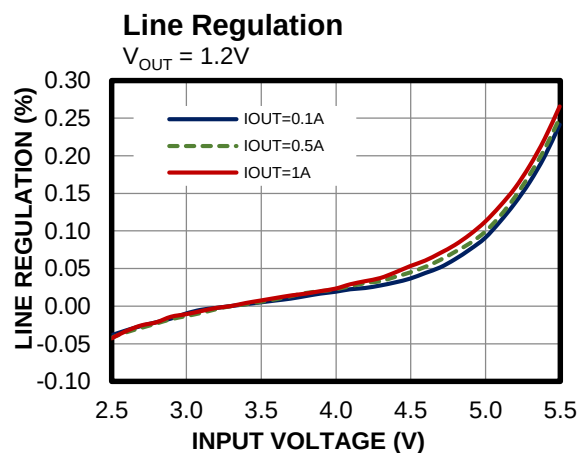
**Load Regulation**

$V_{OUT} = 1.2V$



# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.

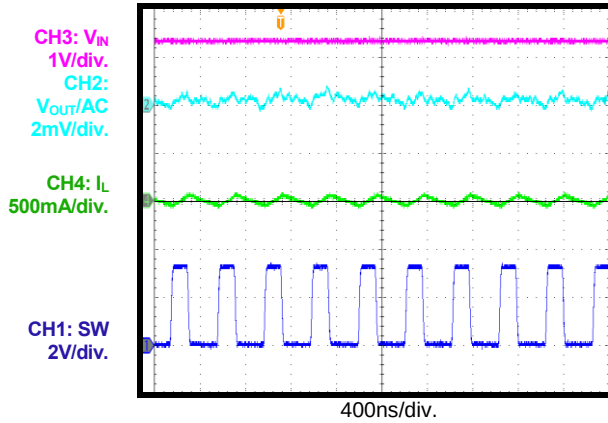


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $L = 2.2\mu H$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

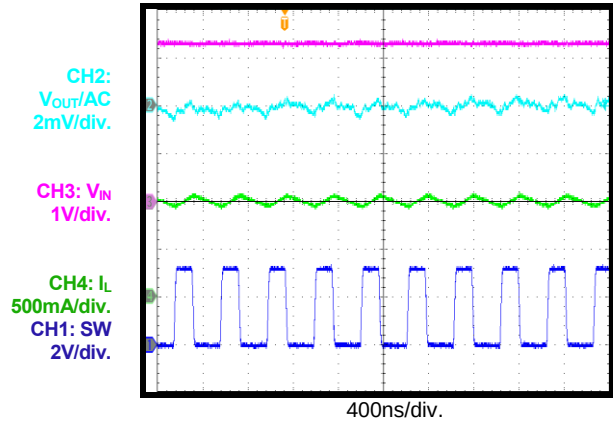
### Steady State

$I_{OUT} = 0A$



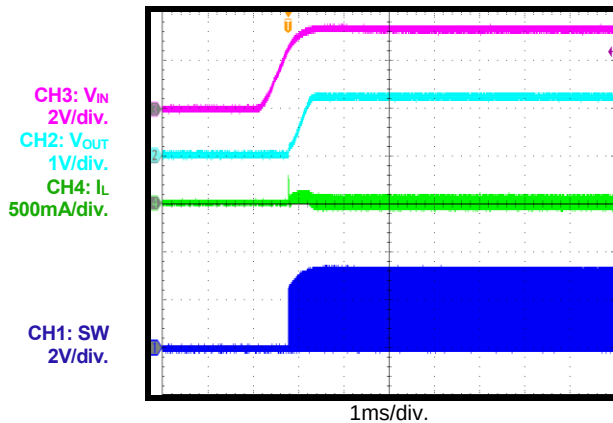
### Steady State

$I_{OUT} = 1A$



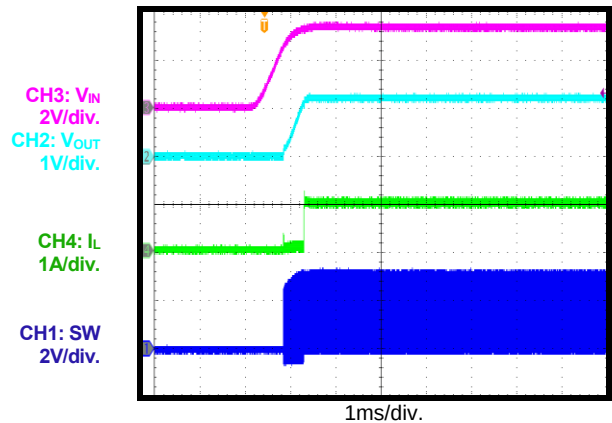
### Start-Up through VIN

$I_{OUT} = 0A$



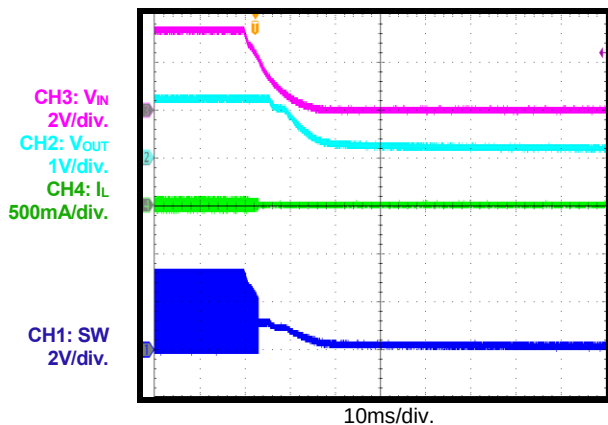
### Start-Up through VIN

$I_{OUT} = 1A$



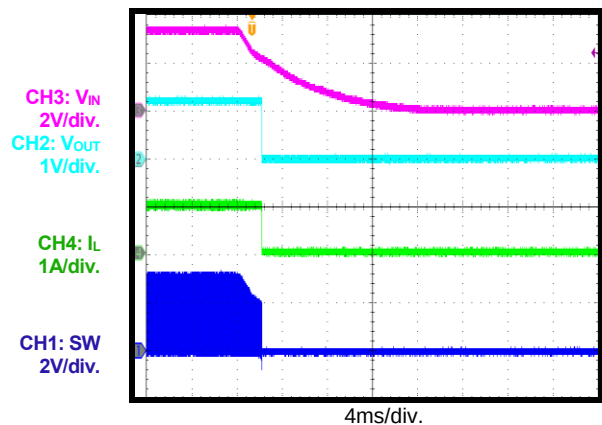
### Shutdown through VIN

$I_{OUT} = 0A$



### Shutdown through VIN

$I_{OUT} = 1A$

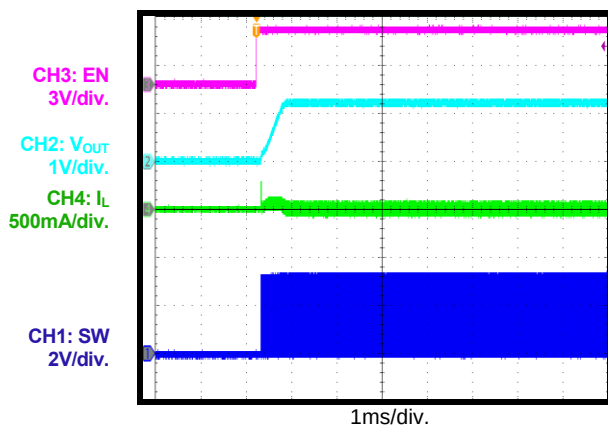


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $L = 2.2\mu H$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

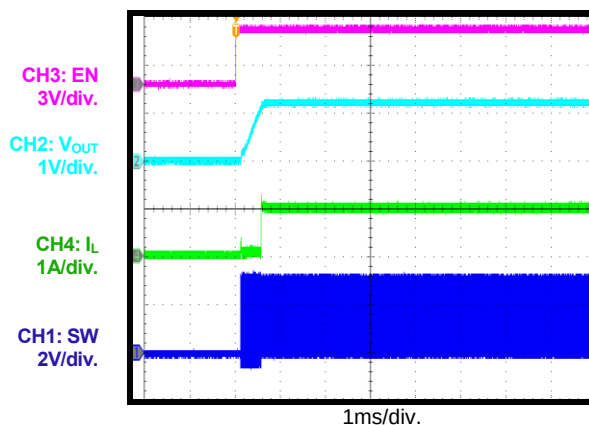
## Start-Up through EN

$I_{OUT} = 0A$



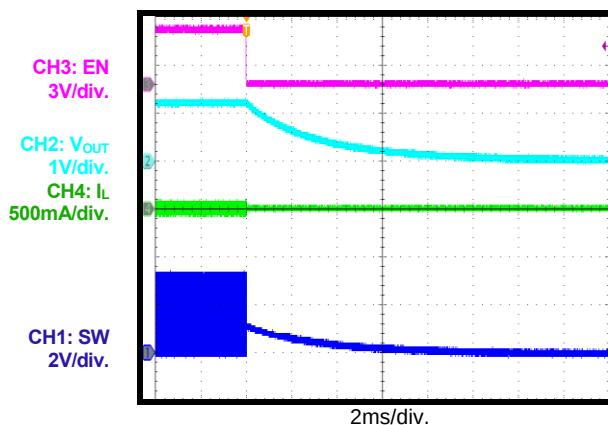
## Start-Up through EN

$I_{OUT} = 1A$



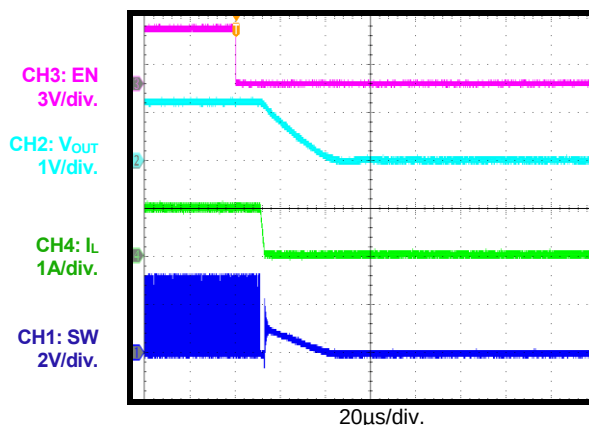
## Shutdown through EN

$I_{OUT} = 0A$



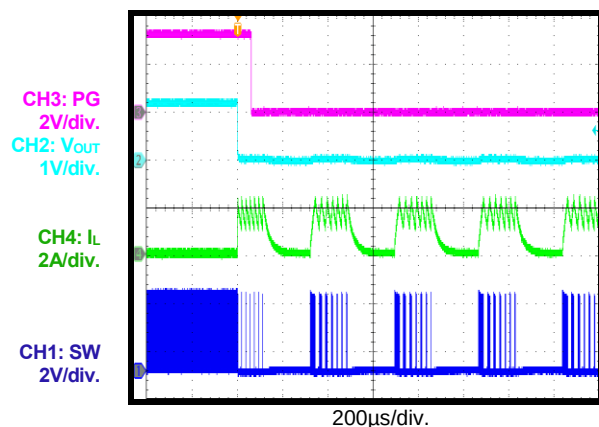
## Shutdown through EN

$I_{OUT} = 1A$



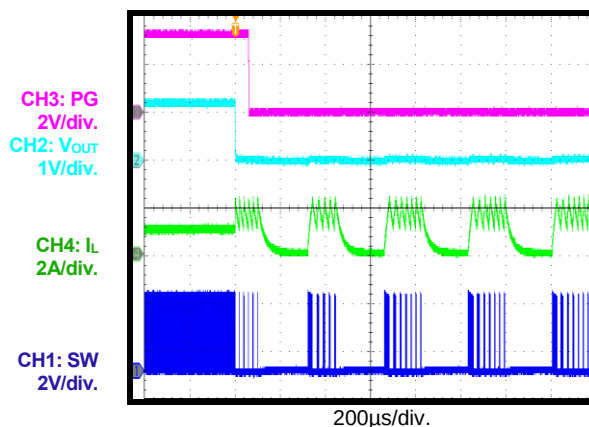
## SCP Entry

$I_{OUT} = 0A$



## SCP Entry

$I_{OUT} = 1A$

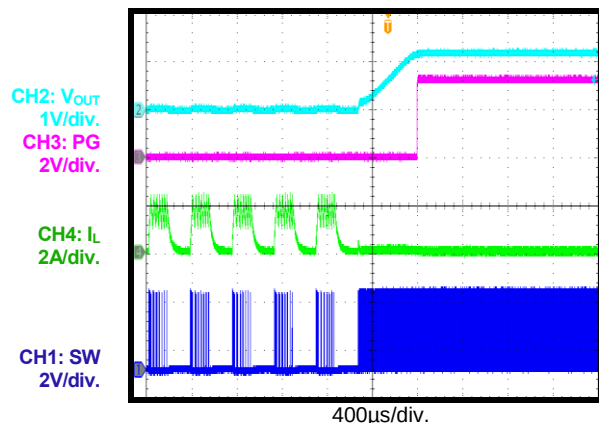


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $L = 2.2\mu H$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

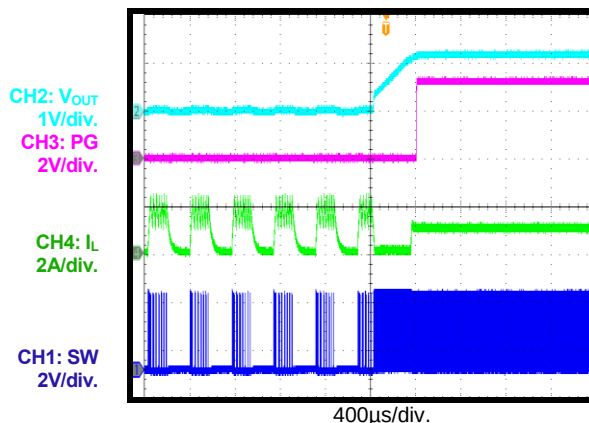
## SCP Recovery

$I_{OUT} = 0A$

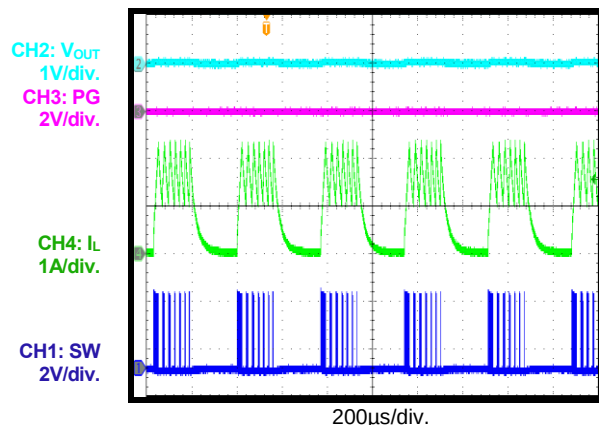


## SCP Recovery

$I_{OUT} = 1A$

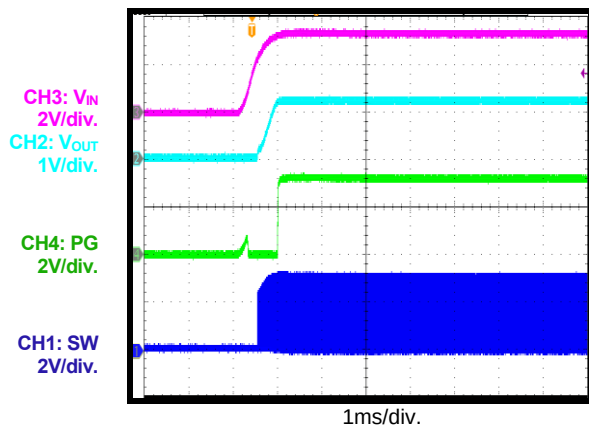


## Short Circuit



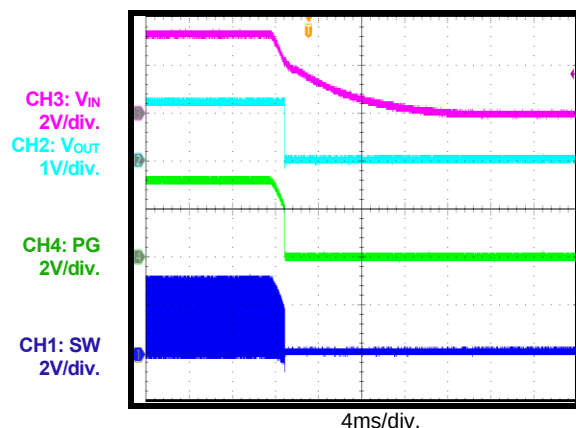
## PG in Start-Up through VIN

$I_{OUT} = 1A$



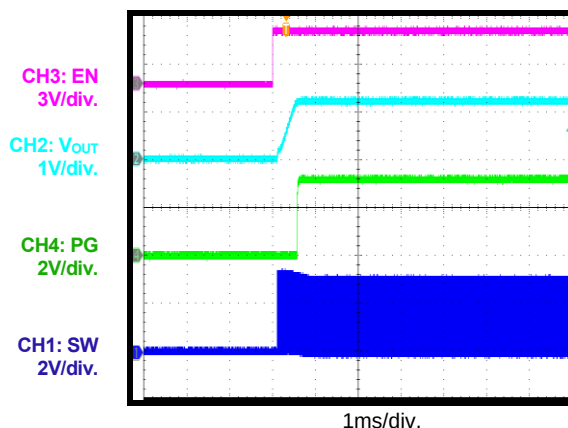
## PG in Shutdown through VIN

$I_{OUT} = 1A$



## PG in Start-Up through EN

$I_{OUT} = 1A$

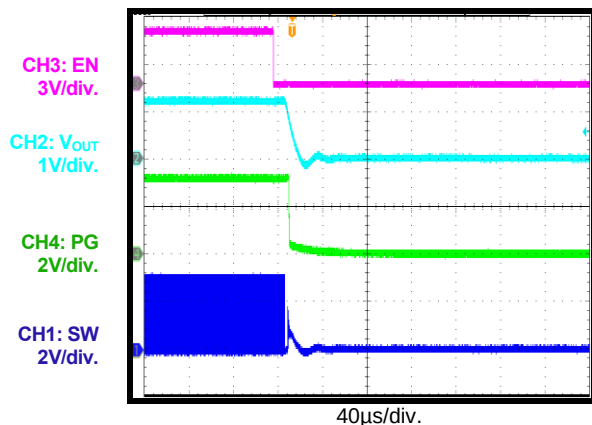


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $L = 2.2\mu H$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

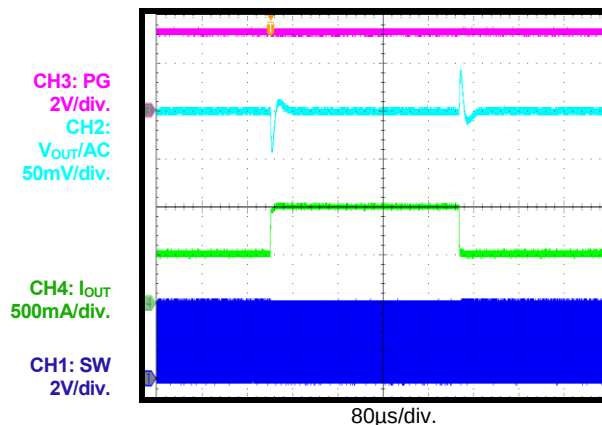
## PG in Shutdown through EN

$I_{OUT} = 1A$



## Load Transient

$I_{OUT} = 0.5A$  to  $1A$ ,  $1A/\mu s$





## FUNCTIONAL BLOCK DIAGRAM

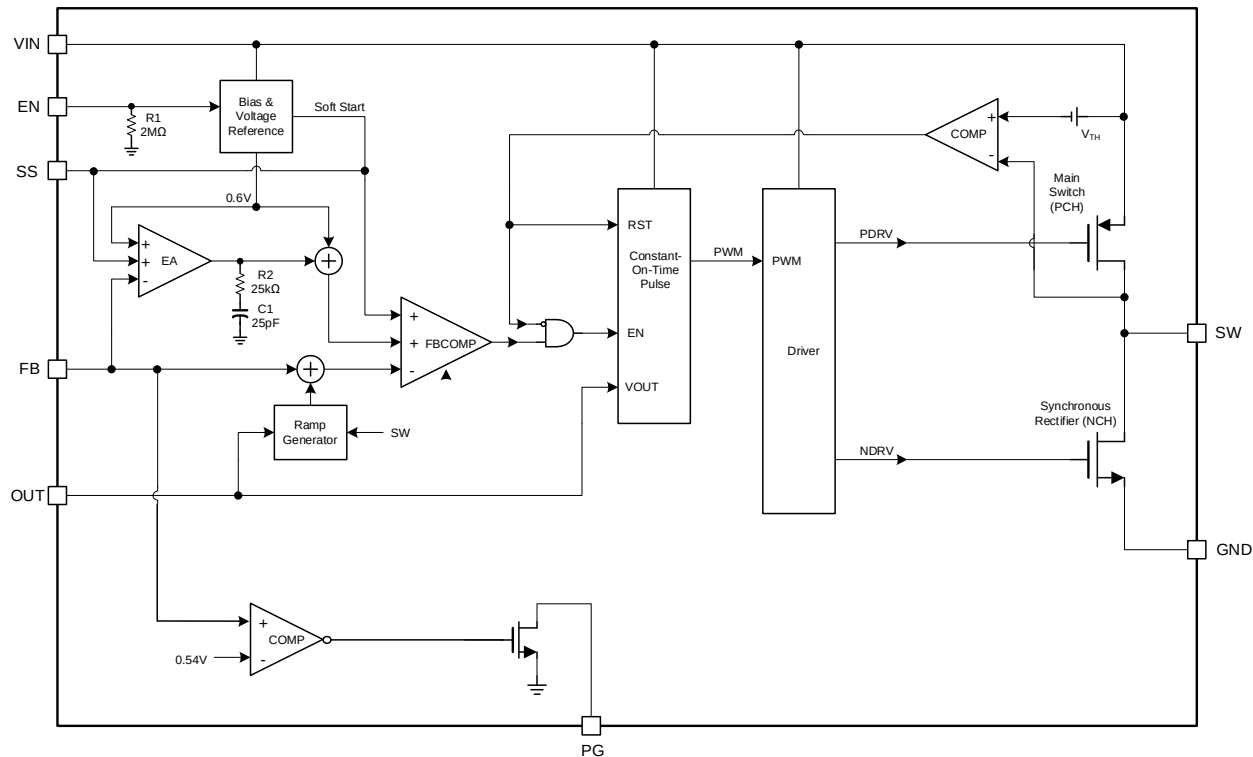


Figure 1: Functional Block Diagram of Adjustable Output Version

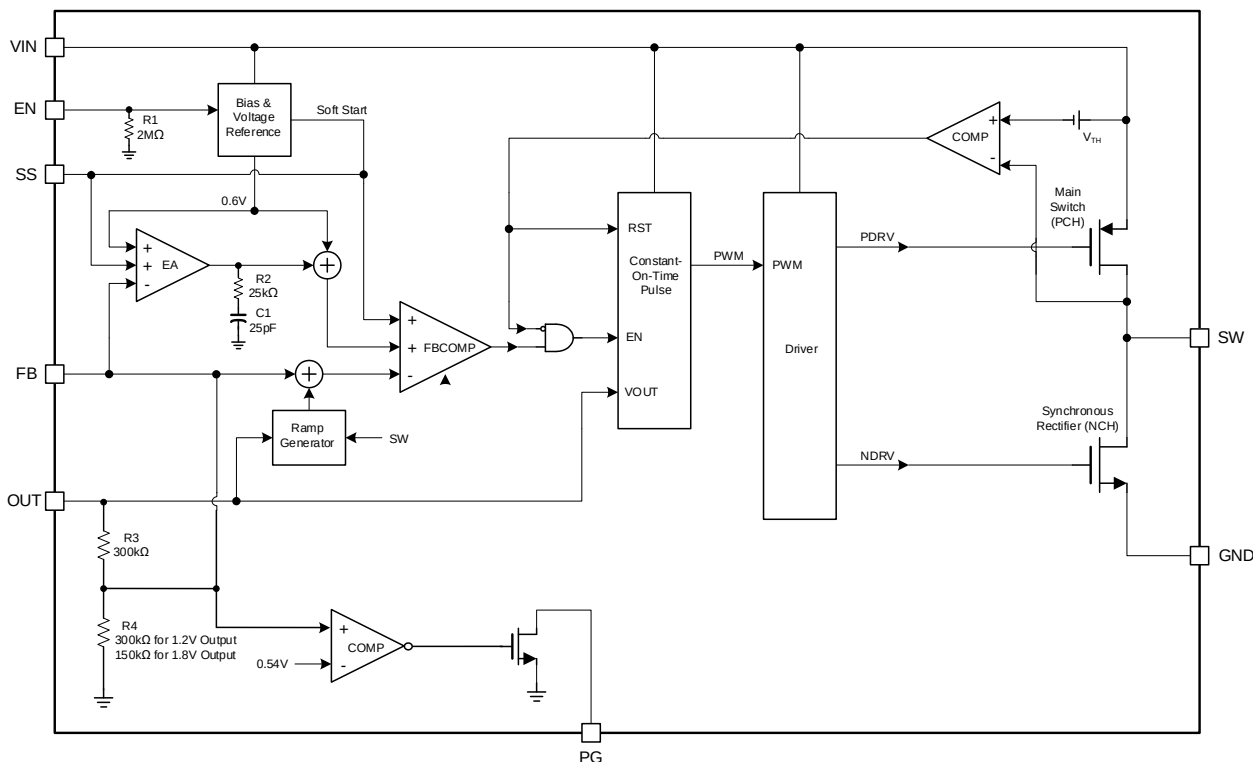


Figure 2: Functional Block Diagram of Fixed Output Version

## OPERATION

The MPQ2177 uses constant-on-time (COT) control with input voltage ( $V_{IN}$ ) feed-forward to stabilize the switching frequency ( $f_{SW}$ ) across the full input range. It achieves 1A of continuous output current ( $I_{OUT}$ ) across a 2.5V to 5.5V  $V_{IN}$  range, with excellent load and line regulation. The output voltage ( $V_{OUT}$ ) can be regulated to as low as 0.6V for the adjustable output version. The MPQ2177 is capable of reaching 100% maximum duty cycle in low-dropout mode.

### Constant-On-Time (COT) Control

Compared to fixed-frequency pulse-width modulation (PWM) control, COT control offers a simpler control loop and faster transient response. To prevent inductor current ( $I_L$ ) runaway during load transient, the MPQ2177's MOSFET has a fixed minimum off time. When low-side N-channel MOSFET (LS-FET) turns on, it remains on for at least  $t_{MIN\_OFF}$ . Then the high-side P-channel MOSFET (HS-FET) turns on when the feedback voltage ( $V_{FB}$ ) drops below the reference voltage ( $V_{REF}$ ), which indicates an insufficient  $V_{OUT}$ . By using  $V_{IN}$  feed-forward, the MPQ2177 maintains a nearly constant  $f_{SW}$  across the input and load ranges. The switching pulse on time ( $t_{ON}$ ) can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400ns \quad (1)$$

In order to improve frequency stability and the reduce output voltage ripple, the MPQ2177 operates in forced continuous conduction mode (FCCM).

### Enable

EN is a digital control pin that turns the MPQ2177 on and off. Pull EN above the EN rising threshold (0.9V) to turn the device on; pull EN below the falling threshold (0.65V) to turn it off. Leaving EN floating or pulling it down to ground disables the MPQ2177. There is an internal 2M $\Omega$  resistor from the EN pin to ground.

### Output Discharge

When the device is disabled, the part automatically goes into output discharge mode and the internal discharge MOSFET provides a resistive discharge path from the OUT pin to

GND for the output capacitor ( $C_{OUT}$ ). Output discharge mode can be blocked by adding an external capacitor between  $V_{OUT}$  and the OUT pin. See the Output Discharge Blocking section on page 21 for more details.

### Soft Start (SS)

The MPQ2177 has an external SS pin that ramps up  $V_{OUT}$  at a controlled slew rate to avoid overshoot during start-up. The SS pin charge current is typically 3 $\mu$ A. The soft-start time ( $t_{SS}$ ) is decided by the soft-start capacitor ( $C_{SS}$ ), and can be calculated with Equation (2):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times 0.6V}{I_{SS}(\mu A)} \quad (2)$$

Where  $C_{SS}$  is the external soft-start capacitor, and  $I_{SS}$  is the internal 3 $\mu$ A SS charge current.

$C_{SS}$  should be 1nF minimum.

The MPQ2177 offers a pre-biased start-up function. Once EN is enabled, the device starts up even if there is a pre-biased voltage on the output. Pre-biased start-up works regardless of whether output discharge mode is blocked.

### Peak and Valley Current Limit

Both the HS-FET and LS-FET have current limit protection. When  $I_L$  reaches the HS-FET's peak current limit (typical 2.5A) during the HS-FET on time, the HS-FET immediately turns off to prevent the current from rising further, and the LS-FET turns on to discharge the energy. The HS-FET does not turn again until  $I_L$  drops below the valley current limit threshold (typically 1A). This current limit scheme helps prevent current runaway during overload and short circuit events.

### Short-Circuit Protection (SCP) and Recovery

If  $V_{OUT}$  is shorted to ground and the MPQ2177 reaches its current limit, then the device enters short-circuit protection (SCP) and tries to recover with hiccup mode. The IC disables the output power stage, begins discharging the SS voltage ( $V_{SS}$ ), and restarts with a full soft start once  $V_{SS}$  is fully discharged. This hiccup process repeats until the fault is removed.

### Over-Voltage Protection (OVP)

The MPQ2177 monitors a resistor-divided feedback voltage to detect over-voltage (OV) conditions. If  $V_{FB}$  exceeds 115% of  $V_{REF}$ , the controller enters the dynamic regulation period. During this period, the LS-FET remains on until the LS-FET current reaches -1.2A; this process discharges  $V_{OUT}$  and tries to keep it within the normal range. If the OV condition still remains, the LS-FET turns on again after a 1.5 $\mu$ s delay. Once  $V_{FB}$  falls below 105% of  $V_{REF}$ , the MPQ2177 exits this regulation period. If the dynamic regulation period cannot prevent  $V_{OUT}$  from increasing and a 6.1V  $V_{IN}$  is detected, the over-voltage protection (OVP) occurs. The MPQ2177 stops switching until  $V_{IN}$  drops below 6V; once this occurs, the MPQ2177 resumes normal operation.

### Power Good (PG) Indicator

The MPQ2177 has one power good (PG) output to indicate normal operation after soft start. PG is the open drain of an internal MOSFET, for which the maximum  $R_{DS(ON)}$  must be below 400 $\Omega$ . PG can be connected to  $V_{IN}$  or an external voltage source through an external resistor (10k $\Omega$  to 100k $\Omega$ ). After  $V_{IN}$  is applied, the MOSFET turns on and PG is pulled to GND before SS is ready. After  $V_{FB}$  reaches 90% of  $V_{REF}$ , PG is pulled high by the external voltage source. When  $V_{FB}$  drops to 85% of  $V_{REF}$ , the PG voltage ( $V_{PG}$ ) is pulled to GND to indicate an output failure.

If  $V_{IN}$  and EN are not available and PG is pulled up by an external power supply, then PG will self-bias and assert. If a 100k $\Omega$  pull-up resistor is used, the voltage on the PG pin is less than 0.7V.

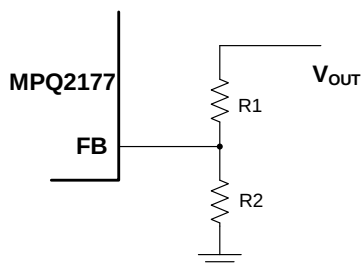
## APPLICATION INFORMATION

### Setting the Output Voltage

The external resistor divider sets  $V_{OUT}$  for the adjustable output version of the MPQ2177. Select the feedback resistor (R1) that reduces the  $V_{OUT}$  leakage current (typically between 10k $\Omega$  and 100k $\Omega$ ). R2 can then be calculated with Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (3)$$

Figure 3 shows the feedback circuit.



**Figure 3: Feedback Network**

Table 1 lists the recommended resistor values for common output voltages.

**Table 1: Resistor Values for Common Output Voltages**

| $V_{OUT}$ (V) | R1 (k $\Omega$ ) | R2 (k $\Omega$ ) |
|---------------|------------------|------------------|
| 1.0           | 30.9 (1%)        | 47 (1%)          |
| 1.2           | 100 (1%)         | 100 (1%)         |
| 1.8           | 36 (1%)          | 18 (1%)          |
| 2.5           | 51 (1%)          | 16 (1%)          |
| 3.3           | 68 (1%)          | 15 (1%)          |

### Frequency Scaling at Low Input Voltages

Under heavy-load conditions, the HS-FET voltage drops as  $t_{ON}$  increases and the duty is extended. At low input voltages and heavy-load conditions, if the minimum off time ( $t_{MIN\_OFF}$ ) is reached, then the frequency scales down. To keep  $f_{SW}$  constant, a higher  $V_{OUT}$  requires a higher  $V_{IN}$  under heavy loads. For a 1.8V  $V_{OUT}$ ,  $V_{IN}$  should be above 2.7V to keep  $f_{SW}$  above 2MHz at a 1A load. When the frequency starts to scale down, estimate  $V_{IN}$  with Equation (4):

$$V_{IN} = \frac{V_{OUT} + R_{DS(ON)_P} \times I_{OUT}}{1 - \frac{t_{MIN\_OFF}}{400 \times 10^{-9}}} \quad (4)$$

Where the maximum  $t_{MIN\_OFF}$  is 125ns.<sup>(7)</sup>

**Note:**

7) Guaranteed by design and bench characterization. Not tested in production.

### Selecting the Inductor

A 0.47 $\mu$ H to 2.2 $\mu$ H inductor is recommended for most applications. Select an inductor with a DC resistance below 25m $\Omega$  to optimize efficiency.

High-frequency, switch-mode power supplies with magnetic devices such as the MPQ2177 can have strong electromagnetic interference (EMI). Unshielded power inductor should be avoided, as they provide poor magnetic shielding. Shielded inductor, such as metal alloy or multiplayer chip power inductors, are recommended, as they effectively reduce EMI.

For most designs, the inductance ( $L_1$ ) can be estimated with Equation (5):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (5)$$

Where  $\Delta I_L$  is the inductor ripple current.

Choose an inductor ripple current that is approximately 30% of the maximum load current. The maximum inductor peak current ( $I_{L(MAX)}$ ) can be calculated with Equation (6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

### Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10 $\mu$ F capacitor is sufficient. Higher output voltages may require a 22 $\mu$ F capacitor to increase system stability.

The input capacitor (C1) requires an adequate ripple current rating because it absorbs the input switching current.

Estimate the RMS current in the input capacitor using Equation (7):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The worst case occurs at  $V_{IN} = 2 \times V_{OUT}$ , calculated with Equation (8):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

C1 can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, ceramic 0.1μF capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to prevent excessive voltage ripple at the input. The input voltage ripple ( $\Delta V_{IN}$ ) caused by the capacitance can be estimated with Equation (9):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

### Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC output voltage. Ceramic capacitors are recommended. Low-ESR capacitors are ideal because they effectively limit the output voltage ripple. Estimate the output voltage ripple ( $\Delta V_{OUT}$ ) with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (10)$$

Where  $L_1$  is the inductance, and  $R_{ESR}$  is the equivalent series resistance (ESR) of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple.

For simplification, the output voltage ripple ( $\Delta V_{OUT}$ ) can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

Ceramic capacitors with X7R or X5R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

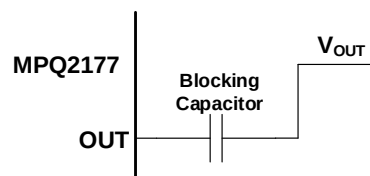
For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output voltage ripple ( $\Delta V_{OUT}$ ) can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

### Output Discharge Blocking

When the device is disabled, an internal resistive discharge path from OUT pin to GND is enabled to discharge the output capacitor (C2). The discharge path can be blocked by adding an external capacitor between  $V_{OUT}$  and the OUT pin (see Figure 4).



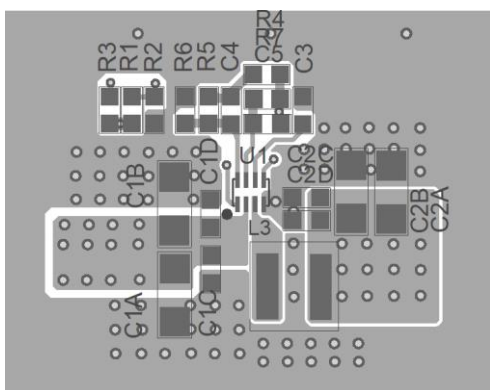
**Figure 4: Circuit with  $V_{OUT}$  Discharge Blocking Capacitor**

In order to avoid influencing the loop and load transient, the blocking capacitor should be at least 10nF. Larger-value blocking capacitors have no impact on loop performance, but are not necessary and have greater costs. A capacitor between 10nF and 100nF is recommended.

## PCB Layout Guidelines

Efficient PCB layout is critical for proper function. Poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 5 and follow the guidelines below:

1. Place the high-current paths (GND,  $V_{IN}$ , and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor (C1) as close as possible to the VIN and GND pins.
3. Place the output capacitor GND needs to close the chip's GND pins.
4. For the adjustable output version, place the external feedback resistors next to the FB pin.
5. Keep the switching node (SW) short and away from the feedback network.
6. Keep the  $V_{OUT}$  sense line as short as possible, and place it as far away from the power inductor as possible. It must not surround the inductor or be close to SW.



## TYPICAL APPLICATION CIRCUITS

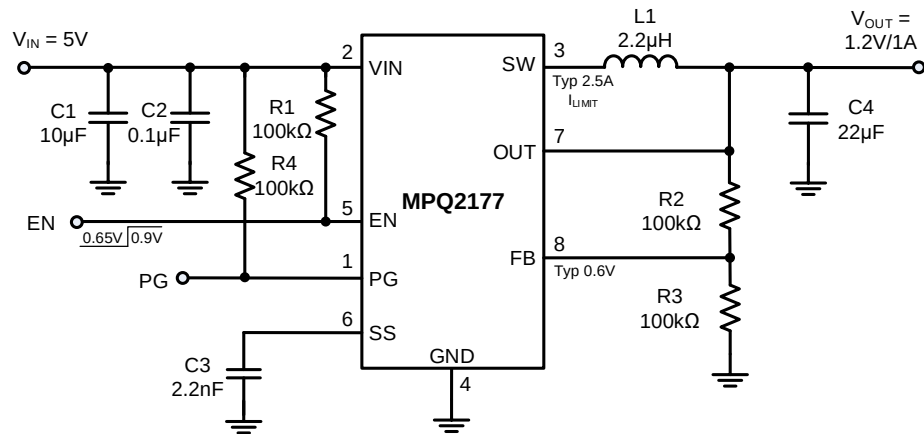


Figure 6: 1.2V Output Application Circuit for Adjustable Output Version

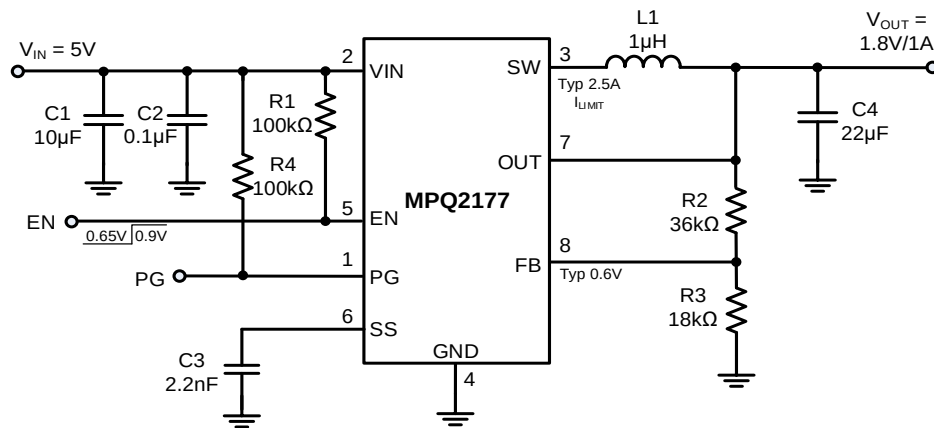


Figure 7: 1.8V Output Application Circuit for Adjustable Output Version

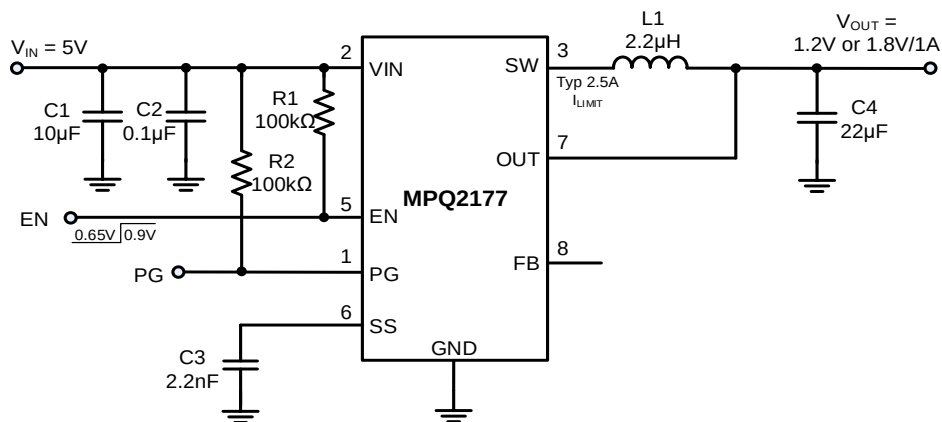
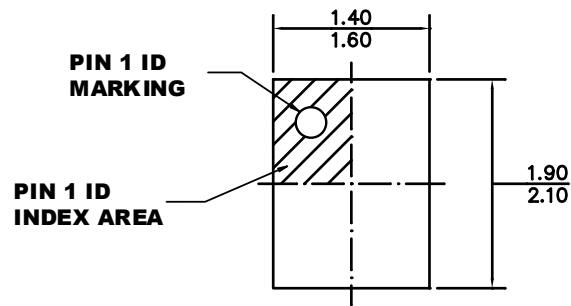


Figure 8: Application Circuit for Fixed Output Version

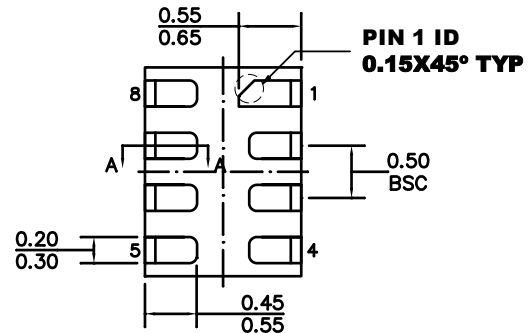
## PACKAGE INFORMATION

### QFN-8 (1.5mmx2mm)

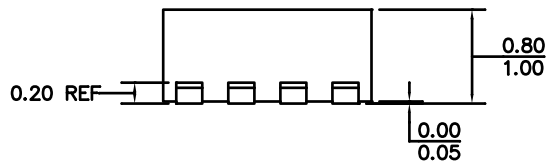
## Wettable Flank



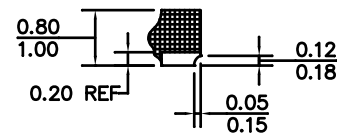
**TOP VIEW**



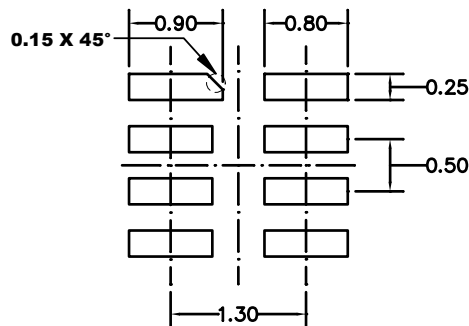
### BOTTOM VIEW



### SIDE VIEW



**SECTION A-A**



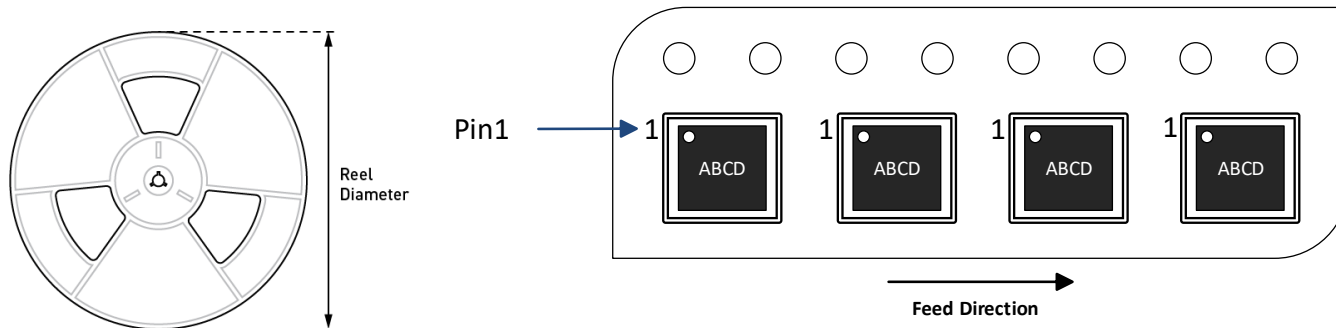
## RECOMMENDED LAND PATTERN

**NOTE:**

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.



## CARRIER INFORMATION



| Part Number           | Package Description  | Quantity /Reel | Quantity /Tube | Quantity /Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|-----------------------|----------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MPQ2177GQHE-Z         | QFN-8<br>(1.5mmx2mm) | 5000           | N/A            | N/A            | 13in          | 8mm                | 4mm                |
| MPQ2177GQHE-AEC1-Z    |                      |                |                |                |               |                    |                    |
| MPQ2177GQHE-12-AEC1-Z |                      |                |                |                |               |                    |                    |
| MPQ2177GQHE-18-AEC1-Z |                      |                |                |                |               |                    |                    |



## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 4/30/2021     | Initial Release | -             |

**NOTICE:** The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.