MPQ2977

Dual-Rail, Digital 6-Phase Controller with PMBus Interface, AEC-Q100 Qualified

DESCRIPTION

The MPQ2977 is a dual-rail, multi-phase digital voltage regulator (VR) controller for autonomous driving applications. The MPQ2977 can work with MPS's Intelli-Phase™ products to complete the multi-phase VR solution with minimal external components. The MPQ2977 is scalable up to six phases between two rails.

The on-chip, multiple-time programmable (MTP) memory stores and restores device configurations. Device configurations and fault parameters can be configured or monitored using the PMBus interface. The MPQ2977 can monitor and report the output current (I_{OUT}) through the Intelli-Phase™ current-sense (CS) output.

The MPQ2977 is based on unique, digital, multi-phase nonlinear control to provide fast transient response to a load step with minimal output capacitors. With only one power loop control method for both the steady state and load transient response, power loop compensation is simple to configure.

The MPQ2977 is available in a TQFN-40 (6mmx6mm) package.

FEATURES

- Dual-Rail Digital PWM Controller with Up to 6-Phase Operation
- PMBus Compliant for Configurations and Monitoring
- Built-In Multiple-Time Programmable (MTP) Memory to Store Custom Configurations
- Automatic Loop Compensation
- Fewer External Components than Conventional Analog Controller
- Automatic Phase-Shedding (APS) with and without Discontinuous Conduction Mode (DCM) to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing
- Input Voltage (V_{IN}) and Output Voltage (V_{OUT}) Monitoring
- Output Current (I_{OUT}) Monitoring
- Regulator Temperature Monitoring
- Under-Voltage Lockout (UVLO), Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), Over-Current Protection (OCP), and Over-Temperature Protection (OTP)
- Cyclic Redundancy Check (CRC) for MTP Transformation
- Separate EN for Each Rail
- Digital, Configurable Load Line
- Available in a TQFN-40 (6mmx6mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Autonomous Driving System-on-Chips (SoCs)
- Infotainment Systems

TYPICAL APPLICATION

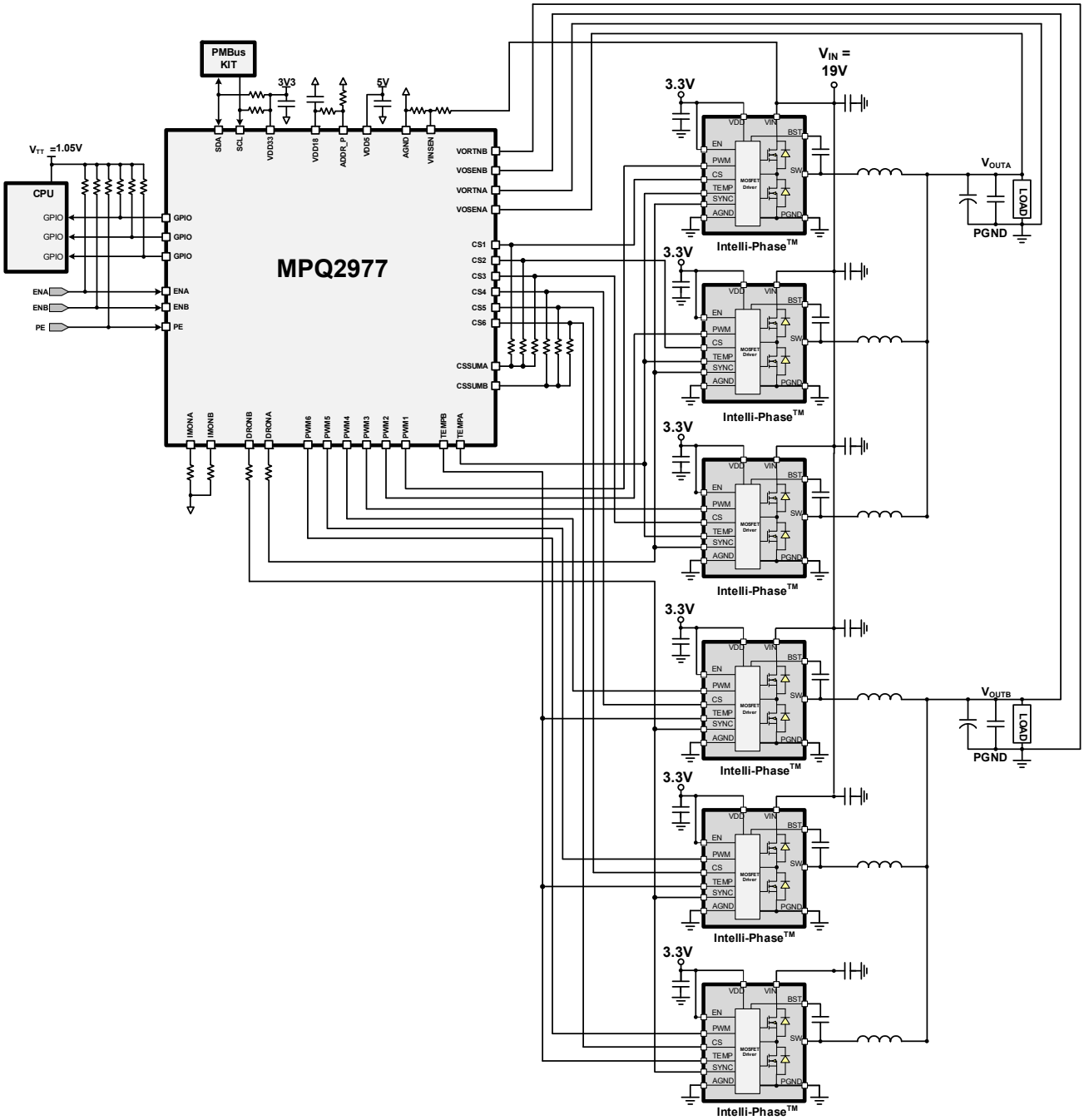


Figure 1: 3 + 3 Solution

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ2977GQKTE-xxxx-AEC1**	TQFN-40 (6mmx6mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MPQ2977GQKTE-xxxx-AEC1-Z).

** "-xxxx" is the configuration code identifier for the register settings stored in the internal, non-volatile memory (NVM). Each "x" can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number.

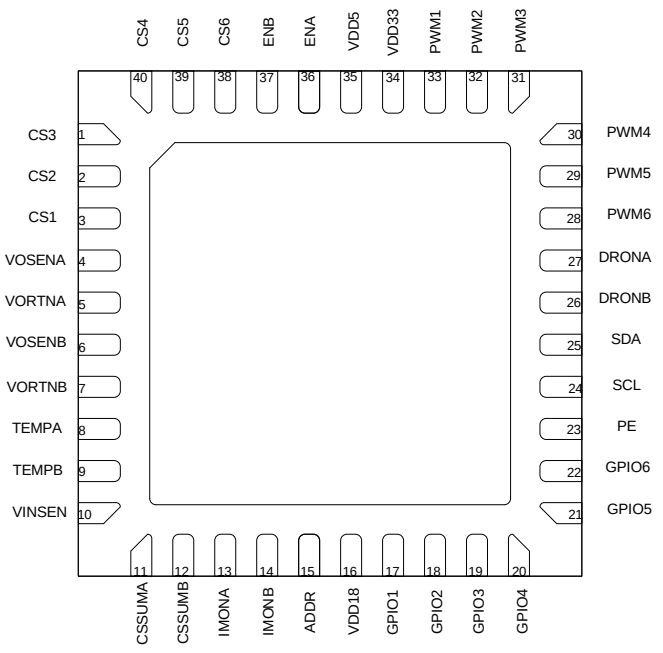
TOP MARKING

MPSYYWW
MP2977
LLLLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP2977: Part number
LLLLLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW



TQFN-40 (6mmx6mm)

PIN FUNCTIONS

Pin #	Name	I/O	Description
1	CS3	A [I]	**Phase 3 current-sense input.** Float the CS pin of any unused phases.
2	CS2	A [I]	**Phase 2 current-sense input.** Float the CS pin of any unused phases.
3	CS1	A [I]	**Phase 1 current-sense input.** Float the CS pin of any unused phases.
4	VOSENA	A [I]	**Positive remote voltage sense input for rail A.** VOSENA is connected directly to the VR's output voltage at the load. VOSENA should be routed differentially with VORTNA.
5	VORTNA	A [I]	**Remote voltage sense return input for rail A.** VORTNA is connected directly to ground at the load. VORTNA should be routed differentially with VOSENA.
6	VOSENB	A [I]	**Positive remote voltage sense input for rail B.** VOSENB is connected directly to the VR's output voltage at the load. VOSENB should be routed differentially with VORTNB.
7	VORTNB	A [I]	**Remote voltage sense return input for rail B.** VORTNB is connected directly to ground at the load. VORTNB should be routed differentially with VOSENB.
8	TEMPA	A [I]	**Analog signal from the VR's rail A to the VID controller.** The TEMPA pin indicates rail A's power stage temperature. Connect all Intelli-Phase's™ VTEMP pins for rail A together to produce the maximum junction temperature, and then connect these pins to the TEMPA pin.
9	TEMPB	A [I]	**Analog signal from the VR's rail B to the VID controller.** The TEMPB pin indicates rail B's power stage temperature. Connect all Intelli-Phase's™ VTEMP pins for rail B together to produce the maximum junction temperature, and then connect these pins to the TEMPB pin.
10	VINSEN	A [I]	**Input voltage sense.** Connect the VINSEN pin to VIN through a 1/16 divider network.
11	CSSUMA	A [I]	**Total phase current monitor for the VR AVP's rail A.** Connect the active phases' CS signals for rail A to the CSSUMA pin through the current-sense resistors.
12	CSSUMB	A [I]	**Total phase current monitor for the VR AVP's rail B.** Connect the active phases' CS signals for rail B to the CSSUMB pin through the current-sense resistors.
13	IMONA	A [I/O]	**Analog total load current signal for the VR's rail A.** The IMONA pin sources a current proportional to the sensed total load current from the CSSUMA pin. Connect an external resistor from IMONA to AGND to configure the gain.
14	IMONB	A [I/O]	**Analog total load current signal for the VR's rail B.** The IMONB pin sources a current proportional to the sensed total load current from the CSSUMB pin. Connect an external resistor from IMONB to AGND to configure the gain.
15	ADDR	A [I]	**PMBus address setting.**
16	VDD18	A [I/O]	**1.8V LDO output for internal digital power supply.** Connect a 1µF bypass capacitor from the VDD18 pin to AGND.

PIN FUNCTIONS *(continued)*

Pin #	Name	I/O	Description
17	GPIO1	D [I/O]	**General-purpose input/output pin.** The GPIO pins can be configured for the following functions: FAULT: When the GPIOx pin functions as FAULT, it acts as an open-drain output that signals when a fault occurs. This function can be separate for both rails. VRRDY: When the GPIOx pin functions as VRRDY, it acts as an open-drain output that signals when the output voltage is outside its proper operating range. This function can be separate for both rails. ALERT: When the GPIOx pin functions as ALERT, it acts as an open-drain output that asserts when a VID change is complete. This function can be separate for both rails. VR_HOT: When the GPIOx pin functions as VR_HOT, it acts as an open-drain output that signals when the monitor temperature exceeds the configured VR_HOT temperature threshold. This function can be separate for both rails.
18	GPIO2		
19	GPIO3		
20	GPIO4		
21	GPIO5		
22	GPIO6		
23	PE	D [I]	**Program enable.** The PE pin is the program enable input for system configurations through the PMBus when EN is off. If this pin is not used, connect it to AGND with a 0Ω resistor.
24	SCL	D [I]	**Source synchronous clock from the PMBus controller.**
25	SDA	D [I/O]	**Data signal between the PMBus controller and VR controller.**
26	DRONB	D [O]	**Low-power mode enable for rail B.** The DRONB pin is a digital output that indicates to the Intelli-Phase™ whether to enable or enter low-power mode (LPM) for rail B.
27	DRONA	D [O]	**Low-power mode enable for rail A.** The DRONA pin is a digital output that indicates to the Intelli-Phase™ whether to enable or enter LPM for rail A.
28	PWM6	D [O]	**Tri-state logic-level PWM outputs.** Each output is connected to the input of the Intelli-Phase's™ PWM pin. The logic levels are 0V for low logic and 3.3V for high logic. The output is set to tri-state to shut down both the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) of the Intelli-Phase™.
29	PWM5	D [O]	
30	PWM4	D [O]	
31	PWM3	D [O]	
32	PWM2	D [O]	
33	PWM1	D [O]	
34	VDD33	A [I/O]	**3.3V LDO output for internal power supply.** Connect a 4.7µF bypass capacitor from the VDD33 pin to ground.
35	VDD5	A [I]	**5V power supply input.** Connect a 4.7µF bypass capacitor from the VDD5 pin to ground.
36	ENA	D [I]	**Enable control for rail A.**
37	ENB	D [I]	**Enable control for rail B.**
38	CS6	A [I]	**Phase 6 current-sense input.** Float the CS pin of any unused phases.
39	CS5	A [I]	**Phase 5 current-sense input.** Float the CS pin of any unused phases.
40	CS4	A [I]	**Phase 4 current-sense input.** Float the CS pin of any unused phases.
PAD	AGND	A [I/O]	**Analog ground.**

ABSOLUTE MAXIMUM RATINGS (1)

VDD5……-0.3V to +6.5V
VDD33……..-0.3V to +4V
VDD18……..-0.3V to +2.2V
AGND……...-0.3V to +0.3V
VORTNA, VORTNB……...-0.3V to +0.3V
CS1 to CS6, VOSENA, VOSENB, ENA, ENB, TEMPA, TEMPB……..-0.3V to +6.5V
PWM1 to PWM6, SCL, SDA, PE, DRONA, DRONB, GPIO1 to GPIO6……-0.3V to +4V
All other pins……-0.3V to +2.2V
Junction temperature……150°C
Lead temperature……..260°C
Storage temperature……... -65°C to +150°C

ESD Ratings (2)

Human body model (HBM)…….Class 2
Charged device model (CDM)……..Class C2b

Recommended Operating Conditions (3)

VDD5……4.5V to 5.5V
Operating junction temp (T_J)…..-40°C to +125°C

Thermal Resistance (4) θ_{JB} θ_{JC_TOP}

TQFN-40 (6mmx6mm)……9…...14….°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Followed ANSI/ESDA/JEDEC JS-001 for HBM and ANSI/ESDA/JEDEC JS-002 for CDM.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 6-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD5 = 5V, current going into pin is positive, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Remote-Sense Amplifier						
Bandwidth (5)	$GBW_{(RSA)}$			20		MHz
VORTN current	I_{VORTN}	EN = 3.3V, V_{VOSEN} = 3V, V_{VORTN} = 0V		-70	-400	µA
VOSEN current	I_{VOSEN}	EN = 3.3V, V_{VORTN} = 0V, V_{VOSEN} = 3V		70	400	µA
Oscillator						
Frequency	f_{OSC}		-10%	1.5625	+10%	MHz
System Interface Control Inputs						
EN/PE						
Input low voltage	$V_{(IL(EN)}$				0.4	V
Input high voltage	$V_{(IH(EN)}$		1.1			V
Enable high leakage	$I_{IH(EN)}$	EN = 3.3V			10	µA
Input low voltage	$V_{IL(PE)}$				0.8	V
Input high voltage	$V_{IH(PE)}$		2.4			V
PE high leakage	$I_{IH(PE)}$	PE = 3.3V			2	µA
Enable delay	t_{EN_DELAY}	EN high to PWM ready		120	200	µs
IMONA/IMONB Outputs						
Current gain accuracy	I_{MON}/I_{CS_SUM}	Measured from I_{CS_SUM} to I_{MON}, I_{CS_SUM} = 1.2mA		1:8		A/A
Digital I_{OUT} error			-3		+3	%
Comparator (Rails A/B, Protection)						
UV threshold	$\Delta V_{VOSEN-VORTN}$ (UV2)	Relative to reference DAC voltage, V_{DIFF} gain set to 1, UV2 set to -300mV to V_{REF}	-340	-300	-260	mV
	$\Delta V_{VOSEN-VORTN}$ (UV1)	UVP1 DAC voltage, V_{DIFF} gain set to 1, UV1 set to 0.3V	0.25	0.3	0.35	V
OV threshold	$\Delta V_{VOSEN-VORTN}$ (OV2)	Relative to reference DAC voltage, V_{DIFF} gain set to 1, OV2 set to 200mV to V_{REF}	160	200	240	mV
	$\Delta V_{VOSEN-VORTN}$ (OV1)	OVP1 DAC voltage, V_{DIFF} gain set to 1, OV1 set to 1.6V	1.54	1.60	1.66	V
Reverse-voltage detection threshold (5)	$\Delta V_{VOSEN-VORTN}$ (RV)	Relative to VORTN	120	160	200	mV

ELECTRICAL CHARACTERISTICS *(continued)*

VDD5 = 5V, current going into pin is positive, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWM1~6 Outputs						
Output low voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = 400µA		10	200	mV
Output high voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = -400µA	2.8			V
Rising and falling time (5)		C = 10pF		10		ns
PWM tri-state leakage		PWM = 1.5V, EN = 0V	-1		+1	µA
Minimum on time (5)	t_{ON_MIN}	Configurable via register		30		ns
Minimum off time (5)	t_{OFF_MIN}	Configurable via register		30		ns
Minimum Hi-Z time (5)	t_{HiZ_MIN}	Configurable via register		100		ns
DRONA/DRONB Outputs						
Output low voltage	$V_{OL(DRONA/B)}$	$I_{DRONA/B(SINK)}$ = 400µA		10	200	mV
Output high voltage	$V_{OH(DRONA/B)}$	$I_{DRONA/B(SOURCE)}$ = -400µA	2.8			V
Rising and falling time (5)		C = 10pF		10		ns
DRONA/B tri-state leakage		DRONA/B = 1.5V, EN = 0V	-1		+1	µA
GPIO1~6						
Output low voltage	$V_{OL(GPIO)}$	$I_{GPIO(SINK)}$ = 400µA		10	200	mV
Rising and falling time (5)		C = 10pF		10		ns
Open-drain output leakage		V_{GPIO} = 3.3V	-1		+1	µA
1.8V Regulator						
1.8V regulator output voltage	V_{DD18}	I_{VDD18} = 0mA	1.63	1.8	1.97	V
3.3V Regulator						
3.3V regulator output voltage	V_{DD33}	I_{VDD33} = 0mA	2.9	3.3	3.6	V
VDD5 Supply						
Supply current	I_{VDD5}	ENA or ENB = high		15	20	mA
		ENA = ENB = PE = low		150	250	µA
Under-voltage lockout (UVLO) threshold voltage	$VDD5_{UVLO}$	VDD5 rising			4.4	V
UVLO hysteresis (5)	$VDD5_{UVLO\_HYSTERESIS}$	VDD5 falling		200		mV
CSSUM Voltage						
CSSUM voltage	V_{CSSUM}		1.2	1.24	1.28	V
Temp Fault Comparator						
TEMP fault threshold	V_{TEMP_FLT}		2	2.2	2.4	V
Analog-to-Digital Converter (ADC)						
Voltage range				0 to 1.55		V
ADC resolution (5)				10		Bits
ADC reference voltage		T_J = 25°C	1.595	1.6	1.605	V
ADC reference voltage		T_J = 125°C	1.55	1.6	1.65	V
DNL (5)				1		LSB
Sample rate (5)				780		kHz

ELECTRICAL CHARACTERISTICS *(continued)*

VDD5 = 5V, current going into pin is positive, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VID Digital-to-Converter (DAC) (Reference Voltage for Rails A/B)						
Range	FS_{DAC}			0 to 1.6		V
Resolution/LSB (5)	Δ_{DAC}			2.5		mV
Output voltage slew rate (5)				100		mV/µs
V_{OUT} DAC (V_{OUT} Calibration for Rails A/B)						
Range	FS_{DAC_VO}			0 to 240		mV
Resolution/LSB (5)	Δ_{DAC_VO}			0.9375		mV
Over-Voltage Protection (OVP1) DAC (Fixed OVP for Rails A/B)						
Range	FS_{DAC_OVP1}	Adjustable via the PMBus		0 to 2.55		V
Resolution/LSB (5)	Δ_{DAC_OVP1}			10		mV
OVP2 DAC (Tracking OVP for Rails A/B)						
Range	FS_{DAC_OVP2}	Adjustable via the PMBus		50 to 400		mV
Resolution/LSB (5)	Δ_{DAC_OVP2}			50		mV
Under-Voltage Protection (UVP1) DAC (Fixed UVP for Rails A/B)						
Range	FS_{DAC_UVP1}	Adjustable via the PMBus		0 to 2.55		V
Resolution/LSB (5)	Δ_{DAC_UVP1}			10		mV
UVP2 DAC (Tracking UVP for Rails A/B)						
Range	FS_{DAC_UVP2}	Adjustable via the PMBus		-400 to -50		mV
Resolution/LSB (5)	Δ_{DAC_UVP2}			50		mV
Phase Over-Current Protection (OCP) DAC (Per-Phase OCP for Rails A/B)						
Range	FS_{DAC_OCP}	Adjustable via the PMBus		1.24 to 2.56		V
Resolution/LSB (5)	Δ_{DAC_OCP}			5.2		mV
Phase Under-Current Protection (UCP) DAC (Per-Phase UCP for Rails A/B)						
Range	FS_{DAC_UCP}	Adjustable via the PMBus		0 to 1.24		V
Resolution/LSB (5)	Δ_{DAC_UCP}			4.8		mV

ELECTRICAL CHARACTERISTICS *(continued)*

VDD5 = 5V, current going into pin is positive, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PMBus DC Characteristics (SDA, SCL)						
Input high voltage (3.3V)	$V_{IH(PMBUS\_3.3V)}$	SCL, SDA	2.1			V
Input low voltage (3.3V)	$V_{IL(PMBUS\_3.3V)}$	SCL, SDA			0.8	V
Input leakage current		SCL = SDA = 3.6V			10	µA
Output low voltage	$V_{OL(PMBUS)}$	SDA sinks 2mA			400	mV
Maximum voltage (5)	V_{MAX}	Transient voltage including ringing	-0.3	3.3	+3.6	V
Pin capacitance (5)	C_{PIN}				10	pF
PMBus Timing Characteristics (5)						
Operating frequency range			10		1000	kHz
Bus free time		Between stop and start command	0.5			µs
Holding time			0.26			µs
Repeated start command set-up time			0.26			µs
Stop condition set-up time			0.26			µs
Data hold time			0			ns
Data set-up time			50			ns
Clock low timeout			25		35	ms
Clock low period			0.5			µs
Clock high period			0.26		50	µs
Clock/data falling time					120	ns
Clock/data rising time					120	ns

Notes:

5) Guaranteed by design or characterization data, not tested in production.

FUNCTIONAL BLOCK DIAGRAM

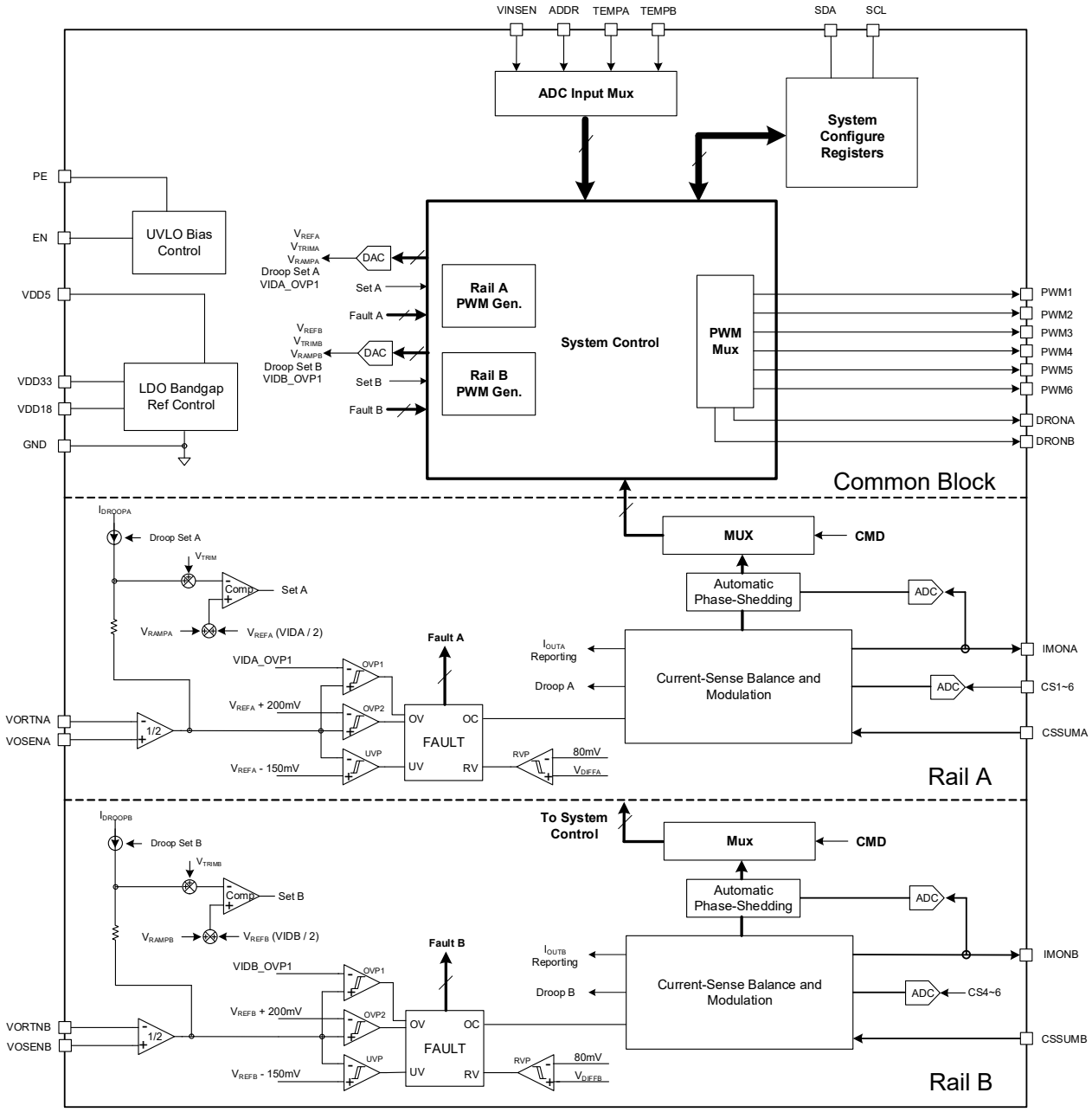


Figure 2: System Functional Block Diagram

OPERATION

The MPQ2977 is dual-rail, multi-phase digital voltage regulator (VR) controller for autonomous driving applications. To improve VR efficiency, the device can adaptively shed or add phases according to the load current.

The MPQ2977 contains blocks of precision digital-to-analog converters (DACs) and analog-to-digital converters (ADCs), differential remote voltage-sense amplifier, current-sense amplifier, internal loop compensation, temperature monitoring, PMBus interface, and multiple-time programmable (MTP) memory for custom configurations.

Fault protection features include input voltage (V_{IN}) under-voltage lockout (UVLO), over-current protection (OCP), under-voltage protection (UVP), over-temperature protection (OTP), and reverse-voltage protection (RVP).

System Rail and Phase Configuration

The MPQ2977 supports multiple rails and phases for different applications or platforms. The device can be configured for up to 6 phases on rail A and up to 3 phases on rail B via the PMBus register MFR_PHASE_CFG (CAh), bits[3:0] (see Table 1).

Table 1: Phase Configuration and Active PWM Pins

MFR_PHASE_CFG, Bits[3:0]	Active PWM Pins	
	Rail A	Rail B
0000	1, 2, 3, 4, 5, 6	-
0001	1, 2, 3, 4, 5	-
0010	1, 2, 3, 4, 5	6
0011	1, 2, 3, 4	-
0100	1, 2, 3, 4	6
0101	1, 2, 3, 4	5, 6
0110	1, 2, 3	-
0111	1, 2, 3	6
1000	1, 2, 3	5, 6
1001	1, 2, 3	4, 5, 6
1010	1, 2	-
1011	1, 2	6
1100	1, 2	5, 6
1101	1	-
1110	1	6
Others	Not supported	

The MPQ2977 provides design flexibility to enable or disable reserved phases without a soldering process. For example, if the design has been previously set as a 3 + 2 solution, CAh can be updated to allow the MPQ2977 to directly support 3 + 1, 3 + 0, 2 + 2, 2 + 1, 2 + 0, 1 + 1, or 1 + 0 solutions without any additional configurations on the Intelli-Phase™ side.

The used rail can be disabled via MFR_EN_COMMAND (20h), bits[1:0] The unused PWM stays in tri-state, and the active phase interleaves automatically. Only the PWM on the enabled rails are active.

PMBus Address

To support multiple VR devices using the same PMBus interface, there is a PMBus address for every device. The PMBus address is a 7-bit code. The 3 MSB are set up by the register, and the lower 4-bit address can either be set up by the register or the voltage on the ADDR pin. The PMBus address can be set via the ADDR pin or MFR_PMBUS_ADDR (F8h), bits[6:0] (see Figure 3).

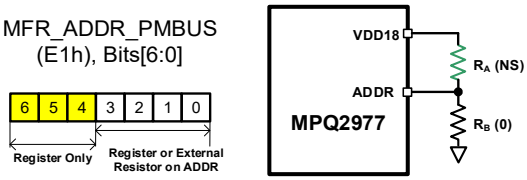


Figure 3: PMBus Address Setting

Connect a resistor divider between the VDD18 pin and ground to set the voltage for the corresponding PMBus address on the ADDR pin. Table 2 lists the possible PMBus addresses that can be set by the external voltage when the default F8h, bits[6:4] = 010b.

Table 2: PMBus Address Setting by the ADDR Voltage

PMBus Address	Recommended Voltage Setting (V)	Min Voltage Setting (V)	Max Voltage Setting (V)
20h	0	0	0.15
21h	0.3	0.25	0.35
22h	0.5	0.45	0.55
23h	0.7	0.65	0.75
24h	0.9	0.85	0.95
25h	1.1	1.05	1.15
26h	1.3	1.25	1.35
27h	1.6	1.45	1.6

The default settings on the external resistors (R_A and R_B) are R_A = NS and R_B = 0Ω, which makes the default PMBus address 20h.

Start-Up Sequence

The MPQ2977 is supplied with a 5V voltage for the analog circuit. The system is reset by the internal power-on reset (POR) signal. After the system exits POR, the data in the MTP is loaded to the registers to configure the VR's operation. The initialization process takes about 0.2ms, plus the delay time (t_A) (see Figure 4). Then the device executes the soft-start process to charge the output capacitor until the reference reaches the target boot voltage (V_{BOOT}). t_B can be calculated with (V_{BOOT} / slew rate).

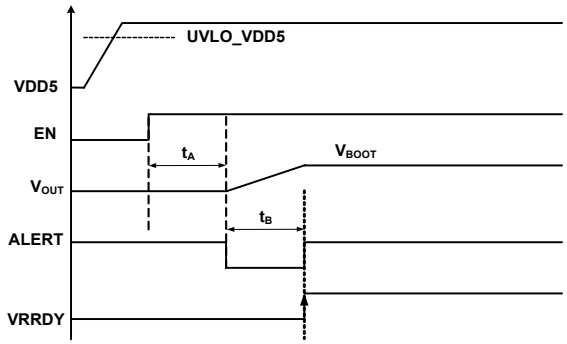


Figure 4: Start Up Sequence

The MPQ2977's VRRDY signal asserts when the VR reaches V_{BOOT}.

The MPQ2977 provides an additional, configurable EN delay by setting the MFR_INITIAL_DLY register. t_A can be set to be longer than 0.2ms, such that t_A = (0.2ms + MFR_INITIAL_DLY). See the MFR_INITIAL_DLY section on page 66 for more details.

When V_{BOOT} is set to 0, the PWM stays in tri-state until a valid SETVID command is received.

Steady State and Switching Frequency (f_{SW})

The MPQ2977 applies digital, non-linear control to provide a fast transient response and easy loop compensation. The duty cycle of each active phase's PWM updates in real time according to the V_{IN} and V_{REF} values under the set switching frequency (f_{SW}). The active phases automatically interleave during steady state. In steady state, f_{SW} is set via MFR_SW_PRD_SET (FCh), bits[15:8].

The MPQ2977 adaptively changes the f_{SW} of individual phases during load transient response to achieve fast transient performance with a minimum BOM cost.

Power State Change

The VR can operate in different power states (PS0, PS1, and PS2) to optimize efficiency under various load conditions. These states are entered by configuring the power state register via the PMBus. The VR uses the power state commands issued by the processor to optimize power loss and flatten the efficiency curve across the entire operating current range.

In PS0 mode, all phases run in continuous conduction mode (CCM). In PS1 mode, one phase runs in CCM, while all other phases are in tri-state. In PS2 mode, one phase runs in diode emulation mode, and f_{SW} drops automatically to reduce power loss under light-load conditions. Table 3 shows how the phases act at different power states.

Table 3: Power State and Phase Activities

Power State	Active Phase	CCM/DCM
PS0	Full-phase PWM	CCM
PS1	1-phase PWM	CCM
PS2	1-phase PWM	DCM

During the dynamic VID (DVID) transition, the MPQ2977 runs in full-phase PWM mode.

Reference

The MPQ2977 supports both 2.5mV VID steps and 5mV VID steps, with only one DAC to generate V_{REF}. There is a control bit (VDIFF_GAIN) in the E4h register that selects the VID step. If this control bit is set to 0, the DAC output (V_{REF}) can be calculated with Equation (1):

$$V_{REF} = VID \times 2.5mV \quad (1)$$

When the control bit is set 1, V_{REF} can be estimated with Equation (2):

$$V_{REF} = VID \times 5mV \quad (2)$$

Output Voltage (V_{OUT}) Sense

The output voltage (V_{OUT}) for each rail is sensed remotely with a half-gain differential amplifier. The configurable gain can be configured via the

register settings. The sensed output voltages are used for closed-loop compensation, OVP, UVP, and PMBus monitoring. A package sense is recommended to enclose the board parasitic within the VR's feedback loop (see Figure 5). This reduces noise and optimizes performance.

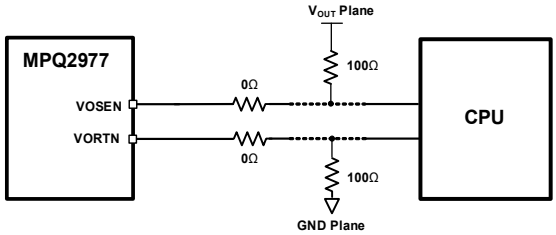


Figure 5: Output Remote Sense

Two 0Ω resistors are placed close to the MPQ2977. To avoid errant operation or board damage if the CPU is absent, connect two 100Ω catch-up resistors to the V_{OUT} and PGND planes to obtain the output feedback even when the CPU is absent.

Input Voltage (V_{IN}) Sense

The power supply input voltage (V_{IN}) is sampled at the VINSEN pin. This voltage is used for feed-forward control, V_{IN} UVLO, V_{IN} OVP, fault protections, and PMBus monitoring. Connect two resistors to the input, and use a 1µF bypass capacitor to obtain a 1/16 divider for VINSEN (see Figure 7). The default value for R_{VIN_1} is 15kΩ, and the default value for R_{VIN_2} is 1kΩ.

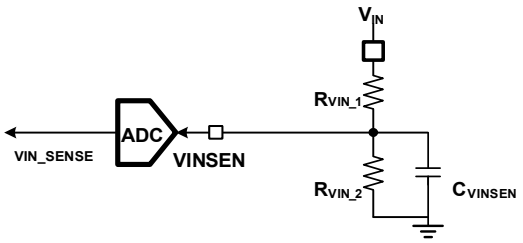


Figure 7: V_{IN} Sense Network

Current Sense

The MPQ2977 works with MPS's Intelli-Phase™ to sense the per-phase inductor current and total current (see Figure 6). The cycle-by-cycle current information is used for phase current balancing, OCP, and load-line setting.

The current-sense resistor (R_{CS}) is connected between the CS and CSSUM pins. CSSUM has a constant voltage (1.23V) that can sink small currents to provide voltage shifts that meet the CS pin's operating voltage range.

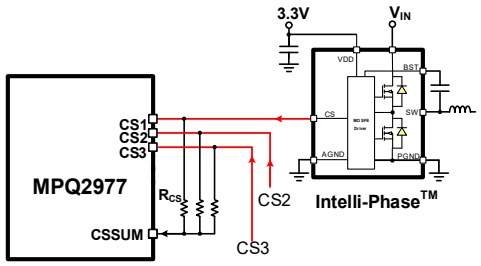


Figure 8: Phase Current Sense with 3-Phase Configuration

Different Intelli-Phase™ products have different operating voltage ranges for CS: V_{CS_MIN}, and V_{CS_MAX}. Refer to each Intelli-Phase™'s datasheet to determine the minimum and maximum operating voltage range.

Calculate R_{CS} with Equation (3):

$$V_{CS\ MIN} < I_L \times K_{CS} \times R_{CS} + 1.23V < V_{CS\ MAX} \quad (3)$$

By pairing the MPQ2977 with an Intelli-Phase™, an accurate current sense can be achieved across a wide temperature and load range without temperature compensation or impedance matching.

IMON and I_{DROOP}

The current flowing out from the IMON pin (I_{SUM}) is 1/8 of the filtered CSSUM. A voltage proportional to the output current can be generated by placing a resistor between the IMON pin and the ground. The IMON voltage is sampled and converted by the ADC, and then it is stored in the output current (I_{OUT}) register, which is scaled such that I_{CCMAX} is equal to the full ADC range (FFh). Then the IMON voltage reaches its peak value (V_{IMON_MAX}) when I_{OUT} reaches I_{CCMAX}.

The IMON voltage can be estimated with Equation (4):

$$V_{IMON} = \frac{I_{OUT} \times K_{CS} \times R_{IMON}}{8} \quad (4)$$

Where K_{CS} is the Intelli-Phase™ current-sense gain, I_{OUT} is the output current, R_{IMON} is the IMON resistor, and V_{IMON_MAX} = 1.6 x 8 / 11V.

When I_{OUT}= I_{CCMAX}, and V_{IMON} = V_{IMON_MAX}, R_{IMON} can be calculated with Equation (5):

$$R_{IMON} = \frac{8 \times V_{IMON\_MAX}}{I_{CCMAX} \times K_{CS}} \quad (5)$$

Figure 9 shows the MPQ2977 IMON sense and I_{DROOP} block diagram.

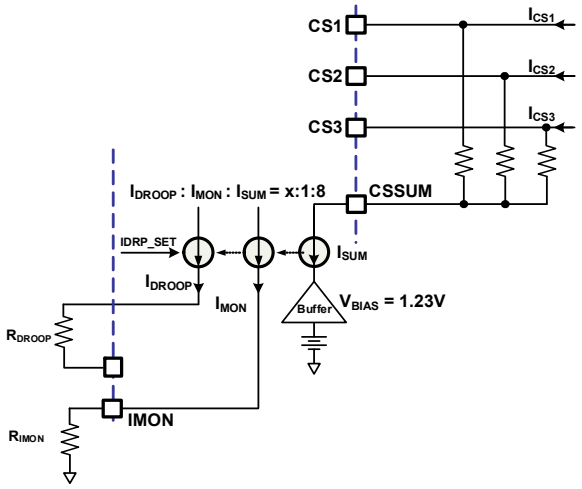


Figure 9: Current Sense I_{MON} and I_{DROOP}

Static Load Line Setting

The MPQ2977 uses an internal droop resistor to set the static load line. The droop current (default 1/8 of I_{SUM}) flowing through the droop resistor (R_{DROOP}) generates the droop voltage for the load line. Given the application's target R_{LL} for load line regulation, R_{DROOP} can be calculated with Equation (6).

$$R_{DROOP} = \frac{R_{LL} \times K_{DIFF}}{K_{CS} \times K_{DROOP}} \quad (6)$$

Where K_{DIFF} is the remote-sense gain of the voltage feedback, and K_{CS} is the Intelli-Phase™ current-sense gain. For example, the MPQ86940 K_{CS} value is 5μA/A. K_{DROOP} is the gain of the droop current mirror, which is 1/8 by default.

Digital, Configurable Load Line

In addition to the load line setting from the internal droop resistance, the MPQ2977 also provides a digital, configurable load line trim via IDRP_SET (A3h, bits[4:3], and A3h, bits[7:6]). Table 4 shows the MPQ2977's droop current mirror gain.

Table 4: Digital Load Line Trim

IDRP_SET, Bits[1:0]	I_{DROOP} Gain
00b	1/16 x I_{SUM}
01b (Default)	1/8 x I_{SUM}
10b	1/4 x I_{SUM}
11b	1/2 x I_{SUM}

The load line can be changed via the PMBus and stored in the MTP. With a digital load line, users can change the droop value without changing the internal droop resistance. The default value of IDRP_SET is 01b, which corresponds to a 1/8 gain for I_{SUM}.

I_{OUT} Report

To avoid exceeding the thermal design point and maximum current capability of the system, the MPQ2977 reports the I_{OUT} to the processor via the PMBus (see Figure 10). The PMBus register READ_IMON is used for total current monitoring and protection. If the automatic phase-shedding (APS) function is enabled via the PMBus, the total current report determines whether to enter or exit the phase-shedding mode. This maximizes the overall efficiency across the operating current range. MFR_IMON_GAIN (1Ch) configures the PMBus's I_{OUT} report gain to ensure that the MPQ2977 tracks the load current.

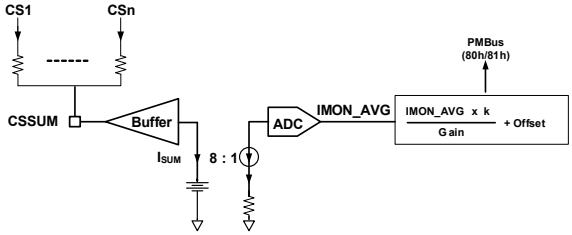


Figure 10: Total Current Sense and Report

Temperature Sense

The MPQ2977 measures the external temperature by connecting all the Intelli-Phase™ VTEMP pins of each rail together (see Figure 11).

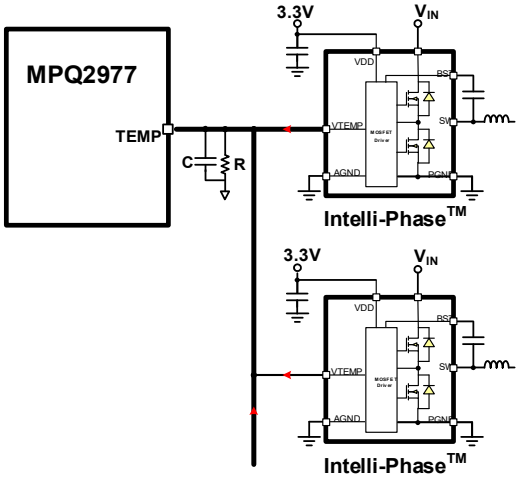


Figure 11: External Temperature Sense

The voltage of the TEMP pin is the highest voltage among the Intelli-Phase™ devices, which indicates the highest temperature of the VR's power system. The sensed temperature is used for over-temperature protection (OTP). To discharge TEMP, connect a 20kΩ resistor in parallel with a 10nF capacitor from TEMP to GND.

V_{TEMP} of the Intelli-Phase™ is a voltage output proportional to the junction temperature (T_J). T_J can be calculated with Equation (7):

$$T_J = \frac{V_{TEMP} - 600mV}{8mV/°C} \quad (7)$$

For example, if the VTEMP voltage is 800mV, then the junction temperature of the Intelli-Phase™ is 25°C.

Dynamic Voltage Identification (DVID)

The dynamic VID slew rate is set via VID_STEP (F1h, bits[7:6], and F2h, bits[7:6]), which is equal to the VID increment or decrement per step. The RATE_TIME (F1h, bits[5:0], and F2h, bits[5:0]) command defines the time duration during which VID changes once.

The fast slew rate can be estimated with Equation (8):

$$\text{Slew Rate} = \frac{(VID\_STEP + 1) \times VID}{RATE\_TIME \times 100ns} \quad (8)$$

As V_{OUT} ramps up, the inductor current rises to charge the output capacitors. This current introduces a large positive droop voltage due to the load line. V_{OUT} may drop below the target voltage, which may cause V_{OUT} to exceed the minimum regulation tolerance budget (TOB).

The MPQ2977 can be configured to ramp up with additional VID steps via F1h, bits[10:8] and F2h, bits[10:8]. VID ramps to the target to make V_{OUT} rise to the regulation TOB more quickly. VID eventually falls back to the target VID at the end of DVID. See the MFR_TRANS_FAST_R1 (F1h) section on Page 65 and the MFR_TRANS_FAST_R2 (F2h) section on Page 66 for more details.

When V_{OUT} is ramping down, the inductor current drops to discharge the output capacitors. The output capacitors are discharged until ramping ends, which may lead to V_{OUT} undershoot. There is a time during which the inductor current must balance the load current to avoid output voltage (V_{OUT}) undershoot.

The MPQ2977 applies a low-pass filter for the VID_DAC to smooth V_{REF} when V_{OUT} is ramping down.

Figure 12 shows V_{OUT} when a DVID upward command is received after the previous downward DVID is complete.

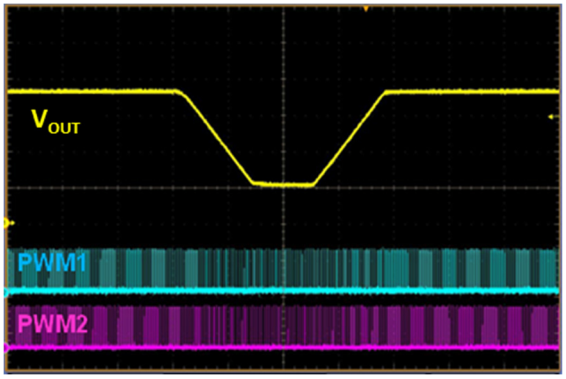


Figure 12: DVID Down and Up

Automatic Phase-Shedding (APS)

The MPQ2977 provides automatic phase-shedding (APS) to improve efficiency, according to the comparison between the total current report and the configurable threshold.

There are 3 types of registers that configure the APS function:

1. MFR_1PHL (B1h, bits[8:4], and B2h, bits[8:4]) sets the phase-shedding level, which is the current level to enter 1-phase CCM from a higher phase count. The thresholds for the higher phase counts are calculated by MFR_1PHL multiplied by the phase number. The threshold to enter 1-phase DCM is fixed to 5A.
2. MFR_PHASE_HYS (B1h, bits[3:0], and B2h, bits[3:0]) sets the hysteresis current value during phase-adding.
3. PHS_DROP_DELAYTIME (30h, bits[2:0], and 30h, bits[10:8]) sets the delay time for phase-shedding after the system's total current is detected to be below the phase-shedding threshold. Once the total current exceeds the phase-adding threshold, the idle phases are added in immediately. See the MFR_APSI_CTRL (30h) section on Page 39 for more details.

Table 5 and Table 6 list the phase-shedding and phase-adding entry conditions based on the current report.

Table 5: Phase Number during Phase-Adding Based on the Current Report

Condition	Phase Number
5 x MFR_1PHL + MFR_PHASE_HYS ≤ I_{OUT}	6-phase CCM or full-phase (<6) CCM
4 x MFR_1PHL + MFR_PHASE_HYS ≤ I_{OUT} < 5 x MFR_1PHL + MFR_PHASE_HYS	5-phase CCM or full-phase (<5) CCM
3 x MFR_1PHL + MFR_PHASE_HYS ≤ I_{OUT} < 4 x MFR_1PHL + MFR_PHASE_HYS	4-phase CCM or full-phase (<4) CCM
2 x MFR_1PHL + MFR_PHASE_HYS ≤ I_{OUT} < 3 x MFR_1PHL + MFR_PHASE_HYS	3-phase CCM or full-phase (<3) CCM
1 x MFR_1PHL + MFR_PHASE_HYS ≤ I_{OUT} < 2 x MFR_1PHL + MFR_PHASE_HYS	2-phase CCM or full-phase (<2) CCM
5A + MFR_PHASE_HYS ≤ I_{OUT} < 1 x MFR_1PHL + MFR_PHASE_HYS	1-phase CCM
I_{OUT} < 5A + MFR_PHASE_HYS	1-phase DCM, if DCM is enabled

Table 6: Phase Number during Phase-Shedding Based on the Current Report

Condition	Phase Number
5 x MFR_1PHL < I_{OUT}	6-phase CCM or full-phase (<6) CCM
4 x MFR_1PHL < I_{OUT} ≤ 5 x MFR_1PHL	5-phase CCM or full-phase (<5) CCM
3 x MFR_1PHL < I_{OUT} ≤ 4 x MFR_1PHL	4-phase CCM or full-phase (<4) CCM
2 x MFR_1PHL < I_{OUT} ≤ 3 x MFR_1PHL	3-phase CCM or full-phase (<3) CCM
1 x MFR_1PHL < I_{OUT} ≤ 2 x MFR_1PHL	2-phase CCM or full-phase (<2) CCM
5A < I_{OUT} ≤ 1 x MFR_1PHL	1-phase CCM
I_{OUT} ≤ 5A	1-phase DCM, if DCM is enabled

In addition to the basic requirements listed in Table 5 and Table 6, follow the instructions below to improve the transient condition:

1. When the configured full-phase number is smaller than the phase-adding number, the system runs with full phase.
2. The DVID process runs with full phase if the VR receives a DVID command from the processor, regardless of whether APS is enabled or disabled. Phase-shedding begins after the VR settles, and if APS is enabled.
3. When a load transient is detected, the VR runs with full phase to avoid V_{OUT} undershoot.

DCM operation can be enabled and disabled for APS via register configurations. See the MFR_APSI_CTRL (30h) section on Page 39 for more details.

Figure 13 shows the phase-adding and phase-shedding process.

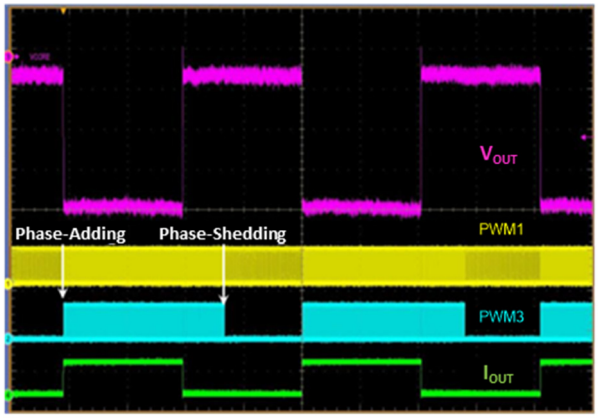


Figure 13: Phase-Shedding and Adding Process

PMBus Communication

The MPQ2977 supports real-time monitoring for the VR operation parameters, as well as status monitoring via the PMBus interface. Table 7 on page 18 lists the monitored parameters.

Table 7: PMBus Monitored Parameters

Parameter	PMBus
Output voltage	✓
Output current	✓
Temperature	✓
Input voltage	✓
Phase current	✓
OV	✓
UV	✓
OC	✓
OT	✓

Input Voltage (V_{IN}) Protections

The MPQ2977 features configurable V_{IN} protections with the following thresholds, configured via the related PMBus registers:

- If the sensed V_{IN} drops below MFR_VIN_ON_OFF (35h), bits[15:8], then the VR tri-state shuts down immediately. If the V_{IN} UVLO mode is set to non-latch mode, then the device restarts when the sensed V_{IN} exceeds MFR_VIN_ON_OFF (35h), bits[7:0].
- If the sensed V_{IN} exceeds MFR_VIN_UVOV_LIMIT (36h), bits[7:0] and the V_{IN} OVP mode is set to latch-off mode, then the VR latches.
- If V_{IN} drops below MFR_VIN_UVOV_LIMIT (36h), bits[15:9] and the V_{IN} UVP mode is set to latch-off mode, then the VR latches.

Over-Voltage Protection (OVP)

The OVP circuit monitors V_{OUT} for an OV condition. Figure 14 shows the OV signal generation.

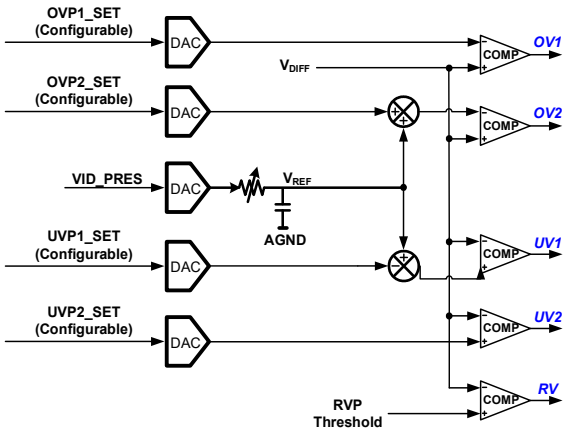


Figure 14: OVP and RVP Trigger Threshold

There are two types of OVP, described in greater detail below.

The first type is OVP1, which is set by MFR_OVP_DA_SET (95h). This is an absolute OV threshold, and is active whenever the controller is enabled, regardless of the operation/fault conditions.

In the event of an OVP1 condition, the PWMs are latched low to turn off the high-side MOSFETs (HS-FETs). The low-side MOSFETs (LS-FETs) turn on to discharge V_{OUT}. The OVP1 latch can only be reset by toggling EN or VCC.

The second type is OVP2, which is the tracking OVP. If the detected V_{OUT} exceeds the reference voltage for a certain time, the controller triggers OVP2 after a delay time. OVP2 latches PWM low to discharge the output until the output drops below the RVP threshold. Figure 15 shows the VR's behavior when OVP2 is triggered.

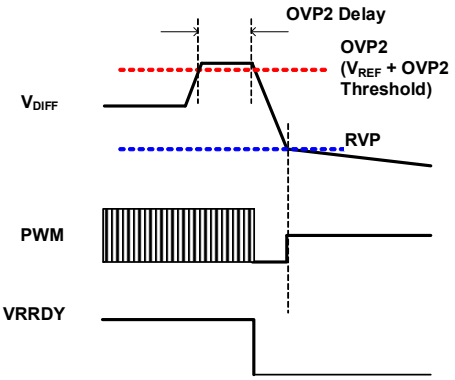


Figure 15: OVP and RVP Fault Protection

To avoid a false trigger, the OVP2 function is blanked during soft start and shutdown, as well as during the VID transition period.

The OVP2 protection mode can be set via MFR_PROTECT_CFG (90h), bits[5:4]). The OVP delay time is set via OVP2_SET_DELAYTIME (91h), bits[11:6].

Reverse-Voltage Protection (RVP)

During OVP, the LS-FET remains on to drive the inductor current negative. A large reverse inductor current can produce negative output voltages that may damage the processor and other components. In addition to OVP, the MPQ2977 implements RVP to prevent negative voltage ringing after the OV logic is triggered.

If V_{DIFF} drops below the RVP threshold, the MPQ2977 triggers RVP by latching all PWM outputs to tri-state. The reverse inductor current can be reset to 0A by dissipating the energy in

the inductor to the input DC voltage source through forward-biased body diode of the HS-FETs (see Figure 15 on page 18).

Over-Current Protection (OCP)

The MPQ2977 provides configurable total current protection for each rail to prevent the VR from working at extremely heavy loads. If the sensed average total I_{OUT} exceeds the over-current (OC) threshold set by MFR_IMONOCP_SET (98h), OCP is triggered.

If the sensed I_{OUT} exceeds the OCP level for the delay time (set via OCP_SET_DELAYTIME (93h), bits[5:0]), the part turns off both the HS-FETs and LS-FETs by setting the PWM to tri-state. Figure 16 shows the OCP process for total current protection.

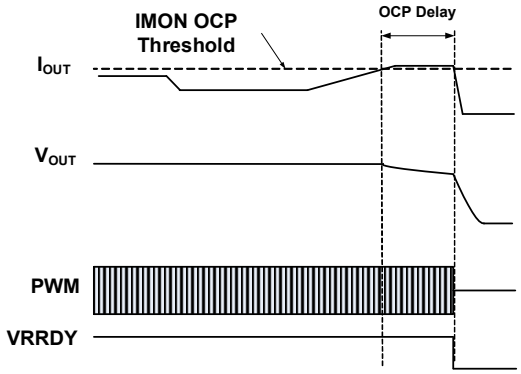


Figure 16: Total Current OCP

Phase Current Limit Protection

In addition to the total OC limit based on the sensed I_{OUT}, the MPQ2977 also utilizes a cycle-by-cycle valley point OC limit method to limit each phase current. If the phase current exceeds the set valley point, the PWM pulse of that phase is not sent when the PWM set signal is sent. The next phase turns on when its own PWM is on, which regulates V_{OUT} at the set point. The phase current limit does not trigger latch-off mode. Latch-off mode is triggered only if the phase current limit is triggered by OCP or UVP.

The valley point OC level can be configured via the PMBus (MFR_OCP_DA_SET (97h)) to limit the per-phase current.

Figure 17 shows the process when V_{OUT} is shorted to ground. During this process, the per-phase OCP limits the phase current immediately. The VR shuts down after a set time.

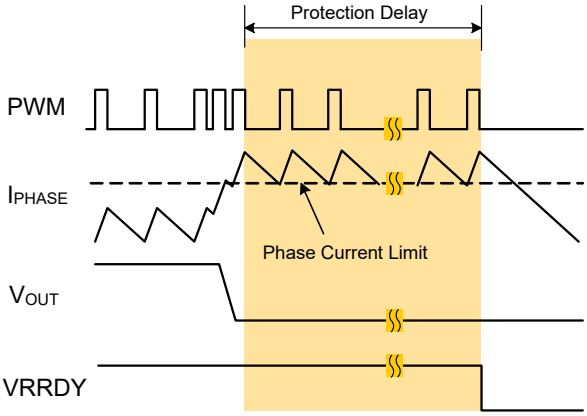


Figure 17: Phase Current Limit Protection when an Output Dead Short Occurs

Under-Voltage Protection (UVP)

Similar to OVP, there are two levels of UVP: fixed UVP (UVP1) and tracking UVP (UVP2). If the sensed output voltage (V_{DIFF}) drops below the UVP threshold for a certain amount of time, the system triggers UVP and immediately turns off all phases by setting the PWM into tri-state. Figure 18 shows the UVP process.

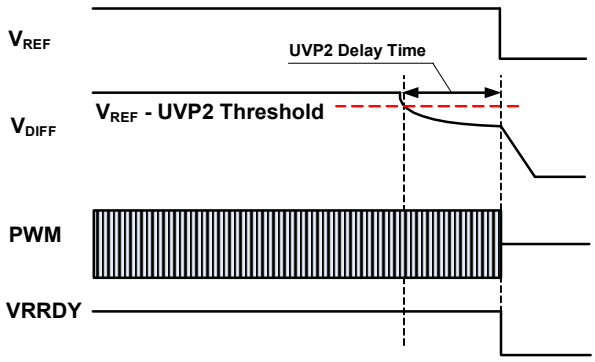


Figure 18: Under-Voltage Protection (UVP)

Normally, UVP is triggered when OCP occurs. The UVP modes can be set via MFR_PROTECT_CFG (90h), bit[7] (for UVP1) and MFR_PROTECT_CFG (90h), bits[9:8] (for UVP2). The UVP2 delay time can be set via UVP2_SET_DELAYTIME (91h), bits[5:0]).

Phase Current Balancing and Thermal Balancing

The MPQ2977 phase current is sensed and calculated with the current reference in the slow current proportion integrate (PI) loop. Each phase's PWM on time is adjusted individually to balance the currents by applying sigma-delta (Σ-Δ) modulation and delay line-loop (DLL)

technology in the current balance modulation. This balances the current and greatly reduces jitter.

Each current balance loop can also include a configurable phase current offset to achieve the thermal balance among the phases. The phase that has the worst cooling capability can be set to take less phase current by adding an offset on the CS sample value. This helps thermally balance the phases.

See the MFR_CS_OFFSET1_2 (EBh), MFR_CS_OFFSET3_4 (ECh), and MFR_CS_OFFSET5_6 (EDh) sections on Page 69 for more details.

DRONA/B Function

The DRONA/B pin sets the Intelli-Phase™ to standby mode. To do so, connect DRONA/B to Intelli-Phase™'s EN/SYNC pin. In standby mode, the DRONA/B pin either goes low or goes to tri-state so that the Intelli-Phase™ can enter low-power mode (LPM) to save power. In normal operation mode, DRONA/B is logic high. Figure 19 shows the connection between the DRONA/B pin and the Intelli-Phase's™ EN/SYNC pin.

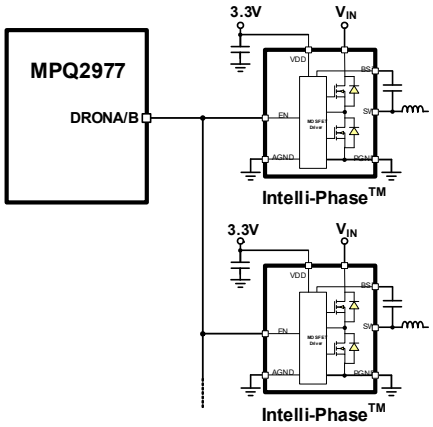


Figure 19: DRONA/B Connection between the MPQ2977 and Intelli-Phase™

FAULT

The FAULT signal asserts if any fault condition is triggered. When a GPIO pin is configured to be FAULT, it can be configured either separately for each rail, or for both rails. The FAULT pin initializes in tri-state at start-up.

VRRDY

VRRDY asserts when the rail output is correctly regulated and no fault condition has been detected. When a GPIO pin is configured to be VRRDY, it can be configured either separately for each rail, or for both rails. The VRRDY pin initializes in a low state at start-up.

ALERT

The ALERT signal asserts when the VR output is within the DVID process, and de-asserts when the DVID process is complete. When a GPIO pin is configured to be ALERT, it can be configured either separately for each rail, or for both rails. The ALERT pin initializes in tri-state at start-up.

VR_HOT

The VR_HOT fault signal asserts when the sensed external temperature exceeds the VR_HOT threshold. This is used for fault reporting only, and it cannot shut down the system. There is a configurable hysteresis to de-assert VR_HOT when the sensed temperature drops below the VR_HOT threshold. When a GPIO pin is configured to be VR_HOT, it can be configured either separately for each rail, or for both rails. The VR_HOT pin initializes in tri-state at start-up.

VID RANGE

The MPQ2977 has two different VID steps: 2.5mV/step or 5mV/step. If the VID step is 2.5mV, the VID range is between 0V and 1.6V. If the VID step is 5mV, the VID range is between 0V and 3.2V. Table 8 shows the VID resolution when the step is 2.5mV. Table 9 on page 24 shows the VID resolution when the VID step is 5mV.

Table 8: 2.5mV/Step VID Table

VID (Hex)	V_{OUT} (V)	VID (Hex)	V_{OUT} (V)	VID (Hex)	V_{OUT} (V)	VID (Hex)	V_{OUT} (V)
0000	0.0000	002F	0.1175	005E	0.2350	008D	0.3525
0001	0.0025	0030	0.1200	005F	0.2375	008E	0.3550
0002	0.0050	0031	0.1225	0060	0.2400	008F	0.3575
0003	0.0075	0032	0.1250	0061	0.2425	0090	0.3600
0004	0.0100	0033	0.1275	0062	0.2450	0091	0.3625
0005	0.0125	0034	0.1300	0063	0.2475	0092	0.3650
0006	0.0150	0035	0.1325	0064	0.2500	0093	0.3675
0007	0.0175	0036	0.1350	0065	0.2525	0094	0.3700
0008	0.0200	0037	0.1375	0066	0.2550	0095	0.3725
0009	0.0225	0038	0.1400	0067	0.2575	0096	0.3750
000A	0.0250	0039	0.1425	0068	0.2600	0097	0.3775
000B	0.0275	003A	0.1450	0069	0.2625	0098	0.3800
000C	0.0300	003B	0.1475	006A	0.2650	0099	0.3825
000D	0.0325	003C	0.1500	006B	0.2675	009A	0.3850
000E	0.0350	003D	0.1525	006C	0.2700	009B	0.3875
000F	0.0375	003E	0.1550	006D	0.2725	009C	0.3900
0010	0.0400	003F	0.1575	006E	0.2750	009D	0.3925
0011	0.0425	0040	0.1600	006F	0.2775	009E	0.3950
0012	0.0450	0041	0.1625	0070	0.2800	009F	0.3975
0013	0.0475	0042	0.1650	0071	0.2825	00A0	0.4000
0014	0.0500	0043	0.1675	0072	0.2850	00A1	0.4025
0015	0.0525	0044	0.1700	0073	0.2875	00A2	0.4050
0016	0.0550	0045	0.1725	0074	0.2900	00A3	0.4075
0017	0.0575	0046	0.1750	0075	0.2925	00A4	0.4100
0018	0.0600	0047	0.1775	0076	0.2950	00A5	0.4125
0019	0.0625	0048	0.1800	0077	0.2975	00A6	0.4150
001A	0.0650	0049	0.1825	0078	0.3000	00A7	0.4175
001B	0.0675	004A	0.1850	0079	0.3025	00A8	0.4200
001C	0.0700	004B	0.1875	007A	0.3050	00A9	0.4225
001D	0.0725	004C	0.1900	007B	0.3075	00AA	0.4250
001E	0.0750	004D	0.1925	007C	0.3100	00AB	0.4275
001F	0.0775	004E	0.1950	007D	0.3125	00AC	0.4300
0020	0.0800	004F	0.1975	007E	0.3150	00AD	0.4325
0021	0.0825	0050	0.2000	007F	0.3175	00AE	0.4350
0022	0.0850	0051	0.2025	0080	0.3200	00AF	0.4375
0023	0.0875	0052	0.2050	0081	0.3225	00B0	0.4400
0024	0.0900	0053	0.2075	0082	0.3250	00B1	0.4425
0025	0.0925	0054	0.2100	0083	0.3275	00B2	0.4450
0026	0.0950	0055	0.2125	0084	0.3300	00B3	0.4475
0027	0.0975	0056	0.2150	0085	0.3325	00B4	0.4500
0028	0.1000	0057	0.2175	0086	0.3350	00B5	0.4525
0029	0.1025	0058	0.2200	0087	0.3375	00B6	0.4550
002A	0.1050	0059	0.2225	0088	0.3400	00B7	0.4575
002B	0.1075	005A	0.2250	0089	0.3425	00B8	0.4600
002C	0.1100	005B	0.2275	008A	0.3450	00B9	0.4625
002D	0.1125	005C	0.2300	008B	0.3475	00BA	0.4650

002E	0.1150	005D	0.2325	008C	0.3500	00BB	0.4675
00BC	0.4700	00F1	0.6025	0126	0.7350	015B	0.8675
00BD	0.4725	00F2	0.6050	0127	0.7375	015C	0.8700
00BE	0.4750	00F3	0.6075	0128	0.7400	015D	0.8725
00BF	0.4775	00F4	0.6100	0129	0.7425	015E	0.8750
00C0	0.4800	00F5	0.6125	012A	0.7450	015F	0.8775
00C1	0.4825	00F6	0.6150	012B	0.7475	0160	0.8800
00C2	0.4850	00F7	0.6175	012C	0.7500	0161	0.8825
00C3	0.4875	00F8	0.6200	012D	0.7525	0162	0.8850
00C4	0.4900	00F9	0.6225	012E	0.7550	0163	0.8875
00C5	0.4925	00FA	0.6250	012F	0.7575	0164	0.8900
00C6	0.4950	00FB	0.6275	0130	0.7600	0165	0.8925
00C7	0.4975	00FC	0.6300	0131	0.7625	0166	0.8950
00C8	0.5000	00FD	0.6325	0132	0.7650	0167	0.8975
00C9	0.5025	00FE	0.6350	0133	0.7675	0168	0.9000
00CA	0.5050	00FF	0.6375	0134	0.7700	0169	0.9025
00CB	0.5075	0100	0.6400	0135	0.7725	016A	0.9050
00CC	0.5100	0101	0.6425	0136	0.7750	016B	0.9075
00CD	0.5125	0102	0.6450	0137	0.7775	016C	0.9100
00CE	0.5150	0103	0.6475	0138	0.7800	016D	0.9125
00CF	0.5175	0104	0.6500	0139	0.7825	016E	0.9150
00D0	0.5200	0105	0.6525	013A	0.7850	016F	0.9175
00D1	0.5225	0106	0.6550	013B	0.7875	0170	0.9200
00D2	0.5250	0107	0.6575	013C	0.7900	0171	0.9225
00D3	0.5275	0108	0.6600	013D	0.7925	0172	0.9250
00D4	0.5300	0109	0.6625	013E	0.7950	0173	0.9275
00D5	0.5325	010A	0.6650	013F	0.7975	0174	0.9300
00D6	0.5350	010B	0.6675	0140	0.8000	0175	0.9325
00D7	0.5375	010C	0.6700	0141	0.8025	0176	0.9350
00D8	0.5400	010D	0.6725	0142	0.8050	0177	0.9375
00D9	0.5425	010E	0.6750	0143	0.8075	0178	0.9400
00DA	0.5450	010F	0.6775	0144	0.8100	0179	0.9425
00DB	0.5475	0110	0.6800	0145	0.8125	017A	0.9450
00DC	0.5500	0111	0.6825	0146	0.8150	017B	0.9475
00DD	0.5525	0112	0.6850	0147	0.8175	017C	0.9500
00DE	0.5550	0113	0.6875	0148	0.8200	017D	0.9525
00DF	0.5575	0114	0.6900	0149	0.8225	017E	0.9550
00E0	0.5600	0115	0.6925	014A	0.8250	017F	0.9575
00E1	0.5625	0116	0.6950	014B	0.8275	0180	0.9600
00E2	0.5650	0117	0.6975	014C	0.8300	0181	0.9625
00E3	0.5675	0118	0.7000	014D	0.8325	0182	0.9650
00E4	0.5700	0119	0.7025	014E	0.8350	0183	0.9675
00E5	0.5725	011A	0.7050	014F	0.8375	0184	0.9700
00E6	0.5750	011B	0.7075	0150	0.8400	0185	0.9725
00E7	0.5775	011C	0.7100	0151	0.8425	0186	0.9750
00E8	0.5800	011D	0.7125	0152	0.8450	0187	0.9775
00E9	0.5825	011E	0.7150	0153	0.8475	0188	0.9800
00EA	0.5850	011F	0.7175	0154	0.8500	0189	0.9825
00EB	0.5875	0120	0.7200	0155	0.8525	018A	0.9850
00EC	0.5900	0121	0.7225	0156	0.8550	018B	0.9875
00ED	0.5925	0122	0.7250	0157	0.8575	018C	0.9900
00EE	0.5950	0123	0.7275	0158	0.8600	018D	0.9925
00EF	0.5975	0124	0.7300	0159	0.8625	018E	0.9950
00F0	0.6000	0125	0.7325	015A	0.8650	018F	0.9975

0190	1.0000	01C5	1.1325	01FA	1.2650	022F	1.3975
0191	1.0025	01C6	1.1350	01FB	1.2675	0230	1.4000
0192	1.0050	01C7	1.1375	01FC	1.2700	0231	1.4025
0193	1.0075	01C8	1.1400	01FD	1.2725	0232	1.4050
0194	1.0100	01C9	1.1425	01FE	1.2750	0233	1.4075
0195	1.0125	01CA	1.1450	01FF	1.2775	0234	1.4100
0196	1.0150	01CB	1.1475	0200	1.2800	0235	1.4125
0197	1.0175	01CC	1.1500	0201	1.2825	0236	1.4150
0198	1.0200	01CD	1.1525	0202	1.2850	0237	1.4175
0199	1.0225	01CE	1.1550	0203	1.2875	0238	1.4200
019A	1.0250	01CF	1.1575	0204	1.2900	0239	1.4225
019B	1.0275	01D0	1.1600	0205	1.2925	023A	1.4250
019C	1.0300	01D1	1.1625	0206	1.2950	023B	1.4275
019D	1.0325	01D2	1.1650	0207	1.2975	023C	1.4300
019E	1.0350	01D3	1.1675	0208	1.3000	023D	1.4325
019F	1.0375	01D4	1.1700	0209	1.3025	023E	1.4350
01A0	1.0400	01D5	1.1725	020A	1.3050	023F	1.4375
01A1	1.0425	01D6	1.1750	020B	1.3075	0240	1.4400
01A2	1.0450	01D7	1.1775	020C	1.3100	0241	1.4425
01A3	1.0475	01D8	1.1800	020D	1.3125	0242	1.4450
01A4	1.0500	01D9	1.1825	020E	1.3150	0243	1.4475
01A5	1.0525	01DA	1.1850	020F	1.3175	0244	1.4500
01A6	1.0550	01DB	1.1875	0210	1.3200	0245	1.4525
01A7	1.0575	01DC	1.1900	0211	1.3225	0246	1.4550
01A8	1.0600	01DD	1.1925	0212	1.3250	0247	1.4575
01A9	1.0625	01DE	1.1950	0213	1.3275	0248	1.4600
01AA	1.0650	01DF	1.1975	0214	1.3300	0249	1.4625
01AB	1.0675	01E0	1.2000	0215	1.3325	024A	1.4650
01AC	1.0700	01E1	1.2025	0216	1.3350	024B	1.4675
01AD	1.0725	01E2	1.2050	0217	1.3375	024C	1.4700
01AE	1.0750	01E3	1.2075	0218	1.3400	024D	1.4725
01AF	1.0775	01E4	1.2100	0219	1.3425	024E	1.4750
01B0	1.0800	01E5	1.2125	021A	1.3450	024F	1.4775
01B1	1.0825	01E6	1.2150	021B	1.3475	0250	1.4800
01B2	1.0850	01E7	1.2175	021C	1.3500	0251	1.4825
01B3	1.0875	01E8	1.2200	021D	1.3525	0252	1.4850
01B4	1.0900	01E9	1.2225	021E	1.3550	0253	1.4875
01B5	1.0925	01EA	1.2250	021F	1.3575	0254	1.4900
01B6	1.0950	01EB	1.2275	0220	1.3600	0255	1.4925
01B7	1.0975	01EC	1.2300	0221	1.3625	0256	1.4950
01B8	1.1000	01ED	1.2325	0222	1.3650	0257	1.4975
01B9	1.1025	01EE	1.2350	0223	1.3675	0258	1.5000
01BA	1.1050	01EF	1.2375	0224	1.3700	0259	1.5025
01BB	1.1075	01F0	1.2400	0225	1.3725	025A	1.5050
01BC	1.1100	01F1	1.2425	0226	1.3750	025B	1.5075
01BD	1.1125	01F2	1.2450	0227	1.3775	025C	1.5100
01BE	1.1150	01F3	1.2475	0228	1.3800	025D	1.5125
01BF	1.1175	01F4	1.2500	0229	1.3825	025E	1.5150
01C0	1.1200	01F5	1.2525	022A	1.3850	025F	1.5175
01C1	1.1225	01F6	1.2550	022B	1.3875	0260	1.5200
01C2	1.1250	01F7	1.2575	022C	1.3900	0261	1.5225
01C3	1.1275	01F8	1.2600	022D	1.3925	0262	1.5250
01C4	1.1300	01F9	1.2625	022E	1.3950	0263	1.5275
0264	1.5300	026C	1.5500	0274	1.5700	027C	1.5900

0265	1.5325	026D	1.5525	0275	1.5725	027D	1.5925
0266	1.5350	026E	1.5550	0276	1.5750	027E	1.5950
0267	1.5375	026F	1.5575	0277	1.5775	027F	1.5975
0268	1.5400	0270	1.5600	0278	1.5800	0280	1.6000
0269	1.5425	0271	1.5625	0279	1.5825	-	-
026A	1.5450	0272	1.5650	027A	1.5850	-	-
026B	1.5475	0273	1.5675	027B	1.5875	-	-

Table 9: 5mV/Step VID Table

VID (Hex)	V_{OUT} (V)	VID (Hex)	V_{OUT} (V)	VID (Hex)	V_{OUT} (V)	VID (Hex)	V_{OUT} (V)
0000	0.000	0028	0.200	0050	0.400	0078	0.600
0001	0.005	0029	0.205	0051	0.405	0079	0.605
0002	0.010	002A	0.210	0052	0.410	007A	0.610
0003	0.015	002B	0.215	0053	0.415	007B	0.615
0004	0.020	002C	0.220	0054	0.420	007C	0.620
0005	0.025	002D	0.225	0055	0.425	007D	0.625
0006	0.030	002E	0.230	0056	0.430	007E	0.630
0007	0.035	002F	0.235	0057	0.435	007F	0.635
0008	0.040	0030	0.240	0058	0.440	0080	0.640
0009	0.045	0031	0.245	0059	0.445	0081	0.645
000A	0.050	0032	0.250	005A	0.450	0082	0.650
000B	0.055	0033	0.255	005B	0.455	0083	0.655
000C	0.060	0034	0.260	005C	0.460	0084	0.660
000D	0.065	0035	0.265	005D	0.465	0085	0.665
000E	0.070	0036	0.270	005E	0.470	0086	0.670
000F	0.075	0037	0.275	005F	0.475	0087	0.675
0010	0.080	0038	0.280	0060	0.480	0088	0.680
0011	0.085	0039	0.285	0061	0.485	0089	0.685
0012	0.090	003A	0.290	0062	0.490	008A	0.690
0013	0.095	003B	0.295	0063	0.495	008B	0.695
0014	0.100	003C	0.300	0064	0.500	008C	0.700
0015	0.105	003D	0.305	0065	0.505	008D	0.705
0016	0.110	003E	0.310	0066	0.510	008E	0.710
0017	0.115	003F	0.315	0067	0.515	008F	0.715
0018	0.120	0040	0.320	0068	0.520	0090	0.720
0019	0.125	0041	0.325	0069	0.525	0091	0.725
001A	0.130	0042	0.330	006A	0.530	0092	0.730
001B	0.135	0043	0.335	006B	0.535	0093	0.735
001C	0.140	0044	0.340	006C	0.540	0094	0.740
001D	0.145	0045	0.345	006D	0.545	0095	0.745
001E	0.150	0046	0.350	006E	0.550	0096	0.750
001F	0.155	0047	0.355	006F	0.555	0097	0.755
0020	0.160	0048	0.360	0070	0.560	0098	0.760
0021	0.165	0049	0.365	0071	0.565	0099	0.765
0022	0.170	004A	0.370	0072	0.570	009A	0.770
0023	0.175	004B	0.375	0073	0.575	009B	0.775
0024	0.180	004C	0.380	0074	0.580	009C	0.780
0025	0.185	004D	0.385	0075	0.585	009D	0.785
0026	0.190	004E	0.390	0076	0.590	009E	0.790
0027	0.195	004F	0.395	0077	0.595	009F	0.795
00A0	0.800	00D5	1.065	010A	1.330	013F	1.595
00A1	0.805	00D6	1.070	010B	1.335	0140	1.600
00A2	0.810	00D7	1.075	010C	1.340	0141	1.605
00A3	0.815	00D8	1.080	010D	1.345	0142	1.610

00A4	0.820	00D9	1.085	010E	1.350	0143	1.615
00A5	0.825	00DA	1.090	010F	1.355	0144	1.620
00A6	0.830	00DB	1.095	0110	1.360	0145	1.625
00A7	0.835	00DC	1.100	0111	1.365	0146	1.630
00A8	0.840	00DD	1.105	0112	1.370	0147	1.635
00A9	0.845	00DE	1.110	0113	1.375	0148	1.640
00AA	0.850	00DF	1.115	0114	1.380	0149	1.645
00AB	0.855	00E0	1.120	0115	1.385	014A	1.650
00AC	0.860	00E1	1.125	0116	1.390	014B	1.655
00AD	0.865	00E2	1.130	0117	1.395	014C	1.660
00AE	0.870	00E3	1.135	0118	1.400	014D	1.665
00AF	0.875	00E4	1.140	0119	1.405	014E	1.670
00B0	0.880	00E5	1.145	011A	1.410	014F	1.675
00B1	0.885	00E6	1.150	011B	1.415	0150	1.680
00B2	0.890	00E7	1.155	011C	1.420	0151	1.685
00B3	0.895	00E8	1.160	011D	1.425	0152	1.690
00B4	0.900	00E9	1.165	011E	1.430	0153	1.695
00B5	0.905	00EA	1.170	011F	1.435	0154	1.700
00B6	0.910	00EB	1.175	0120	1.440	0155	1.705
00B7	0.915	00EC	1.180	0121	1.445	0156	1.710
00B8	0.920	00ED	1.185	0122	1.450	0157	1.715
00B9	0.925	00EE	1.190	0123	1.455	0158	1.720
00BA	0.930	00EF	1.195	0124	1.460	0159	1.725
00BB	0.935	00F0	1.200	0125	1.465	015A	1.730
00BC	0.940	00F1	1.205	0126	1.470	015B	1.735
00BD	0.945	00F2	1.210	0127	1.475	015C	1.740
00BE	0.950	00F3	1.215	0128	1.480	015D	1.745
00BF	0.955	00F4	1.220	0129	1.485	015E	1.750
00C0	0.960	00F5	1.225	012A	1.490	015F	1.755
00C1	0.965	00F6	1.230	012B	1.495	0160	1.760
00C2	0.970	00F7	1.235	012C	1.500	0161	1.765
00C3	0.975	00F8	1.240	012D	1.505	0162	1.770
00C4	0.980	00F9	1.245	012E	1.510	0163	1.775
00C5	0.985	00FA	1.250	012F	1.515	0164	1.780
00C6	0.990	00FB	1.255	0130	1.520	0165	1.785
00C7	0.995	00FC	1.260	0131	1.525	0166	1.790
00C8	1.000	00FD	1.265	0132	1.530	0167	1.795
00C9	1.005	00FE	1.270	0133	1.535	0168	1.800
00CA	1.010	00FF	1.275	0134	1.540	0169	1.805
00CB	1.015	0100	1.280	0135	1.545	016A	1.810
00CC	1.020	0101	1.285	0136	1.550	016B	1.815
00CD	1.025	0102	1.290	0137	1.555	016C	1.820
00CE	1.030	0103	1.295	0138	1.560	016D	1.825
00CF	1.035	0104	1.300	0139	1.565	016E	1.830
00D0	1.040	0105	1.305	013A	1.570	016F	1.835
00D1	1.045	0106	1.310	013B	1.575	0170	1.840
00D2	1.050	0107	1.315	013C	1.580	0171	1.845
00D3	1.055	0108	1.320	013D	1.585	0172	1.850
00D4	1.060	0109	1.325	013E	1.590	0173	1.855
0174	1.860	01A9	2.125	01DE	2.390	0213	2.655
0175	1.865	01AA	2.130	01DF	2.395	0214	2.660
0176	1.870	01AB	2.135	01E0	2.400	0215	2.665
0177	1.875	01AC	2.140	01E1	2.405	0216	2.670
0178	1.880	01AD	2.145	01E2	2.410	0217	2.675

0179	1.885	01AE	2.150	01E3	2.415	0218	2.680
017A	1.890	01AF	2.155	01E4	2.420	0219	2.685
017B	1.895	01B0	2.160	01E5	2.425	021A	2.690
017C	1.900	01B1	2.165	01E6	2.430	021B	2.695
017D	1.905	01B2	2.170	01E7	2.435	021C	2.700
017E	1.910	01B3	2.175	01E8	2.440	021D	2.705
017F	1.915	01B4	2.180	01E9	2.445	021E	2.710
0180	1.920	01B5	2.185	01EA	2.450	021F	2.715
0181	1.925	01B6	2.190	01EB	2.455	0220	2.720
0182	1.930	01B7	2.195	01EC	2.460	0221	2.725
0183	1.935	01B8	2.200	01ED	2.465	0222	2.730
0184	1.940	01B9	2.205	01EE	2.470	0223	2.735
0185	1.945	01BA	2.210	01EF	2.475	0224	2.740
0186	1.950	01BB	2.215	01F0	2.480	0225	2.745
0187	1.955	01BC	2.220	01F1	2.485	0226	2.750
0188	1.960	01BD	2.225	01F2	2.490	0227	2.755
0189	1.965	01BE	2.230	01F3	2.495	0228	2.760
018A	1.970	01BF	2.235	01F4	2.500	0229	2.765
018B	1.975	01C0	2.240	01F5	2.505	022A	2.770
018C	1.980	01C1	2.245	01F6	2.510	022B	2.775
018D	1.985	01C2	2.250	01F7	2.515	022C	2.780
018E	1.990	01C3	2.255	01F8	2.520	022D	2.785
018F	1.995	01C4	2.260	01F9	2.525	022E	2.790
0190	2.000	01C5	2.265	01FA	2.530	022F	2.795
0191	2.005	01C6	2.270	01FB	2.535	0230	2.800
0192	2.010	01C7	2.275	01FC	2.540	0231	2.805
0193	2.015	01C8	2.280	01FD	2.545	0232	2.810
0194	2.020	01C9	2.285	01FE	2.550	0233	2.815
0195	2.025	01CA	2.290	01FF	2.555	0234	2.820
0196	2.030	01CB	2.295	0200	2.560	0235	2.825
0197	2.035	01CC	2.300	0201	2.565	0236	2.830
0198	2.040	01CD	2.305	0202	2.570	0237	2.835
0199	2.045	01CE	2.310	0203	2.575	0238	2.840
019A	2.050	01CF	2.315	0204	2.580	0239	2.845
019B	2.055	01D0	2.320	0205	2.585	023A	2.850
019C	2.060	01D1	2.325	0206	2.590	023B	2.855
019D	2.065	01D2	2.330	0207	2.595	023C	2.860
019E	2.070	01D3	2.335	0208	2.600	023D	2.865
019F	2.075	01D4	2.340	0209	2.605	023E	2.870
01A0	2.080	01D5	2.345	020A	2.610	023F	2.875
01A1	2.085	01D6	2.350	020B	2.615	0240	2.880
01A2	2.090	01D7	2.355	020C	2.620	0241	2.885
01A3	2.095	01D8	2.360	020D	2.625	0242	2.890
01A4	2.100	01D9	2.365	020E	2.630	0243	2.895
01A5	2.105	01DA	2.370	020F	2.635	0244	2.900
01A6	2.110	01DB	2.375	0210	2.640	0245	2.905
01A7	2.115	01DC	2.380	0211	2.645	0246	2.910
01A8	2.120	01DD	2.385	0212	2.650	0247	2.915
0248	2.920	0257	2.995	0266	3.070	0275	3.145
0249	2.925	0258	3.000	0267	3.075	0276	3.150
024A	2.930	0259	3.005	0268	3.080	0277	3.155
024B	2.935	025A	3.010	0269	3.085	0278	3.160
024C	2.940	025B	3.015	026A	3.090	0279	3.165
024D	2.945	025C	3.020	026B	3.095	027A	3.170

024E	2.950	025D	3.025	026C	3.100	027B	3.175
024F	2.955	025E	3.030	026D	3.105	027C	3.180
0250	2.960	025F	3.035	026E	3.110	027D	3.185
0251	2.965	0260	3.040	026F	3.115	027E	3.190
0252	2.970	0261	3.045	0270	3.120	027F	3.195
0253	2.975	0262	3.050	0271	3.125	0280	3.200
0254	2.980	0263	3.055	0272	3.130	-	-
0255	2.985	0264	3.060	0273	3.135	-	-
0256	2.990	0265	3.065	0274	3.140	-	-

PMBUS COMMANDS/REGISTERS (PAGE 0)

Command Code	Command Name	Bytes	Type
0x00	PAGE	1	R/W
0x02	CLEAR_ABIST_FAULT	0	W
0x03	CLEAR_GPIO_FAULT	0	W
0x04	CLEAR_LBIST_FAULT	0	W
0x05	LBIST_USER_TRIGGER	0	W
0x06	READ_FAULT_MESSAGE_PUBLIC	2	R
0x07	MFR_FAULT_MESSAGE_RAIL	2	R
0x08	CLEAR_LAST_FAULT	0	W
0x0F	CLEAR_MTP_FAULT	0	W
0x15	STORE	0	W
0x16	RESTORE	0	W
0x1A	MFR_CODE_REVISION	2	R/W
0x1B	MFR_GATECLK__MTP_CTRL	2	R/W
0x1C	MFR_IMON_GAIN	2	R/W
0x1E	MFR_OPTION_EN	2	R/W
0x20	MFR_EN_COMMAND	2	R/W
0x21	MFR_VOUT_COMMAND_R1	2	R/W
0x22	MFR_VOUT_COMMAND_R2	2	R/W
0x23	MFR_VREF_DIS_FSLOW	2	R/W
0x24	MFR_VOUT_TRIM_CCM1_R1	2	R/W
0x25	MFR_VOUT_TRIM_CCM2_R1_DCM	2	R/W
0x26	MFR_VOUT_TRIM_CCM_R2	2	R/W
0x2A	MFR_ADC_HOLD_TIME	2	R/W
0x2B	MFR_DEBUG	2	R/W
0x2C	MFR_PROTECT_PUBLIC_CFG	2	R/W
0x30	MFR_APSI_CTRL	2	R/W
0x35	MFR_VIN_ON_OFF	2	R/W
0x36	MFR_VIN_UVOV_LIMIT	2	R/W
0x37	MFR_VBOOT_R1	2	R/W
0x38	MFR_VBOOT_R2	2	R/W
0x60	MFR_4DIGIT_CODE	2	R/W
0x61	MFR_PRODUCT_ID	2	R/W
0x62	MFR_PWM_MINLOW_CCM	2	R/W
0x63	MFR_PWM_MINLOW_EXIT_HIZ	2	R/W
0x64	MFR_PWM_UC_ONTIME	2	R/W
0x68	MFR_VR_HOT_SET	2	R/W
0x69	MFR_IOUT_ALERT_SET	2	R/W
0x6A	MFR_TSW_FS_HYS	2	R/W
0x6B	MFR_TPROG	2	R/W
0x74	READ_VCOMP	2	R
0x75	READ_PMBUS_ADDR	2	R
0x76	READ_CS1	2	R
0x77	READ_CS2	2	R
0x78	READ_CS3	2	R
0x79	READ_CS4	2	R
0x7A	READ_VIN	2	R
0x7B	READ_VOUT_R1	2	R
0x7C	READ_VOUT_R2	2	R
0x7D	READ_VFB_R1	2	R
0x7F	READ_VFB_R2	2	R
0x80	READ_IMON_R1	2	R
0x81	READ_IMON_R2	2	R

PMBUS COMMANDS/REGISTERS (PAGE 0) *(continued)*

Command Code	Command Name	Bytes	Type
0x82	READ_TEMP_R1	2	R
0x84	READ_TEMP_R2	2	R
0x85	READ_CS5	2	R
0x86	READ_CS6	2	R
0x90	MFR_PROTECT_CFG	2	R/W
0x91	MFR_OVUV_DELAYTIME	2	R/W
0x92	MFR_OCP_DELAYTIME	2	R/W
0x93	MFR_OVUV_SET_R1	2	R/W
0x94	MFR_OVUV_SET_R2	2	R/W
0x95	MFR_OVP_DA_SET	2	R/W
0x96	MFR_UVP_DA_SET	2	R/W
0x97	MFR_OCP_DA_SET	2	R/W
0x98	MFR_IMONOCP_SET	2	R/W
0x99	MFR_UCP_DA_SET	2	R/W
0x9C	MFR_GPIO_SEL	2	R/W
0x9E	MFR_TEMP_GAIN	2	R/W
0x9F	MFR_TEMP_OFFSET	2	R/W
0xA0	MFR_IDRP_SET_R1	2	R/W
0xA1	MFR_IDRP_SET_R2	2	R/W
0xA2	MFR_RDRP_AC_RST	2	R/W
0xA3	MFR_RVP_SET	2	R/W
0xA4	MFR_I2C_VTH_SEL	2	R/W
0xAC	MFR_BGCHK_H_MAX	2	R/W
0xAD	MFR_BGCHK_H_MIN	2	R/W
0xAE	MFR_BGCHK_L_MAX	2	R/W
0xAF	MFR_BGCHK_L_MIN	2	R/W
0xB0	MFR_PASSWORD_INPUT	2	R/W
0xB1	MFR_1PH_R1	2	R/W
0xB2	MFR_1PH_R2	2	R/W
0xC0	MFR_PSI_TRIM_CCM1_R1	2	R/W
0xC1	MFR_PSI_TRIM_CCM2_R1	2	R/W
0xC2	MFR_PSI_TRIM_CCM_R2	2	R/W
0xC3	MFR_PSI_TRIM_DCM	2	R/W
0xCA	MFR_PHASE_CFG	2	R/W
0xCB	MFR_DYNAMIC_CTRL_R1	2	R/W
0xCC	MFR_DYNAMIC_CTRL_R2	2	R/W
0xCD	MFR_SW_HF_SET	2	R/W
0xCE	MFR_SW_LF_SET	2	R/W
0xCF	MFR_MIN_ONTIME	2	R/W
0xD0	MFR_SLOPE_SR_1P_R1	2	R/W
0xD1	MFR_SLOPE_SR_2P_R1	2	R/W
0xD2	MFR_SLOPE_SR_3P_R1	2	R/W
0xD3	MFR_SLOPE_SR_4P_R1	2	R/W
0xD4	MFR_SLOPE_SR_5P_R1	2	R/W
0xD5	MFR_SLOPE_SR_6P_R1	2	R/W
0xD6	MFR_SLOPE_SR_DCM_R1	2	R/W
0xD7	MFR_SLOPE_SR_1P_R2	2	R/W
0xD8	MFR_SLOPE_SR_2P_R2	2	R/W
0xD9	MFR_SLOPE_SR_3P_R2	2	R/W
0xDA	MFR_SLOPE_SR_DCM_R2	2	R/W
0xDB	MFR_SLOPE_CNT_DCM	2	R/W
0xDC	MFR_SLOPE_CNT_1P_2P_R1	2	R/W

PMBUS COMMANDS/REGISTERS (PAGE 0) *(continued)*

Command Code	Command Name	Bytes	Type
0xDD	MFR_SLOPE_CNT_3P_4P_R1	2	RW
0xDE	MFR_SLOPE_CNT_5P_6P_R1	2	RW
0xE0	MFR_SLOPE_CNT_1P_2P_R2	2	RW
0xE1	MFR_SLOPE_CNT_3P_R2	2	RW
0xE2	MFR_CURRENT_BALANCE_CTRL	2	RW
0xE3	MFR_DCLOOP_PI	2	RW
0xE4	MFR_VR_CONFIG	2	RW
0xE5	MFR_GPIO123_SLCT	2	RW
0xE6	MFR_GPIO456_SLCT	2	RW
0xEB	MFR_CS_OFFSET1_2	2	RW
0xEC	MFR_CS_OFFSET3_4	2	RW
0xED	MFR_CS_OFFSET5_6	2	RW
0xF0	MFR_FILTER_SET	2	RW
0xF1	MFR_TRANS_FAST_R1	2	RW
0xF2	MFR_TRANS_FAST_R2	2	RW
0xF3	MFR_INTIAL_DLY	2	RW
0xF4	MFR_VOUT_LEVEL_R1	2	RW
0xF5	MFR_VOUT_LEVEL_R2	2	RW
0xF6	MFR_VID_01H	2	RW
0xF7	MFR_SHUTDOWN_LEVEL	2	RW
0xF8	MFR_PMBUS_ADDR	2	RW
0xF9	MFR_PASSWORD	2	RW
0xFA	MFR_CHANNEL_OBS	2	RW
0xFB	MFR_VOUT_CMPS_MAX	2	RW
0xFC	MFR_SW_PRD_SET	2	RW
0xFD	MFR_OTP_SET	2	RW

PAGE 0 REGISTER MAP

PAGE (00h)

The PAGE command provides the ability to configure, control, and monitor all registers — including test mode and the MTP — through only one physical address.

Bits	Bit Name	Description
7:1	RESERVED	Reserved.
0	PAGE	Selects the page. 0x0: Page 0. All PMBus commands address operating registers on Page 0 0x1: Page 1. All PMBus commands address operating registers on Page 1

CLEAR_ABIST_FAULT (02h)

The CLEAR_ABIST_FAULT command is a 0-byte command that clears an analog built-in self-test (ABIST) fault.

CLEAR_GPIO_FAULT (03h)

The CLEAR_GPIO_FAULT command is a 0-byte command that resets the FAULT pin.

CLEAR_LBIST_FAULT (04h)

The CLEAR_LBIST_FAULT command is a 0-byte command clears a logic built-in self-test (LBIST) fault.

LBIST_USER_TRIGGER (05h)

The LBIST_USER_TRIGGER command is a 0-byte command that manually triggers LBIST.

READ_FAULT_MESSAGE_PUBLIC (06h)

The READ_FAULT_MESSAGE_PUBLIC command returns the fault messages that do not belong to either rail A or rail B.

Bits	Bit Name	Description
15:12	RESERVED	Reserved.
11	LBIST_ERR	Returns the LBIST error signal. 1’b1: There is an error 1’b0: No error (pass)
10	ABIST_ERR	Returns the ABIST error signal. 1’b1: There is an error 1’b0: No error (pass)
9	GPIO_ERR	Returns the GPIO self-check error signal. 1’b1: There is an error 1’b0: No error (pass)
8	RESERVED	Reserved.
7	BGCHK_ERR	Returns the bandgap voltage error signal. 1’b1: There is an error 1’b0: No error (pass)
6	OSC_ERR	Returns the OSC clock error signal. 1’b1: There is an error 1’b0: No error (pass)
5	VIN_OV	Returns the V_{IN} over-voltage (OV) signal. 1’b1: There is an error 1’b0: No error (pass)

4	VIN_UVLO	Returns the V_{IN} under-voltage lockout (UVLO) signal. 1'b1: There is an error 1'b0: No error (pass)
3	VIN_UV	Returns the V_{IN} under-voltage (UV) signal. 1'b1: There is an error 1'b0: No error (pass)
2	IBIAS_ERR	Returns the biased current from the analog block (I_{BIAS}) error signal. 1'b1: There is an error 1'b0: No error (pass)
1	VDD33_UV	Returns the VDD33 UV error signal. 1'b1: There is an error 1'b0: No error (pass)
0	ANA_ERR	Returns the analog error signal. 1'b1: There is an error 1'b0: No error (pass)

MFR_FAULT_MESSAGE_RAIL (07h)

The MFR_FAULT_MESSAGE_RAIL command returns the fault messages that belong to rail A and rail B.

Bits	Bit Name	Description
15	OVP1_R2	Returns the absolute over-voltage protection (OVP1) signal for rail B. 1'b1: There is an error 1'b0: No error (pass)
14	OVP2_R2	Returns the tracking over-voltage protection (OVP2) signal for rail B. 1'b1: There is an error 1'b0: No error (pass)
13	OCP_R2	Returns the over-current protection (OCP) signal for rail B. 1'b1: There is an error 1'b0: No error (pass)
12	UVP1_R2	Returns the fixed under-voltage protection (UVP1) signal for rail B. 1'b1: There is an error 1'b0: No error (pass)
11	UVP2_R2	Returns the tracking under-voltage protection (UVP2) signal for rail B. 1'b1: There is an error 1'b0: No error (pass)
10	OT_R2	Returns the over-temperature protection (OTP) signal for rail B. 1'b1: There is an error 1'b0: No error (pass)
9	TEMP_FAULT_R2	Returns the temperature fault signal for rail B. 1'b1: There is an error 1'b0: No error (pass)
8	PER_PHASE_OC_R2	Returns the per-phase OCP signal for rail B. 1'b1: There is an error 1'b0: No error (pass)

7	OVP1_R1	Returns the OVP1 signal for rail A. 1'b1: There is an error 1'b0: No error (pass)
6	OVP2_R1	Returns the OVP2 signal for rail A. 1'b1: There is an error 1'b0: No error (pass)
5	OCP_R1	Returns the OCP signal for rail A. 1'b1: There is an error 1'b0: No error (pass)
4	UVP1_R1	Returns the UVP1 signal for rail A. 1'b1: There is an error 1'b0: No error (pass)
3	UVP2_R1	Returns the UVP2 signal for rail A. 1'b1: There is an error 1'b0: No error (pass)
2	OT_R1	Returns the OTP signal for rail A. 1'b1: There is an error 1'b0: No error (pass)
1	TEMP_FAULT_R1	Returns the temperature fault signal for rail A. 1'b1: There is an error 1'b0: No error (pass)
0	PER_PHASE_OC_R1	Returns the per-phase OCP signal for rail A. 1'b1: There is an error 1'b0: No error (pass)

CLEAR_LAST_FAULT (08h)

The CLEAR_LAST_FAULT command is a 0-byte command that clears the last fault signals stored in MTP.

CLEAR_MTP_FAULT (0Fh)

The CLEAR_MTP_FAULT command is a 0-byte command that clears the fault that says the MTP signature is incorrect.

STORE (15h)

The STORE command is a 0-byte command that stores data into the MTP.

RESTORE (16h)

The RESTORE command is a 0-byte command that restores data from the MTP to the registers.

MFR_CODE_REVISION (1Ah)

The MFR_CODE_REVISION command returns the code revision.

Bits	Bit Name	Description
15:8	RESERVED	Reserved.
7:0	CODE_REVISION	Returns the code revision.

MFR_GATECLK_MTP_CTRL (1Bh)

The MFR_GATECLK_MTP_CTRL command enables the clocks of different modules to reduce power consumption. It also configures MTP functions.

Bits	Bit Name	Description
15	CALCULATION_CLK_EN	Enables the calculation module clock. 1'b1: Enabled 1'b0: Disabled
14	DLL_CLK_EN	Enables the DLL module clock. 1'b1: Enabled 1'b0: Disabled
13	MEM_CTRL_CLK_EN	Enables the MEM_CTRL module clock. 1'b1: Enabled 1'b0: Disabled
12	RAIL_CTRL_CLK_EN	Enables the clock of both RAIL_CTRL modules. 1'b1: Enabled 1'b0: Disabled
11	ANALOG_CTRL_CLK_EN	Enables the ANALOG_CTRL module clock. 1'b1: Enabled 1'b0: Disabled
10	PMBUS_CLK_EN	Enables the PMBus module clock. 1'b1: Enabled 1'b0: Disabled
9	RESERVED	Reserved.
8	RESERVED	Reserved.
7	IGNORE_NO_VIN_ TEMP_FAULT	Enables the VR to ignore V_{IN} or temperature faults during start-up. 1'b1: Enable 1'b0: Disabled
6	STORE_TRIM_REG_EN	Enables writing trim registers to the MTP when sending STORE_TRIG (15h). 1'b1: Enabled 1'b0: Disabled
5	LPM_CONFIG2	When the enable signal (ENA and ENB) is pulled low, this bit determines whether to copy the MTP again the next time the enable signal is pulled high. 1'b1: Copy the MTP again 1'b0: Do not copy the MTP; the VR does not enter low-power mode (LPM) when the enable signal is low
4	LPM_CONFIG1	Enables the VR to enter LPM once the enable signal turns low. The MTP is not copied again until this signal goes high. This bit does not work if 1Bh, bit[5] is set to 1'b0. 1'b1: Enable LPM when the enable signal is low 1'b0: Disable LPM
3	RESERVED	Reserved.
2	RESERVED	Reserved.
1	MTP_COPY_EN	Enables copying data from the MTP, except when the VR starts up. 1'b1: Enabled 1'b0: Disabled

0	CRC_PROTECT_EN	Enables cyclic redundancy check (CRC) protection.

MFR_IMON_GAIN (1Ch)

The MFR_IMON_GAIN command sets the I_{CCMAX} value for rail A and rail B.

Bits	Bit Name	Description
15:8	MFR_IMON_GAIN_R1	Sets the rail A IMON gain, calculated with the following equation: MFR_IMON_GAIN_R1 = 1.6V × 8 / 11 / R_{IMON} / G_{IMON} / G_{CS} Where G_{IMON} = 1/8. 1A/LSB.
7:0	MFR_IMON_GAIN_R2	Sets the rail B IMON gain, calculated with the following equation: MFR_IMON_GAIN_R2 = 1.6V × 8 / 11 / R_{IMON} / G_{IMON} / G_{CS} Where G_{IMON} = 1/8. 1A/LSB.

MFR_OPTION_EN (1Eh)

The MFR_OPTION_EN command enables some safety functions.

Bits	Bit Name	Description
15	MTP_SELF_TEST_EN	The VR reads back this data for comparison once it has been sent to the MTP. This bit enables the device to report the comparison error. 1'b1: Enabled 1'b0: Disabled
14:8	RESERVED	Reserved.
7	LBIST_EN	Enables the LBIST function. 1'b1: Enabled 1'b0: Disabled
6	LBIST_ERR_EN	Enables LBIST error detection. 1'b1: Enabled 1'b0: Disabled
5	ABIST_ERR_EN	Enables ABIST error detection. 1'b1: Enabled 1'b0: Disabled
4	OSC2_ERR_EN	Enables OSC period error detection. 1'b1: Enabled 1'b0: Disabled
3	BGCHK_EN	Enables detecting the bandgap (BG) voltage error. 1'b1: Enabled 1'b0: Disabled
2	GPIO_CHK_EN	Enables detecting the GPIO error. 1'b1: Enabled 1'b0: Disabled
1	I2C_CHK_EN	The VR reads back this data for comparison once it is sent to the RAM via the I^2C interface. This bit enables the device to detect the comparison error. 1'b1: Enabled 1'b0: Disabled
0	RESERVED	Reserved.

MFR_EN_COMMAND (20h)

The MFR_EN_COMMAND command enables rail A and rail B via the PMBus.

Bits	Bit Name	Description
15:2	RESERVED	Reserved.
1	EN_R2	Enables rail B via the PMBus. 1'b1: Enabled 1'b0: Disabled
0	EN_R1	Disables rail A via the PMBus. 1'b1: Enabled 1'b0: Disabled

MFR_VOUT_COMMAND_R1 (21h)

The MFR_VOUT_COMMAND_R1 command sets the rail A reference voltage VID.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	VOUT_COMMAND_R1	Sets the reference voltage VID for rail A. It is in VID format, with 2.5mV or 5mV per step. The rail A VID resolution is determined via MFR_VR_CONFIG (E4h), bit[6]. 2.5mV/step when MFR_VR_CONFIG, bit[6] = 1'b0 5mV/step when MFR_VR_CONFIG, bit[6] = 1'b1

MFR_VOUT_COMMAND_R2 (22h)

The MFR_VOUT_COMMAND_R2 command sets the rail B reference voltage VID.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	VOUT_COMMAND_R2	Sets the reference voltage VID for rail B. It is in VID format, with 2.5mV or 5mV per step. The rail B VID resolution is determined by bit[13] of MFR_VR_CONFIG (E4h), bit[13]. 2.5mV/step when MFR_VR_CONFIG, bit[13] = 1'b0 5mV/step when MFR_VR_CONFIG, bit[13] = 1'b1

MFR_VREF_DIS_FSLOW (23h)

The MFR_VREF_DIS_FSLOW command sets the V_{REF} level at which the VR can disable the PWM low frequency function.

Bits	Bit Name	Description
15:8	MFR_VREF_DIS_FSLOW_R2	Sets the V_{REF} level for rail B. At this level, the VR can disable the PWM low frequency function. Its resolution is same as the value set via MFR_VOUT_COMMAND_R2 (22h)
7:0	MFR_VREF_DIS_FSLOW_R1	Sets the V_{REF} level for rail A. At this level, the VR can disable the PWM low frequency function. Its resolution is same as the value set via MFR_VOUT_COMMAND_R1 (21h)

MFR_VOUT_TRIM_CCM1_R1 (24h)

The MFR_VOUT_TRIM_CCM1_R1 command applies a fixed offset voltage to the output voltage at different power states (1-phase to 4-phase CCM operation on rail A). It is used by the end user to trim V_{OUT} via the PMBus when the VR controller is assembled into the end user's board.

Bits	Bit Name	Description
15:12	VOUT_TRIM_4PH_R1	Applies a fixed offset voltage to the rail A output voltage in 4-phase CCM. 1.5625mV/LSB with a 2.5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b0) 3.125mV/LSB with a 5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b1)
11:8	VOUT_TRIM_3PH_R1	Applies a fixed offset voltage to the rail A output voltage in 3-phase CCM. 1.5625mV/LSB with a 2.5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b0) 3.125mV/LSB with a 5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b1)
7:4	VOUT_TRIM_2PH_R1	Applies a fixed offset voltage to the rail A output voltage in 2-phase CCM. 1.5625mV/LSB with a 2.5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b0) 3.125mV/LSB with a 5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b1)
3:0	VOUT_TRIM_1PH_R1	Applies a fixed offset voltage to the rail A output voltage in 1-phase CCM. 1.5625mV/LSB with a 2.5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b0) 3.125mV/LSB with a 5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b1)

MFR_VOUT_TRIM_CCM2_R1_DCM (25h)

The MFR_VOUT_TRIM_CCM2_R1_DCM command applies a fixed offset voltage to the output voltage at different power states (5-phase to 6-phase CCM operation on rail A, 1-phase DCM operation on rail A, and 1-phase DCM operation on rail B). It is used by the end user to trim V_{OUT} via the PMBus when the VR controller is assembled into the end user's board.

Bits	Bit Name	Description
15:12	VOUT_TRIM_DCM_R2	Applies a fixed offset voltage to the rail B output voltage in 1-phase DCM. 1.5625mV/LSB with a 2.5mV/step VID (MFR_VR_CONFIG (E4h), bit[13] = 1'b0) 3.125mV/LSB with a 5mV/step VID (MFR_VR_CONFIG (E4h), bit[13] = 1'b1)
11:8	VOUT_TRIM_DCM_R1	Applies a fixed offset voltage to the rail A output voltage in 1-phase DCM. 1.5625mV/LSB with a 2.5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b0) 3.125mV/LSB with a 5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b1)
7:4	VOUT_TRIM_6PH_R1	Applies a fixed offset voltage to the rail A output voltage in 6-phase CCM. 1.5625mV/LSB with a 2.5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b0) 3.125mV/LSB with a 5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b1)
3:0	VOUT_TRIM_5PH_R1	Applies a fixed offset voltage to the rail A output voltage in 5-phase CCM. 1.5625mV/LSB with a 2.5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b0) 3.125mV/LSB with a 5mV/step VID (MFR_VR_CONFIG (E4h), bit[6] = 1'b1)

MFR_VOUT_TRIM_CCM_R2 (26h)

The MFR_VOUT_TRIM_CCM_R2 command applies a fixed offset voltage to the output voltage at different power states (1-phase to 3-phase operation on rail B). It is used by the end user to trim V_{OUT} via the PMBus when the VR controller is assembled into the end user's board.

Bits	Bit Name	Description
15:12	RESERVED	Reserved.
11:8	VOUT_TRIM_3PH_R2	Applies a fixed offset voltage to the rail B output voltage in 3-phase DCM. 1.5625mV/LSB with a 2.5mV/step VID (MFR_VR_CONFIG (E4h), bit[13] = 1'b0) 3.125mV/LSB with a 5mV/step VID (MFR_VR_CONFIG (E4h), bit[13] = 1'b1)

7:4	VOUT_TRIM_2PH_R2	Applies a fixed offset voltage to the rail B output voltage in 2-phase DCM. 1.5625mV/LSB with a 2.5mV/step VID (MFR_VR_CONFIG (E4h), bit[13] = 1'b0) 3.125mV/LSB with a 5mV/step VID (MFR_VR_CONFIG (E4h), bit[13] = 1'b1)
3:0	VOUT_TRIM_1PH_R2	Applies a fixed offset voltage to the rail B output voltage in 1-phase CCM. 1.5625mV/LSB with a 2.5mV/step VID (MFR_VR_CONFIG (E4h), bit[13] = 1'b0) 3.125mV/LSB with a 5mV/step VID (MFR_VR_CONFIG (E4h), bit[13] = 1'b1)

MFR_ADC_HOLD_TIME (2Ah)

The MFR_ADC_HOLD_TIME command sets the analog-to-digital converter (ADC) result hold time. It also controls the switch in the slope charging loop and sets the slope discharge time.

Bits	Bit Name	Description
15:9	RESERVED	Reserved.
8:4	MFR_ADC_HOLD_ TIME	Sets the ADC result hold time. 100ns/LSB.
3	MFR_SLOPE_ LEAKAGE	Enables the device to turn off the switch in the slope charging loop when the slope is saturated during DCM. 1'b0 : Disabled 1'b1 : Enabled
2:0	SLOPE_DISCHARGE_ TIME	Sets the slope discharge time, calculated with the following equation: Slope Discharge Time = (2Ah, bits[2:0] + 1) x 10ns. 10ns/LSB.

MFR_DEBUG (2Bh)

The MFR_DEBUG command enables the delay line loop (DLL), bandgap (BG) chop clock and sigma-delta (Σ-Δ) modulation.

Bits	Bit Name	Description
15:3	RESERVED	Reserved.
2	PWM_FINE_SEL	Enables the DLL, which can increase the on time accuracy. 1'b1: Enabled 1'b0: Disabled
1	BG_CHOP	Enables the BG chop clock. 1'b1: Enabled 1'b0: Disabled
0	SDM_FRAC_EN	Enables on time calibration with Σ-Δ modulation when the current balance loop enabled. 1'b1: Enabled 1'b0: Disabled

MFR_PROTECT_PUBLIC_CFG (2Ch)

The MFR_PROTECT_PUBLIC_CFG command configures protection options related to both rail A and rail B.

Bits	Bit Name	Description
15:14	RESERVED	Reserved.
13	PHASE_OC_EN_R2	Enables the per-phase over-current protection (OCP) limit for rail B. 1'b1: Enabled 1'b0: Disabled

12	PHASE_OC_EN_R1	Enables the per-phase OCP limit for rail A. 1'b1: Enabled 1'b0: Disabled
11	SS_OC_EN_R2	Enables per-phase OC detection for rail B during soft start. 1'b1: Enabled 1'b0: Disabled
10	SS_OC_EN_R1	Enables per-phase OC detection for rail A during soft start. 1'b1: Enabled 1'b0: Disabled
9	VDD18_DRON_OFF_EN	Enables pulling down DRONA/B if an over-voltage (OV) condition occurs on VDD18. 1'b1: Enabled 1'b0: Disabled
8	VDD18_PWMOFF_EN	Enables cutting off the PWM if an OV condition occurs on VDD18. 1'b1: Enabled 1'b0: Disabled
7	VDD33_DRON_OFF_EN	Enables pulling down DRONA/B if an OV condition occurs on VDD33. 1'b1: Enabled 1'b0: Disabled
6	VDD33_PWMOFF_EN	Enables cutting off the PWM if an OV condition occurs on VDD33. 1'b1: Enabled 1'b0: Disabled
5:4	RESERVED	Reserved.
3	VIN_UVP_LATCH_EN	Sets the V_{IN} under-voltage protection (UVP) mode. 1'b0: Hiccup mode 1'b1: Latch-off mode
2	VIN_UVLO_LATCH_EN	Sets the V_{IN} under-voltage lockout (UVLO) mode. 1'b0: Hiccup mode 1'b1: Latch-off mode
1	VIN_OVP_LATCH_EN	Sets the V_{IN} over-voltage protection (OVP) mode. 1'b0: Hiccup mode 1'b1: Latch-off mode
0	VIN_PROT_EN	Enables V_{IN} protection. 1'b0: Disabled 1'b1: Enabled

MFR_APSI_CTRL (30h)

The MFR_APSI_CTRL command controls the related parameters regarding the automatic phase-shedding (APS) function.

Bits	Bit Name	Description
15:13	RESERVED	Reserved.
12	ADP_CCM_FORCE_EN_R2	If this bit is set, at least one rail B phase operates during APS, and rail B does not enter DCM. 1'b1: Force rail B CCM 1'b0: Disable this function

11	ADP_OC_EXIT_EN_R2	Enables rail B to exit APS when per-phase OCP occurs. 1'b1: Exit APS when per-phase OCP occurs 1'b0: Rail B does not exit APS when per-phase OCP occurs
10:8	PHS_DROP_ DELAYTIME_R2	Sets the phase drop delay time when rail B is in APS mode. 1 sample period/LSB.
7:5	RESERVED	Reserved.
4	ADP_CCM_FORCE_ EN_R1	If this bit is set, at least one rail A phase operates during APS, and rail A does not enter DCM. 1'b1: Force rail A CCM 1'b0: Disable this function
3	ADP_OC_EXIT_EN_R1	Enables rail A to exit APS when per-phase OCP occurs. 1'b1: Exit APS when per-phase OCP occurs 1'b0: Rail A does not exit APS when per-phase OCP occurs
2:0	PHS_DROP_ DELAYTIME_R1	Sets the phase drop delay time when rail A is in APS mode. 1 sample period/LSB.

MFR_VIN_ON_OFF (35h)

The MFR_VIN_ON_OFF command sets the V_{IN} under-voltage lockout (UVLO) rising and falling threshold.

Bits	Bit Name	Description
15:8	VIN_OFF	Sets the V_{IN} under-voltage lockout (UVLO) falling threshold, at which the VR stops power conversion. 0.1V/LSB.
7:0	VIN_ON	Sets the V_{IN} UVLO rising threshold, at which the VR starts power conversion, assuming that VDD33 is ready and EN is high. 0.1V/LSB.

MFR_VIN_UVOV_LIMIT (36h)

The MFR_VIN_UVOV_LIMIT command sets the V_{IN} over-voltage protection (OVP) threshold and the V_{IN} under-voltage protection (UVP) threshold.

Bits	Bit Name	Description
15:9	VIN_UV_FAULT_ LIMIT	Sets the V_{IN} under-voltage protection (UVP) threshold. If V_{IN} is below this value, the system cannot start up when 1Bh, bit[7] = 0. 0.1V/LSB.
8	RESERVED	Reserved.
7:0	VIN_OV_FAULT_LIMIT	Sets the V_{IN} over-voltage protection (OVP) threshold. If V_{IN} exceeds the set value, the VR latches off until power is cycled, or the VR shuts off until V_{IN} falls below the OVP threshold. 0.1V/LSB.

MFR_VBOOT_R1 (37h)

The MFR_VBOOT_R1 command sets the V_{BOOT} VID for rail A.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	MFR_VBOOT_R1	Sets the V_{BOOT} VID for rail A. It is in VID format, with 2.5mV or 5mV per step. The rail A VID resolution is determined by MFR_VR_CONFIG (E4h), bit[6]. 2.5mV/step when MFR_VR_CONFIG, bit[6] = 1'b0. 5mV/step when MFR_VR_CONFIG, bit[6] = 1'b1.

MFR_VBOOT_R2 (38h)

The MFR_VBOOT_R2 command sets the V_{BOOT} VID for rail B.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.

9:0	MFR_VBOOT_R2	Sets the V_{BOOT} VID for rail B. It is in VID format, with 2.5mV or 5mV per step. The rail B VID resolution is determined by MFR_VR_CONFIG (E4h), bit[13]. 2.5mV/step when MFR_VR_CONFIG, bit[13] = 1'b0. 5mV/step when MFR_VR_CONFIG, bit[13] = 1'b1.

MFR_4DIGIT_CODE (60h)

The MFR_4DIGIT_CODE command returns the part number's 4-digit code.

Bits	Bit Name	Description
15:0	4-DIGIT_CODE	Returns the part number's 4-digit code.

MFR_PRODUCT_ID (61h)

The MFR_PRODUCT_ID command returns the 16-bit product ID (2977 for the MPQ2977).

Bits	Bit Name	Description
15:0	MFR_PRODUCT_ID	Returns the 16-bit product ID (2977 for the MPQ2977).

MFR_PWM_MINLOW_CCM (62h)

The MFR_PWM_MINLOW_CCM command sets the minimum PWM low time in CCM, as well as the minimum time during which PWM must remain low before entering tri-state.

Bits	Bit Name	Description
15:11	RESERVED	Reserved.
10:6	MFR_PWM_MINLOW_2HIZ	Sets the minimum time during which PWM must stay low before entering tri-state. 10ns/LSB.
5:0	MFR_PWM_MINLOW_CCM	Sets the minimum PWM low time when the VR is in CCM. 10ns/LSB.

MFR_PWM_MINLOW_EXIT_HIZ (63h)

The MFR_PWM_MINLOW_EXIT_HIZ command sets the minimum PWM tri-state time, as well as the minimum time during which PWM must remain low when exiting a pre-biased state.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:5	MFR_PWM_MINHIZ	Sets the minimum PWM tri-state time. 10ns/LSB
4:0	MFR_PWM_MINLOW_EXIT_HIZ	Sets the minimum time during which PWM must stay low when exiting a pre-biased state. 10ns/LSB.

MFR_PWM_UC_ONTIME (64h)

The MFR_PWM_UC_ONTIME command sets the PWM on time and some other related parameters when per-phase under-current protection (UCP) occurs.

Bits	Bit Name	Description
15:11	RESERVED	Reserved.
10:5	MFR_PWM_UC_BLCTIME	Sets the time during which PWM stays low (from the minimum low state completion to when PWM turns high again). This only occurs when there is an under-current (UC) condition, and it is not affected by the PWM set signal. The duty cycle under a UC condition can be calculated with the following equation: Duty Cycle = MFR_PWM_UC_ONTIME / (MFR_PWM_UC_ONTIME + MFR_PWM_MINLOW_CCM + MFR_PWM_UC_BLCTIME) 10ns/LSB.
4:0	MFR_PWM_UC_ONTIME	Sets the PWM high time when UCP is triggered. 10ns/LSB.

MFR_VR_HOT_SET (68h)

The MFR_VR_HOT_SET command sets the threshold and hysteresis for VR_HOT.

Bits	Bit Name	Description
15	RESERVED	Reserved.
14:7	VR_HOT_THD	Sets the threshold for VR_HOT. 1°C/LSB.
6:0	VR_HOT_HYS	Sets the hysteresis value for the VR_HOT threshold. 1°C/LSB.

MFR_IOUT_ALERT_SET (69h)

The MFR_IOUT_ALERT_SET command sets the threshold for the I_{OUT} alert for rail A and rail B.

Bits	Bit Name	Description
15:8	IOUT_ALERT_THD_R2	Sets the I_{OUT} alert threshold for rail B. 1A/LSB.
7:0	IOUT_ALERT_THD_R1	Sets the I_{OUT} alert threshold for rail A. 1A/LSB.

MFR_TSW_FS_HYS (6Ah)

The MFR_TSW_FS_HYS command sets the hysteresis area of the frequency loop. The FS loop is held within this area.

Bits	Bit Name	Description
15:4	RESERVED	Reserved.
3:0	VALUE	Sets the hysteresis area for the frequency loop, in which the FS loop is held. 40ns/LSB.

MFR_TPROG (6Bh)

The MFR_TPROG command sets the configuration time to store one byte to the MTP. The valid range is between 2ms and 3.5ms. 0.1ms/LSB.

Bits	Bit Name	Description
15:6	RESERVED	Reserved.
5:0	VALUE	Sets the configuration time to store one byte to the MTP. The valid range is between 2ms and 3.5ms. 0.1ms/LSB.

READ_VCOMP (74h)

The READ_VCOMP command returns the V_{COMP} value for rail A and rail B.

Bits	Bit Name	Description
15:8	VALUE_R2	Returns the V_{O_COMP} value of rail B. 1.25mV or 0.9375mV, depending on the V_{O_COMP} DAC reference voltage (320mV or 240mV).
7:0	VALUE_R1	Returns the V_{O_COMP} value of rail A. 1.25mV or 0.9375mV, depending on the V_{O_COMP} DAC reference voltage (320mV or 240mV).

READ_PMBUS_ADDR (75h)

The READ_PMBUS_ADDR command returns the PMBus address.

Bits	Bit Name	Description
15:7	RESERVED	Reserved.
6:0	VALUE	Returns the PMBus address.

READ_CS1 (76h)

The READ_CS1 command returns the CS1 voltage.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	VALUE	Returns the CS1 voltage. 3.125mV/LSB.

READ_CS2 (77h)

The READ_CS2 command returns the CS2 voltage.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	VALUE	Returns the CS2 voltage. 3.125mV/LSB.

READ_CS3 (78h)

The READ_CS3 command returns the CS3 voltage.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	VALUE	Returns the CS3 voltage. 3.125mV/LSB.

READ_CS4 (79h)

The READ_CS4 command returns the CS4 voltage.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	VALUE	Returns the CS4 voltage. 3.125mV/LSB.

READ_VIN (7Ah)

The READ_VIN command returns the V_{IN} value.

Bits	Bit Name	Description
15:8	RESERVED	Reserved.
7:0	VALUE	Returns the V_{IN} value. 100mV/LSB.

READ_VOUT_R1 (7Bh)

The READ_VOUT_R1 command returns the V_{OUT} value for rail A.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	VALUE	Returns the V_{OUT} sample value for rail A. 1.5625mV/LSB.

READ_VOUT_R2 (7Ch)

The READ_VOUT_R2 command returns the V_{OUT} value for rail B.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	VALUE	Returns the V_{OUT} sample value for rail B. 1.5625mV/LSB.

READ_VFB_R1 (7Dh)

The READ_VFB_R1 command returns the V_{FB} sample value for rail A.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	VALUE	Returns the V_{FB} sample value for rail A. 1.5625mV/LSB.

READ_VFB_R2 (7Fh)

The READ_VFB_R2 command returns the V_{FB} sample value for rail B.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	VALUE	Returns the V_{FB} sample value for rail B. 1.5625mV/LSB.

READ_IMON_R1 (80h)

The READ_IMON_R1 command returns the IMON value for rail A.

Bits	Bit Name	Description
15:9	RESERVED	Reserved.
8:0	VALUE	Returns the IMON value for rail A. 1A/LSB.

READ_IMON_R2 (81h)

The READ_IMON_R2 command returns the IMON value for rail B.

Bits	Bit Name	Description
15:9	RESERVED	Reserved.
8:0	VALUE	Returns the IMON value for rail B. 1A/LSB.

READ_TEMP_R1 (82h)

The READ_TEMP_R1 command returns the rail A temperature.

Bits	Bit Name	Description
15:8	RESERVED	Reserved.
7:0	VALUE	Returns the rail A temperature. 1°C/LSB.

READ_TEMP_R2 (84h)

The READ_TEMP_R2 command returns the temperature of Rail B.

Bits	Bit Name	Description
15:8	RESERVED	Reserved.
7:0	VALUE	Returns the rail B temperature. 1°C/LSB.

READ_CS5 (85h)

The READ_CS5 command returns the CS5 voltage.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	VALUE	Returns the CS5 voltage. 3.125mV/LSB.

READ_CS6 (86h)

The READ_CS6 command returns the CS6 voltage.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	VALUE	Returns the CS6 voltage. 3.125mV/LSB.

MFR_PROTECT_CFG (90h)

The MFR_PROTECT_CFG command sets options for different protection cases.

Bits	Bit Name	Description
15	TEMP_FAULT_EN	Enables temperature fault detection. 1’b0: Disabled 1’b1: Enabled
14	PROTECT_ ACCESS_R1TOR2	If this bit is set, rail B also enters a protection mode when rail A enters a protection mode. 1’b1: Enabled 1’b0: Disabled
13	PROTECT_ ACCESS_R2TOR1	If this bit is set, rail A also enters a protection mode when rail B enters a protection mode. 1’b1: Enabled 1’b0: Disabled
12	UCP_EN	Enables per-phase under-current protection (UCP). 1’b0: Disabled 1’b1: Enabled
11	OTP_LATCH_EN	Sets the over-temperature protection (OTP) mode. 1’b0: Hiccup mode 1’b1: Latch-off mode
10	OTP_EN	Enables OTP. 1’b1: Enabled 1’b0: Disabled
9:8	UVP2_SET_MODE	Sets the tracking under-voltage protection (UVP2) mode. 2’b00: No action 2’b01: Latch-off mode 2’b10: Hiccup mode
7	UVP1_LATCH_EN	Sets the fixed under-voltage protection (UVP1) mode. 1’b0: Hiccup mode 1’b1: Latch-off mode
6	UVP1_EN	Enables UVP1. 1’b0: Disabled 1’b1: Enabled
5:4	OVP2_SET_MODE	Sets the tracking over-voltage protection (OVP2) mode. 2’b00: No action 2’b01: Latch-off mode 2’b10: Hiccup mode
3	OVP1_LATCH_EN	Sets the absolute over-voltage protection (OVP1) mode. 1’b0: Hiccup mode 1’b1: Latch-off mode

2	OVP1_EN	Enables OVP1. 1'b0: Disabled 1'b1: Enabled
1:0	OCP_SET_MODE	Sets the IMON over-current protection (OCP) mode. 2'b00: No action 2'b01: Latch-off mode 2'b10: Hiccup mode

MFR_OVUV_DELAYTIME (91h)

The MFR_OVUV_DELAYTIME command sets the delay time for tracking over-voltage protection (OVP2) and under-voltage protection (UVP2).

Bits	Bit Name	Description
15:12	RESERVED	Reserved.
11:6	OVP2_SET_DELAYTIME	Sets the delay time for tracking over-voltage protection (OVP2). If an OV condition remains for this set time, the VR initiates OVP2. 100ns/LSB.
5:0	UVP2_SET_DELAYTIME	Sets the delay time for tracking under-voltage protection (UVP2). If the UV condition remains for this time, the VR initiates UVP2. 20μs/LSB.

MFR_OCP_DELAYTIME (92h)

The MFR_OCP_DELAYTIME command sets the delay time for total over-current protection (OCP).

Bits	Bit Name	Description
15:6	RESERVED	Reserved.
5:0	OCP_SET_DELAYTIME	Sets the total over-current protection (OCP) delay time. If the OC condition remains for this time, the VR initiates total OCP. 20μs/LSB.

MFR_OVUV_SET_R1 (93h)

The MFR_OVUV_SET_R1 command sets the rail A thresholds for UVP2 and OVP2.

Bits	Bit Name	Description
15:13	RESERVED	Reserved.
12	VOLTAGE_STEP_ DIVIDER	Divides all voltage steps by 2 (including the trim). 1'b1: Enabled 1'b0: Disabled
11:6	RESERVED	Reserved.

5:3	UV2_SET_R1	Sets the UVP2 threshold for rail A. 3'b000: UVP = VID - 50mV 3'b001: UVP = VID - 100mV 3'b010: UVP = VID - 150mV 3'b011: UVP = VID - 200mV 3'b100: UVP = VID - 250mV 3'b101: UVP = VID - 300mV 3'b110: UVP = VID - 350mV 3'b111: UVP = VID - 400mV
2:0	OV2_SET_R1	Sets the OVP2 threshold for rail A. 3'b000: OVP = VID + 50mV 3'b001: OVP = VID + 100mV 3'b010: OVP = VID + 150mV 3'b011: OVP = VID + 200mV 3'b100: OVP = VID + 250mV 3'b101: OVP = VID + 300mV 3'b110: OVP = VID + 350mV 3'b111: OVP = VID + 400mV

MFR_OVUV_SET_R2 (94h)

The MFR_OVUV_SET_R2 command sets the rail B thresholds for UVP2 and OVP2.

Bits	Bit Name	Description
15:13	RESERVED	Reserved.
12	VOLTAGE_STEP_ DIVIDER	Divides all voltage steps by 2 (including trim). 1'b1: Enabled 1'b0: Disabled
11:6	RESERVED	Reserved.

5:3	UV2_SET_R2	Sets the UVP2 threshold for rail B. 3'b000: UVP = VID - 50mV 3'b001: UVP = VID - 100mV 3'b010: UVP = VID - 150mV 3'b011: UVP = VID - 200mV 3'b100: UVP = VID - 250mV 3'b101: UVP = VID - 300mV 3'b110: UVP = VID - 350mV 3'b111: UVP = VID - 400mV
2:0	OV2_SET_R2	Sets the OVP2 threshold for rail B. 3'b000: OVP = VID + 50mV 3'b001: OVP = VID + 100mV 3'b010: OVP = VID + 150mV 3'b011: OVP = VID + 200mV 3'b100: OVP = VID + 250mV 3'b101: OVP = VID + 300mV 3'b110: OVP = VID + 350mV 3'b111: OVP = VID + 400mV

MFR_OVP_DA_SET (95h)

The MFR_OVP_DA_SET command sets the over-voltage protection (OVP) threshold for both rails.

Bits	Bit Name	Description
15:8	MFR_OVP_DA_SET_R2	Sets the over-voltage protection (OVP) threshold for rail B. 10mV/LSB.
7:0	MFR_OVP_DA_SET_R1	Sets the OVP threshold for rail A. 10mV/LSB.

MFR_UVP_DA_SET (96h)

The MFR_UVP_DA_SET command sets the under-voltage protection (UVP) threshold for both rails.

Bits	Bit Name	Description
15:8	MFR_UVP_DA_SET_R2	Sets the under-voltage protection (UVP) threshold for rail B. 10mV/LSB.
7:0	MFR_UVP_DA_SET_R1	Sets the UVP threshold for rail A. 10mV/LSB.

MFR_OCP_DA_SET (97h)

The MFR_OCP_DA_SET command sets the over-current protection (OCP) threshold for both rails.

Bits	Bit Name	Description
15:8	MFR_OCP_DA_SET_R2	Sets the per-phase over-current protection (OCP) threshold for rail B. Ranges between 1.24V and 2.56V. 5mV/LSB.
7:0	MFR_OCP_DA_SET_R1	Sets the per-phase OCP threshold for rail A. Ranges between 1.24V and 2.56V. 5mV/LSB.

MFR_IMONOCP_SET (98h)

The MFR_IMONOCP_SET command sets the total over-current protection (OCP) limit.

Bits	Bit Name	Description
15:14	RESERVED	Reserved.
13:7	MFR_IMONOCP_SET_R2	Sets the rail B total current limit level, calculated with the following equation: Total Current Limit = 98h, bits[13:7] x Phase Number 1A/LSB.
6:0	MFR_IMONOCP_SET_R1	Sets the rail A total current limit level, calculated with the following equation: Total Current Limit = 98h, bits[6:0] x Phase Number 1A/LSB.

MFR_UCP_DA_SET (99h)

The MFR_UCP_DA_SET command set the under-current protection (UCP) threshold for both rails.

Bits	Bit Name	Description
15:8	MFR_UCP_DA_SET_R2	Sets the per-phase under-current protection (UCP) threshold for rail B. Ranges between 0V and 1.24V. 5mV/LSB.
7:0	MFR_UCP_DA_SET_R1	Sets the per-phase UCP threshold for rail A. Ranges between 0V and 1.24V. 5mV/LSB.

MFR_GPIO_SEL (9Ch)

The MFR_GPIO_SEL command sets the GPIO driving strength and determines whether the GPIO output belongs to rail A or rail B.

Bits	Bit Name	Description
15:13	RESERVED	Reserved.
12	GPIO_DRIVE_ STRENGTH	Increases the GPIO drive strength. 1’b1: Enabled 1’b0: Disabled
11:10	VR_HOT_SEL	Selects rail A, rail B, or both for VR_HOT_SEL. 2’b00: Rail A 2’b01: Rail B 2’b1x: Both rails
9:8	RESERVED	Reserved.
7:6	RESERVED	Reserved.
5:4	ALERT_SEL	Selects rail A, rail B, or both for ALERT_SEL. 2’b00: Rail A 2’b01: Rail B 2’b1x: Both rails
3:2	VRRDY_SEL	Selects rail A, rail B, or both for VRRDY_SEL. 2’b00: Rail A 2’b01: Rail B 2’b1x: Both rails
1:0	FAULT_SEL	Selects rail A, rail B, or both for FAULT. 2’b00: Rail A 2’b01: Rail B 2’b1x: Both rails

MFR_TEMP_GAIN (9Eh)

The MFR_TEMP_GAIN command sets the temperature gain for rail A and rail B.

Bits	Bit Name	Description
15:8	MFR_TEMPB_GAIN	Sets the temperature gain for rail B, calculated with the following equation: $T_J = (V_{TEMP} - 600mV) / 8mV/°C = V_{SENSE\_TEMP} \times 1.6 / 1024 / 8mV/°C - 75°C$ $= (V_{SENSE\_TEMP} \times MFR\_TEMP\_GAIN / 256 - MFR\_TEMP\_OFFSET)°C$ $MFR\_TEMP\_GAIN = 1.6 \times 256 / 0.008 / 1024 = 50$ The default value is 50.
7:0	MFR_TEMPA_GAIN	Sets the temperature gain for rail A, calculated with the following equation: $T_J = (V_{TEMP} - 600mV) / 8mV/°C = V_{SENSE\_TEMP} \times 1.6 / 1024 / 8mV/°C - 75°C$ $= (V_{SENSE\_TEMP} \times MFR\_TEMP\_GAIN / 256 - MFR\_TEMP\_OFFSET)°C$ $MFR\_TEMP\_GAIN = 1.6 \times 256 / 0.008 / 1024 = 50$ The default value is 50.

MFR_TEMP_OFFSET (9Fh)

The MFR_TEMP_OFFSET command sets the temperature offset for rail A and rail B.

Bits	Bit Name	Description
15:8	MFR_TEMPB_OFFSET	Calculates the rail B temperature, calculated with the following equation: $T_J = (V_{TEMP} - 600mV) / 8mV/°C = V_{SENSE\_TEMP} \times 1.6 / 1024 / 8mV/°C - 75°C$ $= (V_{SENSE\_TEMP} \times MFR\_TEMP\_GAIN / 256 - MFR\_TEMP\_OFFSET)°C$ The default value is -75.
7:0	MFR_TEMPA_OFFSET	Calculates the rail A temperature, calculated with the following equation: $T_J = (V_{TEMP} - 600mV) / 8mV/°C = V_{SENSE\_TEMP} \times 1.6 / 1024 / 8mV/°C - 75°C$ $= (V_{SENSE\_TEMP} \times MFR\_TEMP\_GAIN / 256 - MFR\_TEMP\_OFFSET)°C$ The default value is -75.

MFR_IDRP_SET_R1 (A0h)

The MFR_IDRP_SET_R1 command sets the DC droop, AC droop, and related parameters for rail A.

Bits	Bit Name	Description
15	IDRP_DC_SET_R1_BIT3	Enables I_{DROOP} for rail A's DC droop. 1'b1: Enabled 1'b0: Disabled
14	IDRP_DC_SET_R1_BIT2	Reduces the bandwidth (BW) for rail A. 1'b1: Enabled 1'b0: Disabled
13	IDRP_DC_SET_R1_BIT1	Enables reducing the bias current (reduce BW) for rail A. 1'b1: Enabled 1'b0: Disabled
12	IDRP_DC_SET_R1_BIT0	Enables increasing the compensation cap (reduce BW) for rail A. 1'b1: Enabled 1'b0: Disabled
11:8	RDRP_AC_SET_R1	Sets R_{DRP_AC} for rail A. 100Ω/LSB.

7	N_INPUT_FILTER_ SPEED_SEL_R1	Sets the negative input of the internal error amplifier for the error amplifier (n-input side) filter speed. 1'b0: Select the fast filter 1'b1: Select the slow filter
6:4	N_INPUT_FILTER_R1	Sets the n-input side filter time. If selecting the fast filter (A0h, bit[7] = 1'b0): tau = 20ns x (7 - A0h, bits[6:4]) If selecting the slow filter (A0h, bit[7] = 1'b1): tau = 4μs x (7 - A0h, bits[6:4])
3	P_INPUT_FILTER_ SPEED_SEL_R1	Sets the positive input of the internal error amplifier for the error amplifier (p-input side) filter speed. 1'b0: Select fast filter 1'b1: Select slow filter
2:0	P_INPUT_FILTER_R1	Sets the p-input side filter time. If selecting the fast filter (A0h, bit[3] = 1'b0): tau = 20ns x (7 - A0h, bits[2:0]) If selecting the slow filter (A0h, bit[3] = 1'b1): tau = 4μs x (7 - A0h, bits[2:0])

MFR_IDRP_SET_R2 (A1h)

The MFR_IDRP_SET_R2 command sets the DC droop, AC droop, and related parameters for rail B.

Bits	Bit Name	Description
15	IDRP_DC_SET_R2_BIT3	Enables I_{DROOP} for rail B's DC droop. 1'b1: Enabled 1'b0: Disabled
14	IDRP_DC_SET_R2_BIT2	Reduces the bandwidth (BW) for rail B. 1'b1: Enabled 1'b0: Disabled
13	IDRP_DC_SET_R2_BIT1	Enables reducing the bias current (reduce BW) for rail B. 1'b1: Enabled 1'b0: Disabled
12	IDRP_DC_SET_R2_BIT0	Enables increasing the compensation cap (reduce BW) for rail B. 1'b1: Enabled 1'b0: Disabled
11:8	RDRP_AC_SET_R2	Sets R_{DRP_AC} for rail B. 100Ω/LSB.
7	N_INPUT_FILTER_ SPEED_SEL_R2	Sets the n-input side filter speed. 1'b0: Select the fast filter 1'b1: Select the slow filter
6:4	N_INPUT_FILTER_R2	Sets the n-input side filter time. If selecting the fast filter (A0h, bit[7] = 1'b0): tau = 20ns x (7 - A1h, bits[6:4]) If selecting the slow filter (A0h, bit[7] = 1'b1): tau = 4μs x (7 - A1h, bits[6:4])
3	P_INPUT_FILTER_ SPEED_SEL_R2	Sets the p-input side filter speed. 1'b0: Select the fast filter 1'b1: Select the slow filter
2:0	P_INPUT_FILTER_R2	Sets the p-input side filter time. If selecting the fast filter (A0h, bit[3] = 1'b0): tau = 20ns x (7 - A1h, bits[2:0]) If selecting the filter (A0h, bit[3] = 1'b1): tau = 4μs x (7 - A1h, bits[2:0])

MFR_RDRP_AC_RST (A2h)

The MFR_RDRP_AC_RST command resets the AC filter and sets R_{DROOP}.

Bits	Bit Name	Description
15	IDRP_AC_RST_R2	Resets the AC filter for rail B. 1'b1: Reset 1'b0: No action
14	IDRP_AC_RST_R1	Resets the AC filter for rail A. 1'b1: Reset 1'b0: No action
13	SHORT_FIRST_ HALF_RES_R2	Shorts the first half of resistors on rail B. 1'b1: Enabled 1'b0: Disabled
12:7	RDRP2_SET	Sets R_{DROOP} for V_{FB} compensation for rail B. 50Ω/LSB.
6	SHORT_FIRST_ HALF_RES_R1	Shorts the first half of resistors on rail A. 1'b1: Enabled 1'b0: Disabled
5:0	RDRP1_SET	Sets R_{DROOP} for V_{FB} compensation for rail A. 50Ω/LSB.

MFR_RVP_SET (A3h)

The MFR_RVP_SET command sets the threshold for reverse-voltage protection (RVP) and the droop current mirror gain.

Bits	Bit Name	Description
15:11	RESERVED	Reserved.
10:9	MFR_DRON_HIZ_SEL	Sets DRONA and DRONB to Hi-Z when the DrMOS must enter low-power mode (LPM). MFR_DRON_HIZ_SEL, bit[10] is for rail B, while MFR_DRON_HIZ_SEL, bit[9] is for rail A. 1'b1: Enabled 1'b0: Disabled
8	IDRP2_CURRENT_ MIRROR_HEADROOM	Sets the current mirror headroom for rail B's I_{DROOP}. 1'b1: Low VID value (0.25V) 1'b0: Normal VID value
7:6	IDRP2_SET	Sets the first current mirror ratio for rail B's I_{DROOP}. 2'b00: 1/16 2'b01: 1/8 2'b10: 1/4 2'b11: 1/2
5	IDRP1_CURRENT_ MIRROR_HEADROOM	Sets the current mirror headroom for rail A's I_{DROOP}. 1'b1: Low VID value (0.25V) 1'b0: Normal VID value
4:3	IDRP1_SET	Sets the first current mirror ratio for rail A's I_{DROOP}. 2'b00: 1/16 2'b01: 1/8 2'b10: 1/4 2'b11: 1/2
2	RESERVED	Reserved.

1:0	MFR_RVP_SET	Sets the reverse-voltage protection (RVP) threshold. Bit[1] is for rail B, while bit[0] is for rail A. 1'b1: 160mV 1'b0: 80mV

MFR_I2C_VTH_SEL (A4h)

The MFR_I2C_VTH_SEL command sets the I²C threshold, selects the reference voltage of V_{O_COMP} DAC, and enables the comparator hysteresis.

Bits	Bit Name	Description
15	COMPDAC_HI_SET	Choose the reference voltage for the V_{O_COMP} DAC. 1'b1: 320mV 1'b0: 240mV
14	HYST_EN	Enables the comparator hysteresis. 1'b1: Enabled 1'b0: Disabled
13:10	PMB_VTH_TRIM	Trim for the I²C threshold.
9:8	MFR_I2C_VTH_SEL	Selects a different voltage for the I²C threshold. 2'b00: 3.3V I²C interface; ViH = 1.8V, ViL = 1.01V 2'b01: 1.8V I²C interface; ViH = 1.12V, ViL = 0.56V 2'b10: 1.2V I²C interface; ViH = 0.788V, ViL = 0.45V 2'b11: I²C threshold is configurable. The higher threshold is set by bits[7:4] of this command, the lower threshold is set by bits[3:0] of this command
7:0	PMB_VTH_DAC	Sets the configurable I²C threshold. Bits[7:4] set the high threshold, while bits[3:0] set the low threshold. V_{DAC} can be calculated with the following equation: V_{DAC} = (bits[3:0] of this command + 1) x 1800 / 16mV

MFR_BGCHK_H_MAX (ACh)

The MFR_BHCHK_H_MAX command sets the maximum bandgap voltage from the analog side (V_BGCHK_H). If the ADC result of V_BGCHK_H exceeds this value (and 1Eh, bit[3] is set), a BGCHK_ERR can be reported.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	BGCHK_H_MAX	Sets the maximum level for V_BGCHK_H. 1.5625mV/LSB.

MFR_BGCHK_H_MIN (ADh)

The command MFR_BHCHK_H_MIN command sets the minimum level of V_BGCHK_H. If the ADC result of V_BGCHK_H is below this value (and 1Eh, bit[3] is set), a BGCHK_ERR can be reported.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	BGCHK_H_MIN	Sets the minimum level of V_BGCHK_H. 1.5625mV/LSB.

MFR_BGCHK_L_MAX (AEh)

The MFR_BHCHK_L_MAX command sets the maximum level of the bandgap voltage from the analog side (V_BGCHK_L). If the ADC result of V_BGCHK_L exceeds this value (and 1Eh, bit[3] is set), a BGCHK_ERR can be reported.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	BGCHK_L_MAX	Sets the maximum level for V_BGCHK_L. 1.5625mV/LSB.

MFR_BGCHK_L_MIN (AFh)

The MFR_BHCHK_L_MIN command sets the minimum level of V_BGCHK_L voltage. If the ADC result of V_BGCHK_L is below this value (and 1Eh, bit[3] is set), a BGCHK_ERR can be reported.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:0	BGCHK_L_MIN	Sets the minimum level for V_BGCHK_L. 1.5625mV/LSB.

MFR_PASSWORD_INPUT (B0h)

The MFR_PASSWORD_INPUT command returns the password input.

Bits	Bit Name	Description
15:8	RESERVED	Reserved.
7:0	PASSWORD	Returns the password input. If this value does not match the value in F9h, bits[7:0], the PMBus write access is forbidden.

MFR_1PH_R1 (B1h)

The MFR_1PH_R1 command sets the phase-shedding threshold and hysteresis for rail A.

Bits	Bit Name	Description
15:9	RESERVED	Reserved.
8:4	MFR_1PH_R1	Sets the phase-shedding threshold from 2-phase CCM to 1-phase CCM. 1A/LSB.
3:0	MFR_PHASE_HYS_R1	Sets the current hysteresis value of APS. 1A/LSB.

MFR_1PH_R2 (B2h)

The MFR_1PH_R2 command sets the phase-shedding threshold and hysteresis for rail B.

Bits	Bit Name	Description
15:9	RESERVED	Reserved.
8:4	MFR_1PH_R2	Sets the phase-shedding threshold from 2-phase CCM to 1-phase CCM. 1A/LSB.
3:0	MFR_PHASE_HYS_R2	Sets the current hysteresis value of APS. 1A/LSB.

MFR_PSI_TRIM_CCM1_R1 (C0h)

The MFR_PSI_TRIM_CCM1_R1 command sets an initial value to trim the rail A output voltage in 1-phase, 2-phase, or 3-phase CCM.

Bits	Bit Name	Description
15	RESERVED	Reserved.

14:10	MFR_PSI_TRIM_3PH_R1	Sets an initial value to trim the rail A output voltage for 3-phase CCM operation. 7.5mV/LSB when setting the V_{COMP} DAC reference voltage to 240mV (Reg A4h, bit[15] = 0). 10mV/LSB when setting the V_{COMP} DAC reference voltage to 320mV (Reg A4h, bit[15] = 1).
9:5	MFR_PSI_TRIM_2PH_R1	Sets an initial value to trim the rail A output voltage for 2-phase CCM operation. 7.5mV/LSB when setting the V_{COMP} DAC reference voltage to 240mV (Reg A4h, bit[15] = 0). 10mV/LSB when setting the V_{COMP} DAC reference voltage to 320mV (Reg A4h, bit[15] = 1).
4:0	MFR_PSI_TRIM_1PH_R1	Sets an initial value to trim the rail A output voltage for 1-phase CCM operation. 7.5mV/LSB when setting the V_{COMP} DAC reference voltage to 240mV (Reg A4h, bit[15] = 0). 10mV/LSB when setting the V_{COMP} DAC reference voltage to 320mV (Reg A4h, bit[15] = 1).

MFR_PSI_TRIM_CCM2_R1(C1h)

The MFR_PSI_TRIM_CCM2_R1 command sets an initial value to trim the rail A output voltage in 4-phase, 5-phase, or 6-phase CCM.

Bits	Bit Name	Description
15	RESERVED	Reserved.
14:10	MFR_PSI_TRIM_6PH_R1	Sets an initial value to trim the rail A output voltage for 6-phase CCM operation 7.5mV/LSB when setting the V_{COMP} DAC reference voltage to 240mV (Reg A4h, bit[15] = 0). 10mV/LSB when setting the V_{COMP} DAC reference voltage to 320mV (Reg A4h, bit[15] = 1).
9:5	MFR_PSI_TRIM_5PH_R1	Sets an initial value to trim the rail A output voltage for 5-phase CCM operation 7.5mV/LSB when setting the V_{COMP} DAC reference voltage to 240mV (Reg A4h, bit[15] = 0). 10mV/LSB when setting the V_{COMP} DAC reference voltage to 320mV (Reg A4h, bit[15] = 1).
4:0	MFR_PSI_TRIM_4PH_R1	Sets an initial value to trim the rail A output voltage for 4-phase CCM operation 7.5mV/LSB when setting the V_{COMP} DAC reference voltage to 240mV (Reg A4h, bit[15] = 0). 10mV/LSB when setting the V_{COMP} DAC reference voltage to 320mV (Reg A4h, bit[15] = 1).

MFR_PSI_TRIM_CCM_R2 (C2h)

The MFR_PSI_TRIM_CCM_R2 command sets an initial value to trim the rail B output voltage in 1-phase, 2-phase, or 3-phase CCM.

Bits	Bit Name	Description
15	RESERVED	Reserved.
14:10	MFR_PSI_TRIM_3PH_R2	Sets an initial value to trim the rail B output voltage for 3-phase CCM operation 7.5mV/LSB when setting the V_{COMP} DAC reference voltage to 240mV (Reg A4h, bit[15] = 0). 10mV/LSB when setting the V_{COMP} DAC reference voltage to 320mV (Reg A4h, bit[15] = 1).

9:5	MFR_PSI_TRIM_2PH_R2	Sets an initial value to trim the rail B output voltage for 2-phase CCM operation 7.5mV/LSB when setting the V_{COMP} DAC reference voltage to 240mV (Reg A4h, bit[15] = 0). 10mV/LSB when setting the V_{COMP} DAC reference voltage to 320mV (Reg A4h ,bit[15] = 1).
4:0	MFR_PSI_TRIM_1PH_R2	Sets an initial value to trim the rail B output voltage for 1-phase CCM operation 7.5mV/LSB when setting the V_{COMP} DAC reference voltage to 240mV (Reg A4h, bit[15] = 0). 10mV/LSB when setting the V_{COMP} DAC reference voltage to 320mV (Reg A4h, bit[15] = 1).

MFR_PSI_TRIM_DCM (C3h)

The MFR_PSI_TRIM_DCM command sets an initial value to trim the rail A and rail B output voltages in the DCM power state.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:5	MFR_PSI_TRIM_DCM_R2	Sets an initial value to trim the rail B output voltage for 1-phase DCM operation 7.5mV/LSB when setting the V_{COMP} DAC reference voltage to 240mV (Reg A4h, bit[15] = 0). 10mV/LSB when setting the V_{COMP} DAC reference voltage to 320mV (Reg A4h, bit[15] = 1).
4:0	MFR_PSI_TRIM_DCM_R1	Sets an initial value to trim the rail A output voltage for 1-phase DCM operation 7.5mV/LSB when setting the V_{COMP} DAC reference voltage to 240mV (Reg A4h, bit[15] = 0). 10mV/LSB when setting the V_{COMP} DAC reference voltage to 320mV (Reg A4h, bit[15] = 1).

MFR_PHASE_CFG (CAh)

The MFR_PHASE_CFG command sets the initial phase number for the VR.

Bits	Bit Name	Description
15:4	RESERVED	Reserved.
3:0	MFR_PHASE_CFG	Sets the phase number and whether they belong to rail A or rail B. 4’b0000: Rail A: phases 1–6; rail B: no phase 4’b0001: Rail A: phases 1–5; rail B: no phase 4’b0010: Rail A: phases 1–5; rail B: phase 6 4’b0011: Rail A: phases 1–4; rail B: no phase 4’b0100: Rail A: phases 1–4; rail B: phase 6 4’b0101: Rail A: phases 1–4; rail B: phases 5–6 4’b0110: Rail A: phases 1–3; rail B: no phase 4’b0111: Rail A: phases 1–3; rail B: phase 6 4’b1000: Rail A: phases 1–3; rail B: phase 5–6 4’b1001: Rail A: phases 1–3; rail B: phases 4–6 4’b1010: Rail A: phases 1–2; rail B: no phase 4’b1011: Rail A: phases 1–2; rail B: phase 6 4’b1100: Rail A: phases 1–2; rail B: phases 5–6 4’b1101: Rail A: phase 1; rail B: no phase 4’b1110: Rail A: phase 1; rail B: phase 6 Others: Rail A: no phase; rail B: no phase

MFR_DYNAMIC_CTRL_R1 (CBh)

The MFE_DYNAMIC_CTRL_R1 command sets the hold conditions for the DC loop, current balance, and automatic phase-shedding (APS) under different dynamic cases.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:7	DCAL_ISHR_HOLD_ DELAYTIME	Sets the hold time for rail A's DC loop and current balance loop. 1 sample period/LSB.
6:5	DCAL_ISHR_HOLD_EN	Enables holding rail A's DC loop and current balance loop during load transitions and DVID. DCAL_ISHR_HOLD_EN[1]: 1'b0: The DC loop and current balance loop keep running when DVID occurs 1'b1: Hold the DC loop and current balance loop when DVID occurs DCAL_ISHR_HOLD_EN[0]: 1'b0: The DC loop and current balance loop keep running when load transitions occur 1'b1: Hold the DC loop and current balance loop when load transitions occur
4:2	APS_HOLD_DELAYTIME	These bits set the hold time for rail A's APS. 1 sample period/LSB.
1:0	APS_HOLD_EN	Enables holding rail A's APS function during load transitions and DVID. APS_HOLD_EN[1]: 1'b0: APS keeps running when DVID occurs 1'b1: Hold APS when DVID occurs APS_HOLD_EN[0]: 1'b0: APS keeps running when load transitions occur 1'b1: Hold APS when load transitions occur

MFR_DYNAMIC_CTRL_R2 (CCh)

The MFE_DYNAMIC_CTRL_R2 command sets the hold conditions for the DC loop, current balance, and automatic phase-shedding (APS) under different dynamic cases.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:7	DCAL_ISHR_HOLD_ DELAYTIME	Sets the hold time for rail B's DC loop and current balance loop. 1 sample period/LSB.
6:5	DCAL_ISHR_HOLD_EN	Enables holding rail B's DC loop and current balance loop during load transitions and DVID. DCAL_ISHR_HOLD_EN[1]: 1'b0: The DC loop and current balance loop keep running when DVID occurs 1'b1: Hold the DC loop and current balance loop when DVID occurs DCAL_ISHR_HOLD_EN[0]: 1'b0: The DC loop and current balance loop keep running when load transitions occur 1'b1: Hold the DC loop and current balance loop when load transitions occur
4:2	APS_HOLD_DELAYTIME	These bits set the hold time for rail B's APS. 1 sample period/LSB.

1:0	APS_HOLD_EN	Enables holding rail B's APS function during load transitions and DVID. APS_HOLD_EN[1]: 1'b0: APS keeps running when DVID occurs 1'b1: Hold APS when DVID occurs APS_HOLD_EN[0]: 1'b0: APS keeps running when load transitions occur 1'b1: Hold APS when load transitions occur

MFR_SW_HF_SET (CDh)

The MFR_SW_HF_SET command sets the parameters related to high-frequency detection.

Bits	Bit Name	Description
15	HIGH_FREQ_ DETECT_EN_R2	Enables rail B's switching frequency detection if the real-time switching frequency exceeds the high-frequency threshold. 1'b0: Disabled 1'b1: Enabled
14:8	MFR_SW_HF_SET_R2	Sets rail B's high frequency threshold period, which should exceed the switching frequency. 20ns/LSB.
7	HIGH_FREQ_ DETECT_EN_R1	Enables rail A's switching frequency detection if the real-time switching frequency exceeds the high-frequency threshold. 1'b0: Disabled 1'b1: Enabled
6:0	MFR_SW_HF_SET_R1	Sets rail A's high frequency threshold period, which should exceed the switching frequency. 20ns/LSB.

MFR_SW_LF_SET (CEh)

The MFR_SW_LF_SET command sets the parameters related to low-frequency detection.

Bits	Bit Name	Description
15	LOW_FREQ_ DETECT_EN_R2	Enables rail B's switching frequency detection if the frequency is below the low-frequency threshold. 1'b0: Disabled 1'b1: Enabled
14:8	SW_LF_SET_R2	Sets rail B's low-frequency threshold, which should be below the switching frequency. 80ns/LSB.
7	LOW_FREQ_ DETECT_EN_R1	Enables rail A's switching frequency detection if the frequency is below the low frequency threshold. 1'b0: Disabled 1'b1: Enabled
6:0	SW_LF_SET_R1	Sets rail A's low-frequency threshold, which should be below the switching frequency. 80ns/LSB.

MFR_MIN_ONTIME (CFh)

The MFR_MIN_ONTIME command sets the minimum on time and blank time.

Bits	Bit Name	Description
15:11	RESERVED	Reserved.
10:6	MFR_BLANK_TIME	Sets the minimum time between different phases' consecutive PWM rising edges. 10ns/LSB.
5:0	MFR_MIN_ONTIME	Sets the PWM minimum on time. 5ns/LSB.

MFR_SLOPE_SR_1P_R1 (D0h)

The MFR_SLOPE_SR_1P_R1 command sets the VR's slope compensation slew rate during 1-phase CCM operation on rail A.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:6	CAP	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is (16 - CAP) x 2.93pF. 2.93pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_2P_R1 (D1h)

The MFR_SLOPE_SR_2P_R1 command sets the VR's slope compensation slew rate during 2-phase CCM operation on rail A.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:6	CAP	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is (16 - CAP) x 2.93pF. 2.93pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_3P_R1 (D2h)

The MFR_SLOPE_SR_3P_R1 command sets the VR's slope compensation slew rate during 3-phase CCM operation on rail A.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:6	CAP	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is (16 - CAP) x 2.93pF. 2.93pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_4P_R1 (D3h)

The MFR_SLOPE_SR_4P_R1 command sets the VR's slope compensation slew rate during 4-phase CCM operation on rail A.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:6	CAP	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is (16 - CAP) x 2.93pF. 2.93pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_5P_R1 (D4h)

The MFR_SLOPE_SR_5P_R1 command sets the VR's slope compensation slew rate during 5-phase CCM operation on rail A.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:6	CAP	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is (16 - CAP) x 2.93pF. 2.93pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_6P_R1 (D5h)

The MFR_SLOPE_SR_6P_R1 command sets the VR's slope compensation slew rate during 6-phase CCM operation on rail A.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:6	CAP	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is (16 - CAP) x 2.93pF. 2.93pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_DCM_R1 (D6h)

The MFR_SLOPE_SR_DCM_R1 command sets the VR's slope compensation slew rate during 1-phase DCM operation on rail A.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:6	CAP	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is (16 - CAP) x 2.93pF. 2.93pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_1P_R2 (D7h)

The MFR_SLOPE_SR_1P_R2 command sets the VR's slope compensation slew rate during 1-phase CCM operation on rail B.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:6	CAP	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is (16 - CAP) x 2.93pF. 2.93pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_2P_R2 (D8h)

The MFR_SLOPE_SR_2P_R2 command sets the VR's slope compensation slew rate during 2-phase CCM operation on rail B.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:6	CAP	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is (16 - CAP) x 2.93pF. 2.93pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_3P_R2 (D9h)

The MFR_SLOPE_SR_3P_R2 command sets the VR's slope compensation slew rate during 3-phase CCM operation on rail B.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:6	CAP	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is (16 - CAP) x 2.93pF. 2.93pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_SR_DCM_R2 (DAh)

The MFR_SLOPE_SR_DCM_R2 command sets the VR's slope compensation slew rate during 1-phase DCM operation on rail B.

Bits	Bit Name	Description
15:10	RESERVED	Reserved.
9:6	CAP	Sets the capacitor quantity for slope voltage generation. The actual capacitor quantity is (16 - CAP) x 2.93pF. 2.93pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source quantity for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_CNT_DCM (DBh)

The MFR_SLOPE_CNT_DCM command sets the slope voltage ramping time for rail A and rail B during 1-phase DCM.

Bits	Bit Name	Description
15:8	SLOPE_CNT_DCM_R2	Sets the slope compensation ramping time for rail B in 1-phase DCM. 20ns/LSB.
7:0	SLOPE_CNT_DCM_R1	Sets the slope compensation ramping time for rail A in 1-phase DCM. 20ns/LSB.

MFR_SLOPE_CNT_1P_2P_R1 (DCh)

The MFR_SLOPE_CNT_1P_2P_R1 command sets the slope voltage ramping time for rail A in 1-phase and 2-phase CCM.

Bits	Bit Name	Description
15:8	SLOPE_CNT_2P_R1	Sets the slope compensation ramping time for rail A in 2-phase CCM. 20ns/LSB.
7:0	SLOPE_CNT_1P_R1	Sets the slope compensation ramping time for rail A in 1-phase CCM. 20ns/LSB.

MFR_SLOPE_CNT_3P_4P_R1 (DDh)

The MFR_SLOPE_CNT_3P_4P_R1 command sets the slope voltage ramping time for rail A in 3-phase and 4-phase CCM.

Bits	Bit Name	Description
15:8	SLOPE_CNT_4P_R1	Sets the slope compensation ramping time for rail A in 4-phase CCM. 20ns/LSB.
7:0	SLOPE_CNT_3P_R1	Sets the slope compensation ramping time for rail A in 3-phase CCM. 20ns/LSB.

MFR_SLOPE_CNT_5P_6P_R1 (DEh)

The MFR_SLOPE_CNT_5P_6P_R1 command sets the slope voltage ramping time for rail A in 5-phase and 6-phase CCM.

Bits	Bit Name	Description
15:8	SLOPE_CNT_6P_R1	Sets the slope compensation ramping time for rail A in 6-phase CCM. 20ns/LSB.
7:0	SLOPE_CNT_5P_R1	Sets the slope compensation ramping time for rail A in 5-phase CCM. 20ns/LSB.

MFR_SLOPE_CNT_1P_2P_R2 (E0h)

The MFR_SLOPE_CNT_1P_2P_R2 command sets the slope voltage ramping time for rail B in 1-phase and 2-phase CCM.

Bits	Bit Name	Description
15:8	SLOPE_CNT_2P_R2	Sets the slope compensation ramping time for rail B in 2-phase CCM. 20ns/LSB.
7:0	SLOPE_CNT_1P_R2	Sets the slope compensation ramping time for rail B in 1-phase CCM. 20ns/LSB.

MFR_SLOPE_CNT_3P_R2 (E1h)

The MFR_SLOPE_CNT_3P_R2 command sets the slope voltage ramping time for rail B in 3-phase CCM.

Bits	Bit Name	Description
15:8	RESERVED	Reserved.
7:0	SLOPE_CNT_3P_R2	Sets the slope compensation ramping time for rail B in 3-phase CCM. 20ns/LSB.

MFR_CURRENT_BALANCE_CTRL (E2h)

The MFR_CURRENT_BALACNE_CTRL command sets the integral parameter and saturation values for the current balance.

Bits	Bit Name	Description
15:14	RESERVED	Reserved.
13:10	CB_SATU_NEG	Defines the negative saturation level for the current balance calculation.
9:6	CB_SATU_POS	Defines the positive saturation level for the current balance calculation.
5:0	CB_PI	Sets the proportional integral (PI) value for current balance.

MFR_DCLOOP_PI (E3h)

The MFR_DCLOOP_PI command sets the integral parameter for the DC loop.

Bits	Bit Name	Description
15:6	RESERVED	Reserved.
5:0	DCLOOP_PI	Sets the integral parameter for the DC loop.

MFR_VR_CONFIG (E4h)

The MFR_VR_CONFIG command sets the basic functions of the MPQ2977.

Bits	Bit Name	Description
15:14	FS_LOOP_CFG	Controls the frequency loop. 2'b00: Disable the frequency loop 2'b01: Enable the frequency loop all the time 2'b10: Invalid 2'b11: Enable the frequency loop when the VR is stable; disable during DCM, DVID, or load transitions
13	VDIFF_GAIN_R2	Selects the resolution for rail B's VID table. 1'b0: 2.5mV/step 1'b1: 5mV/step
12:11	ADP_PSI_MODE_R2	Sets the power state for rail B. 2'b00: Full-phase CCM 2'b01: 1-phase CCM 2'b10: 1-phase DCM 2'b11: Automatic phase-shedding
10	DCM_DCLOOP_EN_R2	Enables the DC loop during 1-phase DCM on rail B for optimal V_{OUT} regulation. 1'b0: Disable the DC loop in DCM 1'b1: Enable the DC loop in DCM if DC LOOP_EN = 1
9	DCLOOP_EN_R2	Enables the DC loop in CCM on rail B for optimal V_{OUT} regulation. 1'b0: Disable the DC loop in CCM 1'b1: Enable the DC loop in CCM

8	CURRENT_ BALANCE_EN_R2	Enables automatic current balancing calibration during multi-phase operation on rail B. 1'b0: Disabled 1'b1: Enabled
7	DCM_TON_REDUCE_ EN_R2	Enables t_{ON} 1/4 reduction during DCM on rail B. When this function is enabled, the on time is reduced by 1/4 during 1-phase DCM to reduce the output voltage ripple. 1'b0: Disabled 1'b1: Enabled
6	VDIFF_GAIN_R1	Selects the resolution for rail A's VID table. 1'b0: 2.5mV/step 1'b1: 5mV/step
5:4	ADP_PSI_MODE_R1	Sets the power state for rail A. 2'b00: Full-phase CCM 2'b01: 1-phase CCM 2'b10: 1-phase DCM 2'b11: Automatic phase-shedding
3	DCM_DCLOOP_EN_ R1	Enables the DC loop during 1-phase DCM on rail A for optimal V_{OUT} regulation. 1'b0: Disable the DC loop in DCM 1'b1: Enable the DC loop in DCM if DC LOOP_EN = 1
2	DCLOOP_EN_R1	Enables the DC loop in CCM on rail A for optimal V_{OUT} regulation. 1'b0: Disable the DC loop in CCM 1'b1: Enable the DC loop in CCM
1	CURRENT_ BALANCE_EN_R1	Enables automatic current balancing calibration during multi-phase operation on rail A. 1'b0: Disabled 1'b1: Enabled
0	DCM_TON_REDUCE_ EN_R1	Enables t_{ON} 1/4 reduction during DCM on rail A. When this function is enabled, the on time is reduced by 1/4 during 1-phase DCM to reduce the output voltage ripple. 1'b0: Disabled 1'b1: Enabled

MFR_GPIO123_SLCT (E5h)

The MFR_GPIO123_SLCT command sets the functions for GPIO1, GPIO2, and GPIO3.

Bits	Bit Name	Description
15:9	RESERVED	Reserved.
8:6	GPIO3_SLCT	Sets the function of GPIO3. 3'd0: FAULT 3'd1: VR_READY 3'd2: ALERT 3'd4: VR_HOT
5:3	GPIO2_SLCT	Sets the function of GPIO2. 3'd0: FAULT 3'd1: VR_READY 3'd2: ALERT 3'd4: VR_HOT

2:0	GPIO1_SLCT	Sets the function of GPIO1. 3'd0: FAULT 3'd1: VR_READY 3'd2: ALERT 3'd4: VR_HOT

MFR_GPIO456_SLCT (E6h)

The MFR_GPIO456_SLCT command sets the functions for GPIO4, GPIO5, and GPIO6.

Bits	Bit Name	Description
15:9	RESERVED	Reserved.
8:6	GPIO6_SLCT	Sets the function of GPIO6. 3'd0: FAULT 3'd1: VR_READY 3'd2: ALERT 3'd4: VR_HOT
5:3	GPIO5_SLCT	Sets the function of GPIO5. 3'd0: FAULT 3'd1: VR_READY 3'd2: ALERT 3'd4: VR_HOT
2:0	GPIO4_SLCT	Sets the function of GPIO4. 3'd0: FAULT 3'd1: VR_READY 3'd2: ALERT 3'd4: VR_HOT

MFR_CS_OFFSET1_2 (EBh)

The MFR_CS_OFFSET1_2 command sets the CS1 and CS2 pins' sense offset to achieve thermal balance in multi-phase operation for phase 1 and phase 2.

Bits	Bit Name	Description
15:8	MFR_CS_OFFSET2	Sets the CS2 offset in the current balance loop. 3.125mV/LSB. Ranges between -400mV and +396.875 mV
7:0	MFR_CS_OFFSET1	Sets the CS1 offset in the current balance loop. 3.125mV/LSB. Ranges between -400mV and +396.875 mV

MFR_CS_OFFSET3_4 (ECh)

The MFR_CS_OFFSET3_4 command sets the CS3 and CS4 pins' sense offset to achieve thermal balance in multi-phase operation for phase 3 and phase 4.

Bits	Bit Name	Description
15:8	MFR_CS_OFFSET4	Sets the CS4 offset in the current balance loop. 3.125mV/LSB. Ranges between -400mV and +396.875 mV
7:0	MFR_CS_OFFSET3	Sets the CS3 offset in the current balance loop. 3.125mV/LSB. Ranges between -400mV and +396.875 mV

MFR_CS_OFFSET5_6 (EDh)

The MFR_CS_OFFSET5_6 command sets the CS5 and CS6 pins' sense offset to achieve thermal balance in multi-phase operation for phase 5 and phase 6.

Bits	Bit Name	Description
15:8	MFR_CS_OFFSET6	Sets the CS6 offset in the current balance loop. 3.125mV/LSB. Ranges between -400mV and +396.875 mV
7:0	MFR_CS_OFFSET5	Sets the CS5 offset in the current balance loop. 3.125mV/LSB. Ranges between -400mV and +396.875 mV

MFR_FILTER_SET (F0h)

The MFR_FILTER_SET command sets related parameters about VID DAC for rail A and rail B.

Bits	Bit Name	Description
15:8	RESERVED	Reserved.
7	MFR_DAC_CMP_EN_R2	Enables the DAC comparator for rail B. 1'b1: Enabled 1'b0: Disabled
6	MFR_VID_FILTER_EN_R2	Enables the VID filter in DAC for rail B. 1'b1: Enabled 1'b0: Disabled
5:4	MFR_VID_FILTER_R2	Selects the filter time constant for rail B. 2'b00: 2.35μs 2'b01: 4.7μs 2'b10: 7.05μs 2'b11: 9.4μs
3	MFR_DAC_CMP_EN_R1	Enables the DAC comparator for rail A. 1'b1: Enabled 1'b0: Disabled
2	MFR_VID_FILTER_EN_R1	Enables the VID filter in DAC for rail A. 1'b1: Enabled 1'b0: Disabled
1:0	MFR_VID_FILTER_R1	Selects the filter time constant for rail A. 2'b00: 2.35μs 2'b01: 4.7μs 2'b10: 7.05μs 2'b11: 9.4μs

MFR_TRANS_FAST_R1 (F1h)

The MFR_TRANS_FAST_R1 command sets the slew rate and other related parameters for rail A.

Bits	Bit Name	Description
15:12	RESERVED	Reserved.
11	TRANS_FAST_EN_R1	Sets the VID downward rate after the rising step. 1'b1: 1/8 x normal slew rate 1'b0: 1/4 x normal slew rate
10:8	RISING_STEP_R1	During an upward DVID, the VR continues to rise a certain step after its VID value reaches the target. This bit sets the value of the rising step. 1 VID step/LSB.
7:6	VID_STEP_R1	Sets the value of the VID step. Its resolution is same as the value set by MFR_VOUT_COMMAND_R1 (21h).

5:0	RATE_TIME_R1	Sets the rate time of each VID step. 100ns/LSB.

MFR_TRANS_FAST_R2 (F2h)

The MFR_TRANS_FAST_R2 command sets the slew rate and other related parameters for rail A.

Bits	Bit Name	Description
15:12	RESERVED	Reserved.
11	TRANS_FAST_EN_R2	Sets the VID downward rate after the rising step. 1'b1: 1/8 x normal slew rate 1'b0: 1/4 x normal slew rate
10:8	RISING_STEP_R2	During an upward DVID, the VR continues to rise a certain step after its VID value reaches the target. This bit sets the value of the rising step. 1 VID step/LSB.
7:6	VID_STEP_R2	Sets the value of the VID step. Its resolution is same as the value set by MFR_VOUT_COMMAND_R2 (22h).
5:0	RATE_TIME_R2	Sets the rate time of each VID step. 100ns/LSB.

MFR_INTIAL_DLY (F3h)

The MFR_INITIAL_DLY command sets the VR's start-up delay time, from when system initialization ends to when V_{REF} starts ramping up.

Bits	Bit Name	Description
15:8	RESERVED	Reserved.
7:4	MFR_INTIAL_DLY_R2	If there is no V_{IN} or temperature fault in rail B, the VR must wait MFR_INTIAL_DLY_R2 x 20µs before outputting power. 20µs/LSB.
3:0	MFR_INTIAL_DLY_R1	If there is no V_{IN} or temperature fault in rail A, the VR must wait MFR_INTIAL_DLY_R1 x 20µs before outputting power. 20µs/LSB.

MFR_VOUT_LEVEL_R1 (F4h)

The MFR_VOUT_LEVEL_R1 command sets the maximum and minimum VID target for rail A.

Bits	Bit Name	Description
15:6	MFR_VOUT_MAX_R1	Sets the maximum VID target for rail A. Its resolution is the same as the value set by MFR_VOUT_COMMAND_R1 (21h).
5:0	MFR_VOUT_MIN_R1	Sets the minimum VID target for rail A. Its resolution is the same as the value set by MFR_VOUT_COMMAND_R1 (21h).

MFR_VOUT_LEVEL_R2 (F5h)

The MFR_VOUT_LEVEL_R2 command sets the maximum and minimum VID target for rail B.

Bits	Bit Name	Description
15:6	MFR_VOUT_MAX_R2	Sets the maximum VID target for rail B. Its resolution is the same as the value set by MFR_VOUT_COMMAND_R2 (22h).
5:0	MFR_VOUT_MIN_R2	Sets the minimum VID target for rail B. Its resolution is the same as the value set by MFR_VOUT_COMMAND_R2 (22h).

MFR_VID_01H (F6h)

The MFR_VID_01H command sets the offset value of VID 01h for rail A and rail B.

Bits	Bit Name	Description
15:12	RESERVED	Reserved.
11:6	MFR_VID_01H_R2	Sets the rail B VID 01h offset value. Its resolution is the same as the value set by MFR_VOUT_COMMAND_R2 (22h).

5:0	MFR_VID_01H_R1	Sets the rail A VID 01h offset value. Its resolution is the same as the value set by MFR_VOUT_COMMAND_R1 (21h).

MFR_SHUTDOWN_LEVEL (F7h)

The MFR_SHUTDOWN_LEVEL command sets the VR's shutdown level. When the VID target is set to 0 and the current VID falls below shutdown level, the PWM goes to Hi-Z.

Bits	Bit Name	Description
15:8	RESERVED	Reserved.
7:4	MFR_SHUTDOWN_ LEVEL_R2	Sets the rail B VID shutdown level. Its resolution is the same as the value set by MFR_VOUT_COMMAND_R2 (22h).
3:0	MFR_SHUTDOWN_ LEVEL_R1	Sets the rail A VID shutdown level. Its resolution is the same as the value set by MFR_VOUT_COMMAND_R1 (21h).

MFR_PMBUS_ADDR (F8h)

The MFR_PMBUS_ADDR command sets the MTP password and PMBus address.

Bits	Bit Name	Description
15:8	MTP_PASSWORD	Sets the MTP password.
7	PMBUS_ADDR_ SELECT	Selects where bits[3:0] of the final PMBus address are set. 1'b0: Bits[3:0] are set by the ADDR pin's voltage 1'b1: Bits[3:0] are set by bits[3:0] of MFR_PMBUS_ADDR (F8h)
6:0	PMBUS_ADDR	Sets the initial PMBus address.

MFR_PASSWORD (F9h)

The MFR_PASSWORD command sets the VR password.

Bits	Bit Name	Description
15:8	RESERVED	Reserved.
7:0	PASSWORD	Sets the VR password. The register value can be read only when the input password is correct (Reg B0h, bits[7:0] = Reg F9h, bits[7:0]), or it returns 8'h00.

MFR_CHANNEL_OBS (FAh)

The MFR_CHANNEL_OBS command sets the observed analog-to-digital (ADC) channel. This function is not applicable to the MPQ2977

Bits	Bit Name	Description
15:7	RESERVED	Reserved.
6:0	RESERVED	Reserved.

MFR_VOUT_CMPS_MAX (FBh)

The MFR_VOUT_CMPS_MAX command sets the maximum value for rail A and rail B's V_{O_COMP}.

Bits	Bit Name	Description
15:8	VOUT_CMPS_MAX_R2	Sets the maximum value for rail B's V_{O_COMP}. 0.9375mV/LSB if A4h, bit[15] = 1'b0 1.25mV/LSB if A4h, bit[15] = 1'b1
7:0	VOUT_CMPS_MAX_R1	Sets the maximum value for rail A's V_{O_COMP}. 0.9375mV/LSB if A4h, bit[15] = 1'b0 1.25mV/LSB if A4h, bit[15] = 1'b1

MFR_SW_PRD_SET (FCh)

The MFR_SW_PRD_SET command sets the PWM switching period, as well as the V_{IN} sample hysteresis and offset.

Bits	Bit Name	Description
15:8	SW_PRD_SET	Sets the PWM switching period. 40ns/LSB.
7:4	VIN_SENSE_OFFSET	Sets the V_{IN} sample offset. Bit[3] is the signed bit. 25mV/LSB.
3:0	VIN_HYS	Sets the threshold for the V_{IN} sample result variation to trigger the on time calculation. The on time refreshes when the V_{IN} sample variation exceeds MFR_VIN_HYS. 25mV/LSB. (1.6 / 1024 x 16 = 0.025V/LSB.)

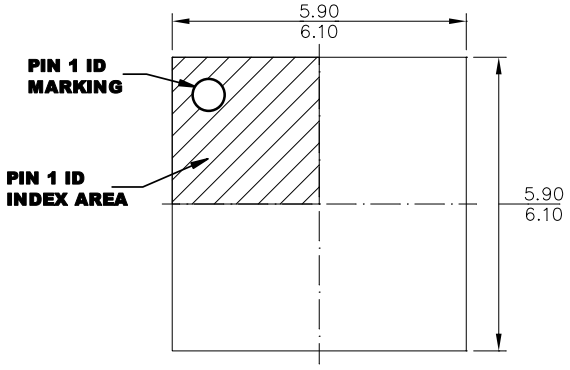
MFR_OTP_SET (FDh)

The MFR_OTP_SET command sets the over-temperature protection (OTP) threshold.

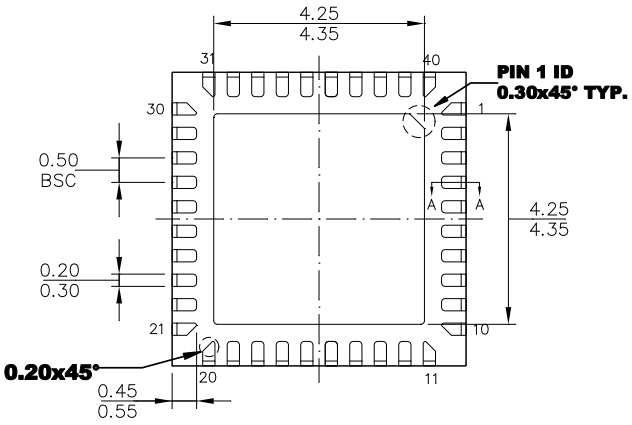
Bits	Bit Name	Description
15	RESERVED	Reserved.
14:7	OTP_LIMIT	Sets the over-temperature protection (OTP) fault limit. When the junction temperature monitored on the VTEMP pin exceeds OTP_LIMIT, the VR shuts down. 1°C/LSB.
6:0	OTP_HYS	Sets the hysteresis for the OTP threshold. If the junction temperature monitored on the VTEMP pin drops below OTP_LIMIT - OTP_HYS, the PWM initiates a soft start as it would during a normal start-up (if OTP is set to hiccup mode). 1°C/LSB.

PACKAGE INFORMATION

TQFN-40 (6mmx6mm)

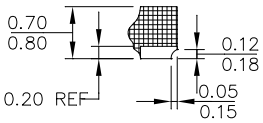


TOP VIEW

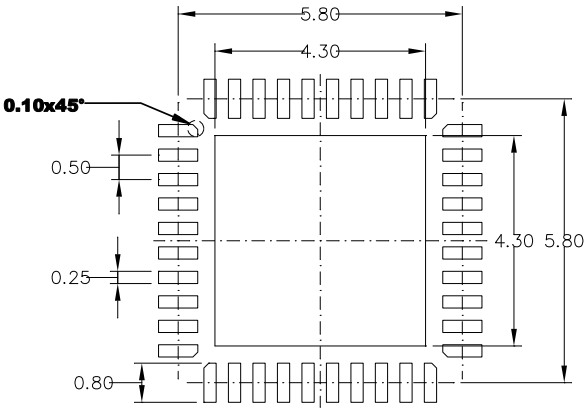


BOTTOM VIEW

SIDE VIEW



SECTION A-A

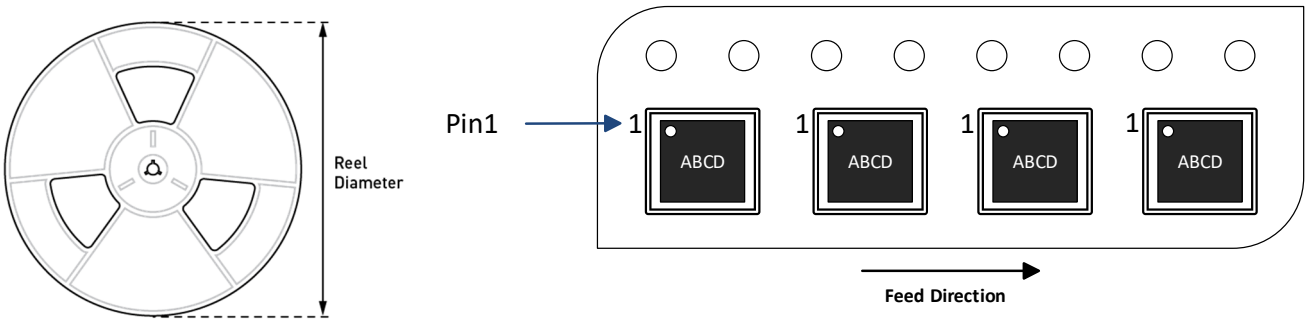


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2977GQKTE -xxxx-AEC1-Z	TQFN-40 (6mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/28/2022	Initial Release	-
1.1	3/1/2024	Corrected a typo in the name of pin 14 in the Package Reference section.	3
		Removed the Comparator (Rails A/B, Warning) section from the Electrical Characteristics table.	7
		Removed the OVP Warning DAC (OVP Warning for Rails A/B) and the UVP Warning DAC (UV for Rails A/B) sections from the Electrical Characteristics table.	9
		Updated the description of V_{IN} dropping below MFR_VIN_UVOV_LIMIT (36h), bits[15:9] in the Input Voltage (V_{IN}) Protections section.	18
		Updated the description of 36h, the bit name and description of 36h, bits[15:9], and made minor copyedits to 36h, bits[15:9] and bits[7:0].	40
		Updated the description of 93h and reserved 93h, bits[11:6].	46
		Updated the description of 94h and reserved 94h, bits[11:6].	47