MPQ4322

42V Load Dump Tolerant, 2A, Ultra-Compact, Low-I_Q, Synchronous Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ4322 is a configurable-frequency (350kHz to 2.5MHz), synchronous, step-down switching converter with integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). The device provides up to 2A of highly efficient output current (I_{OUT}) with peak current mode control.

The wide 3.3V to 36V input voltage (V_{IN}) range and 42V load dump tolerance accommodates a variety of step-down applications in automotive input environments. A 1µA shutdown current (I_{SD}) allows the device to be used in battery-powered applications.

High power conversion efficiency across the entire load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce the switching and gate driving losses.

An open drain power good (PG) signal indicates whether the output is within 94.5% to 105.5% of its nominal voltage.

Frequency foldback helps prevent inductor current (I_L) runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

High duty cycle and low drop-out (LDO) mode are provided for automotive cold-crank conditions.

The MPQ4322 is available in QFN-12 (2mmx3mm) and QFN-12 (3mmx4mm) packages.

FEATURES

- Designed for Automotive Applications:
  - 42V Load Dump Tolerance
  - Supports 3.1V for Cold Crank Conditions
  - Up to 2A of Continuous Output Current
  - Continuous Operation Up to 36V
  - -40°C to +150°C Junction Temperature (T_J) Range
- Increases Battery Life:
  - 1µA Shutdown Supply Current (I_{SD})
  - 20µA Sleep Mode Quiescent Current (I_Q)
  - Advanced Asynchronous Modulation (AAM) Mode Increases Efficiency under Light Loads
- High Performance for Improved Thermals:
  - Integrated 70mΩ/50mΩ MOSFETs
  - 65ns Minimum On Time (t_{ON_MIN})
  - 50ns Minimum Off Time (t_{OFF_MIN})
- Optimized for EMC/EMI:
  - Frequency Spread Spectrum (FSS) Modulation
  - Symmetric VIN Pinout
  - CISPR25 Class 5 Compliant
  - 350kHz to 2.5MHz Configurable Switching Frequency (f_{SW})
  - MeshConnect™ Flip-Chip Package
- Additional Features:
  - Power Good (PG) Output
  - Low-Dropout (LDO) Mode
  - Fixed Output Options [(1)]: 1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, 5V
  - Hiccup Over-Current Protection (OCP)
  - Available in a QFN-12 (2mmx3mm) Package or a QFN-12 (3mmx4mm) Package with Wettable Flanks
  - Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Advanced Driver-Assistance Systems (ADAS)
- Industrial Power Systems

Note:

1) See the Ordering Information section on page 3 for details regarding the fixed-output versions. Additional output voltages may be available. Contact MPS for more details.

TYPICAL APPLICATION

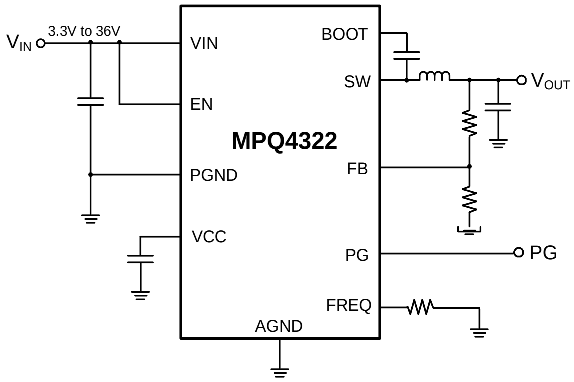
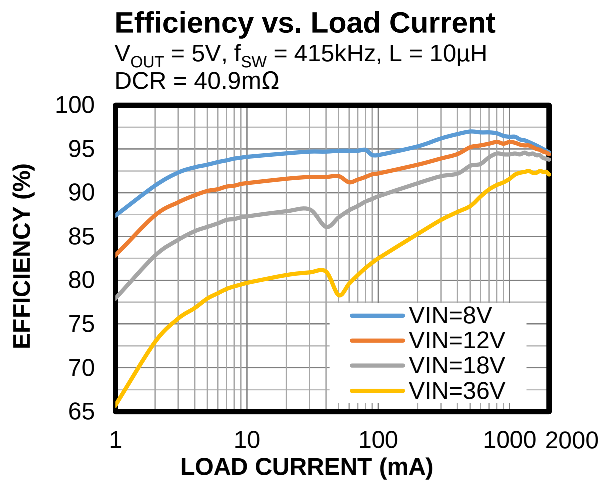


Figure 1: Typical Application (Adjustable Output)



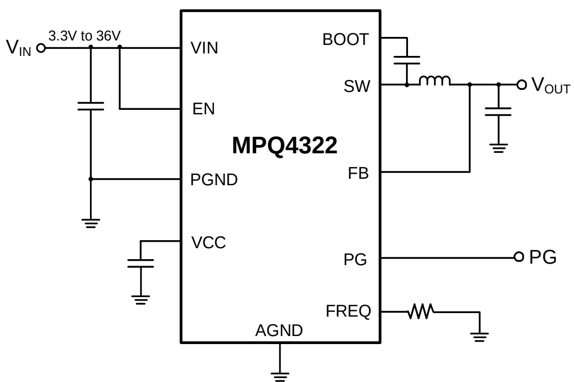


Figure 2: Typical Application (Fixed Output)

ORDERING INFORMATION

Part Number (2)*	Package	Top Marking	MSL Rating**
MPQ4322GDE-AEC1***	QFN-12 (2mmx3mm)	*See Below*	1
MPQ4322GLE-AEC1***	QFN-12 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ4322GDE-AEC1-Z).

**Moisture Sensitivity Level Rating

***Wettable flank

Note:

2) Additional output voltages may be available. Contact MPS for details.

TOP MARKING
(MPQ4322GDE-AEC1)

BRK
YWW
LLLL

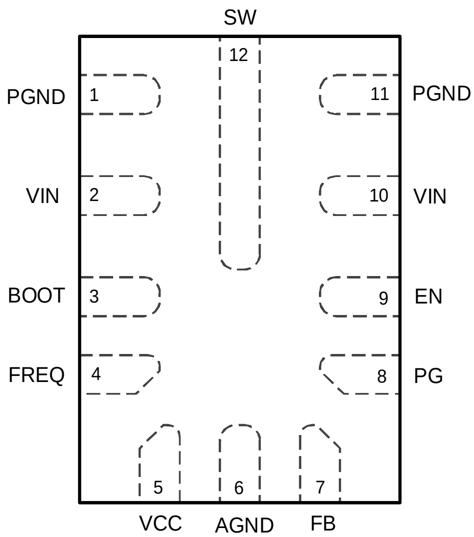
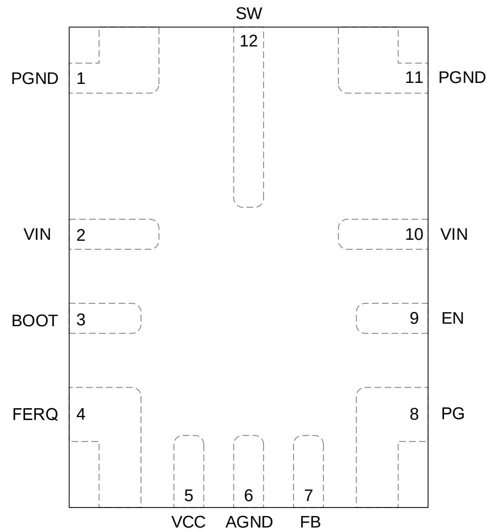
BRK: Production code
Y: Year code
WW: Week code
LLLL: Lot number

TOP MARKING
(MPQ4322GLE-AEC1)

MPYW
4322
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
4322: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
QFN-12 (2mmx3mm)	**QFN-12 (3mmx4mm)**

PIN FUNCTIONS

Pin #	Name	Description
1, 11	PGND	**Power ground.**
2, 10	VIN	**Input supply.** The VIN pins supply power to the internal control circuitry and the power MOSFET connected to the SW pin. The two VIN pins are connected internally. Place a decoupling capacitor connected to PGND as close as possible to each VIN pin to minimize switching spikes.
3	BOOT	**Bootstrap.** The BOOT pin is the positive power supply for the high-side MOSFET (HS-FET) driver connected to SW. Connect a bypass capacitor between the BOOT and SW pins.
4	FREQ	**Switching frequency configuration.** Connect a resistor between the FREQ pin and AGND to set the switching frequency (f_{SW}).
5	VCC	**Bias supply.** The VCC pin is the output of the internal regulator that supplies power to the internal control circuit and gate drivers. Place a minimum 1µF decoupling capacitor between VCC and AGND. The capacitor should be placed as close as possible to VCC.
6	AGND	**Analog ground.**
7	FB	**Feedback input.** The FB pin is the negative input of the error amplifier (EA) (typically 0.8V). For the fixed-output version, connect FB directly to the output voltage (V_{OUT}). For the adjustable-output version, connect FB to the middle point of the external feedback divider between the output and AGND to set V_{OUT}.
8	PG	**Power good output.** The PG pin is an open-drain output. If PG is used, connect PG to a power source via a pull-up resistor. If V_{OUT} is within 94.5% to 105.5% of the nominal voltage, then PG goes high. If V_{OUT} exceeds 107% or drops below 93% of the nominal voltage, then PG goes low. Float PG if not used.
9	EN	**Enable.** Pull the EN pin above 1.02V to turn the converter on; pull EN below 0.85V to turn it off. EN does not require an internal pull-up or pull-down resistor. Do not float EN.
12	SW	**Switch node.** The SW pin is the source of the HS-FET and the drain of the low-side MOSFET (LS-FET).

ABSOLUTE MAXIMUM RATINGS (3)

VIN, EN………42V for automotive load dump (4)
VIN, EN……………………………..-0.3V to +40V
SW……………………….-0.3V to V_{IN_MAX} + 0.3V
BOOT…………………………........... V_{SW} + 5.5V
FREQ, VCC…………………………..….5.5V
All other pins…………… ....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (5)
QFN-12 (2mmx3mm)…………… 3.5W (9)
QFN-12 (3mmx4mm)…………… 3.6W (10)
Operating junction temperature ....150°C
Lead temperature……………..................260°C
Storage temperature…………..-65°C to +150°C

ESD Ratings

Human body model (HBM)……..……..Class 2 (6)
Charged device model (CDM).........Class C2b (7)

Recommended Operating Conditions

Input voltage (V_{IN})…………………….3.3V to 36V
Minimum V_{IN} for start-up……………………3.9V
Minimum V_{IN} after start-up……..…………...3.1V
Output voltage (V_{OUT})……......…0.8V to 0.95 x V_{IN}
Operating junction temp (T_J)…..-40°C to +150°C

Thermal Resistance θJA θJC

QFN-12 (2mmx3mm)
JESD51-7…...…...…..……60…....7.3...°C/W (8)
EVQ4322-D-00A……........35.5.............°C/W (9)
QFN-12 (3mmx4mm)
JESD51-7…...…................50.......7.5...°C/W (8)
EVQ4322-L-00A……........34.3...........°C/W (10)

ΨJT

QFN-12 (2mmx3mm)
JESD51-7…...…..………….....1.1.....°C/W (8)
EVQ4322-D-00A………...............3.5.....°C/W (9)
QFN-12 (3mmx4mm)
JESD51-7…...…..………….....1.2.....°C/W (8)
EVQ4322-L-00A………...............3.7....°C/W (10)

Notes:

3) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
4) Refer to ISO16750.
5) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
6) Per AEC-Q100-002.
7) Per AEC-Q100-011.
8) Measured on a JESD51-7, a 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from junction-to-case bottom, and the Ψ_{JT} value shows the characterization parameter from junction-to-case top.
9) Measured on the MPS MPQ4322GDE standard EVB, an 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB. The Ψ_{JT} value shows the characterization parameter from junction-to-case top.
10) Measured on the MPS MPQ4322GLE standard EVB, an 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB. The Ψ_{JT} value shows the characterization parameter from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		3.4	3.65	3.9	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		2.6	2.9	3.1	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			750		mV
VIN quiescent current	I_Q	V_{FB} = 0.85V, no load, T_J = 25°C		20	28	µA
		V_{FB} = 0.85V, no load, T_J = -40°C to +125°C (11)			34	µA
		V_{FB} = 0.85V, no load, T_J = -40°C to +150°C			80	µA
VIN quiescent switching current (11)	$I_{Q\_SWITCHING}$	Switching, R_{FB1} = 1MΩ, R_{FB2} = 191kΩ, no load		25		µA
VIN shutdown current	I_{SD}	V_{EN} = 0V		1	10	µA
V_{IN} over-voltage protection (OVP) rising threshold	$V_{IN\_OVP\_RISING}$		35.5	37.5	40	V
V_{IN} OVP falling threshold	$V_{IN\_OVP\_FALLING}$		34.5	36.5	39	V
V_{IN} OVP hysteresis	$V_{IN\_OVP\_HYS}$			1		V
Switches and Frequency						
Switching frequency without frequency spread spectrum (FSS)	f_{SW}	R_{FREQ} = 86.6kΩ	332	415	498	kHz
		R_{FREQ} = 34.8kΩ	900	1000	1100	kHz
		R_{FREQ} = 15kΩ	1980	2200	2420	kHz
FSS span				±10		%
FSS modulation frequency				15		kHz
Minimum on time (11)	t_{ON_MIN}			65	80	ns
Minimum off time (11)	t_{OFF_MIN}			50	70	ns
Maximum duty cycle	D_{MAX}		98	99.5		%
Switch leakage current	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = V_{BOOT} = 0V or V_{IN} (T_J = 25°C)		0.01	1	µA
		V_{EN} = 0V, V_{SW} = V_{BOOT} = 0V or V_{IN} (T_J = -40°C to +150°C)		0.01	5	µA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{BOOT} - V_{SW} = 5V		70	130	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{CC} = 5V		50	90	mΩ
Output and Regulation						
FB voltage (adjustable-output version)	V_{FB}	T_J = 25°C	0.794	0.8	0.806	V
		T_J = -40°C to +150°C	0.790	0.8	0.810	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

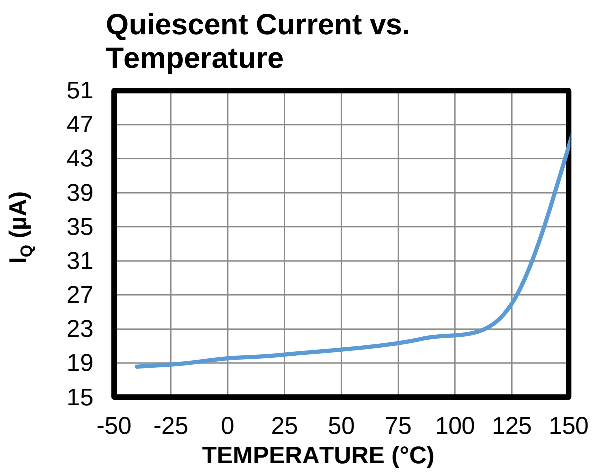
Parameter	Symbol	Condition	Min	Typ	Max	Units
Output and Regulation						
FB input current	I_{FB}	Adjustable-output version		0	100	nA
V_{OUT} discharge current	$I_{DISCHARGE}$	V_{EN} = 0V, V_{OUT} = 0.3V	2	4		mA
BOOT						
BOOT - SW refresh rising threshold	V_{BOOT_RISING}			2.5	2.9	V
BOOT - SW refresh falling threshold	$V_{BOOT\_FALLING}$			2.3	2.7	V
BOOT - SW refresh hysteresis	V_{BOOT_HYS}			0.2		V
Enable (EN)						
EN rising threshold	V_{EN_RISING}		0.97	1.02	1.07	V
EN falling threshold	$V_{EN\_FALLING}$		0.8	0.85	0.9	V
EN threshold hysteresis	V_{EN_HYS}			170		mV
Soft Start (SS) and VCC						
Soft-start time	t_{SS}	EN high to SS finishes	3	5	7	ms
VCC voltage	V_{CC}	I_{VCC} = 0	4.7	5	5.3	V
VCC regulation		I_{VCC} = 30mA		1		%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	50	70		mA
Power Good (PG)						
PG rising threshold (V_{FB} / V_{REF})	PG_{VTH_RISING}	V_{OUT} rising	93	94.5	96	%
		V_{OUT} falling	104	105.5	107	%
PG falling threshold (V_{FB} / V_{REF})	$PG_{VTH\_FALLING}$	V_{OUT} falling	91.5	93	94.5	%
		V_{OUT} rising	105.5	107	108.5	%
PG threshold hysteresis (V_{FB} / V_{REF})	PG_{VTH_HYS}			1.5		%
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising deglitch time	t_{PG_R}			70		µs
PG falling deglitch time	t_{PG_F}			60		µs
Protections						
High-side (HS) peak current limit	I_{LIMIT_HS}	Duty cycle = 30%	2.7	3.4	4.6	A
Low-side (LS) valley current limit	I_{LIMIT_LS}		2	2.7	3.8	A
Zero-current detection (ZCD) current	I_{ZCD}		-0.05	0.05	+0.15	A
Thermal shutdown (11)	T_{SD}		160	175	185	°C
Thermal shutdown hysteresis (11)	T_{SD_HYS}			20		°C

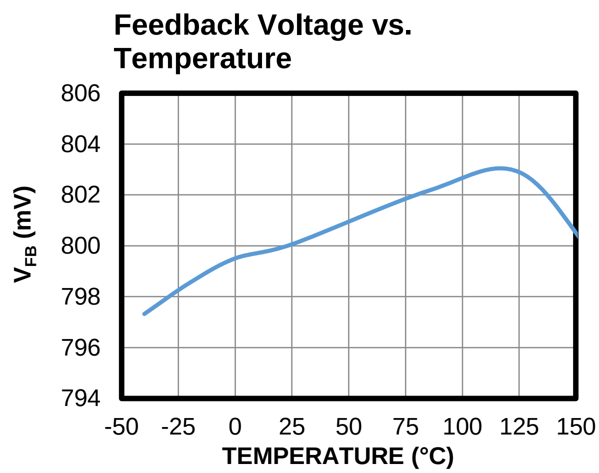
Note:

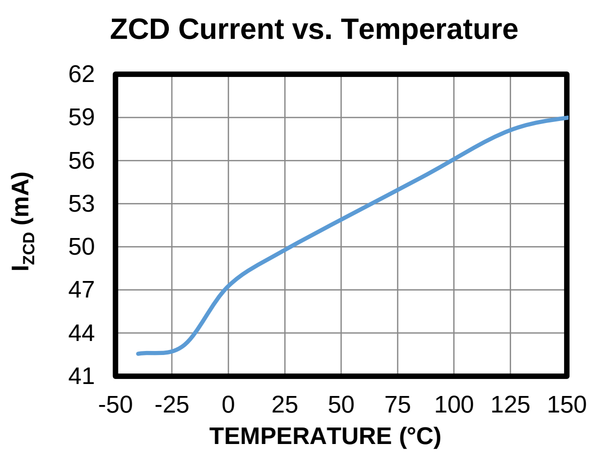
11) Not tested in production. Guaranteed by design and characterization.

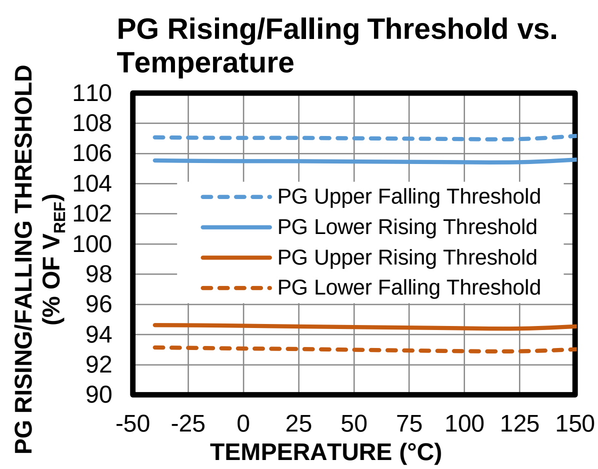
TYPICAL CHARACTERISTICS

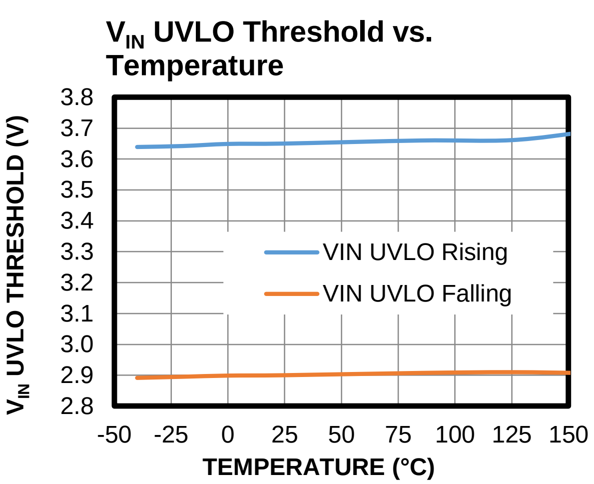
V_{IN} = 12V, unless otherwise noted.

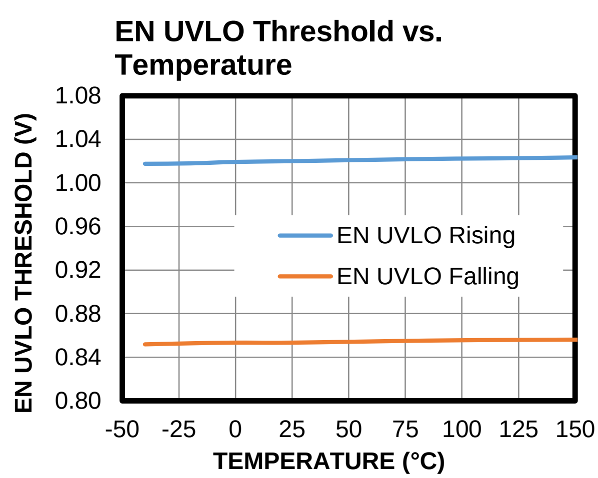






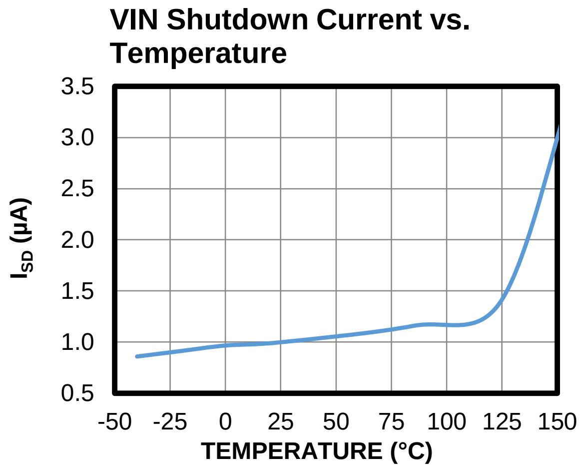


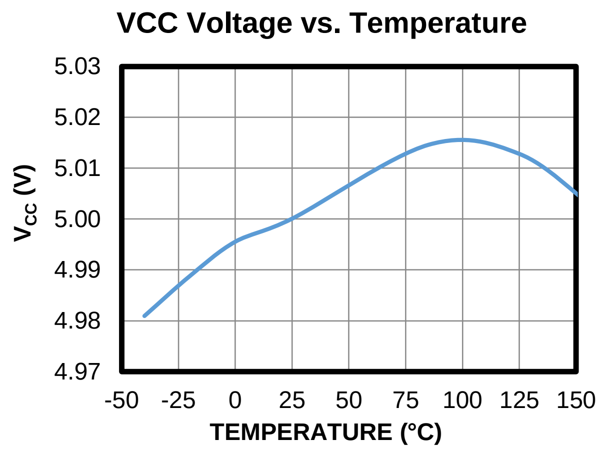


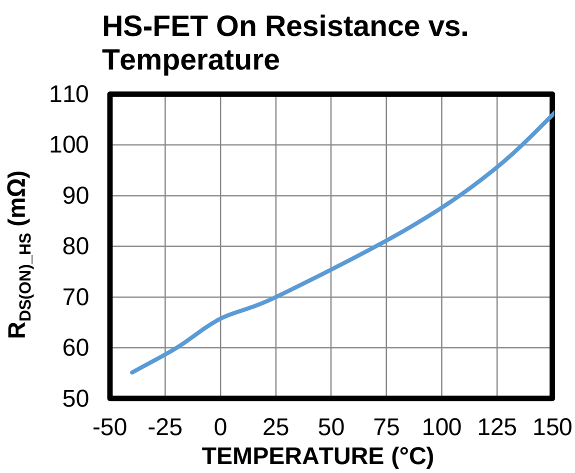


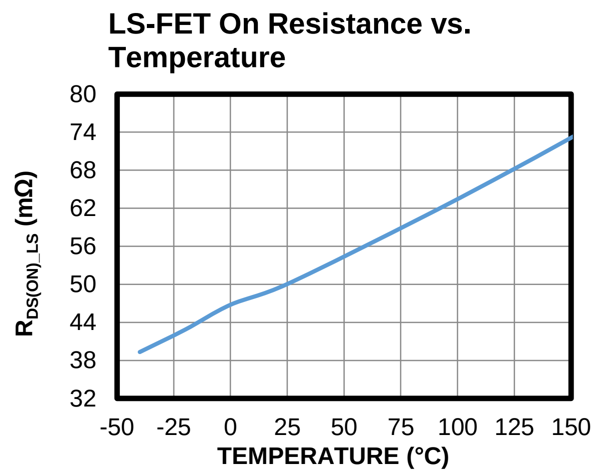
TYPICAL CHARACTERISTICS *(continued)*

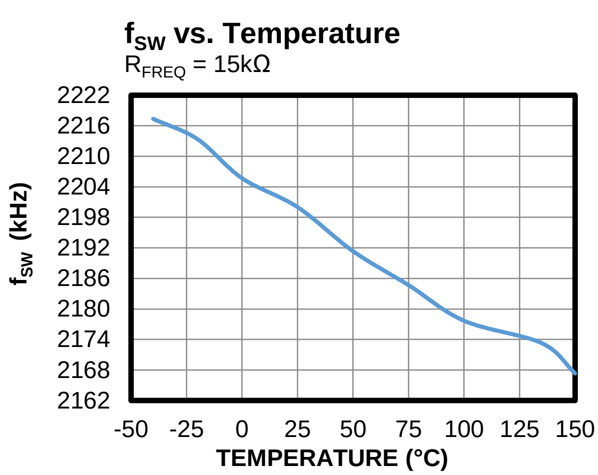
V_{IN} = 12V, unless otherwise noted.

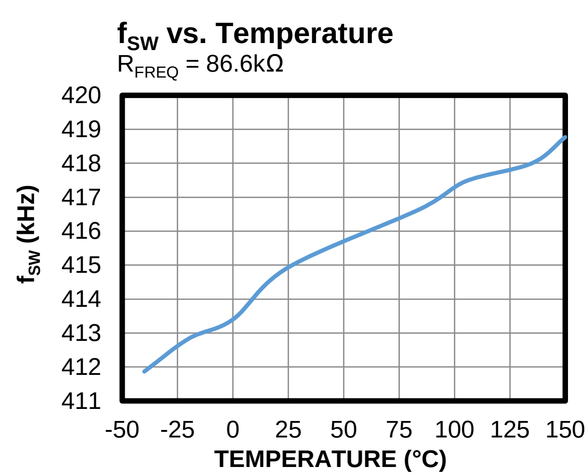








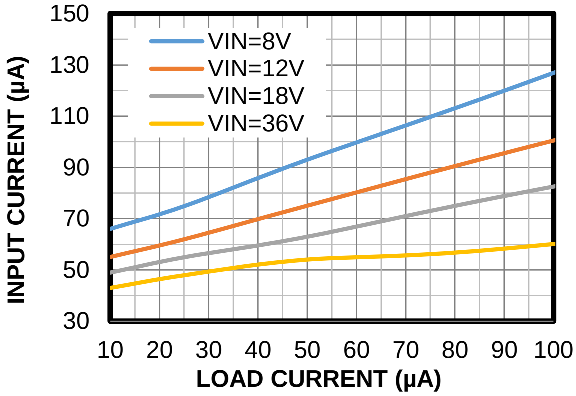




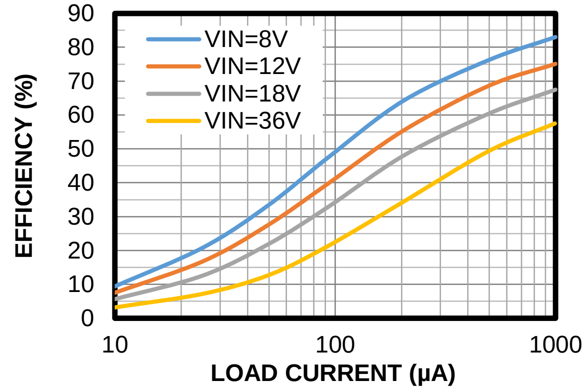
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

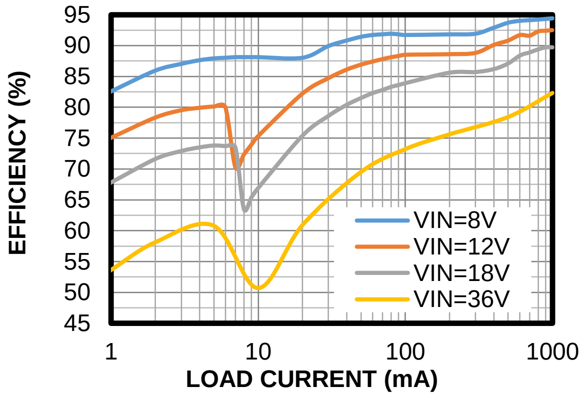
Input Current vs. Load Current
R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ,
DCR = 22.1mΩ



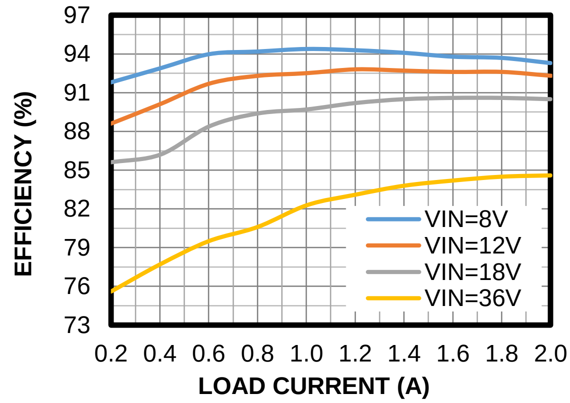
Efficiency vs. Load Current
R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ,
DCR = 22.1mΩ



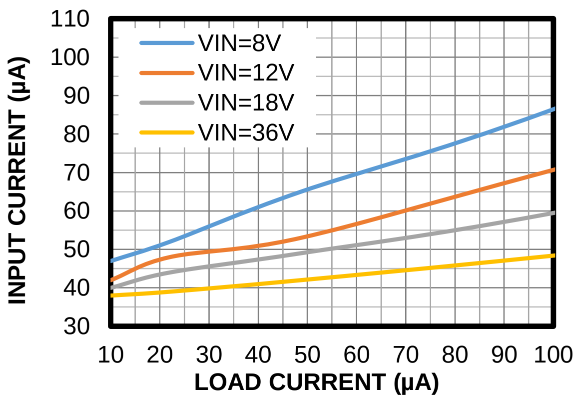
Efficiency vs. Load Current
DCR = 22.1mΩ



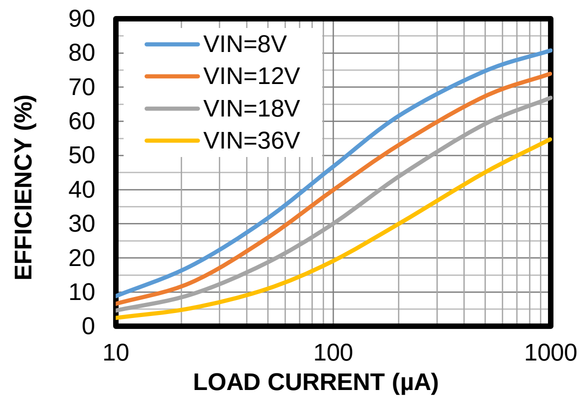
Efficiency vs. Load Current
DCR = 22.1mΩ



Input Current vs. Load Current
V_{OUT} = 3.3V, R_{FB1} = 100kΩ,
R_{FB2} = 31.6kΩ, DCR = 22.1mΩ



Efficiency vs. Load Current
V_{OUT} = 3.3V, R_{FB1} = 100kΩ,
R_{FB2} = 31.6kΩ, DCR = 22.1mΩ

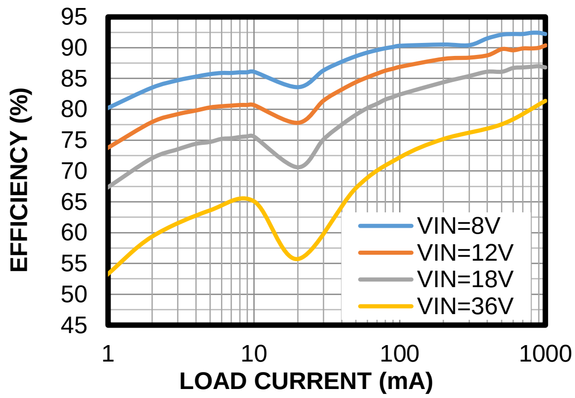


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

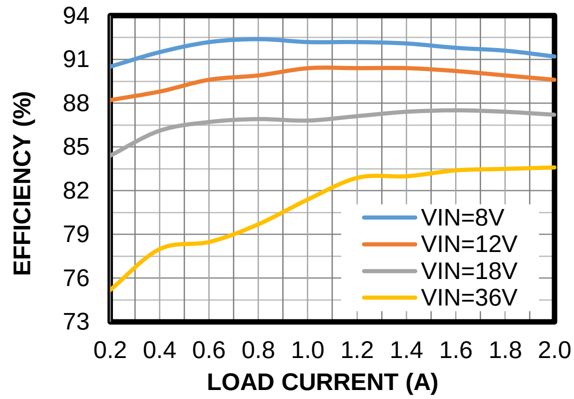
Efficiency vs. Load Current

V_{OUT} = 3.3V, DCR = 22.1mΩ



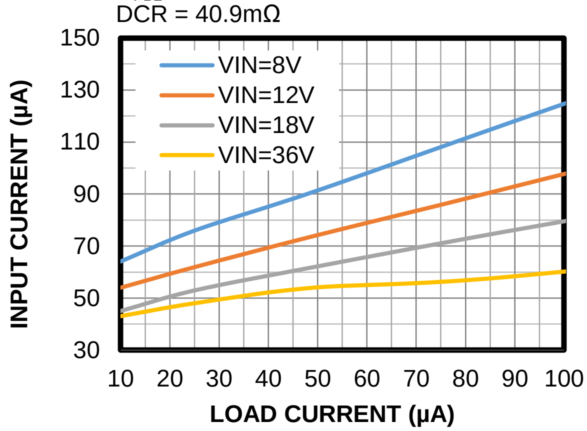
Efficiency vs. Load Current

V_{OUT} = 3.3V, DCR = 22.1mΩ



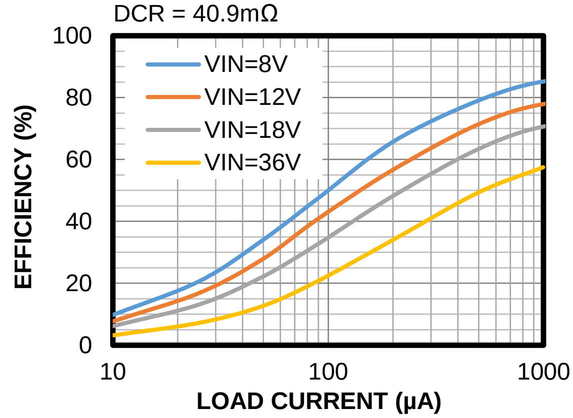
Input Current vs. Load Current

f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 10µH, DCR = 40.9mΩ



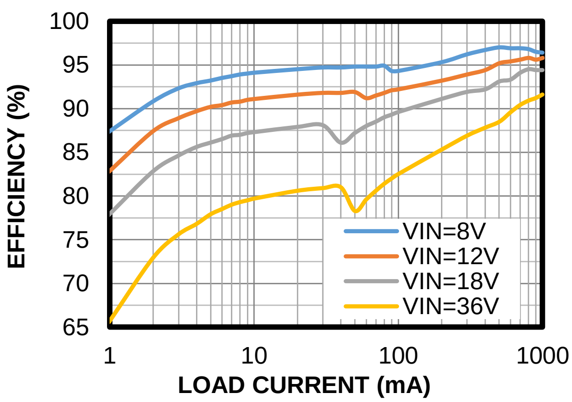
Efficiency vs. Load Current

f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 10µH, DCR = 40.9mΩ



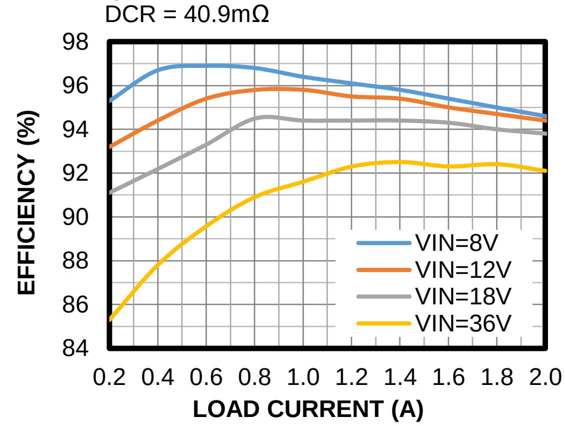
Efficiency vs. Load Current

f_{SW} = 415kHz, L = 10µH, DCR = 40.9mΩ



Efficiency vs. Load Current

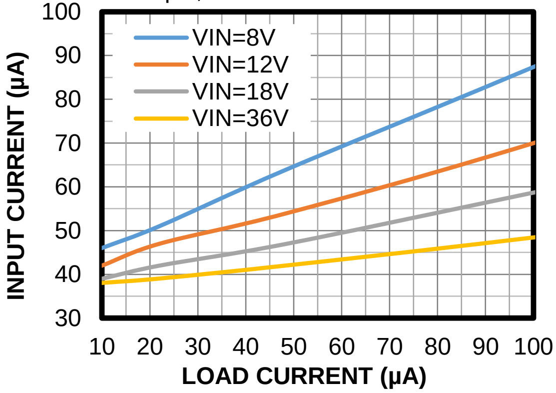
f_{SW} = 415kHz, L = 10µH, DCR = 40.9mΩ



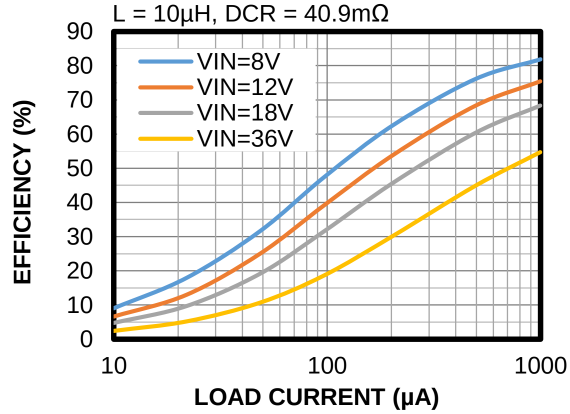
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

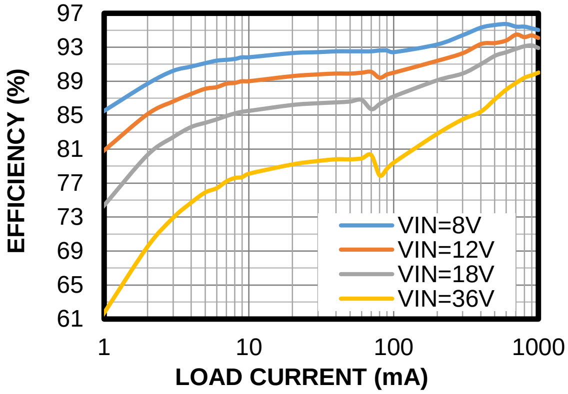
Input Current vs. Load Current
V_{OUT} = 3.3V, f_{SW} = 415kHz,
R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ,
L = 10µH, DCR = 40.9mΩ



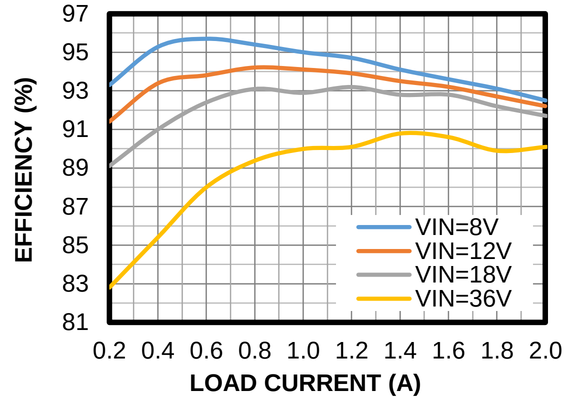
Efficiency vs. Load Current
V_{OUT} = 3.3V, f_{SW} = 415kHz,
R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ,
L = 10µH, DCR = 40.9mΩ



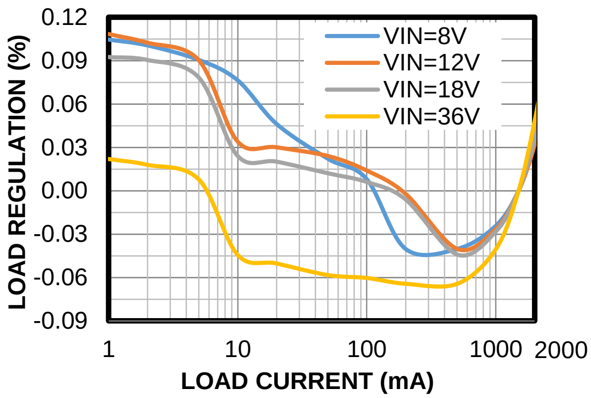
Efficiency vs. Load Current
V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 10µH
DCR = 40.9mΩ



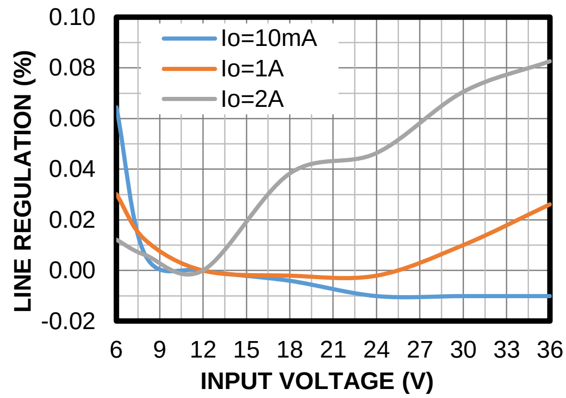
Efficiency vs. Load Current
V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 10µH
DCR = 40.9mΩ



Load Regulation
DCR = 22.1mΩ



Line Regulation
DCR = 22.1mΩ

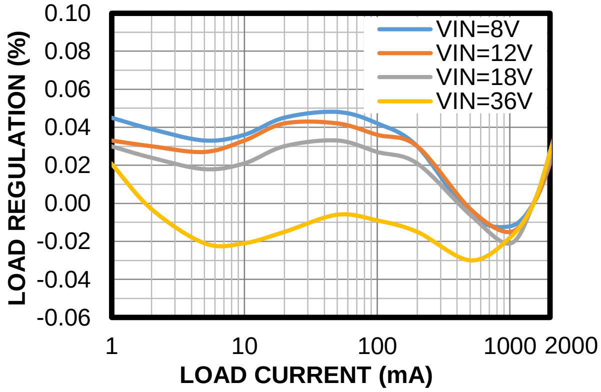


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

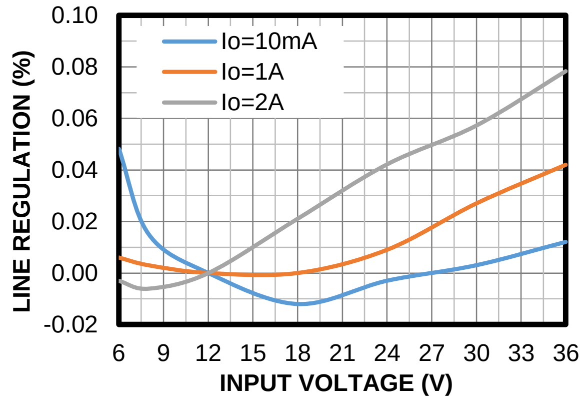
Load Regulation

V_{OUT} = 3.3V, DCR = 22.1mΩ



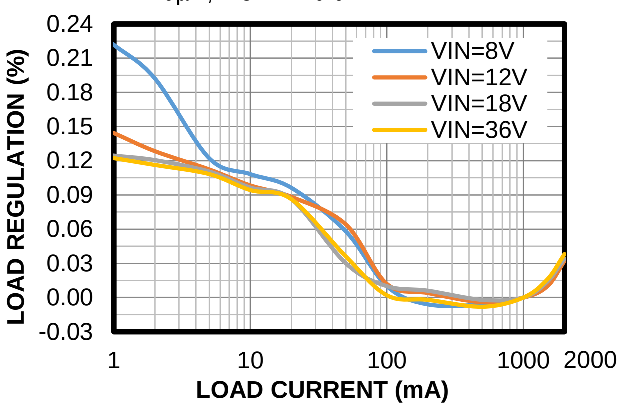
Line Regulation

V_{OUT} = 3.3V, DCR = 22.1mΩ



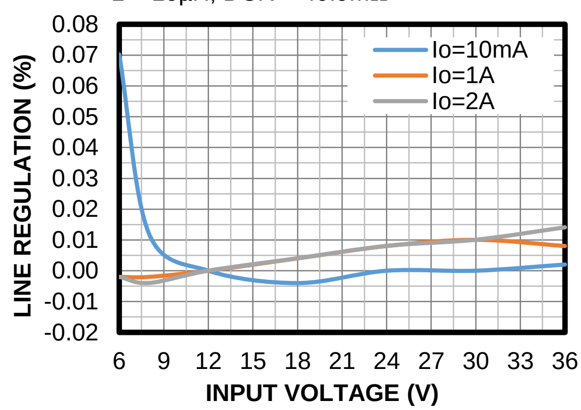
Load Regulation

f_{SW} = 415kHz, C_{OUT} = 47µF x 2,
L = 10µH, DCR = 40.9mΩ



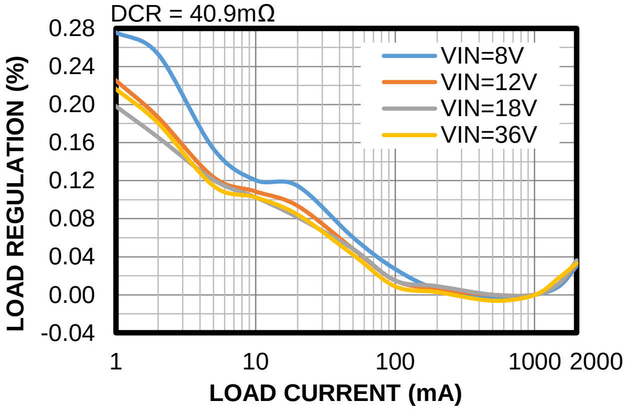
Line Regulation

f_{SW} = 415kHz, C_{OUT} = 47µF x 2,
L = 10µH, DCR = 40.9mΩ



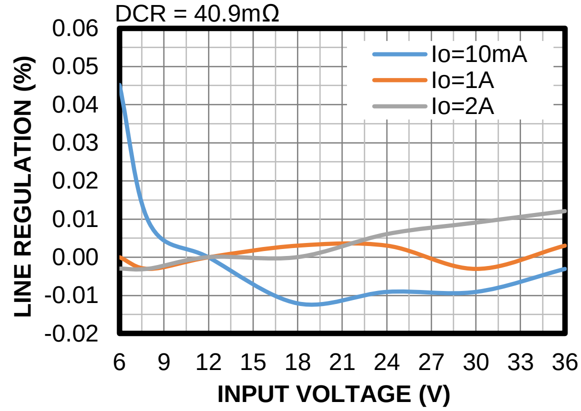
Load Regulation

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 47µF x 2, L = 10µH,
DCR = 40.9mΩ



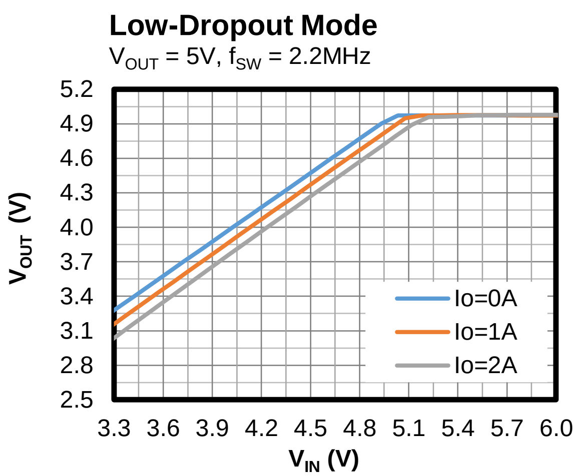
Line Regulation

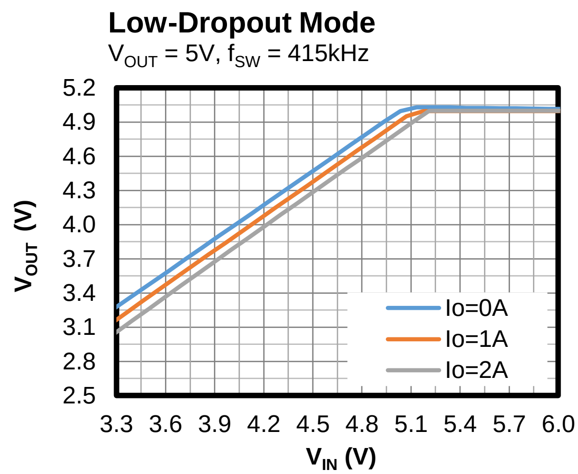
V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 47µF x 2, L = 10µH,
DCR = 40.9mΩ

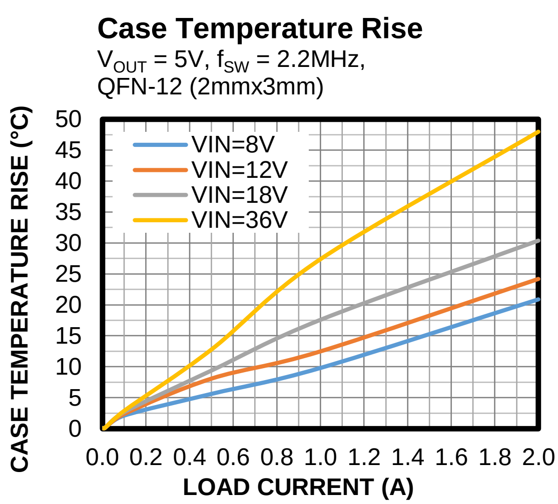


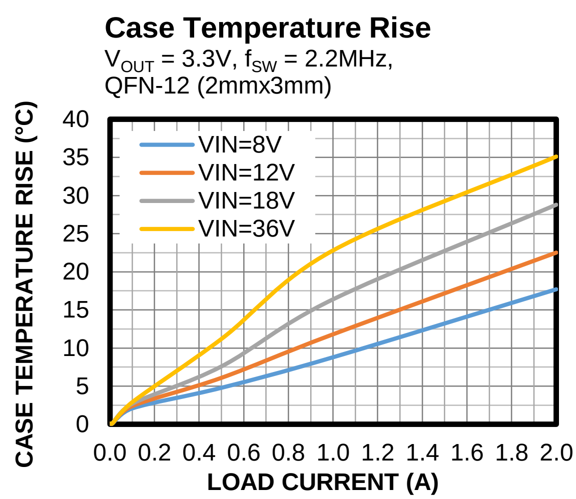
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

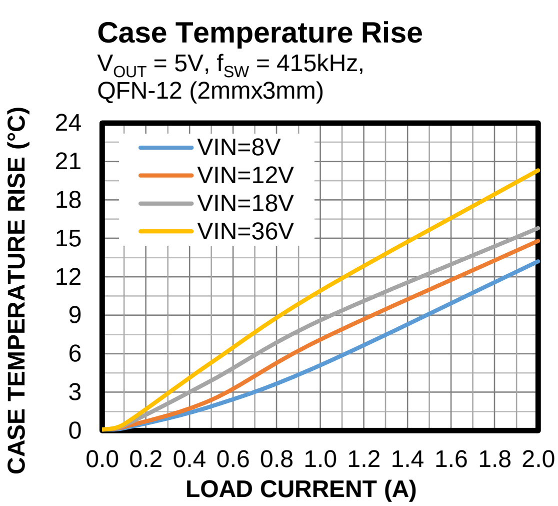
V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

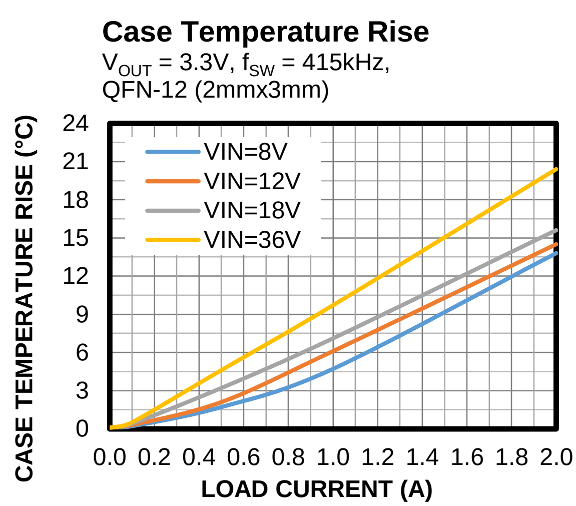






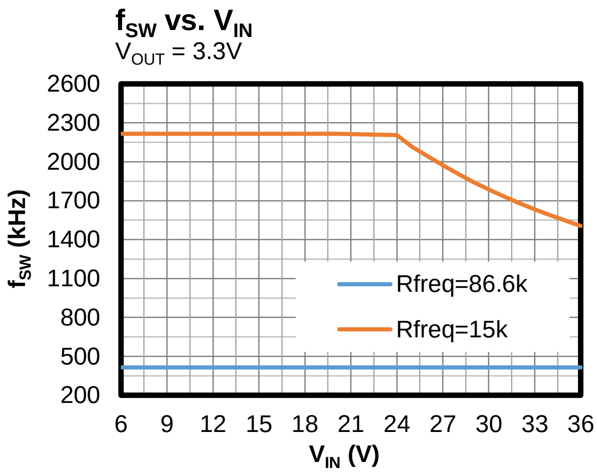


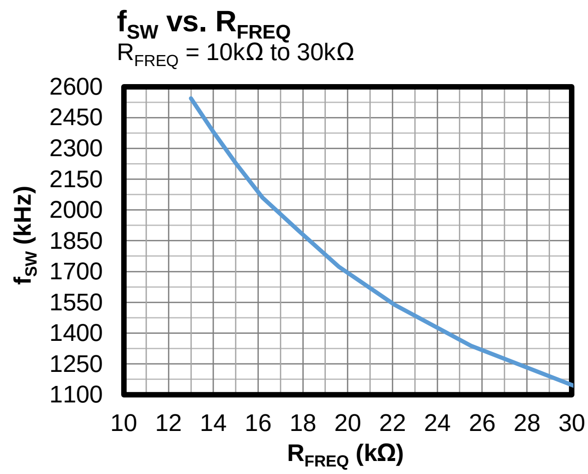


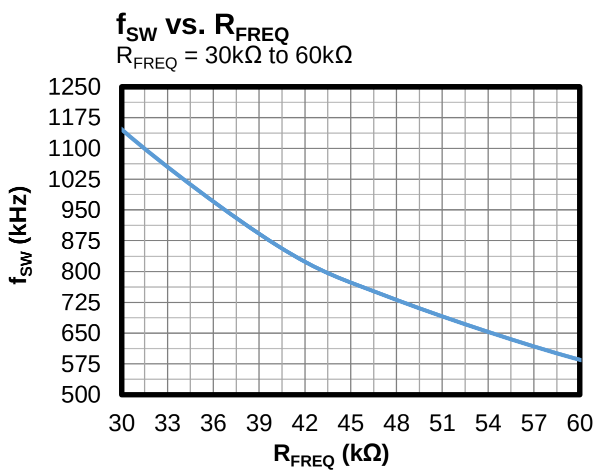


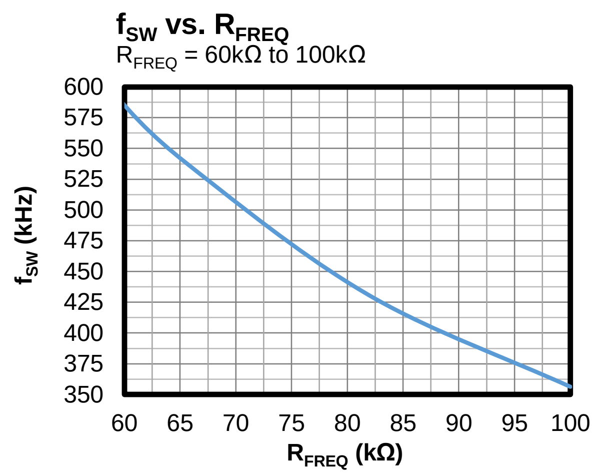
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.







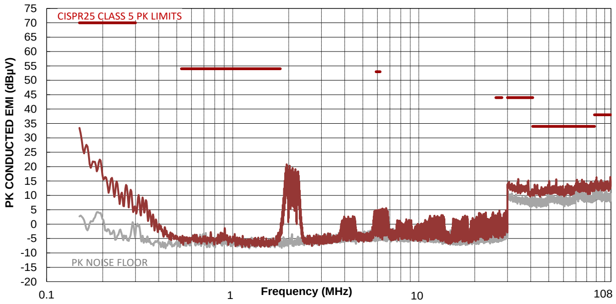


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted. (12)

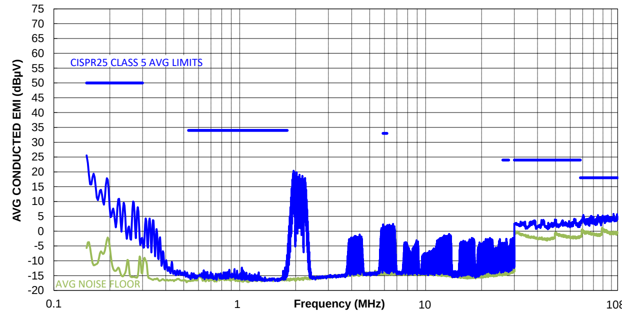
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



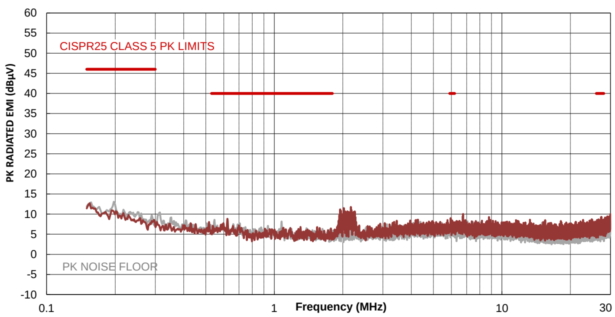
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



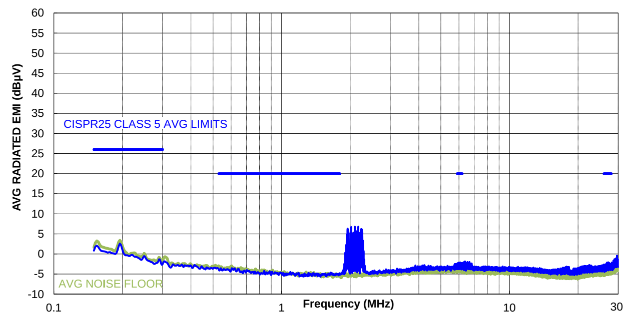
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



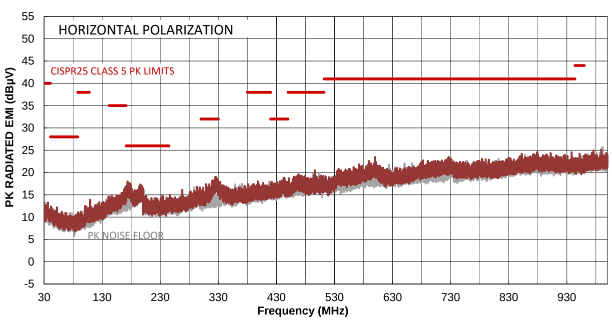
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



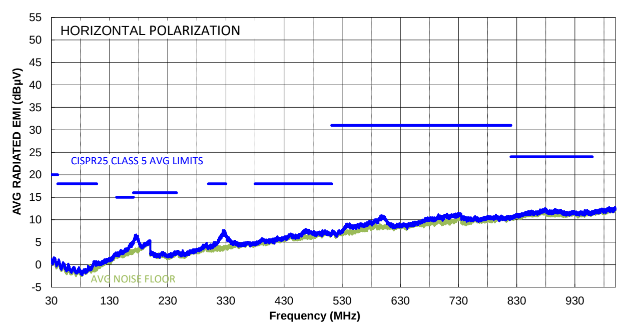
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

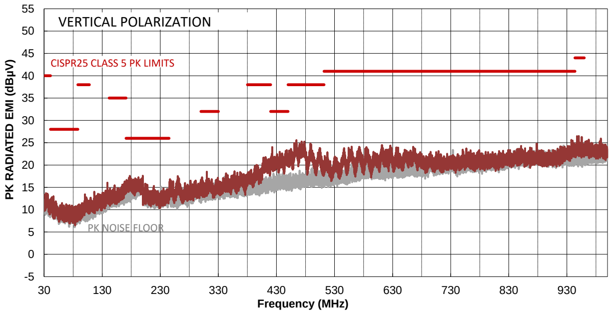


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted. (12)

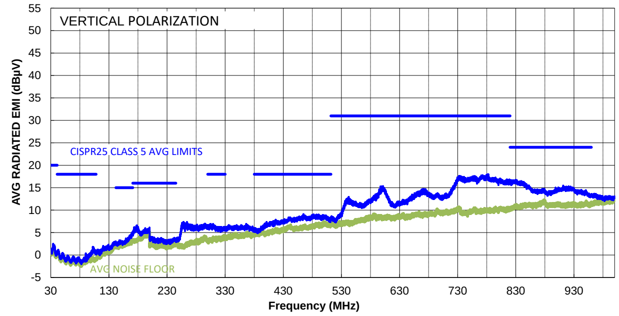
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



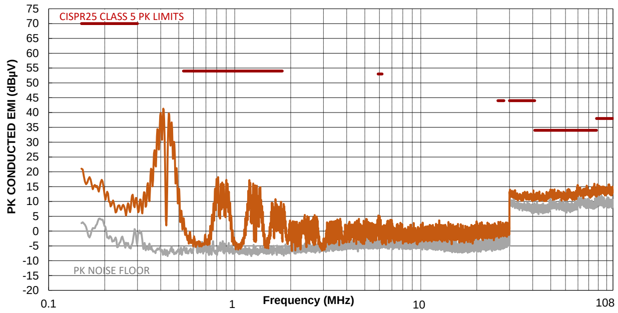
Note:

12) The EMC test results are based on the typical application circuit with EMI filters (see Figure 16 on page 38).

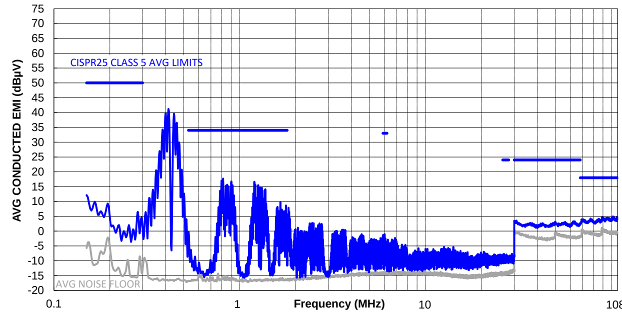
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 415kHz, L = 10µH, C_{OUT} = 47µF x 2, T_A = 25°C, unless otherwise noted. (13)

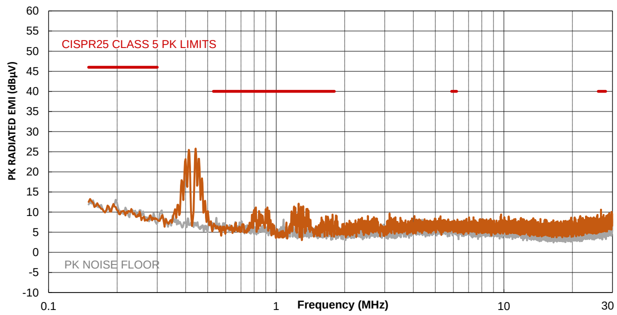
CISPR25 Class 5 Peak Conducted Emissions
150kHz to 108MHz



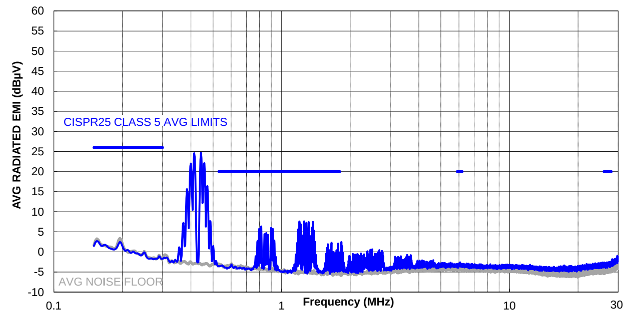
CISPR25 Class 5 Average Conducted Emissions
150kHz to 108MHz



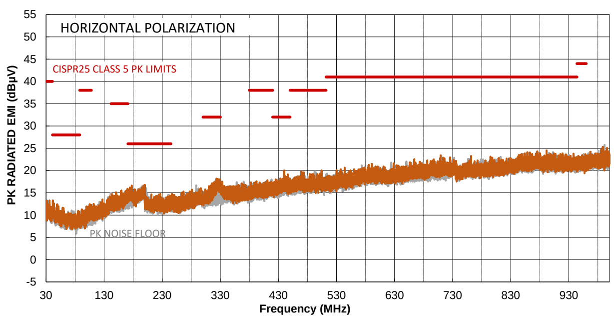
CISPR25 Class 5 Peak Radiated Emissions
150kHz to 30MHz



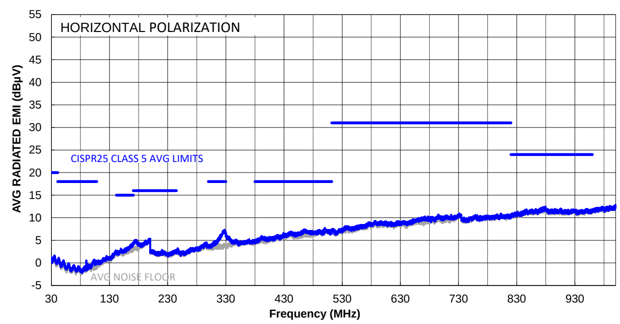
CISPR25 Class 5 Average Radiated Emissions
150kHz to 30MHz



CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions
Horizontal, 30MHz to 1GHz

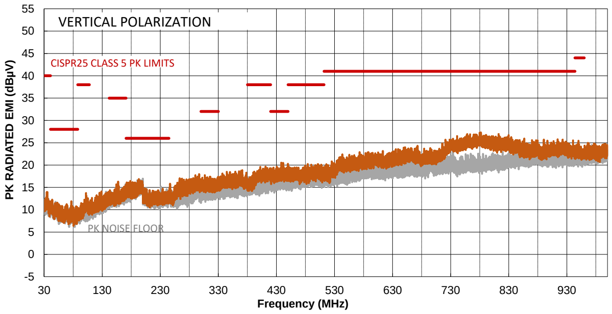


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 415kHz, L = 10µH, C_{OUT} = 47µF x 2, T_A = 25°C, unless otherwise noted. (13)

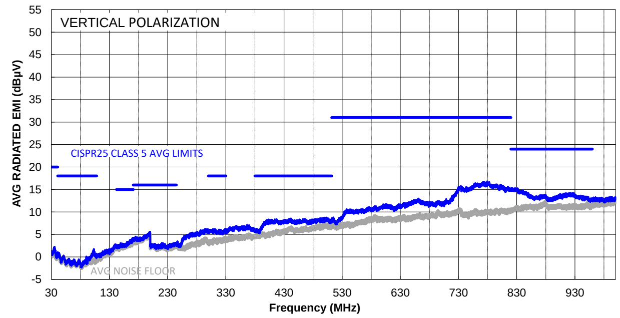
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

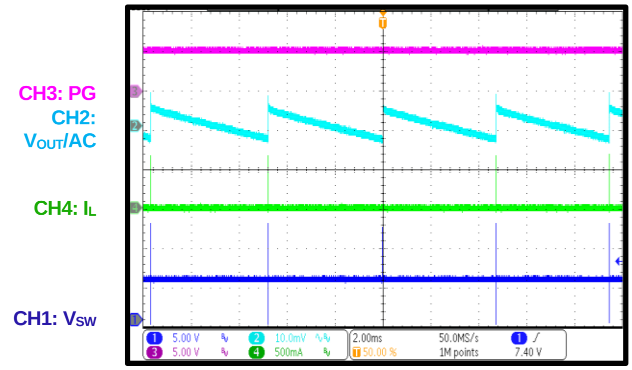
13) The EMC test results are based on the typical application circuit with EMI filters (see Figure 17 on page 39).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 22μF x 2, T_A = 25°C, unless otherwise noted.

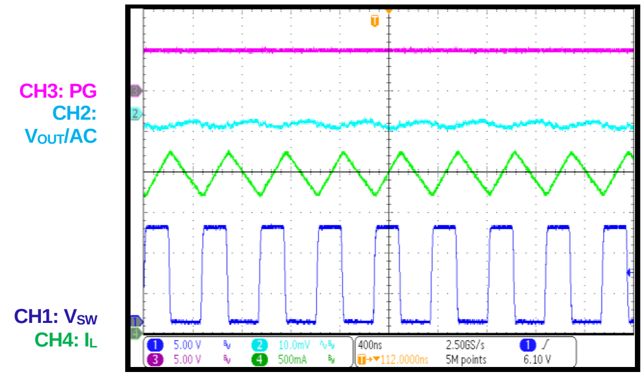
Steady State

I_{OUT} = 0A



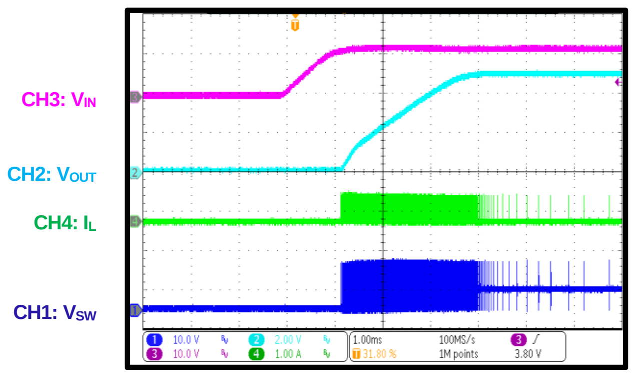
Steady State

I_{OUT} = 2A



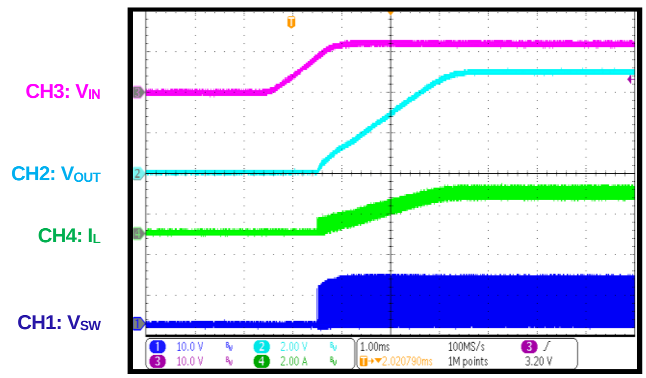
Start-Up through VIN

I_{OUT} = 0A



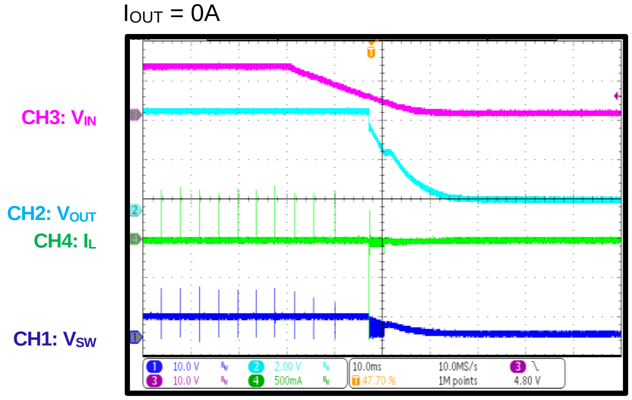
Start-Up through VIN

I_{OUT} = 2A



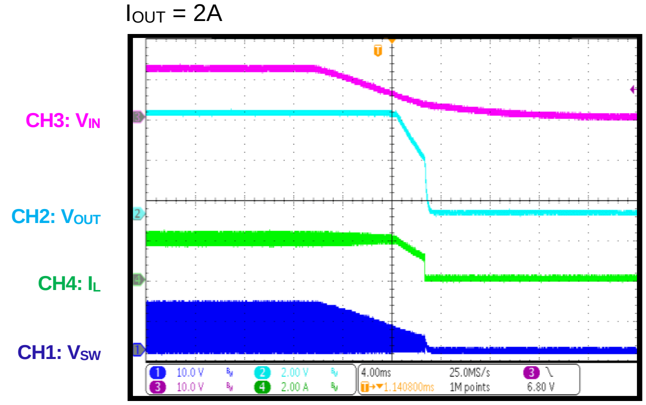
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 2A

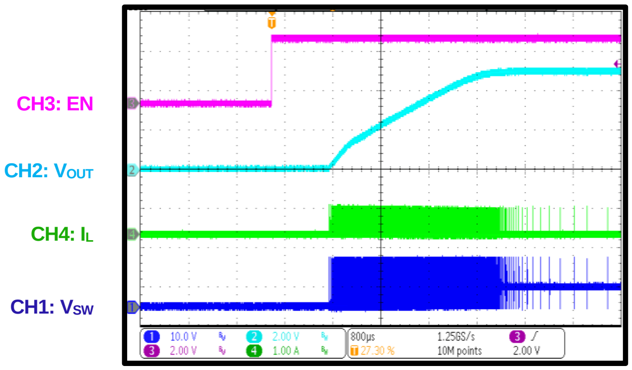


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

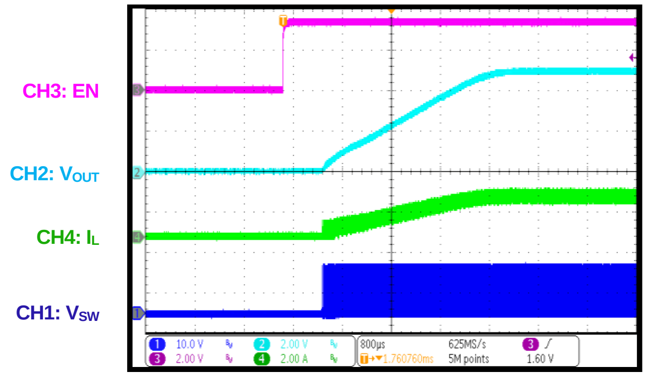
Start-Up through EN

I_{OUT} = 0A



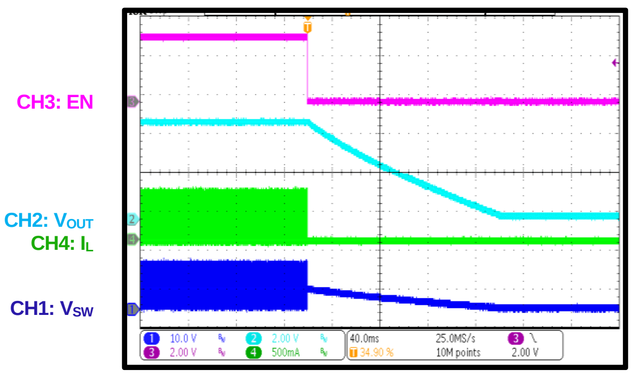
Start-Up through EN

I_{OUT} = 2A



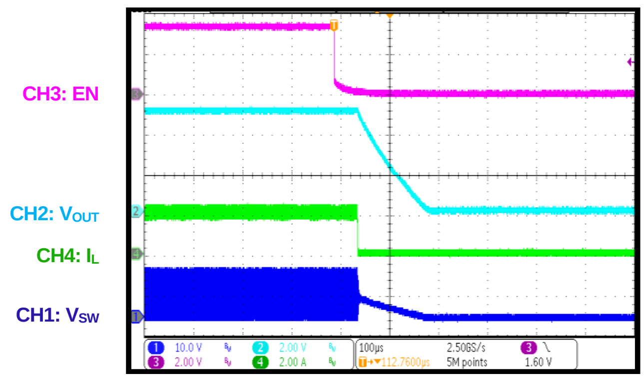
Shutdown through EN

I_{OUT} = 0A



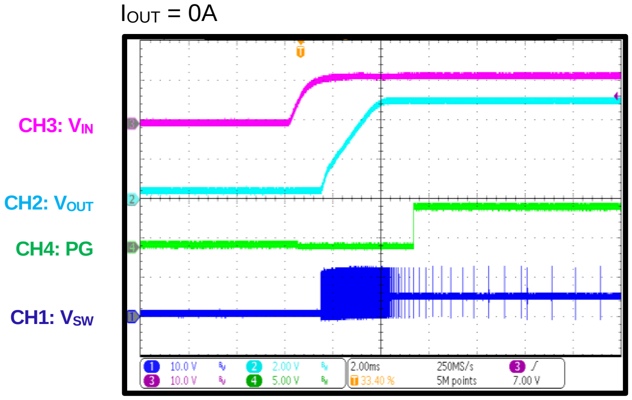
Shutdown through EN

I_{OUT} = 2A



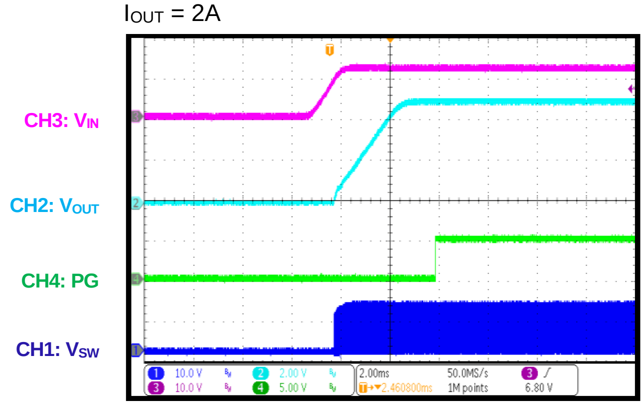
PG in Start-Up through VIN

I_{OUT} = 0A



PG in Start-Up through VIN

I_{OUT} = 2A

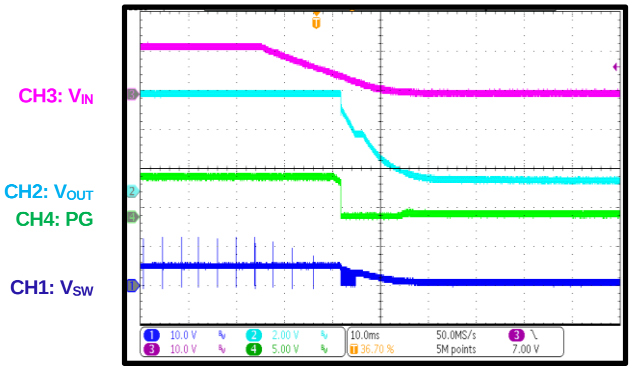


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

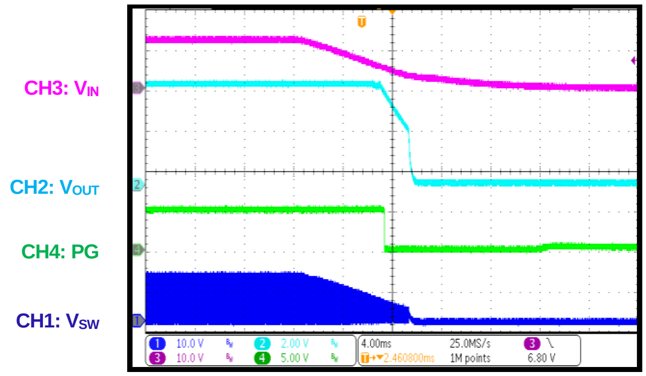
PG in Shutdown through VIN

I_{OUT} = 0A



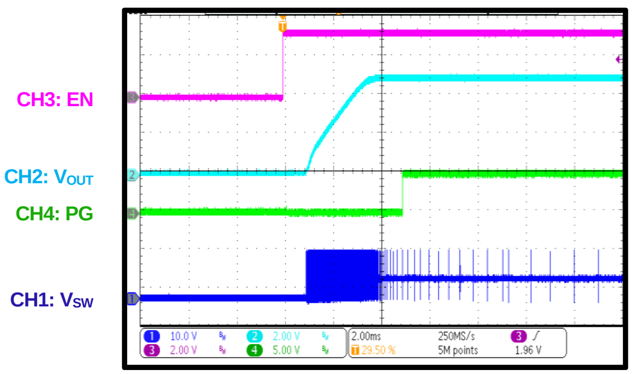
PG in Shutdown through VIN

I_{OUT} = 2A



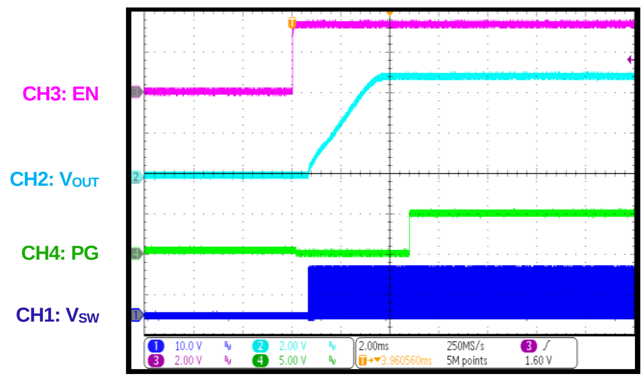
PG in Start-Up through EN

I_{OUT} = 0A



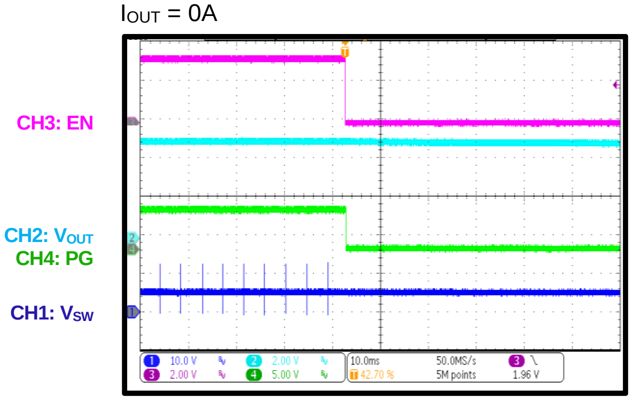
PG in Start-Up through EN

I_{OUT} = 2A



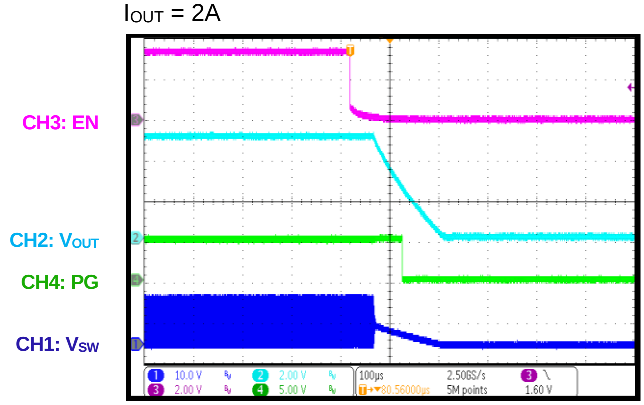
PG in Shutdown through EN

I_{OUT} = 0A



PG in Shutdown through EN

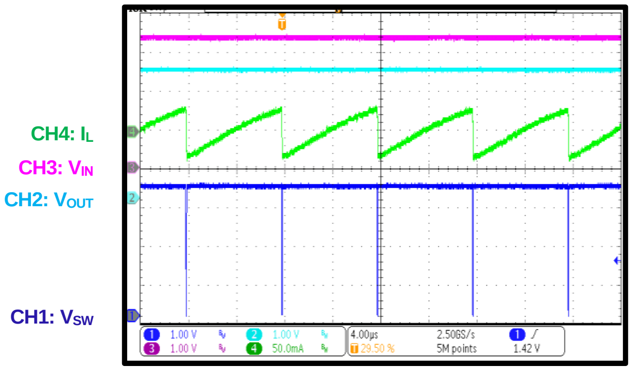
I_{OUT} = 2A



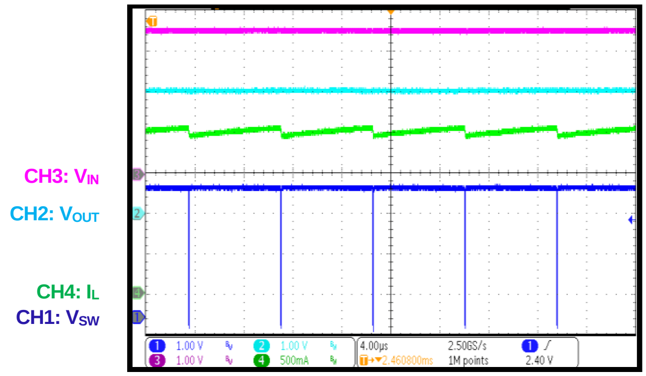
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 22μF x 2, T_A = 25°C, unless otherwise noted.

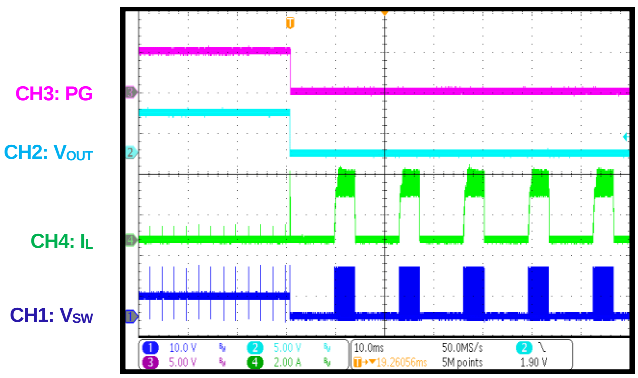
Low-Dropout Mode
I_{OUT} = 0A, V_{IN} = 3.3V



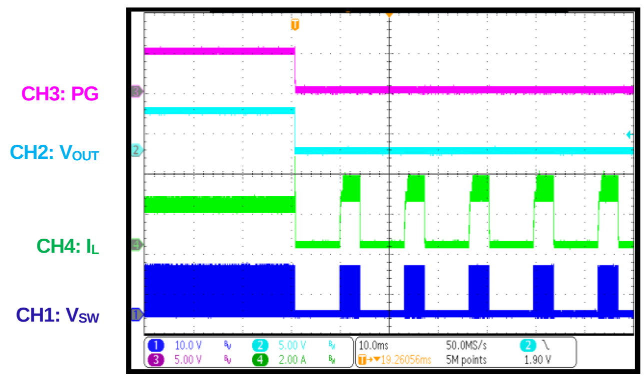
Low-Dropout Mode
I_{OUT} = 2A, V_{IN} = 3.3V



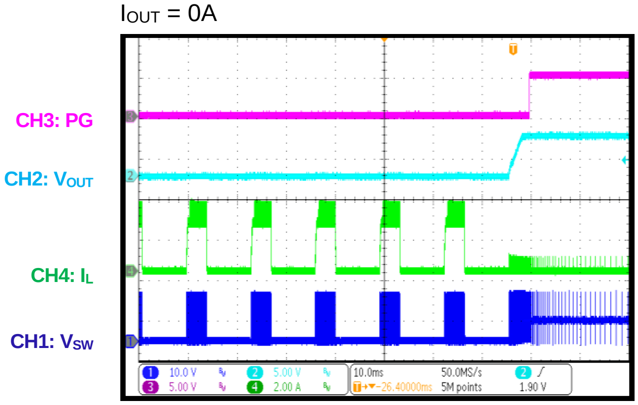
SCP Entry
I_{OUT} = 0A



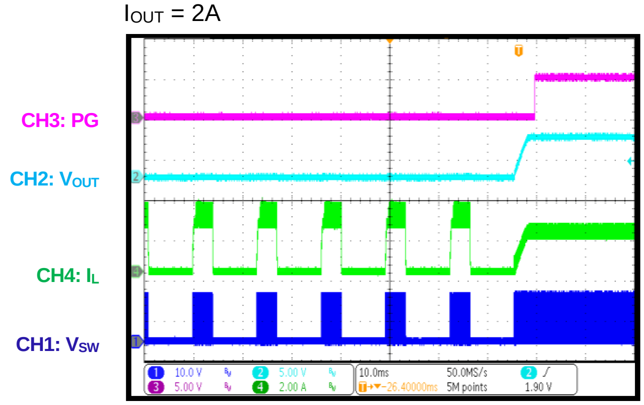
SCP Entry
I_{OUT} = 2A



SCP Recovery
I_{OUT} = 0A



SCP Recovery
I_{OUT} = 2A

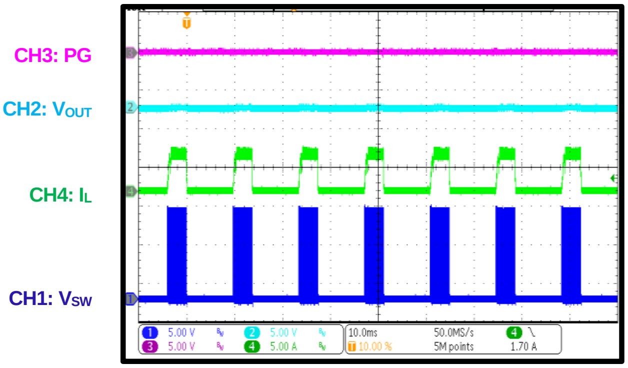


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

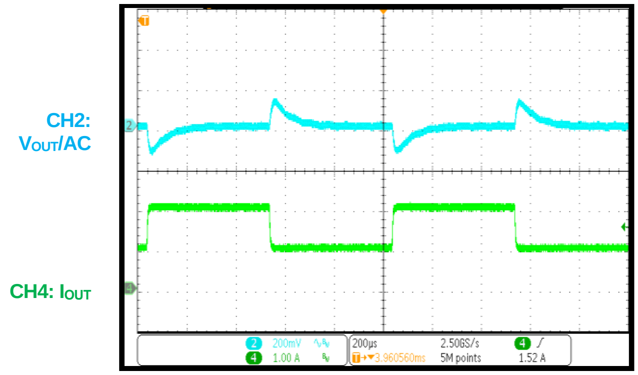
SCP Steady State

I_{OUT} = 0A



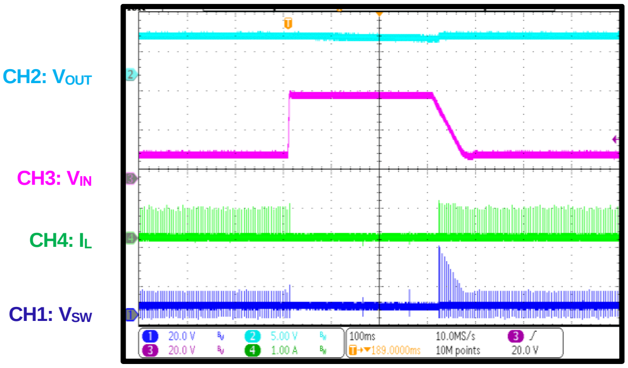
Load Transient

I_{OUT} = 1A to 2A, 1.6A/µs



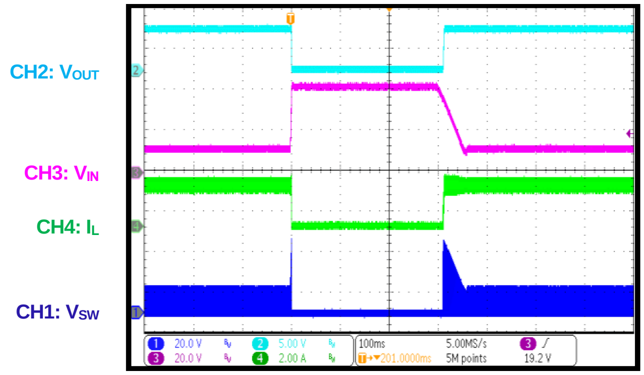
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 0A



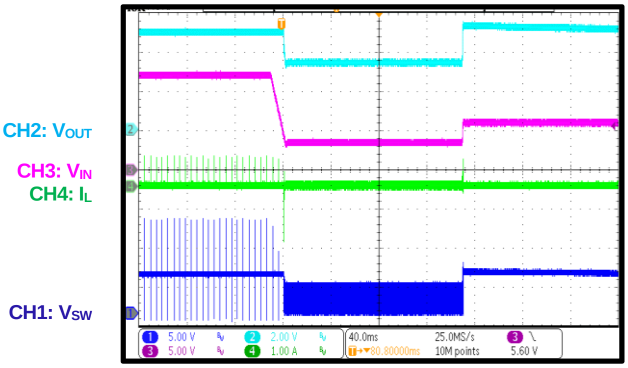
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 2A



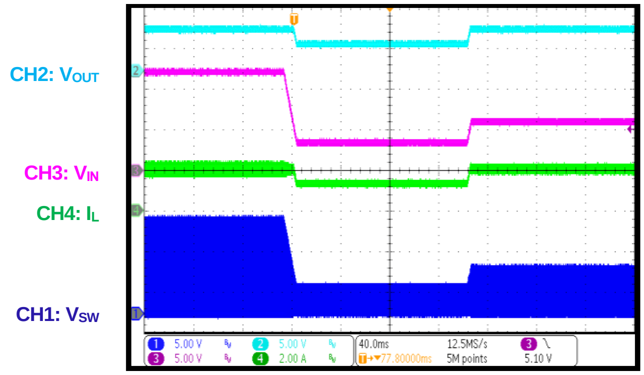
Cold Crank

V_{IN} = 12V to 3.3V to 6V, I_{OUT} = 0A



Cold Crank

V_{IN} = 12V to 3.3V to 6V, I_{OUT} = 2A

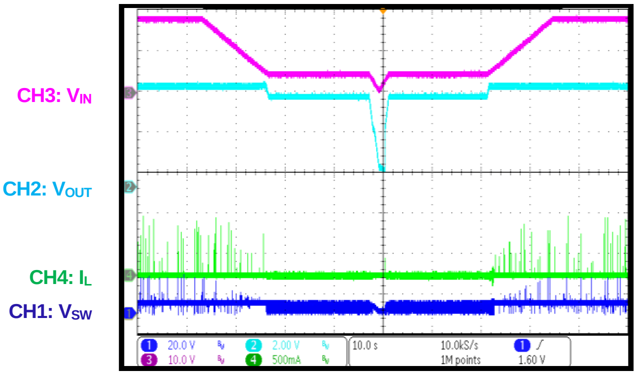


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

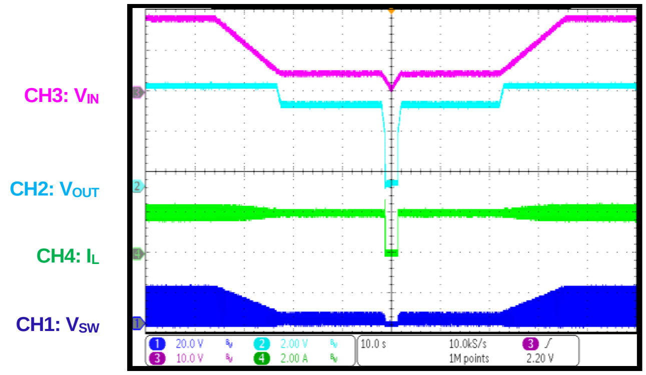
V_{IN} Ramping Down and Up

V_{IN} = 18V to 4.5V to 0V to 4.5V to18V,
I_{OUT} = 0A



V_{IN} Ramping Down and Up

V_{IN} = 18V to 4.5V to 0V to 4.5V to18V,
I_{OUT} = 2A



FUNCTIONAL BLOCK DIAGRAM

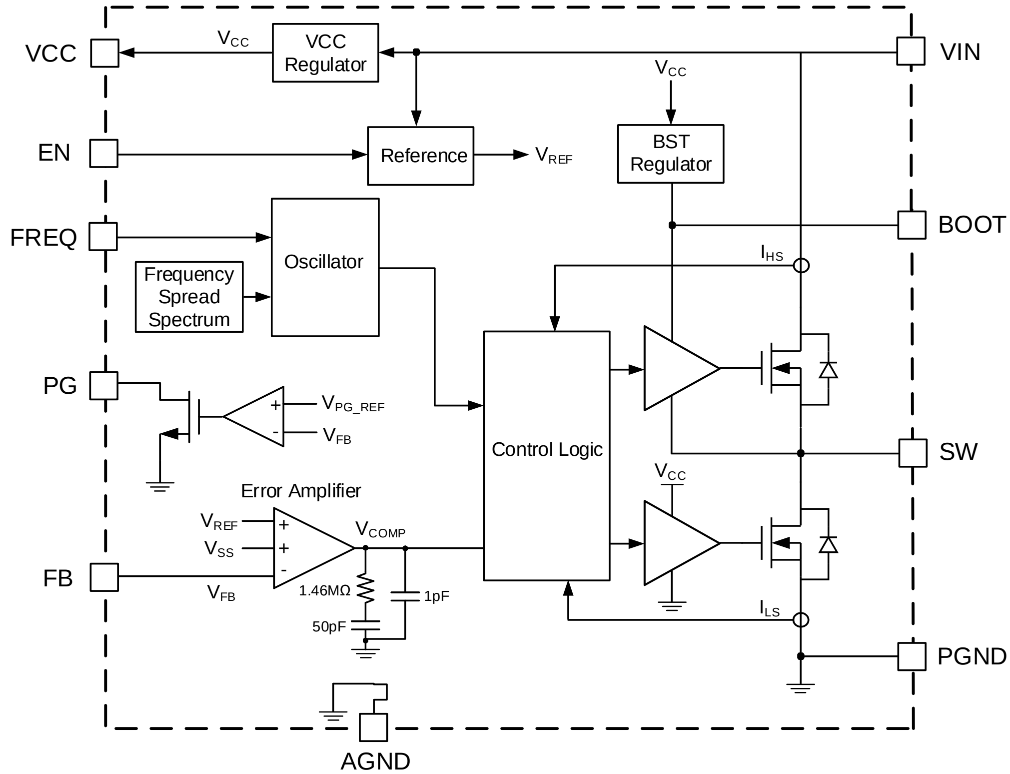


Figure 3: Functional Block Diagram (Adjustable-Output Version)

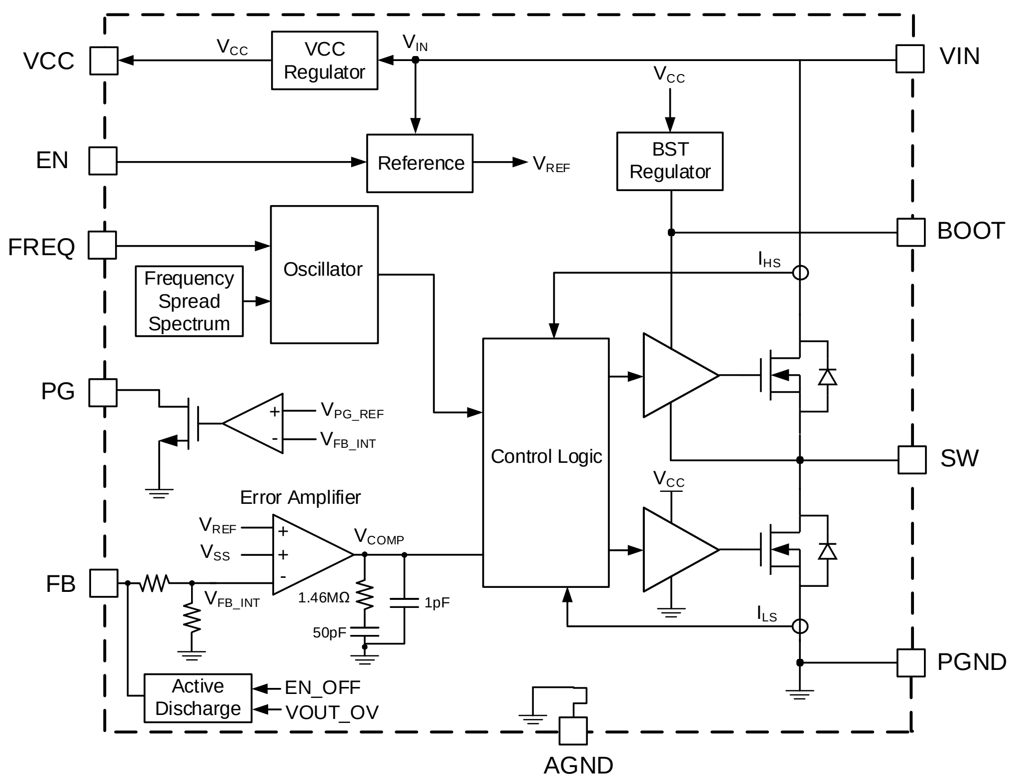


Figure 4: Functional Block Diagram (Fixed-Output Version)

OPERATION

The MPQ4322 is a synchronous, step-down switching converter with integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). It can achieve up to 2A of highly efficient output current (I_{OUT}) with peak current control mode.

The device features a wide input voltage (V_{IN}) range, 350kHz to 2.5MHz configurable switching frequency (f_{SW}), internal soft start (SS), and precise current limiting. The MPQ4322's low operational quiescent current (I_Q) makes it well-suited for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MPQ4322 operates with a fixed frequency, peak current mode control to regulate the output voltage (V_{OUT}). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the clock's rising edge, the HS-FET turns on and remains on until the control signal reaches the value set by the internal COMP voltage (V_{COMP}).

When the HS-FET is off, the LS-FET turns on immediately and remains on until the next cycle starts or the inductor current (I_L) falls below the zero-current detection (ZCD) threshold. The LS-FET remains off for at least the minimum off time (t_{OFF_MIN}) before the next cycle starts.

If the current in the HS-FET cannot reach the value set by V_{COMP} within one PWM period, then the HS-FET remains on and skips a turn-off operation. The HS-FET is forced on until it reaches the value set by V_{COMP}, or its maximum on time (t_{ON_MAX}) (7µs) is complete. This mode extends the duty cycle, which achieves low dropout when $V_{IN} \approx V_{OUT}$.

Light-Load Operation

The MPQ4322 operates in asynchronous advanced modulation (AAM) mode to optimize efficiency under light-load and no-load conditions.

The MPQ4322 enters asynchronous operation as I_L approaches 0A under light-load conditions. If the load decreases further, V_{COMP} drops to its set value, and the device enters AAM mode (see Figure 5).

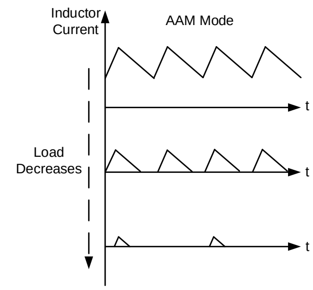


Figure 5: AAM Mode

In AAM mode, the internal clock resets once V_{COMP} reaches its set value. The crossover time is used as a benchmark for the next clock. If the load increases and V_{COMP} exceeds its set value, then the devices operates in continuous conduction mode (CCM) or discontinuous conduction mode (DCM) with a constant f_{SW}.

Error Amplifier (EA)

The error amplifier (EA) compares the feedback (FB) voltage (V_{FB}) with the internal reference voltage (V_{REF}) (typically 0.8V), and outputs a current proportional to the difference between the two voltages. This current charges the compensation network to form V_{COMP}, which controls the power MOSFET's duty cycle.

During normal operation, the minimum V_{COMP} is clamped to 0.5V, and the maximum V_{COMP} is clamped to 2.5V. If the IC shuts down, V_{COMP} is pulled down to GND internally.

Frequency Spread Spectrum (FSS)

The MPQ4322 employs a 15kHz modulation frequency with a 128-step triangular profile to spread the internal f_{SW} across a 20% (±10%) window. The steps vary with the set f_{SW} to ensure that the exact f_{SW} steps cycle by cycle (see Figure 6).

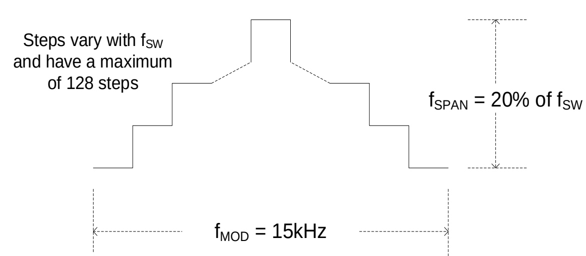


Figure 6: Frequency Spread Spectrum

Sidebands are created by modulating f_{SW} via the triangle modulation waveform. The emission power of the fundamental f_{SW} and its harmonics are distributed into smaller pieces. This significantly reduces peak EMI noise.

Soft Start (SS)

Soft start (SS) is implemented to prevent V_{OUT} from overshooting during start-up. The soft-start time (t_{SS}) is fixed internally.

Once SS is initiated, the soft-start voltage (V_{SS}) rises from 0V to 1.2V with a set slew rate. If V_{SS} drops below the internal V_{REF} (0.8V), then V_{SS} takes over and the EA uses V_{SS} as its reference. If V_{SS} exceeds V_{REF}, then V_{REF} regains control.

During start-up through EN, the first pulse occurs after about 830µs. During this period, the VCC voltage (V_{CC}) is regulated, the internal bias is generated, and the compensator network is charged. After another 2.9ms, V_{OUT} ramps up and reaches its set value. SS is complete after another 1.5ms. PG is also pulled high after a 70µs delay.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} during start-up, this means that the output has a pre-biased voltage. Both the HS-FET and LS-FET remain off until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown prevents the device from operating at exceedingly high temperatures and protects it from thermal runaway. If the die temperature exceeds its upper threshold (about 175°C), the device shuts down. Once the temperature drops below 155°C, the device restarts and resumes normal operation.

Start-Up and Shutdown

If both V_{IN} and the EN voltage (V_{EN}) exceed their respective thresholds, the IC starts up. The reference block starts up first to generate a stable V_{REF} and reference currents. Then the internal regulator is enabled to provide a stable supply for the remaining circuitries.

Once the internal supply rail is up, the internal circuits begin operating. If the BOOT voltage (V_{BOOT}) does not reach its refresh rising threshold (about 2.5V), then the LS-FET turns on to charge BOOT. The HS-FET remains off during this charging period. When the soft start block is enabled, V_{OUT} starts to ramp up slowly and smoothly until it reaches its target voltage. V_{OUT} should reach its target voltage within 5ms.

Three events can shut down the chip: EN going low, V_{IN} falls below its UVLO threshold, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} is pulled down and the floating driver disables the HS-FET.

APPLICATION INFORMATION

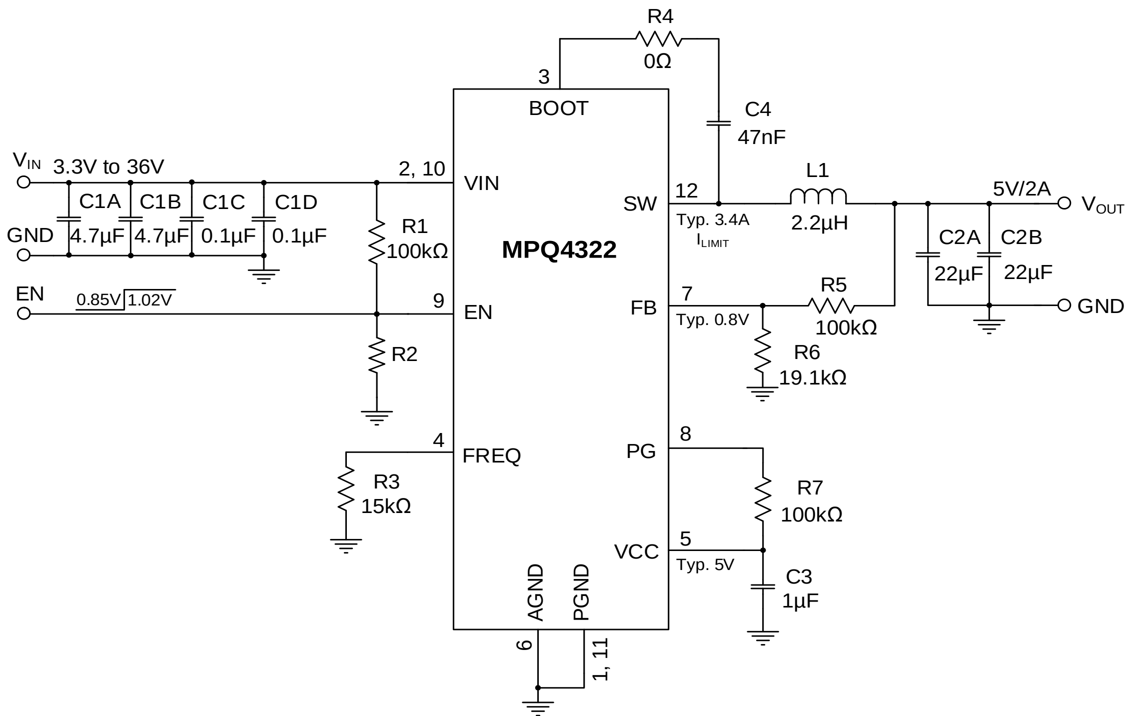


Figure 7: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz)

Table 1: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1, 11	PGND	-	GND Connection (GND, Pins 1, 6, and 11)
2, 10	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors (VIN, Pins 2 and 10)
3	BOOT	R4, C4	Floating Driver and Bootstrap Charging (BOOT, Pin 3)
4	FREQ	R3	Setting the Switching Frequency (FREQ, Pin 4)
5	VCC	C3	Internal VCC (VCC, Pin 5)
6	AGND	-	GND Connection (GND, Pins 1, 6, and 11)
7	FB	R5, R6	Feedback (FB, Pin 7)
8	PG	R7	Power Good (PG) Indicator (PG, Pin 8)
9	EN	R1, R2	Enable and Under-Voltage Lockout (UVLO) (EN, Pin 9)
12	SW	L1, C2A, C2B	Selecting the Inductor (SW, Pin 12) Selecting the Output Capacitors (SW, Pin 12)

GND Connection (Pins 1, 6, and 11)

See the PCB Layout Guidelines section on page 35 for more details.

Selecting the Input Capacitors (VIN, Pins 2 and 10)

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and small temperature coefficients.

For most applications, a 4.7µF to 10µF capacitor is sufficient. It is strongly recommended to use an additional, lower-value capacitor (e.g. 0.1µF) with a small package size (e.g. 0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and PGND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in C_{IN} (I_{CIN}) can be estimated with Equation (1):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \qquad (1)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (2):

$$I_{CIN} = \frac{I_{LOAD}}{2} \qquad (2)$$

For simplification, choose C_{IN} with an RMS current rating greater than half of the maximum load current (I_{LOAD_MAX}) C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (3):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \qquad (3)$$

Floating Driver and Bootstrap Charging (BOOT, Pin 3)

The BOOT capacitor (C4, also called C_{BOOT}) is recommended to be between 22nF to 100nF.

It is not recommended to place a resistor (R_{BOOT}) in series with C_{BOOT}, unless there is a strict EMI requirement. R_{BOOT} reduces EMI and voltage stress at high input voltages; however, it also generates additional power consumption and reduces efficiency. If necessary, R_{BOOT} should be less than 4Ω.

The voltage between the BOOT and SW pins ($V_{BOOT-SW}$) is regulated to about 5V by the dedicated, internal bootstrap regulator. If $V_{BOOT-SW}$ drops below its regulated value, then an N-channel MOSFET pass transistor connected between VCC and BOOT turns on to charge C_{BOOT}. The external circuit should provide enough voltage headroom to facilitate the charging.

When the HS-FET is on, V_{BOOT} exceeds V_{CC} so C_{BOOT} cannot charge. At higher duty cycle operation, the time available for bootstrap charging is shorter, so C_{BOOT} may not charge sufficiently. In this case, the external circuit has insufficient voltage and time to charge C_{BOOT}. External circuitry can be used to ensure that V_{BOOT} remains within its normal operating range.

If V_{BOOT} falls below its UVLO threshold, then the HS-FET turns off and the LS-FET turns on for t_{OFF_MIN} to refresh V_{BOOT} via the set f_{SW}.

Setting the Switching Frequency (FREQ, Pin 4)

A frequency resistor (R3, also called R_{FREQ}) can be used to set f_{SW} (see Table 2 on page 32 and the f_{SW} vs. R_{FREQ} curves on page 16).

Place R_{FREQ} between the FREQ pin and AGND as close as possible to the IC to configure the MPQ4322's f_{SW}. Table 2 on page 32 shows the relationship between f_{SW} and R_{FREQ}.

Table 2: f_{SW} vs. R_{FREQ}

R_{FREQ} (kΩ)	f_{SW} (kHz)	R_{FREQ} (kΩ)	f_{SW} (kHz)
100	355	30.1	1150
93.1	385	26.1	1300
86.6	415	22.6	1450
80.6	450	20.5	1600
75	480	19.6	1750
68.1	520	17.8	1900
59	600	16.2	2050
51.1	700	15	2200
40.2	850	14.3	2350
34.8	1000	13.3	2500

It is not possible to have both a high f_{SW} and V_{IN} due to the HS-FET's limited minimum on time (t_{ON_MIN}). The MPQ4322's control loop automatically sets the maximum possible f_{SW} to the set frequency, which also reduces excessive power loss. V_{OUT} is regulated by varying the duration of the HS-FET's off time, which reduces f_{SW}.

The MPQ4322 is guaranteed to adhere to the HS-FET's t_{ON_MIN}. An advantage of this method is that the device operates at the target f_{SW} for as long as possible, and f_{SW} only changes when the device operates at high input voltages. For more details, see the f_{SW} vs. V_{IN} curve on page 16, where R_{FREQ} = 15kΩ and V_{OUT} = 3.3V.

Internal VCC (VCC, Pin 5)

The VCC capacitor (C3) is recommended to be 1µF.

Most of the internal circuitry is powered by the internal, 5V VCC regulator. This regulator uses V_{IN} as its input and operates across the entire V_{IN} range. If V_{IN} exceeds 5V, then V_{CC} is in full regulation. If V_{IN} drops below 5V, then the VCC output degrades.

Feedback (FB, Pin 7)

For the adjustable-output version, the typical feedback voltage (V_{FB}) is 0.8V. The external resistor dividers (R6 and R5) connected to FB set V_{OUT} (see Figure 8).

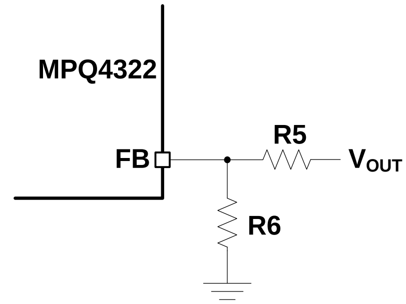


Figure 8: Feedback Divider Network for Adjustable-Output Version

Calculate R6 with Equation (4):

$$R6 = \frac{R5}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

For the fixed-output version, the FB resistor dividers (R_{FB1} and R_{FB2}) are integrated internally (see Figure 9). Connect FB directly to the output to set V_{OUT}. The following fixed outputs can be selected: 1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, 5V.

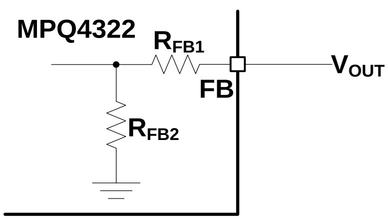


Figure 9: Feedback Divider Network for Fixed-Output Version

Table 3 shows the relationship between the internal R_{FB} and V_{OUT}.

Table 3: R_{FB} vs. V_{OUT}

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
1	64	256
1.8	320	256
2.5	544	256
3	704	256
3.3	800	256
3.8	960	256
5	1344	256

Power Good Indicator (PG, Pin 8)

The PG resistor (R7, also called R_{PG}) should have a resistance of about 100kΩ.

The MPQ4322 includes an open-drain power good (PG) output that indicates whether V_{OUT} is within its nominal range.

If using PG, connect it to a logic high level power source (e.g. 3.3V) via a pull-up resistor. If V_{OUT} is within 94.5% to 105.5% of the nominal voltage, PG goes high; if V_{OUT} exceeds 107% or falls below 93% of the nominal voltage, PG goes low. Float PG if it is not used.

Enable and Under-Voltage Lockout (UVLO) (EN, Pin 9)

The EN pin is a digital control pin that turns the converter on and off.

Enabled by an External Logic High/Low Signal

If the EN voltage (V_{EN}) reaches about 0.7V, the bottom gate turns on when V_{IN} exceeds about 2.7V. The bottom gate then provides an accurate reference voltage for the EN threshold. Pull EN above its 1V rising threshold to enable the part. Pull EN below 0.85V to shut down the part. There is no internal pull-up or pull-down resistor connected to the EN pin. To avoid an uncertain state, do not float EN. If the control signal cannot give an accurate high or low logic, then an external pull-up or pull-down resistor is required.

Configurable V_{IN} Under-Voltage Lockout (UVLO) Threshold

The MPQ4322 has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3.65V, and the falling threshold is about 2.9V. For applications that require a higher UVLO, place an external resistor divider between VIN and EN to raise the equivalent UVLO threshold (see Figure 10).

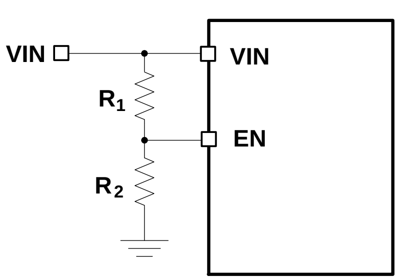


Figure 10: Configurable UVLO via the EN Divider

The UVLO rising threshold ($V_{IN\_UVLO\_RISING}$) can be calculated with Equation (5):

$$V_{IN\_UVLO\_RISING} = (1 + \frac{R_1}{R_2}) \times V_{EN\_RISING} \quad (5)$$

Where V_{EN_RISING} is 1.02V.

The UVLO falling threshold ($V_{IN\_UVLO\_FALLING}$) can be calculated with Equation (6):

$$V_{IN\_UVLO\_FALLING} = (1 + \frac{R_1}{R_2}) \times V_{EN\_FALLING} \quad (6)$$

Where $V_{EN\_FALLING}$ is 0.85V.

If EN is not used to turn the IC on and off, connect EN to a high-voltage source (e.g. VIN) to turn the device on by default.

Selecting the Inductor and Output Capacitors (SW, Pin 12)

The inductance (L1) can be estimated with Equation (7):

$$L1 = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

A 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, it also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current.

The peak inductor current (I_{L_PEAK}) can be calculated with Equation (8):

$$I_{L\_PEAK} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Choose an inductor that does not saturate under I_{L_PEAK}.

The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor (C_{OUT}).

Selecting the Output Capacitors (SW, Pin 12)

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low-ESR capacitors to keep ΔV_{OUT} low.

For ceramic capacitors**,** the capacitance dominates the impedance at f_{SW} and causes the majority of the output voltage ripple (ΔV_{OUT}). For simplification, ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

When selecting C_{OUT}, consider the allowable overshoot in V_{OUT} if the load is suddenly removed. In this scenario, energy stored in the inductor is transferred to C_{OUT}, causing its voltage to rise. To achieve an optimal overshoot relative to the regulated voltage, C_{OUT} can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^{2} \times L}{V_{OUT}^{2} \times ((V_{OUT\_MAX} / V_{OUT})^{2} - 1)} \quad (12)$$

Where V_{OUT_MAX} / V_{OUT} is the allowable maximum overshoot.

After calculating the capacitance that meets both the ripple and overshoot requirements, choose the larger capacitance. When V_{OUT} is below 3.3V, it is recommended for C_{OUT} to exceed 100µF.

The C_{OUT} characteristics also affect the stability of the regulation system. The MPQ4322 can be optimized for a wide range of capacitances and ESR values.

V_{IN} Over-Voltage Protection (OVP)

If V_{IN} exceeds its over-voltage (OV) rising threshold (typically 37.5V), the MPQ4322 stops switching. Once V_{IN} drops below the OV falling threshold (typically 36.5V), the device resumes normal operation.

Peak and Valley Current Limit

Both the HS-FET and LS-FET have cycle-by-cycle current limit protection. If the inductor current (I_L) reaches the high-side (HS) peak current limit (typically 3.4A) during the HS-FET on time, the HS-FET is immediately forced off to prevent the current from rising further.

When the LS-FET is on, the next clock's rising edge is held until I_L drops below the low-side (LS) valley current limit (typically 2.7A). Once the HS-FET turns on again, I_L drops to a sufficiently low value. This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

Short-Circuit Protection (SCP)

If the output is shorted to ground and V_{OUT} drops below 70% of its nominal output, then the MPQ4322 shuts down momentarily and discharges V_{SS}. Once V_{SS} is fully discharged, the device initiates SS and attempts normal operation. This hiccup process is repeated until the fault is removed.

Output Over-Voltage Protection (OVP) and Discharge

If V_{OUT} exceeds 130% of its nominal voltage, the MPQ4322 stops switching. An internal 75Ω discharge path from FB to AGND discharges V_{OUT}. This discharge path is only active if the output is fixed. Once V_{OUT} drops to 125% of its nominal voltage, the part resumes switching. The fixed-output discharge path is also disabled.

For the fixed-output version, the V_{OUT} discharge path also activates if a shutdown through EN occurs while V_{CC} exceeds its UVLO rising threshold. Once V_{CC} drops below its UVLO threshold, the discharge path is deactivated.

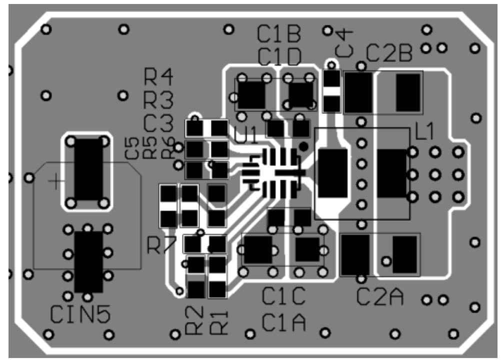
PCB Layout Guidelines (14)

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 11 and follow the guidelines below:

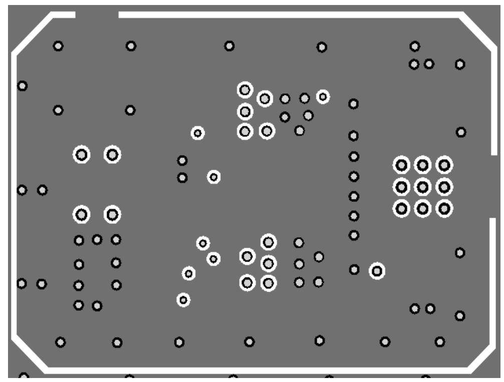
1. Place the symmetric input capacitors as close to VIN and PGND as possible.
2. Connect a large ground plane directly to PGND.
3. If the bottom layer is a ground plane, add vias near PGND.
4. Ensure that the high-current paths at PGND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and AGND as possible.
8. Route SW and BOOT away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip, and ensure that the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

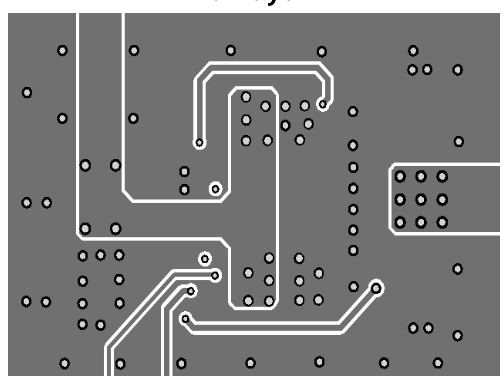
14) The recommended PCB layout is based on Figure 7 on page 30.



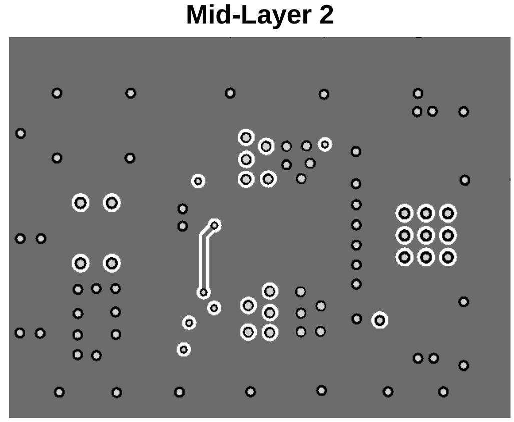
Top Silk and Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer and Bottom Silk

Figure 11: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

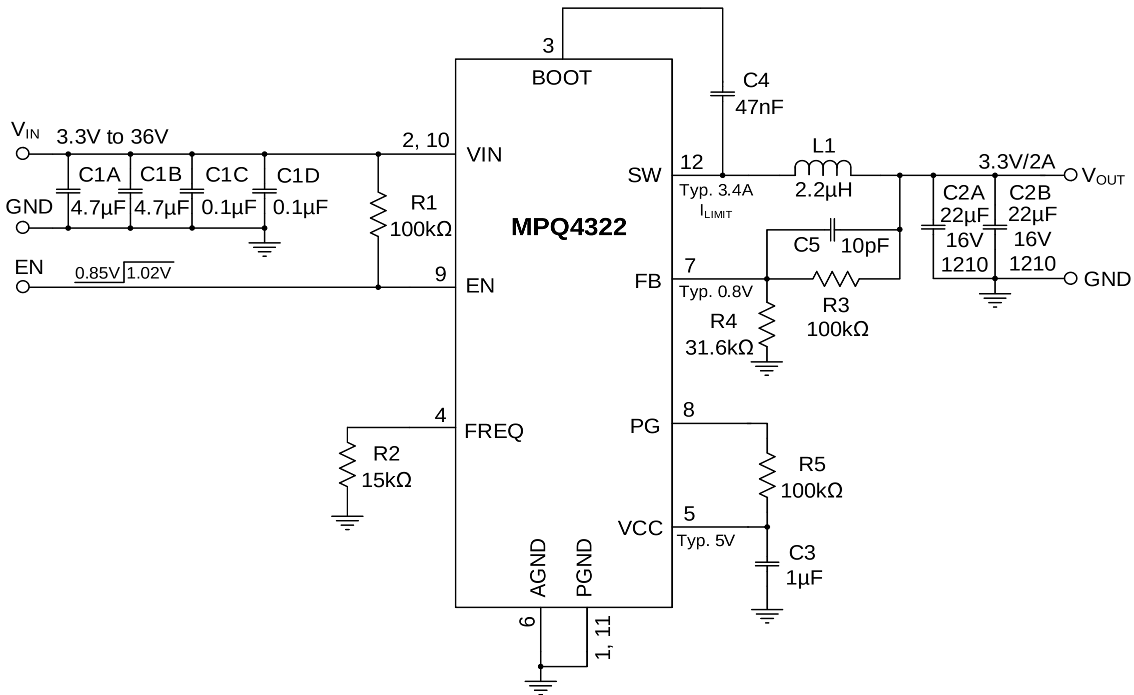


Figure 12: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 2.2MHz)

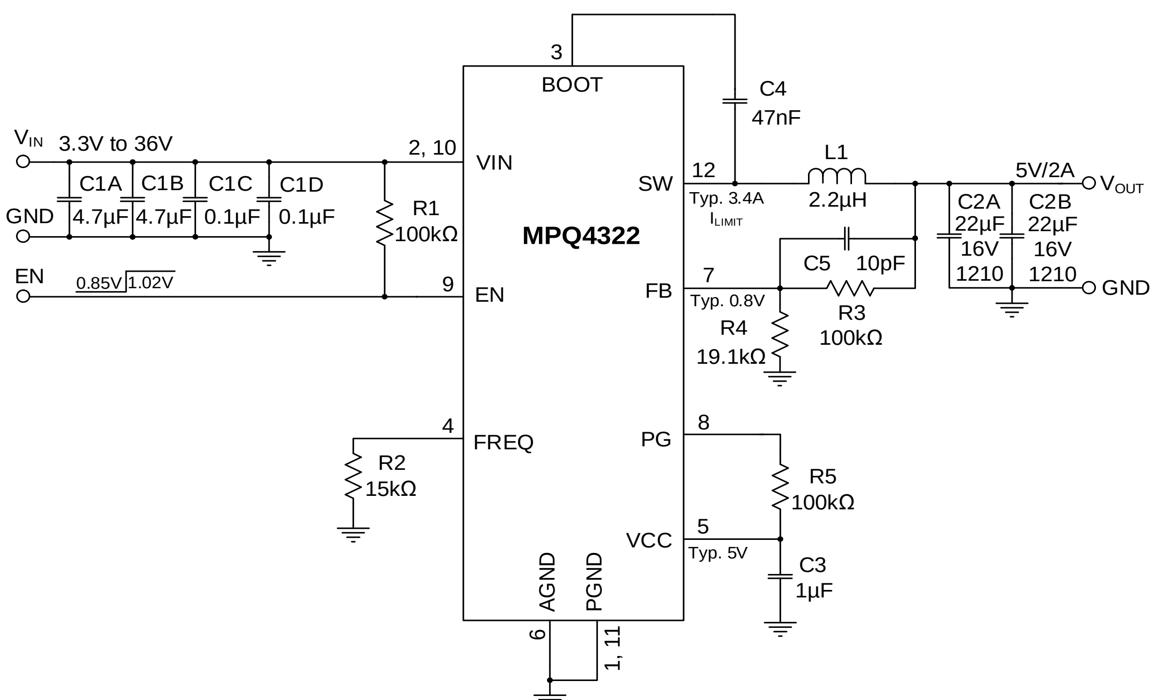


Figure 13: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

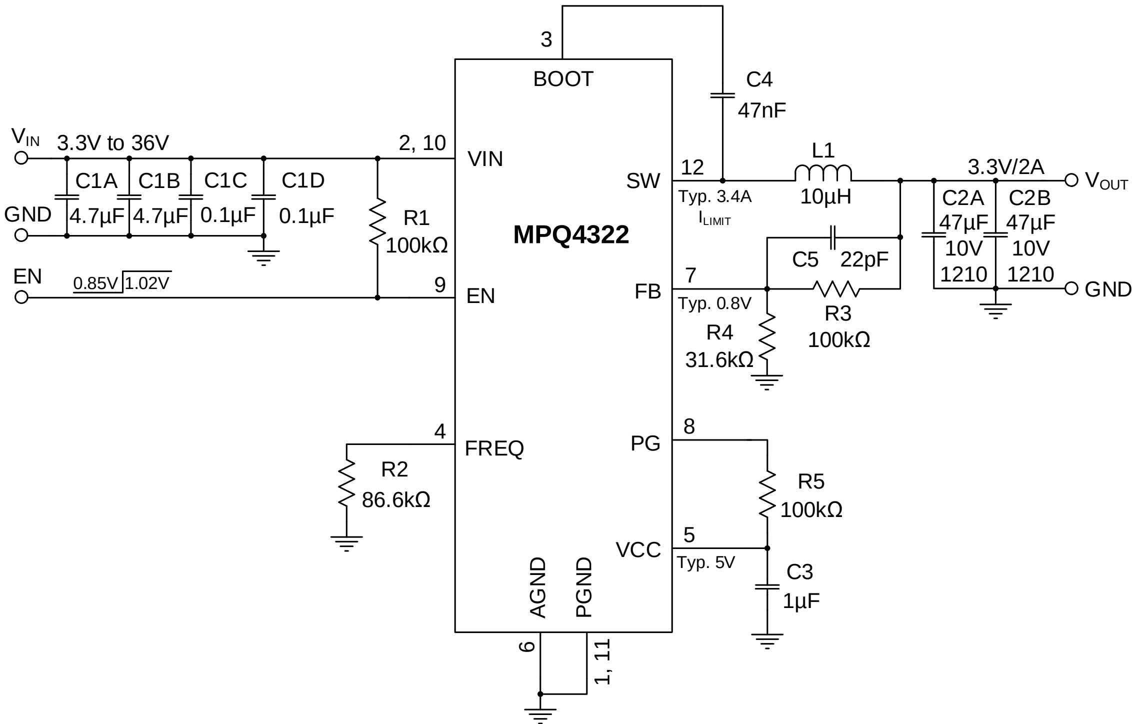


Figure 14: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 415kHz)

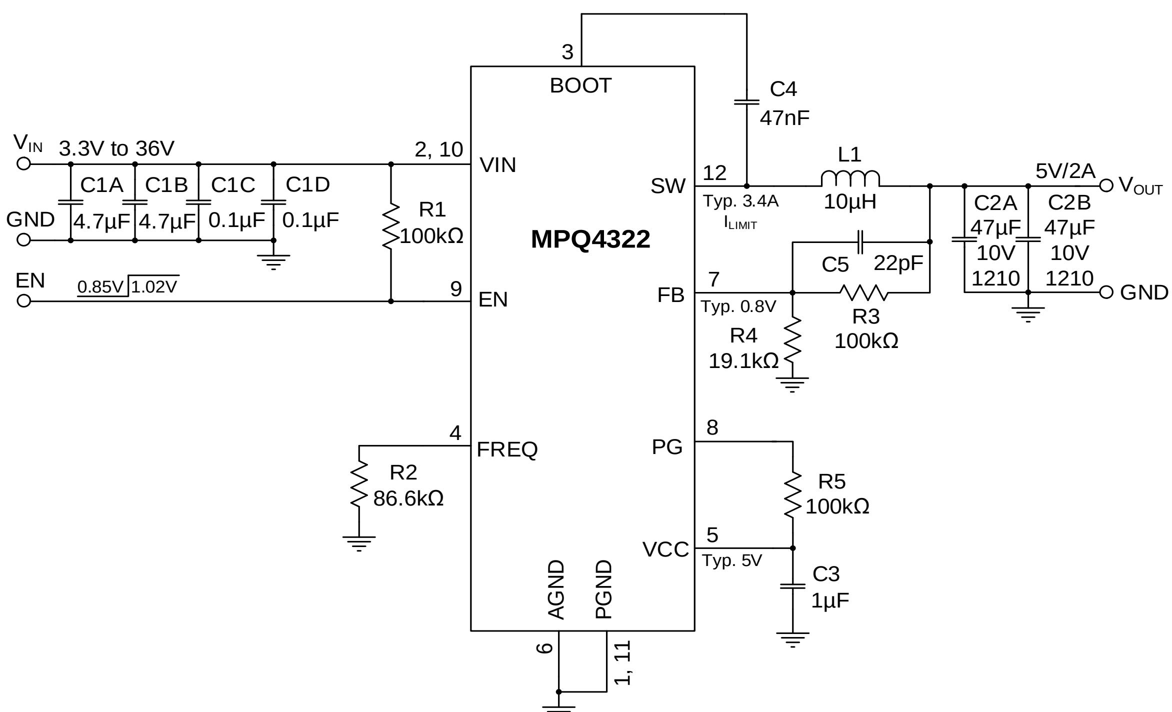


Figure 15: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 415kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

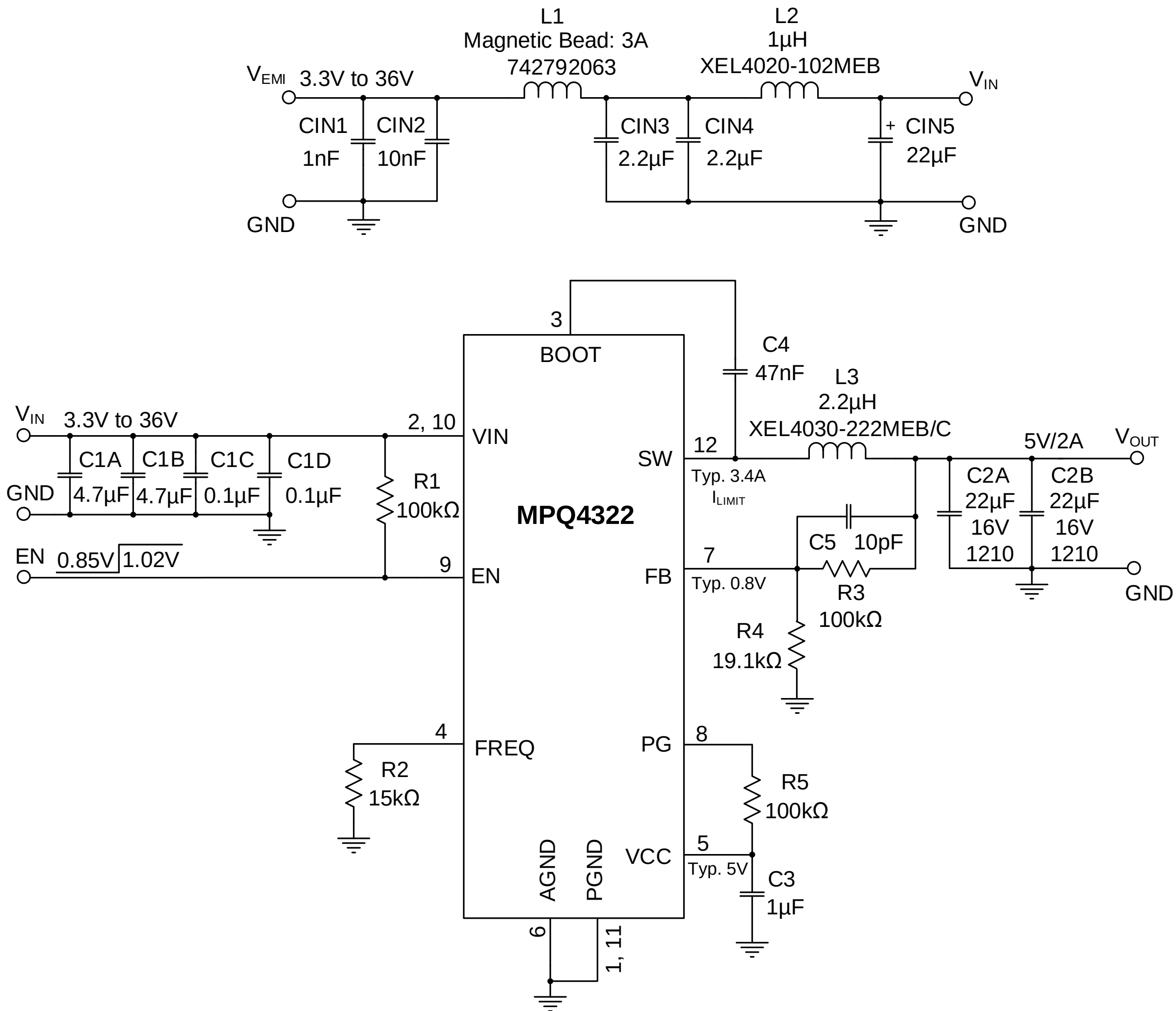


Figure 16: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz with EMI Filters)

TYPICAL APPLICATION CIRCUITS *(continued)*

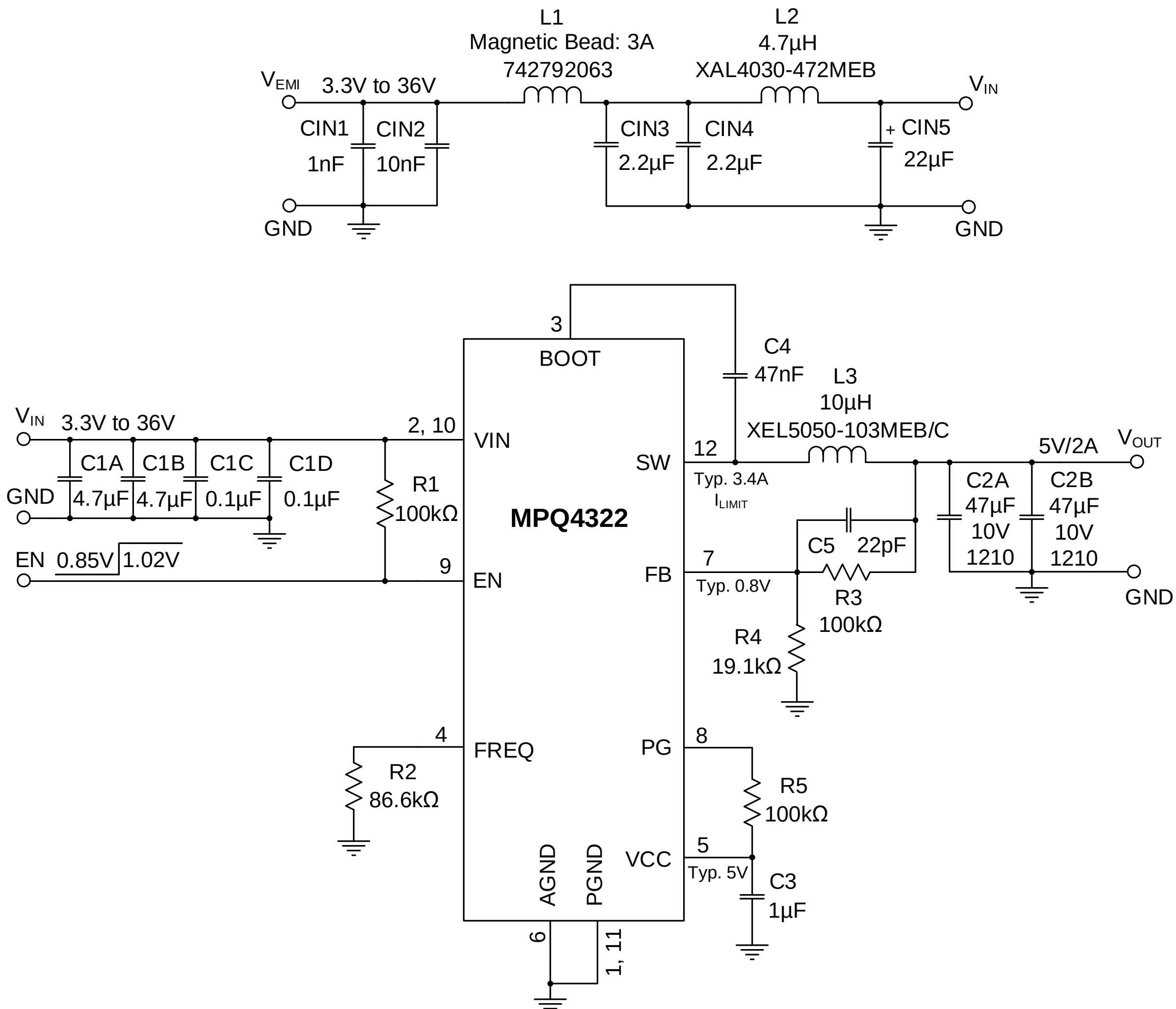
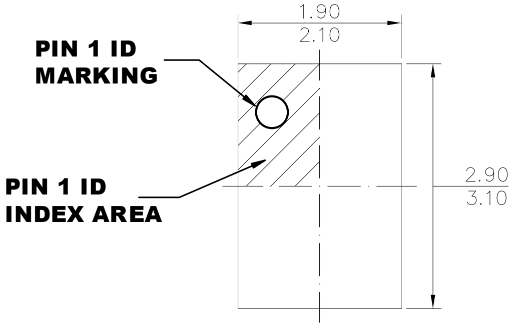


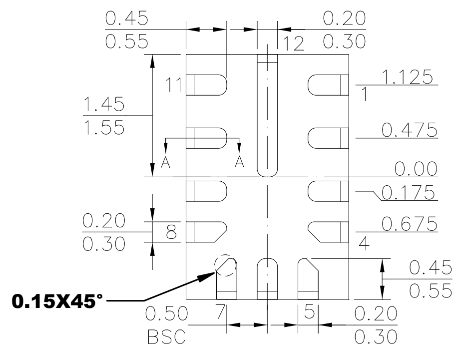
Figure 17: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 415kHz with EMI Filters)

PACKAGE INFORMATION

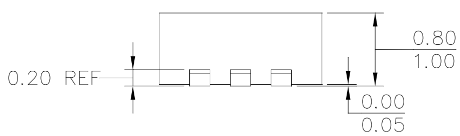
QFN-12 (2mmx3mm)
Wettable Flank



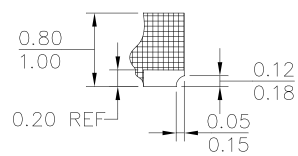
TOP VIEW



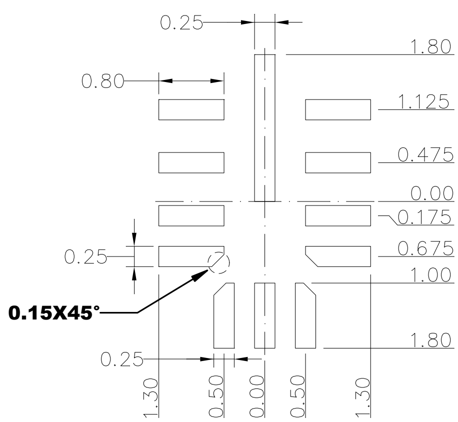
BOTTOM VIEW



SIDE VIEW



SECTION A-A



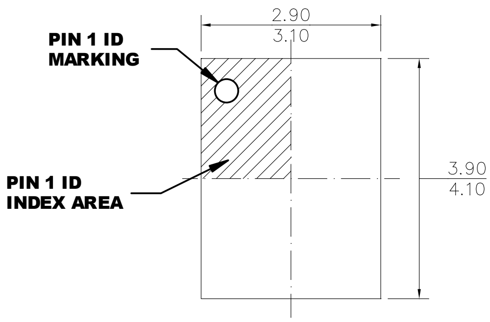
RECOMMENDED LAND PATTERN

NOTE:

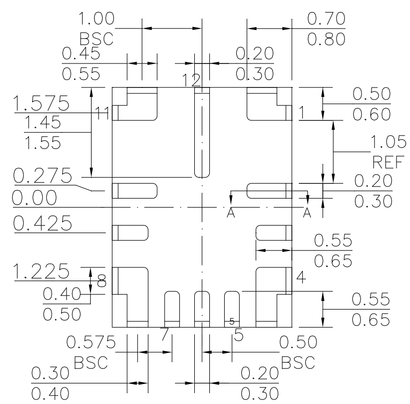
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION

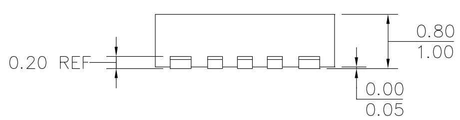
QFN-12 (3mmx4mm)
Wettable Flank



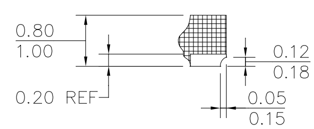
TOP VIEW



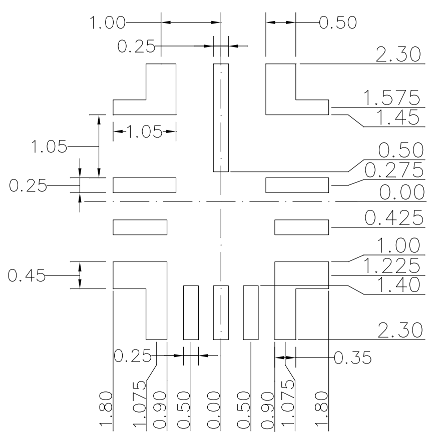
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

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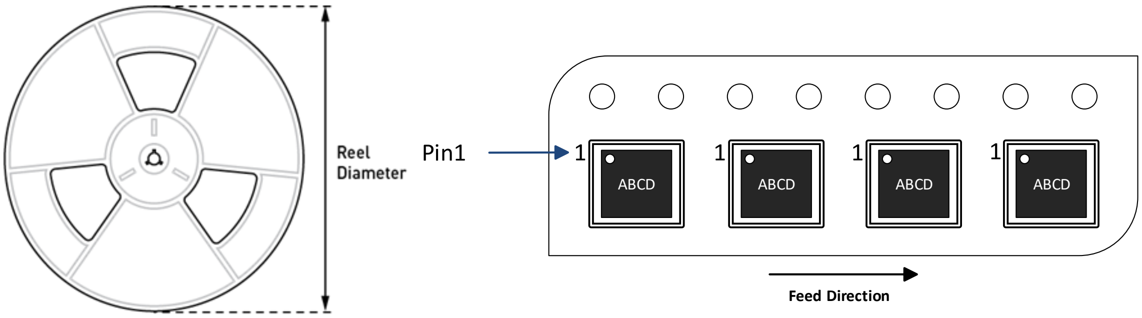
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (15)	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4322GDE-AEC1-Z	QFN-12 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4322GLE-AEC1-Z	QFN-12 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

15) N/A indicates “not available” in tubes. For 500-piece tape & reel prototype quantities, contact the factory. (Order code for 500-piece partial reel is “-P”, tape & reel dimensions remain the same as the full reel.)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/6/2023	Initial Release	-