MPQ4423C

36V, 6A, Synchronous Buck Converter with Selectable Frequency and Frequency Spread Spectrum, AEC-Q100 Qualified

DESCRIPTION

The MPQ4423C is a high-frequency, synchronous, rectified, step-down, switch-mode converter with integrated internal power MOSFETs. It offers a compact solution that can achieve up to 6A of peak output current (I_{OUT}) across a wide 4V to 36V input voltage (V_{IN}) range, with excellent load and line regulation.

Synchronous mode offers high efficiency across the entire I_{OUT} load range. Peak current control mode provides fast transient response and improved loop stabilization.

Full protection features include over-current protection (OCP) with hiccup mode, output over-voltage protection (OVP), and thermal shutdown.

The MPQ4423C requires a minimal number of readily available, standard external components, and is available in a QFN-16 (3mmx4mm) package.

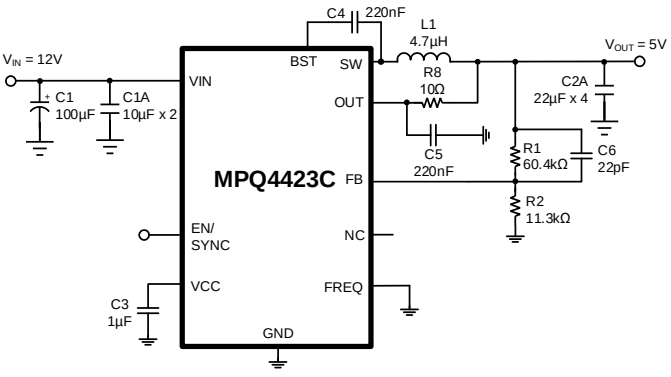
FEATURES

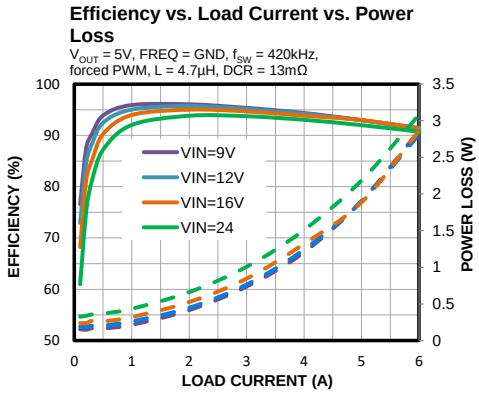
- Wide 4V to 36V Operating Input Voltage (V_{IN}) Range
- 50mΩ/30mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Up to 6A Peak Output Current (I_{OUT})
- Up to 2.2MHz Switching Frequency (f_{SW})
- 420kHz/2.2MHz Selectable f_{SW} with Frequency Spread Spectrum (FSS)
- OUT to VCC Switch over LDO for High Efficiency
- 200kHz to 2.2MHz External SYNC Clock
- Adjustable Forced Pulse-Width Modulation (PWM) Mode or Auto-PWM/PFM Mode
- Passive Output Discharge
- Adjustable Output from 0.8V
- Output Over-Voltage Protection (OVP), Over-Current Protection (OCP) with Hiccup Mode, and Thermal Shutdown
- Available in a QFN-16 (3mmx4mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Infotainment Systems
- Wireless Chargers
- USB Power Delivery (PD) Applications

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ4423CGLE-AEC1	QFN-16 (3mmx4mm)	See below	1

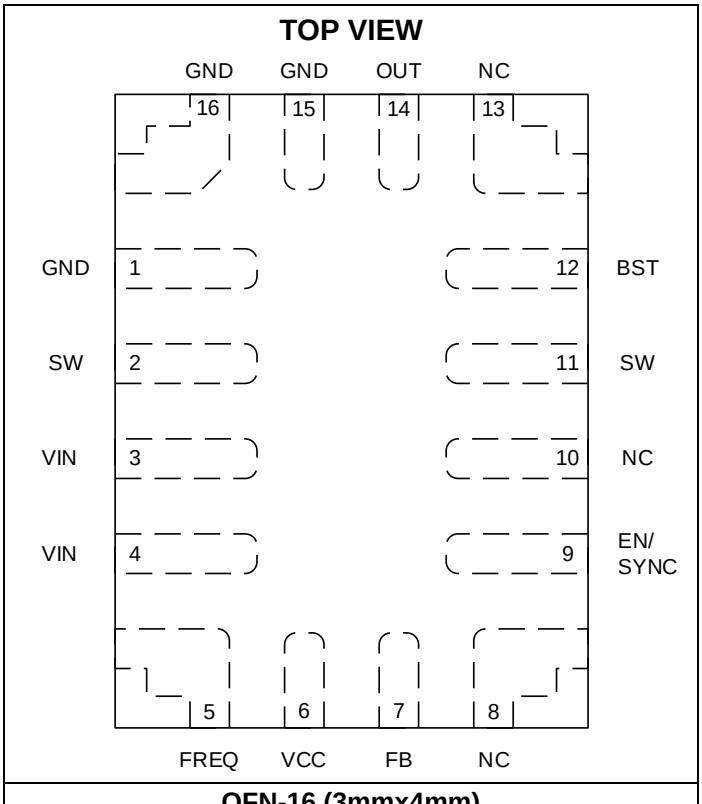
* For Tape & Reel, add suffix -Z (e.g. MPQ4423CGLE-AEC1-Z)

TOP MARKING

MPYW
4423
CLLL
E

MP: MPS prefix
Y: Year code
W: Week code
4423C: Part number
LLL: Lot number
E: Wettable flank package

PACKAGE REFERENCE



QFN-16 (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 15, 16	GND	**Power ground.**
2, 11	SW	**Switch output.** Use a wide PCB trace to connect the SW pin to the inductor.
3, 4	VIN	**Supply voltage.** The MPQ4423C operates from a 4V to 36V input rail. Place an input capacitor (C1) as close to the IC as possible. Use a wide PCB trace to connect the VIN pin to C1 and the input power source.
5	FREQ	**Switching frequency setting.** The FREQ pin sets the switching frequency (f_{SW}). FREQ can support three modes with frequency spread spectrum (FSS). If FREQ is connected to GND, then the part operates in forced pulse-width modulation (PWM) mode with a 420kHz f_{SW} and FSS. If FREQ is floating, then the part operates in auto-PWM/pulse-frequency modulation (PFM) mode with a 420kHz f_{SW} and FSS. If FREQ is connected to VCC, then the part operates in forced PWM mode with a 2.2MHz f_{SW} and FSS.
6	VCC	**Internal 5V LDO regulator output.** Decouple the VCC pin with a 1µF decoupling capacitor.
7	FB	**Feedback.** To set the output voltage (V_{OUT}), connect the FB pin to the tap of an external resistor divider connected between the output and GND. The frequency foldback comparator decreases f_{SW} once the FB voltage (V_{FB}) drops below 400mV to prevent current limit runaway when a short occurs.
8, 10, 13	NC	**No connection.** The NC pin can be tied to GND. For improved PCB layout and stability, pin 10 can be connected to SW.
9	EN/SYNC	**Enable/synchronous input.** Pull EN/SYNC high to turn the converter on; pull EN/SYNC low to turn it off. The EN/SYNC pin is pulled to ground internally via a 500kΩ resistor. To configure f_{SW}, apply an external clock to EN/SYNC.
12	BST	**Bootstrap.** Connect a 220nF capacitor between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
14	OUT	**Buck converter output.** Connect the OUT pin to an external power supply (5V ≤ V_{OUT} ≤ 20V), or connect OUT to the VOUT trace to reduce the power dissipation and improve efficiency. Float OUT or connect OUT to GND if not used.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V_{IN}, V_{OUT}) ..... -0.4V to +40V
V_{SW} ..... -0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST} ..... V_{SW} + 5.5V
V_{EN} ..... -0.3V to +5.5V (2)
All other pins ..... -0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (3) (7)
QFN-16 (3mmx4mm) 5.34W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (6)

Operation input voltage ..... 4V to 36V
Output voltage range ..... 0.8 to V_{IN} x D_{MAX}
Output current ..... 6A Peak
Operating junction temp (T_J). ... -40°C to +150°C

ESD Ratings (4) (5)

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±750V

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-16 (3mmx4mm)			
EVQ4423C-L-00A (7)	23.4	7.1	°C/W
JESD51-7 (8)	48	11	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For details on EN's ABS maximum rating, see the Enable/Synchronous (EN/SYNC) Control section on page 14.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The human body model (HBM) is according to JEDEC specification JESD22-A114. JEDEC document JEP155 states that a 500V HBM allows for safe manufacturing with a standard ESD control process. HBM is with regards to GND.
5) The charged device model (CDM) is according to JEDEC specification JESD22-C101, and AEC specification AEC-Q100-011. JEDEC document JEP157 states that a 250V CDM allows for safe manufacturing with a standard ESD control process.
6) The device is not guaranteed to function outside of its operating conditions.
7) Measured on the EVQ4423C-L-00A evaluation board (70mmx55mm), 4-layer PCB.
8) The value of θJA given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown current	I_{SD}	V_{EN} = 0V, T_J = 25°C			1	μA
		V_{EN} = 0V, T_J = -40°C to +150°C			8	
Quiescent current	I_Q	V_{FB} = 1V		0.75	1.1	mA
EN rising threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN falling threshold	$V_{EN\_FALLING}$		1.05	1.25	1.45	V
EN Input Current	I_{EN1}	V_{EN} = 2V		4.5	6	μA
	I_{EN2}	V_{EN} = 0V		0	0.2	
Thermal shutdown (9)	T_{SD}			165		°C
Thermal hysteresis (9)	T_{SD_HYS}			20		°C
VCC regulator	V_{CC}	I_{CC} = 0mA	4.8	5	5.2	V
VCC load regulation	V_{CC_REG}	I_{CC} = 5mA		1.5	4	%
Step-Down Converter						
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		3.5	3.7	3.9	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		3.05	3.25	3.45	V
High-side MOSFET (HS-FET) On Resistance	$R_{DS(ON)\_HS}$			50	90	mΩ
Low-side MOSFET (LS-FET) On Resistance	$R_{DS(ON)\_LS}$			30	55	mΩ
Output discharge resistance	$R_{DISCHARGE}$			250	400	Ω
Feedback (FB) voltage	V_{FB}		776	792	808	mV
FB current	I_{FB}	V_{FB} = 820mV		10	100	nA
Synchronous frequency	f_{SYNC}		0.2		2.4	MHz
Switching frequency	f_{SW1}	V_{FB} = 750mV, FREQ is floating	340	420	500	kHz
	f_{SW2} (9)	V_{FB} = 750mV, FREQ is connected to VCC		2.2		MHz
Frequency spread spectrum (FSS)	f_{SS1}	FREQ is connected to GND, based on the default 420kHz f_{SW} (f_{SW1})		±10		%
	f_{SS2} (9)	FREQ is connected to VCC, based on the 2.2MHz f_{SW} (f_{SW2})		±10		%
Foldback frequency	$f_{FOLDBACK}$	V_{FB} < 400mV		1/2		
Maximum duty cycle	D_{MAX}	f_{SW1} = 420kHz	94.5	96		%
Switch leakage current	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to +150°C			10	μA
HS-FET peak current limit (9)	I_{LIMIT_PEAK}		7	10		A
LS-FET valley current limit (9)	I_{LIMIT_VALLEY}			9		A
LS-FET negative current limit (9)	I_{NEG_LS}			-3		A
Minimum on time (9)	t_{ON_MIN}			60		ns
Output over-voltage protection (OVP) rising threshold	V_{OVP_RISING}		112	115	118	%
Output OVP recovery	$V_{OVP\_RECOVERY}$			105		%
Soft-start time	t_{SS}	Output is between 10% and 90% of V_{OUT}		1.5		ms

Notes:

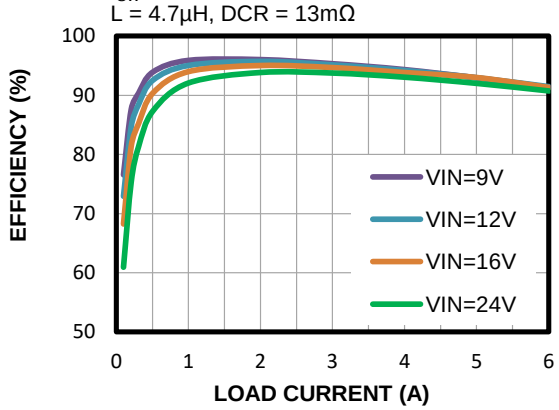
9) Guaranteed by design and engineering sample characterization.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

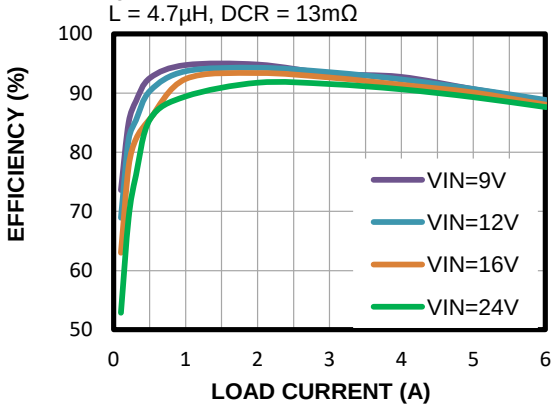
Efficiency vs. Load Current

V_{OUT} = 5V, FREQ is connected to GND, f_{SW} = 420kHz, forced PWM mode, L = 4.7µH, DCR = 13mΩ



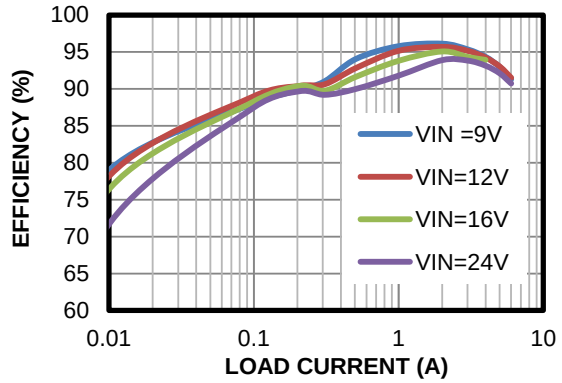
Efficiency vs. Load Current

V_{OUT} = 3.3V, FREQ is connected to GND, f_{SW} = 420kHz, forced PWM mode, L = 4.7µH, DCR = 13mΩ



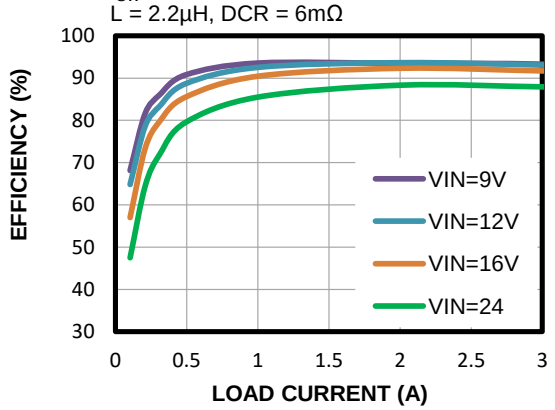
Efficiency vs. Load Current

V_{OUT} = 5V, FREQ is floating, f_{SW} = 420kHz, auto-PWM/PFM mode,L = 4.7µH, DCR = 13mΩ



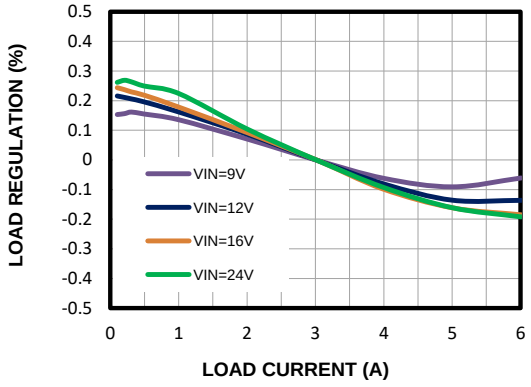
Efficiency vs. Load Current

V_{OUT} = 5V, FREQ is connected to VCC, f_{SW} = 2.2MHz, forced PWM mode, L = 2.2µH, DCR = 6mΩ



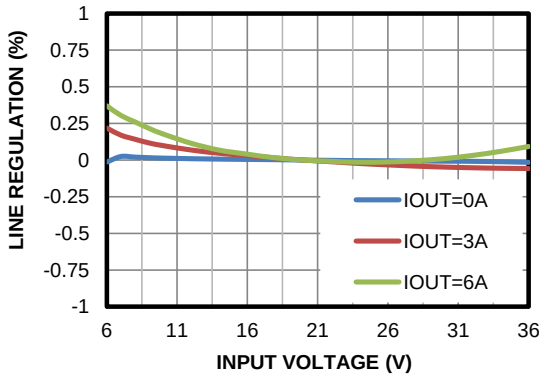
Load Regulation

V_{OUT} = 5V, FREQ is connected to GND, f_{SW} = 420kHz, forced PWM mode, L = 4.7µH, DCR = 13mΩ



Line Regulation

V_{OUT} = 5V, FREQ is connected to GND, f_{SW} = 420kHz, forced PWM mode, L = 4.7µH, DCR = 13mΩ

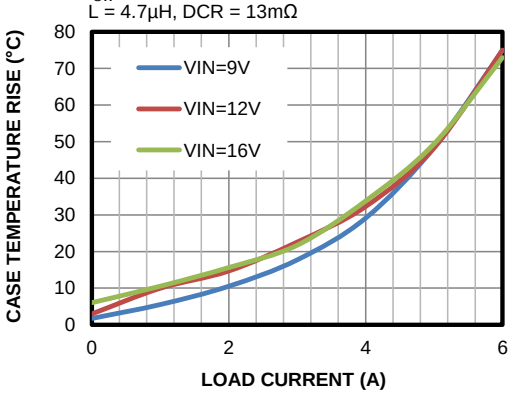


TYPICAL PERFORMANCE CHARACTERISTICS

FREQ is connected to VCC, f_{SW} = 2.2MHz, forced PWM mode, L = 2.2µH, DCR = 6mΩ, T_A = 25°C, unless otherwise noted.

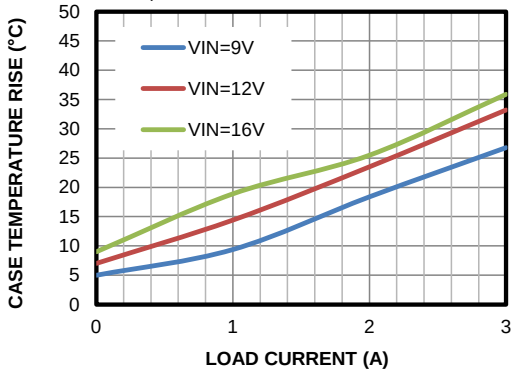
Case Temperature Rise

V_{OUT} = 5V, FREQ is connected to GND,
f_{SW} = 420kHz, forced PWM mode,
L = 4.7µH, DCR = 13mΩ

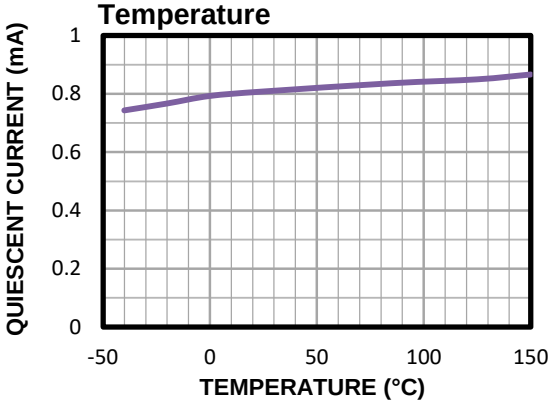


Case Temperature Rise

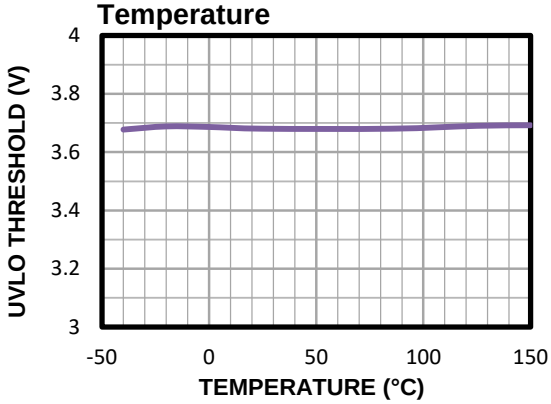
V_{OUT} = 5V, FREQ is connected to VCC,
f_{SW} = 2.2MHz, forced PWM mode,
L = 2.2µH, DCR = 6mΩ



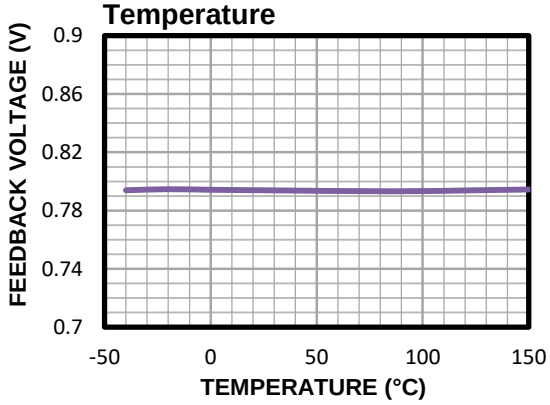
Quiescent Current vs. Temperature



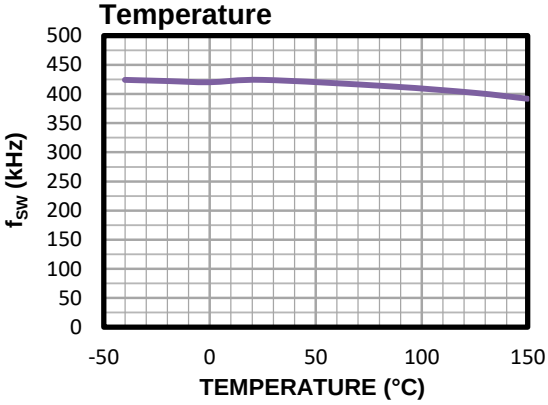
UVLO Threshold vs. Temperature



Feedback Voltage vs. Temperature



Switching Frequency vs. Temperature

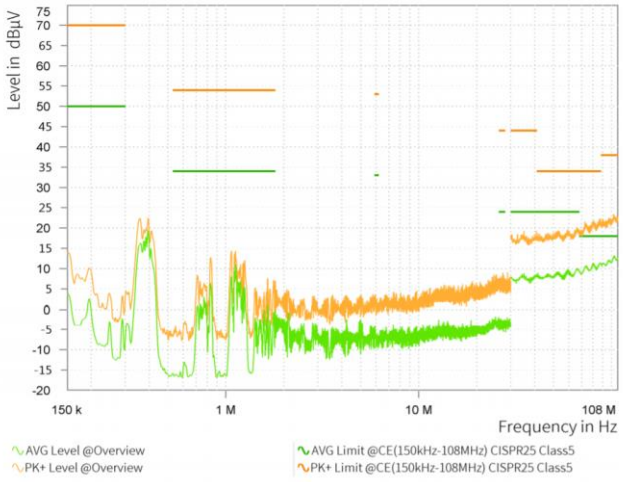


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

FREQ is connected to VCC, f_{SW} = 2.2MHz, forced PWM mode, L = 2.2µH, DCR = 6mΩ, T_A = 25°C, unless otherwise noted.

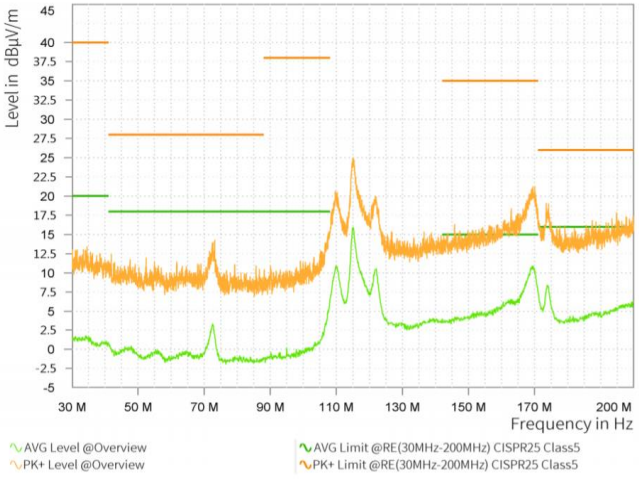
Conducted EMI

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, L = 4.7µH, FREQ is connected to GND, f_{SW} = 420KHZ, forced PWM mode



Radiated EMI

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, L = 4.7µH, FREQ is connected to GND, f_{SW} = 420KHZ, forced PWM mode

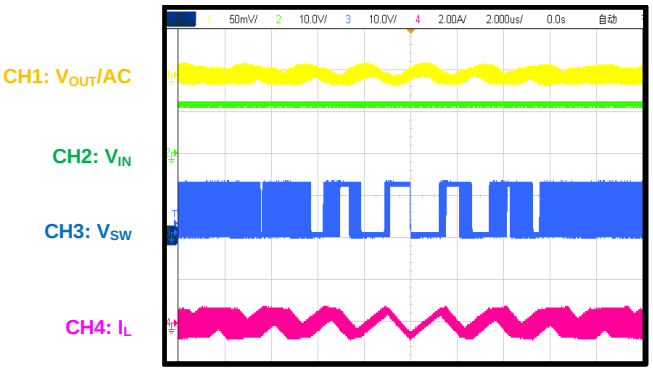


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

FREQ is connected to VCC, f_{SW} = 2.2MHz, forced PWM mode, L = 2.2µH, DCR = 6mΩ, T_A = 25°C, unless otherwise noted.

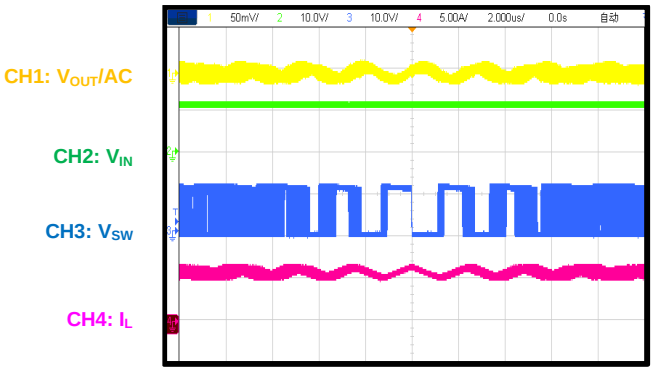
Steady State

FREQ is connected to GND, f_{SW} = 420kHz, forced PWM mode, I_{OUT} = 0A



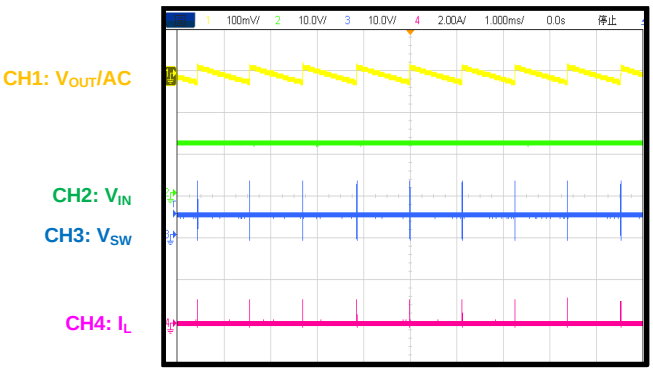
Steady State

FREQ is connected to GND, f_{SW} = 420kHz, forced PWM mode, I_{OUT} = 6A



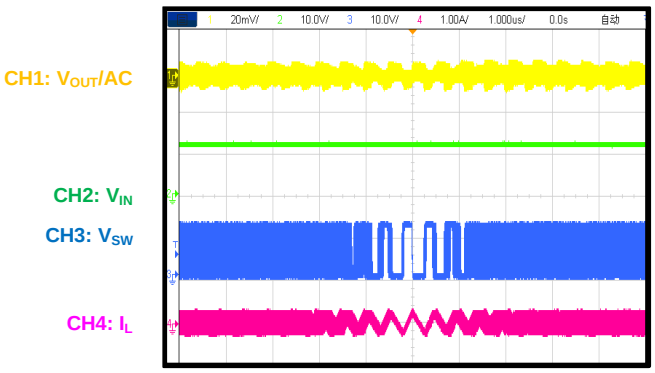
Steady State

FREQ is floating, f_{SW} = 420kHz, auto-PWM/PFM mode, I_{OUT} = 0A



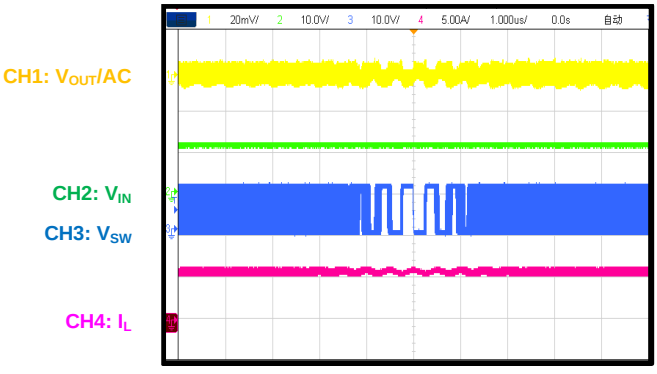
Steady State

FREQ is connected to VCC, L = 2.2µH, f_{SW} = 2.2MHz, forced PWM mode, I_{OUT} = 0A



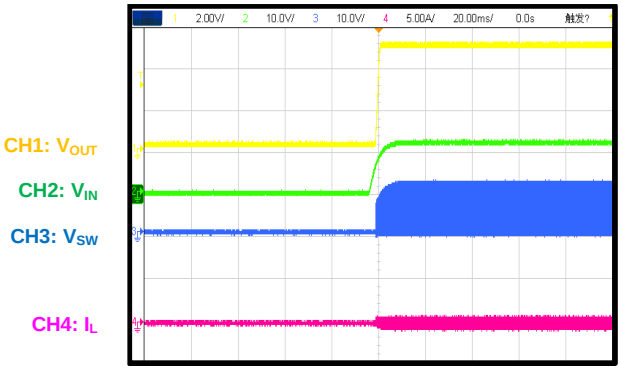
Steady State

FREQ is connected to VCC, L = 2.2µH, f_{SW} = 2.2MHz, forced PWM mode, I_{OUT} = 6A



Start-Up

I_{OUT} = 0A

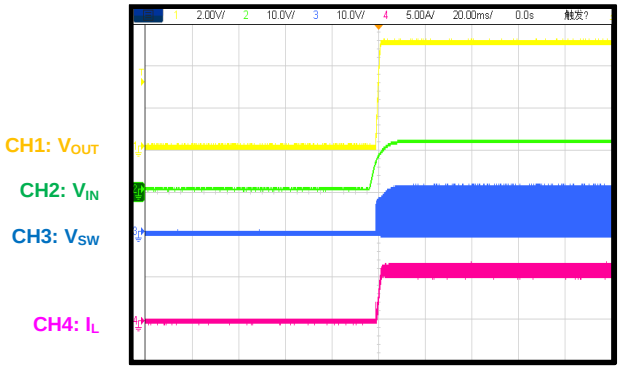


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

FREQ is connected to VCC, f_{SW} = 2.2MHz, forced PWM mode, L = 2.2µH, DCR = 6mΩ, T_A = 25°C, unless otherwise noted.

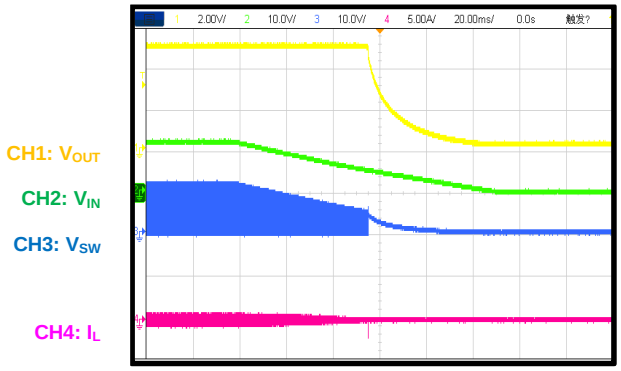
Start-Up

I_{OUT} = 6A



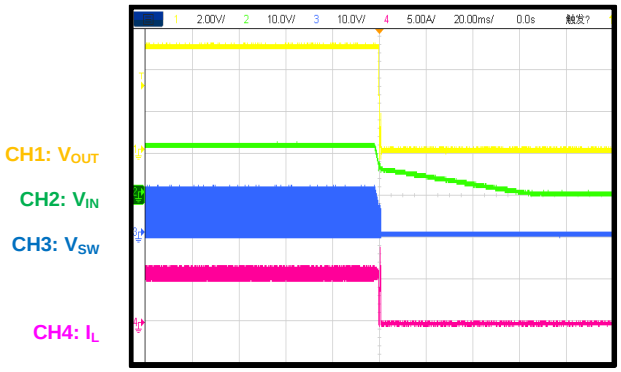
Shutdown

I_{OUT} = 0A



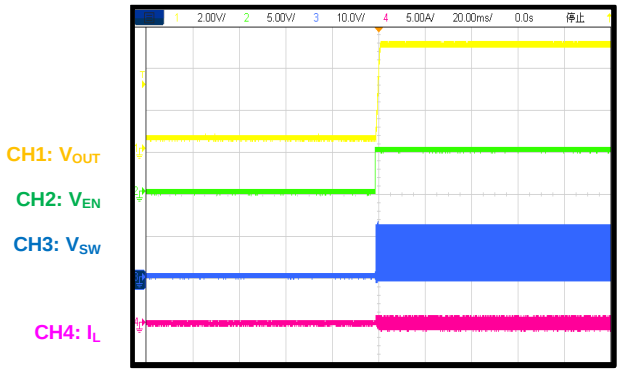
Shutdown

I_{OUT} = 0A



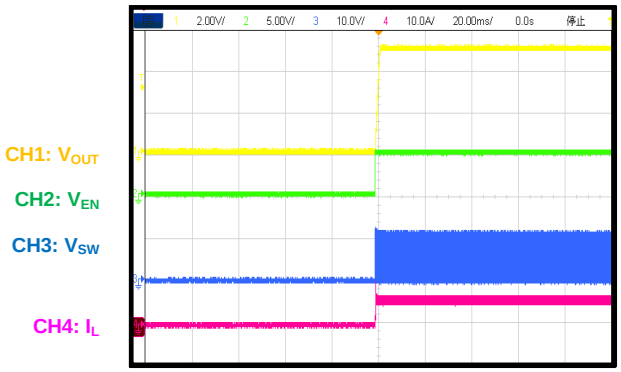
Start-Up through EN

I_{OUT} = 0A



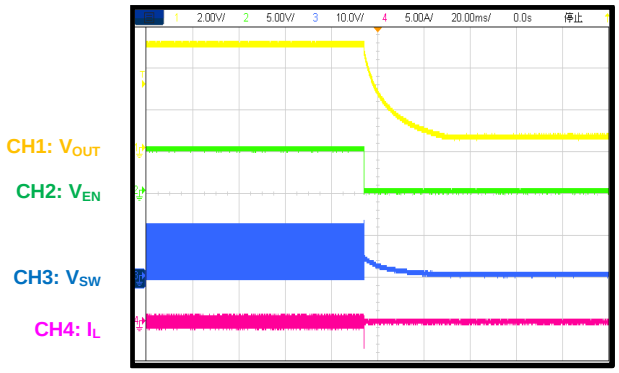
Start-Up through EN

I_{OUT} = 6A



Shutdown through EN

I_{OUT} = 0A

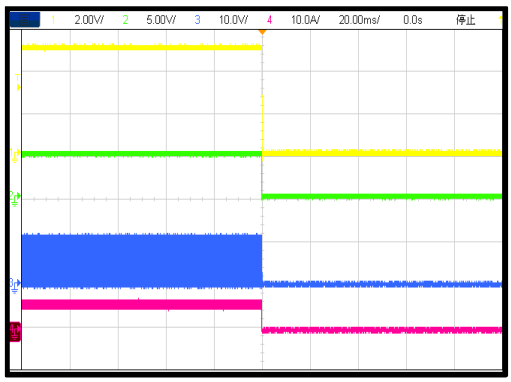


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

FREQ is connected to VCC, f_{SW} = 2.2MHz, forced PWM mode, L = 2.2µH, DCR = 6mΩ, T_A = 25°C, unless otherwise noted.

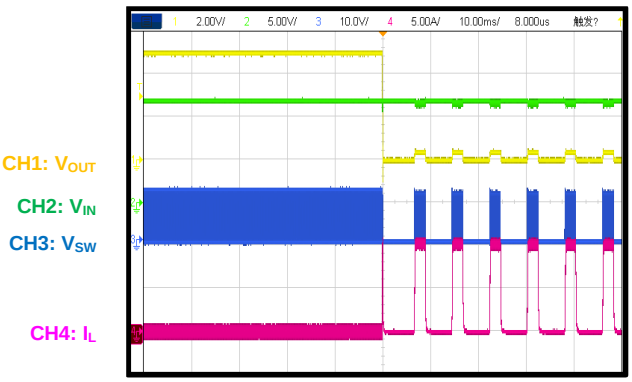
Shutdown through EN

I_{OUT} = 6A



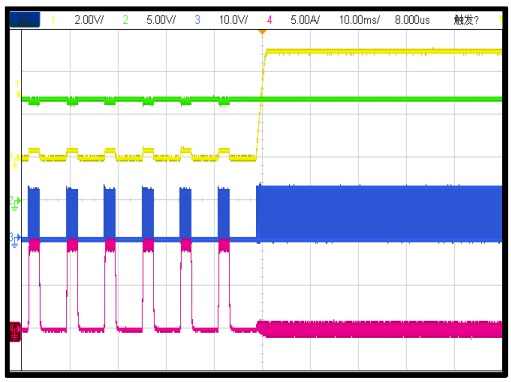
SCP Entry

I_{OUT} = 0A



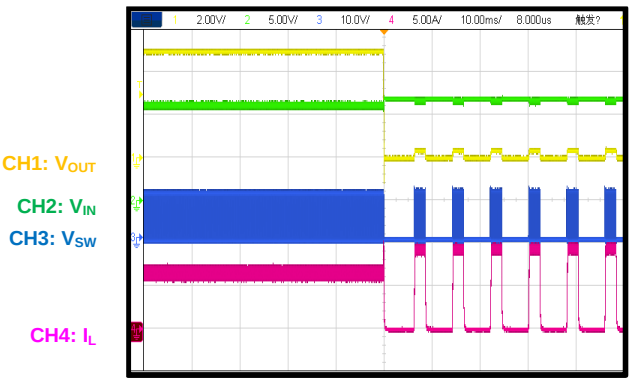
SCP Recovery

I_{OUT} = 0A



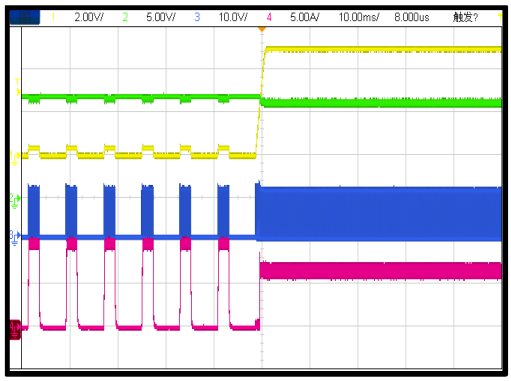
SCP Entry

I_{OUT} = 6A

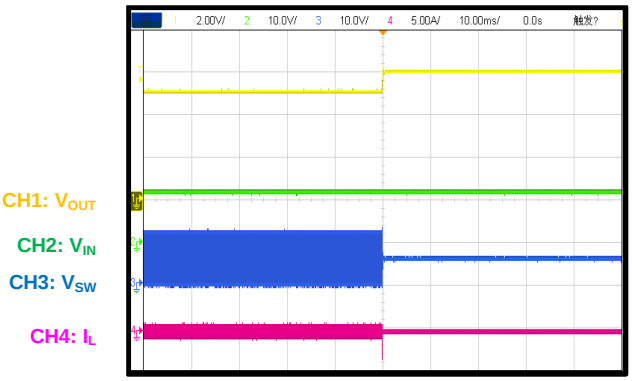


SCP Recovery

I_{OUT} = 6A



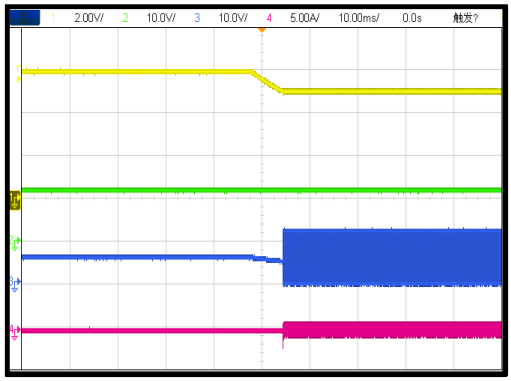
OVP Entry



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

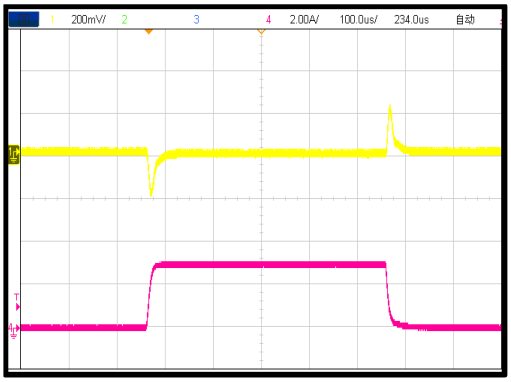
FREQ is connected to VCC, f_{SW} = 2.2MHz, forced PWM mode, L = 2.2µH, DCR = 6mΩ, T_A = 25°C, unless otherwise noted.

OVP Recovery



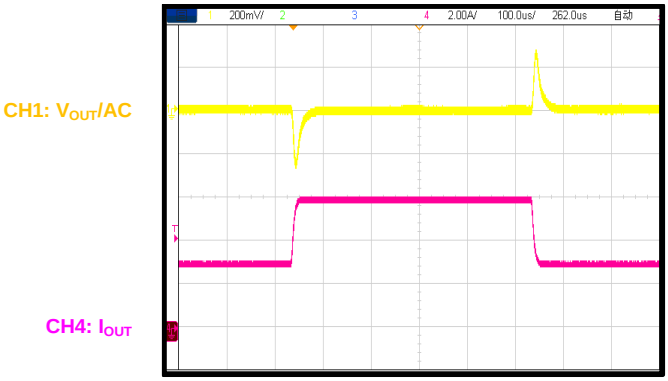
Load Transient

I_{OUT} = 0A to 3A, 0.4A/µs slew rate

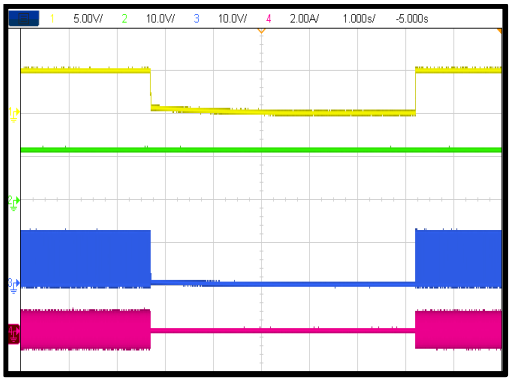


Load Transient

I_{OUT} = 3A to 6A, 0.4A/µs slew rate

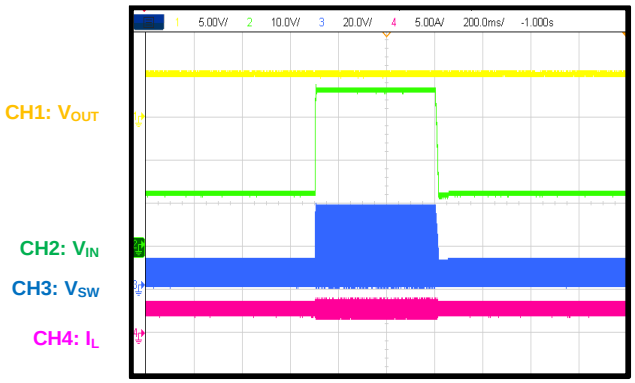


OTP Entry and Recovery



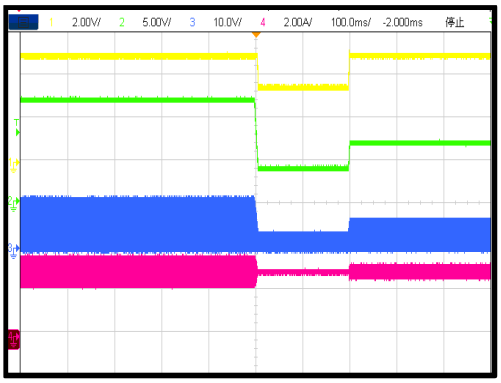
Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 3A



Cold Crank

V_{IN} = 12V to 4V to 7V, I_{OUT} = 3A



FUNCTIONAL BLOCK DIAGRAM

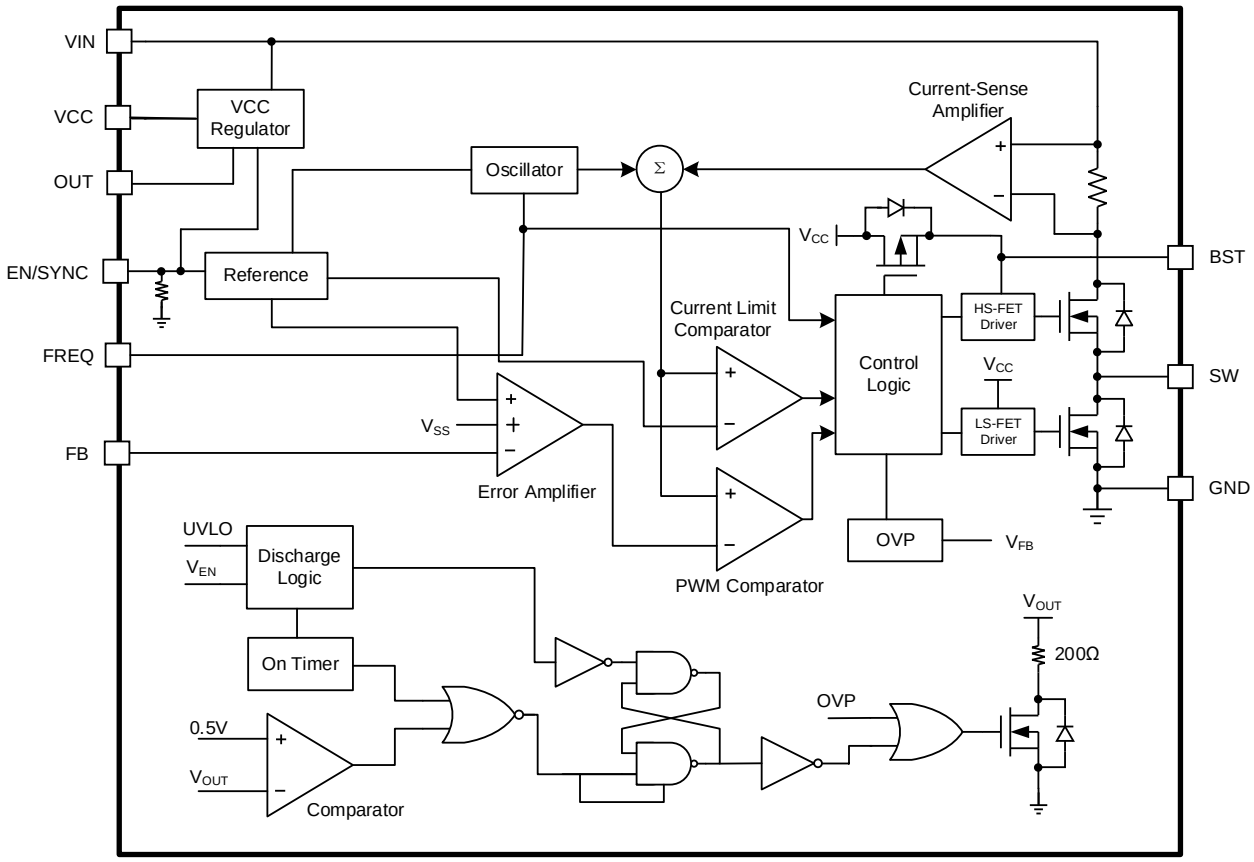


Figure 1: Functional Block Diagram

OPERATION

The MPQ4423C is a monolithic synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a compact solution that can achieve up to 6A of peak continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) range, with excellent load and line regulation.

Pulse-Width Modulation (PWM) Control

The MPQ4423C operates with a fixed frequency in peak current control mode to regulate the output voltage (V_{OUT}). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the rising edge of the clock, the high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the internal comparator (V_{COMP}). The HS-FET remains off until the next clock cycle begins.

If the HS-FET current does not reach V_{COMP} within 96% of one PWM cycle (f_{SW} = 420kHz), the HS-FET turns off.

Error Amplifier (EA)

The error amplifier (EA) compares the feedback (FB) voltage (V_{FB}) to the internal reference voltage (V_{REF}) (typically 0.792V), and outputs a V_{COMP}. This V_{COMP} controls the power MOSFET's current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Internal Regulator (VCC)

The 5V internal regulator powers most of the internal circuitry. This regulator uses either the VOUT pin or VIN pin as its input and operates across the entire V_{IN} range. If V_{IN} exceeds 5V, then VCC is in full regulation. If V_{IN} drops below 5V, then the output decreases with V_{IN}. If the output voltage (V_{OUT}) exceeds 4.75V, then VCC uses V_{OUT} to reduce the LDO power loss. Decouple VCC via an external 0.22µF to 1µF ceramic decoupling capacitor.

Enable/Synchronous (EN/SYNC) Control

EN/SYNC is a digital control pin that turns the converter on and off. Pull EN/SYNC high to turn the converter on; pull EN/SYNC low to turn it off. An internal 500kΩ resistor connected between EN/SYNC and GND allows the device to be shut down by floating EN/SYNC.

The EN/SYNC pin is clamped internally via a 6.5V Zener diode (see Figure 2). It is recommended to connect EN/SYNC to the VIN and GND pins via a resistor divider. When selecting a pull-up resistor, ensure that it has a large enough resistance to limit the current flowing into EN/SYNC to below 100µA.

For example, if the EN/SYNC pull-up resistor is 100kΩ and the pull-down resistor is 36kΩ, then the IC starts up once V_{IN} exceeds 6V.

To connect EN/SYNC directly to a voltage source without a pull-up resistor, the voltage amplitude should be below 5.5V to prevent damage to the Zener diode.

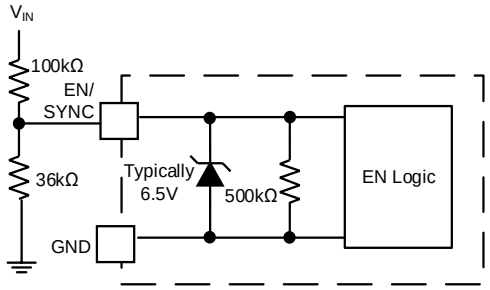


Figure 2: 6.5V Zener Diode

To configure the switching frequency (f_{SW}), connect a 200kHz to 2.2MHz external clock to EN/SYNC. The external clock signal's pulse width should be less than 10% of the duty cycle. It is recommended to float EN/SYNC when synchronizing f_{SW} via an external clock.

Setting the Switching Frequency (f_{SW})

The FREQ pin sets the MPQ4423C's f_{SW}. FREQ has three settings:

- If FREQ is connected to ground, the MPQ4423C operates in forced PWM mode with a 420kHz f_{SW} and frequency spread spectrum and (FSS).
- If FREQ is floating, the MPQ4423C operates in Auto-PWM/Pulse-Frequency Modulation (PFM) Mode with a 420kHz f_{SW} and FSS.
- If FREQ is connected to VCC, the MPQ4423C operates in forced PWM mode with a 2.2MHz f_{SW} and FSS.

Auto-PWM/PFM Mode

The MPQ4423C operates in continuous conduction mode (CCM) at heavy loads. As the load decreases, the MPQ4423C enters discontinuous conduction mode (DCM). In DCM, the device operates with a fixed frequency as the inductor current (I_L) approaches 0A. If the load continues to decrease or if there is no load, then the inductor peak current drops below the advanced asynchronous modulation (AAM) mode peak current threshold (V_{AAM}), and the device enters pulse-skip mode (PSM) to improve efficiency under light-load conditions.

At very light loads or no load, the feedback (FB) voltage (V_{FB}) decreases and V_{COMP} increases until AAM mode is triggered. If the clock goes high, then the HS-FET turns on and remains on until the I_L sense resistor (V_{IL_SENSE}) reaches V_{COMP}. If V_{COMP} drops below V_{AAM}, then the internal clock is blocked, and the MPQ4423C skips some pulses in PFM mode. This control scheme improves efficiency by scaling down the f_{SW} to reduce the switching and gate driver losses.

As I_{OUT} increases at light loads, both V_{COMP} and f_{SW} increase. If I_{OUT} exceeds the critical level set by V_{COMP}, the device operates with fixed-frequency PWM control.

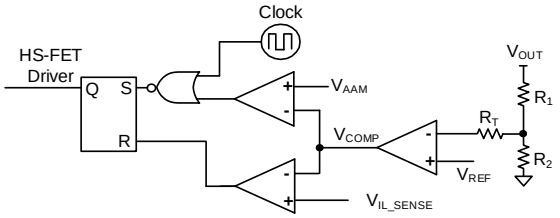


Figure 3: Auto-PWM/PFM Mode

Forced Pulse-Width Modulation (PWM) Mode

The MPQ4423C operates in CCM mode continuously. It operates with a fixed f_{SW} regardless across the full load range. Advantages of CCM include the controllable fixed frequency, lower V_{OUT} ripple, and sufficient bootstrap (BST) capacitor (C4) charge time; however, CCM does have low efficiency under light-load conditions. Select an inductance that avoids triggering the low-side MOSFET (LS-FET) negative current limit (I_{NEG_LS}) (typically 3A). If I_{NEG_LS} is triggered, the LS-FET turns off and the HS-FET turns on once the internal clock begins.

Frequency Spread Spectrum (FSS)

The MPQ4423C employs a 4kHz triangle wave (125µs rising and 125µs falling) to modulate the internal oscillator. The FSS's frequency span is ±10% (see Figure 4). This minimizes the peak emissions at specific frequencies to optimize FSS performance.

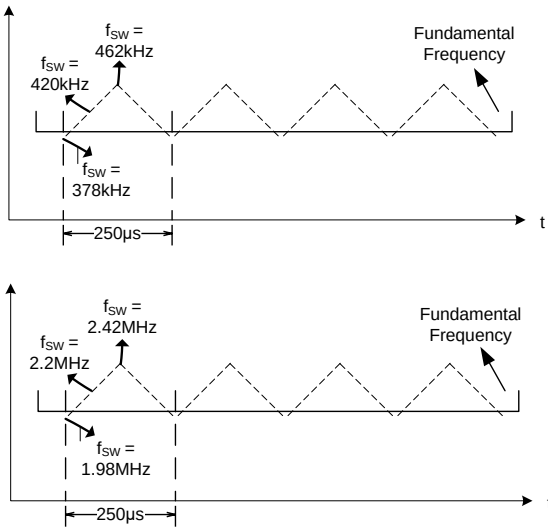


Figure 4: Frequency Spread Spectrum

For a 420kHz f_{SW} with FSS, connect FREQ to GND or float FREQ. For a 2.2MHz f_{SW} with FSS, connect FREQ to VCC.

Under-Voltage Lockout (UVLO) Protection

The under-voltage lockout (UVLO) comparator monitors V_{IN} to protect the chip from operating at an insufficient V_{IN}. The UVLO rising threshold is 3.7V, and its falling threshold is 3.25V.

Internal Soft Start (SS)

The MPQ4423C implements soft start (SS) to prevent V_{OUT} from overshooting during start-up.

Once a SS is initiated, the internal circuitry generates a SS voltage (V_{SS}) that ramps up from 0V to 5V. If the soft-start voltage (V_{SS}) drops below V_{REF}, then V_{SS} overrides V_{REF} and the EA uses V_{SS} as the reference. If V_{SS} exceeds V_{REF}, then the EA uses V_{REF} as the reference.

Pre-Biased Start-Up

If the output is pre-biased to a certain voltage during start-up, the HS-FET and LS-FET do not

turn on until V_{SS} exceeds V_{FB}.

Over-Current Protection (OCP) with Hiccup Mode

The MPQ4423C employs cycle by cycle current limiting for when the inductor peak current exceeds its current limit, and V_{FB} drops below the under-voltage (UV) threshold (typically 50% below V_{REF}). Once V_{FB} drops below the UV threshold, the part enters hiccup mode to restart the part periodically. This protection mode is especially useful if an output short to ground occurs. Over-current protection (OCP) reduces short circuits, alleviates thermal issues, and protects the chip from over-current (OC) faults. The MPQ4423C exits hiccup mode once the OC condition is removed.

Over-Voltage Protection (OVP)

The MPQ4423C detects output over-voltage (OV) conditions via the FB pin. If V_{FB} exceeds 115% of its target voltage, the over-voltage protection (OVP) comparator's output goes high. If OVP is triggered, the MPQ4423C enters output discharge mode. The MPQ4423C auto-recovers and resumes normal operation once V_{OUT} drops below 105% of its target voltage.

Bootstrap (BST) Charging

An external bootstrap (BST) capacitor powers the floating HS-FET driver. This floating driver has its own UVLO protection. Its UVLO rising threshold is 2.2V, with a hysteresis of 150mV. The VIN and VCC pins regulate the BST capacitor (C4) internally via D1, D2, M1, C4, L1, and C2 (see Figure 5). VCC charges the C4 voltage quickly via M1. If the LS-FET is not turned on, the 1µA input to BST current source can charge C4.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the MPQ4423C starts up. The reference block starts up first to generate a stable V_{REF} and currents. Then the internal regulator starts up to provide a stable supply for the remaining circuitries.

Three events can shut down the IC: V_{EN} going low, V_{IN} going low, and thermal shutdown. Once shutdown is initiated, the signaling path is blocked to avoid triggering any faults. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Output Discharge

The MPQ4423C's output discharge function provides a resistive discharge path for the external output capacitor (C2). This function remains active even if the part is disabled (e.g. if V_{IN} triggers UVLO or if the part is turned off via EN/SYNC), or if an OV condition occurs. If V_{OUT} drops below 0.5V or if the 200ms maximum time has elapsed, the discharge path turns off.

Thermal Shutdown

Thermal shutdown prevents the IC from operating at exceedingly high temperatures. If the die temperature exceeds the thermal shutdown threshold (about 165°C), then the device shuts down. Once the temperature drops below 145°C the device initiates a new SS and resumes normal operation.

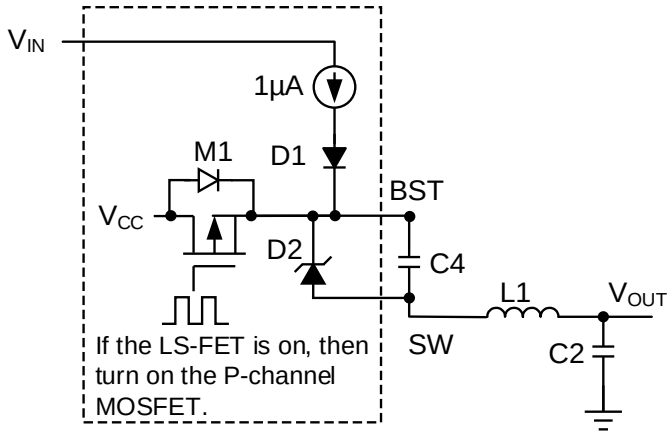


Figure 5: Internal Bootstrap Charging Circuit

APPLICATION INFORMATION

Component Selection

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application section on page 1).

The feedback resistor (R1) sets the feedback loop bandwidth via an internal compensation capacitor. Choose R1 to be about 60.4kΩ. Then the feedback resistance (R2) can be calculated with Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.792V} - 1} \quad (1)$$

If V_{OUT} is low, it is highly recommended to use a T-type network (see Figure 6).

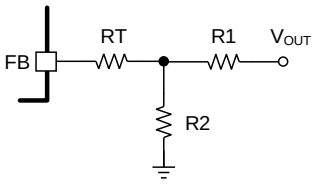


Figure 6: T-Type Feedback Network

A resistor divider (RT + R1) sets the loop bandwidth. A higher RT + R1 results in a lower bandwidth. To ensure loop stability, it is recommended to set the bandwidth below 40kHz. (10)

Table 1 lists the recommended T-type resistor values for common output voltages.

Table 1: Recommended Resistor Values for Common Output Voltages (10)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
3.3	60.4	19
5	60.4	11.3
9	64.9	6.2

Selecting the Inductor

For most applications, an inductor with a DC current rating of at least 25% greater than the maximum load current (I_{LOAD_MAX}) is recommended. For higher efficiency, choose an inductor with a lower DC resistance. The inductance (L) can be estimated with Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose ΔI_L to be between 30% and 50% of I_{LOAD_MAX}. The maximum inductor peak current (I_{L_MAX}) can be calculated with Equation (3):

$$I_{L\_MAX} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

For most applications, a 4.7µH inductance is recommended for a 420kHz f_{SW}, and a 2.2µH inductance is recommended for a 2.2MHz f_{SW}.

Selecting the Input Capacitor (C1)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in C1 (I_{C1}) can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, where:

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose a C1 with an RMS current rating greater than half of I_{LOAD_MAX}.

C1 can be electrolytic, tantalum, or ceramic. If using electrolytic capacitors, place two high-quality ceramic capacitors as close to the VIN pin as possible. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Note:

10) Values are based on the 420kHz default f_{SW} (f_{SW1}).

Selecting Output Capacitor (C2)

The output capacitor (C2 maintains the DC V_{OUT}. The output voltage ripple (ΔV_{OUT}) can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (7)$$

Where L_1 is the inductance, and R_{ESR} is the equivalent series resistance of C2.

For electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

The characteristics of C2 also affect the stability of the regulatory system. Ceramic capacitors are recommended for a lower ΔV_{OUT} and improved control loop stability. For polymer or tantalum capacitors, it is recommended to use a 100µF capacitor with an ESR rating below 50mΩ. Ceramic capacitors are recommended to be 10µF.

Setting the V_{IN} Under-Voltage Lockout (UVLO) Threshold

The MPQ4423C has an internal, fixed UVLO threshold. The rising threshold is 3.7V, and the falling threshold is about 3.25V For applications that require a higher UVLO, place an external resistor divider between the VIN and EN/SYNC pins to raise the UVLO threshold (see Figure 7).

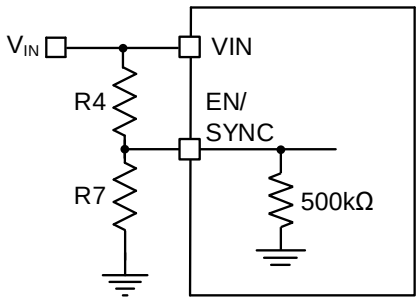


Figure 7: Adjustable UVLO Using EN/SYNC Divider

The UVLO rising threshold ($V_{IN\_UVLO\_RISING}$) can be calculated with Equation (9):

$$V_{IN\_UVLO\_RISING} = (1 + \frac{R4}{500k\Omega // R7}) \times V_{EN\_RISING} \quad (9)$$

Where V_{EN_RISING} is 1.4V.

The UVLO falling threshold ($V_{IN\_UVLO\_FALLING}$) can be calculated with Equation (10):

$$V_{IN\_UVLO\_FALLING} = (1 + \frac{R4}{500k\Omega // R7}) \times V_{EN\_FALLING} \quad (10)$$

Where $V_{EN\_FALLING}$ is 1.25V.

Ensure that R4 has a large enough resistance to limit the current flowing through EN/SYNC below 100µA.

PCB Layout Guidelines [11]

Efficient PCB layout is critical for stable operation and thermal dissipation. For the best results, refer to Figure 8 and follow the guidelines below:

1. Place the high current paths (GND, VIN, and SW) close to the IC via short, direct, and wide traces.
2. Place C1 as close to the VIN and GND pins as possible.
3. Place the VCC capacitor (C_{VCC}) as close to the VCC pin as possible.
4. Place three or more vias on C_{VCC} connected to GND.
5. Connect a large copper plane directly to PGND.
6. Add multiple vias to the PGND plane to improve thermal dissipation.
7. Route the SW and BST traces away from sensitive analog areas, such as FB.

Notes:

11) The recommended PCB layout is based on the typical application circuit with a 5V V_{OUT}, 6A I_{OUT}, and 420kHz f_{SW} with FSS (see Figure 9 on page 19).

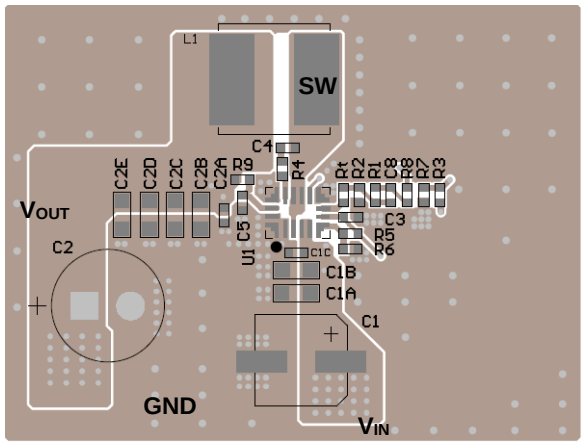


Figure 8: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

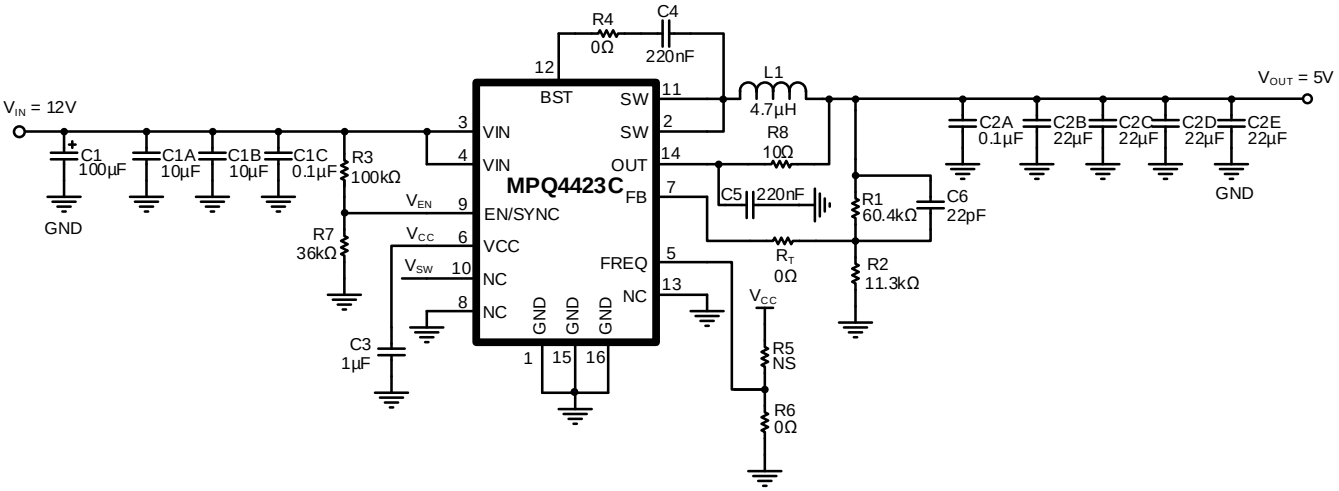


Figure 9: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, f_{SW} = 420kHz with FSS)

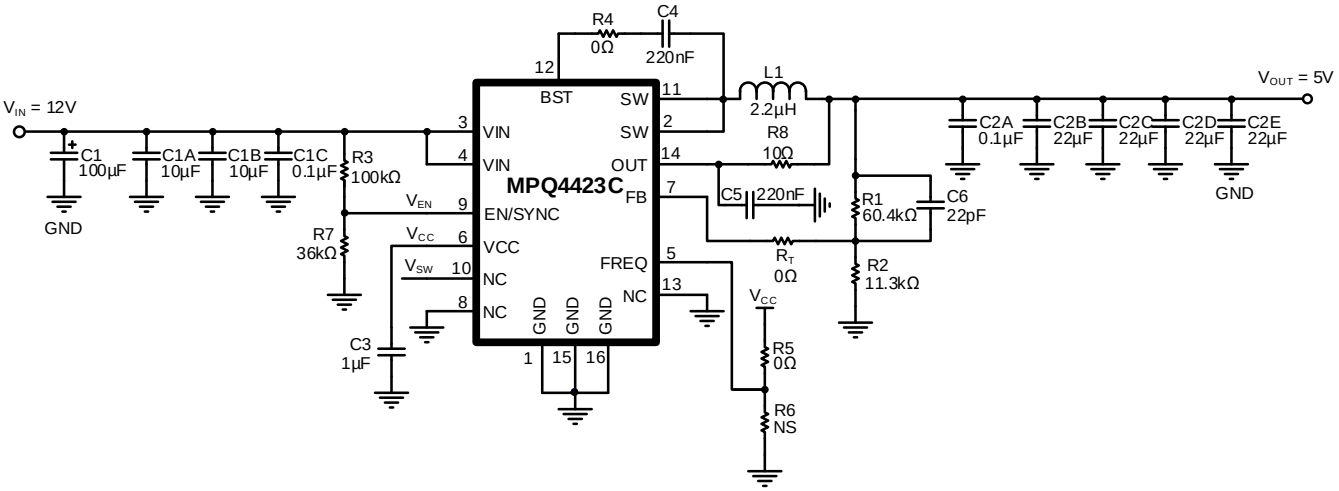


Figure 10: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, f_{SW} = 2.2MHz with FSS)

TYPICAL APPLICATION CIRCUITS *(continued)*

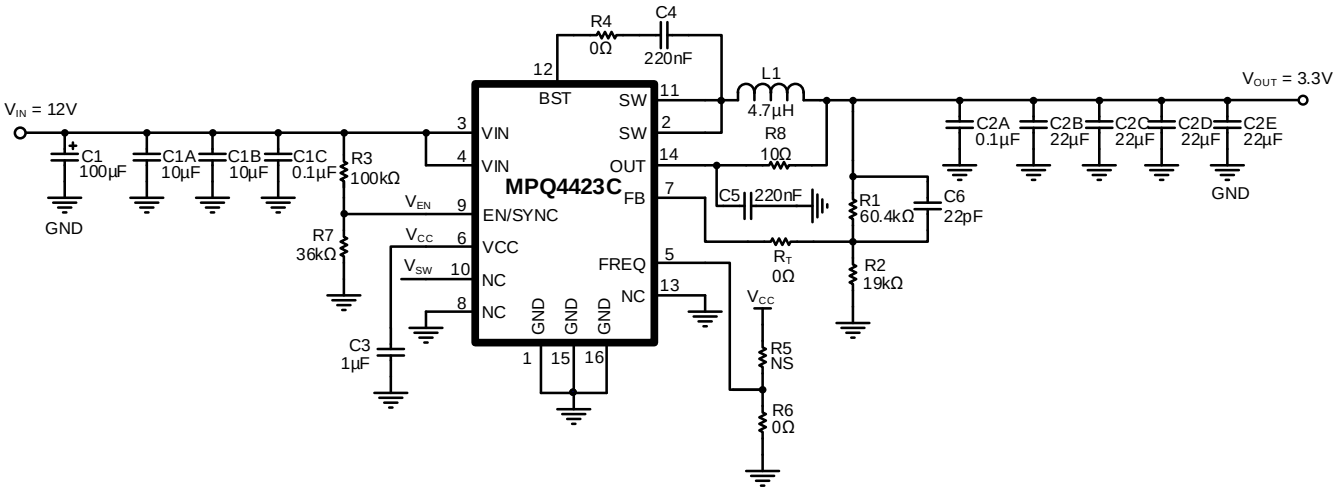


Figure 11: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 6A, f_{SW} = 420kHz with FSS)

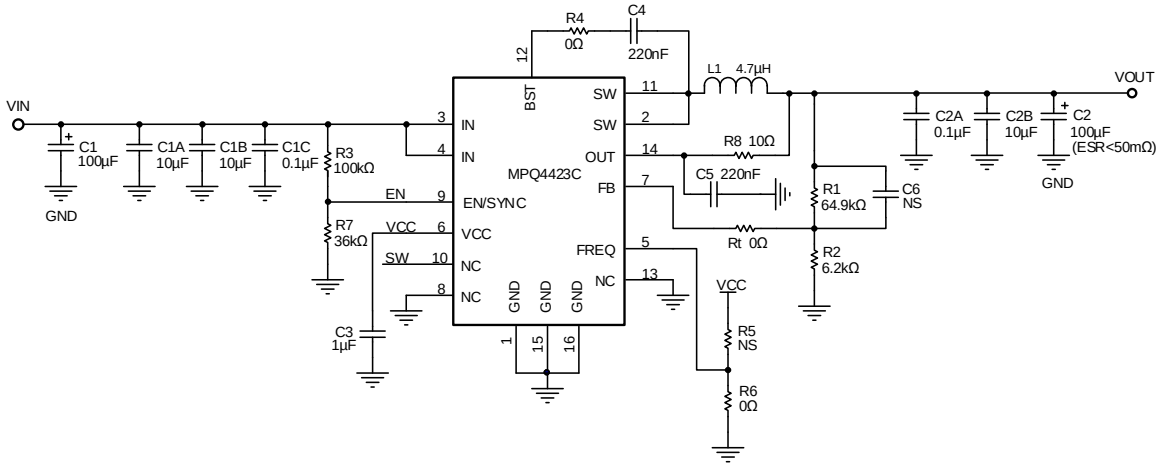
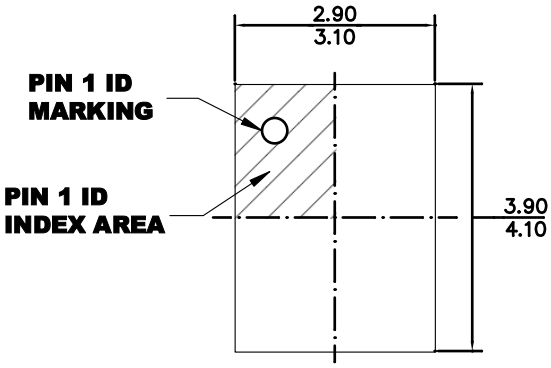


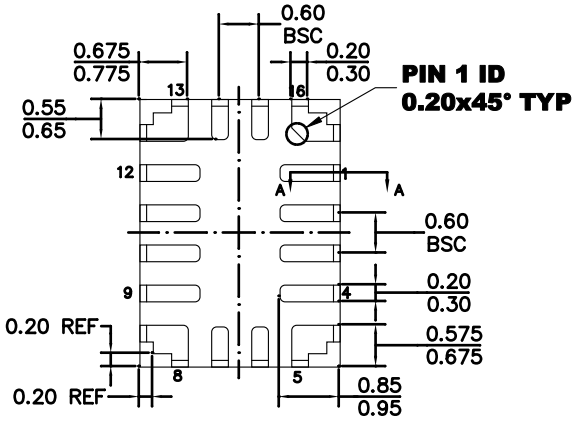
Figure 12: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 9V, I_{OUT} = 6A, f_{SW} = 420kHz with FSS)

PACKAGE INFORMATION

QFN-16 (3mmx4mm)

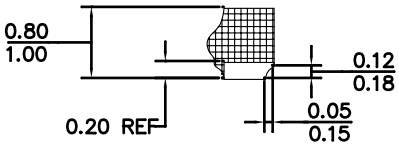


TOP VIEW

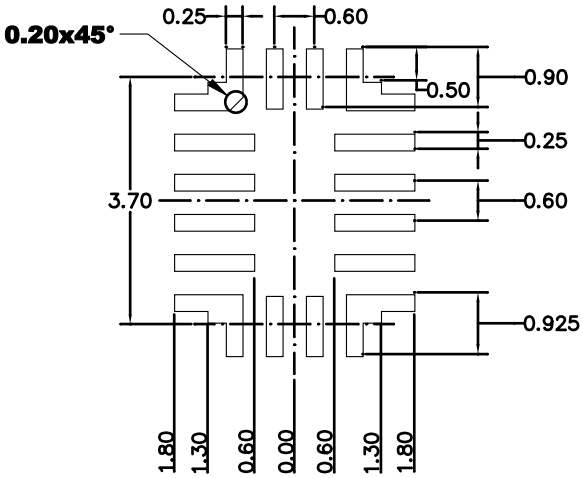


BOTTOM VIEW

SIDE VIEW



SECTION A-A

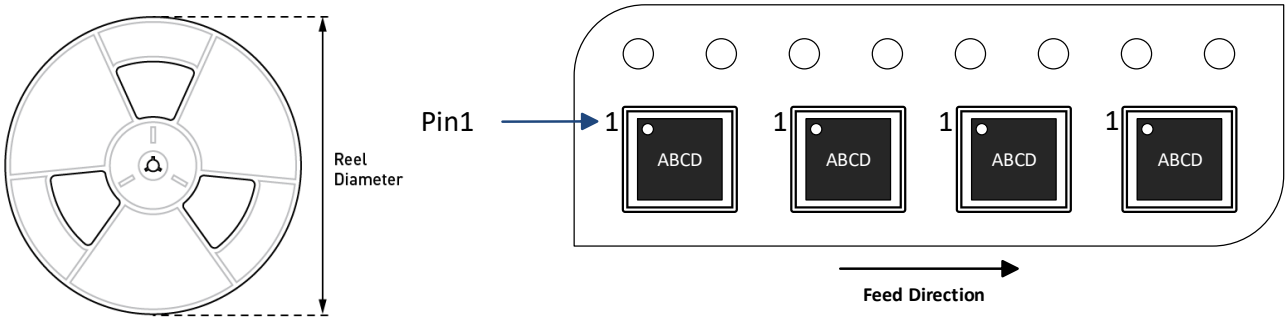


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITIES SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4423CGLE-AEC1-Z	QFN-16 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/28/2021	Initial Release	-