



MPQ6614-AEC1

35V, H-Bridge DC Motor Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ6614-AEC1 is an H-bridge motor driver used for driving reversible motors. It can drive one DC motor, one winding of a stepper motor, or other loads. The H-bridge consists of four N-channel power MOSFETs, and an internal charge pump generates the gate driver voltages.

The MPQ6614-AEC1 operates on a motor power supply voltage from 5V to 35V, which can deliver up to 1.5A of continuous output current (I_{OUT}), depending on thermal and PCB conditions.

An internal current-sense circuit provides an output with a voltage that is proportional to the load current. In addition, cycle-by-cycle current regulation and limiting is provided. These features do not require the use of a low-ohmic shunt resistor.

The MPQ6614-AEC1 has a pulse-width modulation (PWM) input interface, which is compatible with industry-standard devices. A brake is applied when stopping the motor. When disabled, the MPQ6614-AEC1 can achieve a low standby circuit current.

Internal shutdown functions include over-current protection (OCP), short-circuit protection (SCP), under-voltage lockout (UVLO), and thermal shutdown.

The MPQ6614-AEC1 requires a minimal number of readily available, standard external components. The MPQ6614-AEC1 is available in a QFN-8 (2mmx3mm) package with wettable flanks.

FEATURES

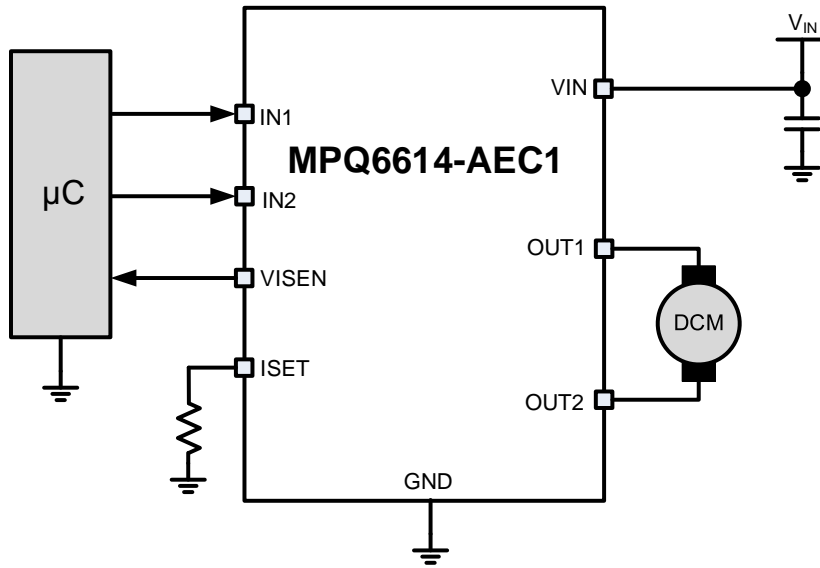
- Wide 5V to 35V Operating Input Voltage (V_{IN}) Range
- Internal Full H-Bridge Driver Supports 100% Duty Cycle
- 1.5A Continuous Output Current (I_{OUT})
- Low On Resistance:
 - High-Side (HS): 250m Ω
 - Low-Side (LS): 190m Ω
- Simple, Versatile Logic Interfaces
- 3.3V and 5V Compatible Logic Supply
- Cycle-by-Cycle Current Regulation/Limit
- Low Standby Circuit Current
- Over-Current Protection (OCP)
- Thermal Shutdown
- Under-Voltage Lockout (UVLO)
- Internal Charge Pump
- Available in a QFN-8 (2mmx3mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Solenoid Drivers
- Brushed DC Motor Drivers

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ6614GDE-AEC1	QFN-8 (2mmx3mm)	See Below	1

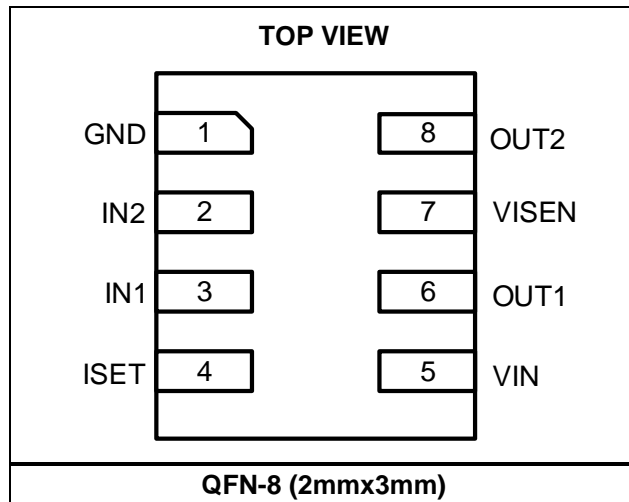
* For Tape & Reel, add suffix -Z (e.g. MPQ6614GDE-AEC1-Z).

TOP MARKING

BRP
YWW
LLLL

BRP: Product code
Y: Year code
WW: Week code
LLLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	GND	Ground.
2	IN2	Input 2. The IN2 pin is connected to an internal pull-down resistor.
3	IN1	Input 1. The IN1 pin is connected to an internal pull-down resistor.
4	ISET	Output current configuring resistor. Connect a resistor from ISET to ground to set the current limit and the VISEN pin's output voltage.
5	VIN	Supply voltage. Connect an input capacitor to VIN to prevent large voltage spikes from appearing at the input.
6	OUT1	Output terminal 1.
7	VISEN	Current-sense output voltage.
8	OUT2	Output terminal 2.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply voltage (V_{IN})	-0.3V to +38V
V_{OUTX}	-0.3V to $V_{IN} + 0.3V$
V_{ISET}	-0.3V to +5V
All other pins to GND	-0.3V to +6V
Continuous power dissipation.....($T_A = 25^\circ C$) ⁽²⁾	
QFN-8 (2mmx3mm)	1.78W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

ESD Ratings

Human body model (HBM)	±2kV
Charged device model (CDM)	±2kV

Recommended Operating Conditions ⁽³⁾

Supply voltage (V_{IN})	5V to 35V
Continuous output current (I_{OUT})	±1.5A
Load current (I_{VISEN})	±2mA
Operating junction temp (T_J)	-40°C to +125°C

Thermal Resistance ⁽⁴⁾

θ_{JA}	θ_{JC}
QFN-8 (2mmx3mm)	70 15... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operation conditions.
- Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.

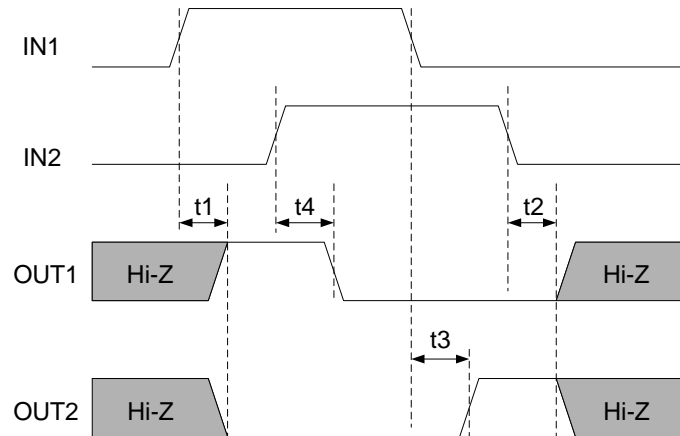
Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
V _{IN} operating range	V _{IN}		5		35	V
Turn-on threshold	V _{IN_ON}	V _{IN} rising edge		4.4	4.7	V
Turn-on hysteretic voltage	V _{IN_HY}			0.2		V
IC Supply						
Shutdown current	I _{IN_SD}	IN1 = IN2 = 0, V _{IN} = 12V		0.1	1.45	μA
		IN1 = IN2 = 0, V _{IN} = 35V		0.15	7	μA
Operating current		IN1 or IN2 = 1, V _{IN} = 12V, no load current		1.3	2.5	mA
		IN1 or IN2 = 1, V _{IN} = 35V, no load current		1.4	2.6	mA
		50kHz PWM, V _{IN} = 12V, no load current		1.6	3	mA
		50kHz PWM, V _{IN} = 35V, no load current		1.8	4	mA
Input Logic (IN1, IN2)						
Input high voltage	V _{IH}		1.5			V
Input low voltage	V _{IL}				0.4	V
Input high current	I _{IH}	V _{IH} = 5V			50	μA
Input low current	I _{IL}	V _{IL} = 0V	-5		+5	μA
Input pull-down resistance	R _{PD}			300		kΩ
Sleep entry time		IN1 = 0V, IN2 = 0V for 2ms		2	5	ms
Sleep recovery time		IN1 or IN2 (or both) = high level		250	500	μs
Switching Frequency						
Externally applied PWM frequency	f _{PWM}				50	kHz
Power MOSFET						
High-side MOSFET (HS-FET) on resistance	R _{DSON_HS}	I _{OUT} = 100mA, T _J = 25°C	180	250	320	mΩ
		I _{OUT} = 100mA, T _J = -40°C to +125°C			380	mΩ
Low-side MOSFET (LS-FET) on resistance	R _{DSON_LS}	I _{OUT} = 100mA, T _J = 25°C	140	190	240	mΩ
		I _{OUT} = 100mA, T _J = -40°C to +125°C			350	mΩ
Minimum on time				250		ns
Output enable time	t ₁				200	ns
Output disable time	t ₂				200	ns
Delay time	t ₃				420	ns
	t ₄				300	ns
Output rising time		R _L = 20Ω	10		100	ns
Output falling time		R _L = 20Ω	10		100	ns
Dead time				200		ns

ELECTRICAL CHARACTERISTICS (continued)
 $V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Protections						
Over-current (OC) threshold			3	4	5	A
Over-current protection (OCP) retry time	t_{OCR}			1		ms
OC deglitch time ⁽⁵⁾				500		ns
Thermal shutdown				165		$^{\circ}C$
Thermal shutdown hysteresis				25		$^{\circ}C$
Current Control						
Off time	t_{ITRIP}	After ITRIP		15		μs
Blanking time				800		ns
ISET current	I_{SET}	$I_{OUT} = 1A$	90	100	110	$\mu A/A$
Current trip voltage (rising)	$V_{ITRIP-R}$	At the VISEN pin	2.88	3	3.12	V
Current trip voltage (falling)	$V_{ITRIP-F}$	At the VISEN pin	2.3	2.4	2.5	V
VISEN Output						
Output voltage accuracy	ΔV_{VISEN}	$0.1V < V_{ISET} < 0.5V$	-10		+10	%
		$V_{ISET} > 0.5V$	-5		+5	%

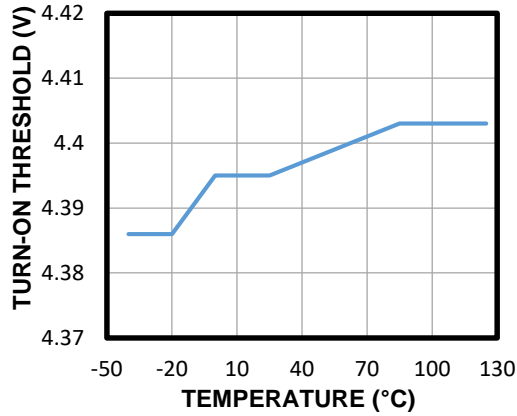
Note:

5) Guaranteed by design. Not tested in production.


Figure 1: Input/Output Timing

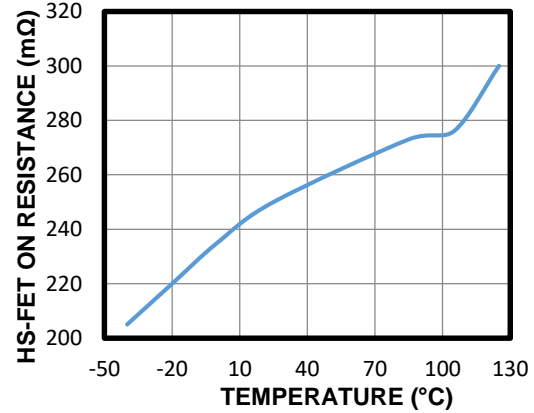
TYPICAL CHARACTERISTICS

Turn-On Threshold vs. Temperature



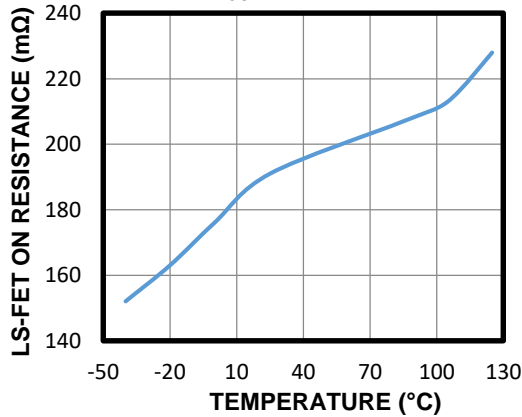
HS-FET On Resistance vs. Temperature

$V_{IN} = 12V, I_{OUT} = 100mA$



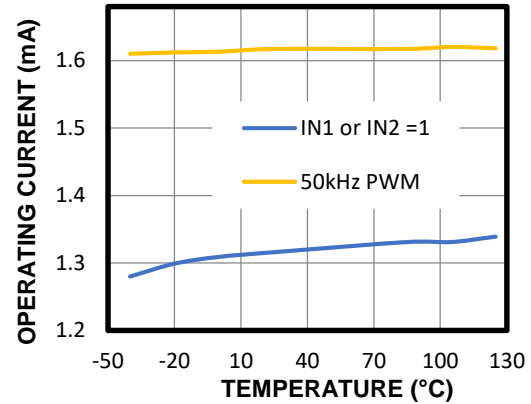
LS-FET On Resistance vs. Temperature

$V_{IN} = 12V, I_{OUT} = 100mA$



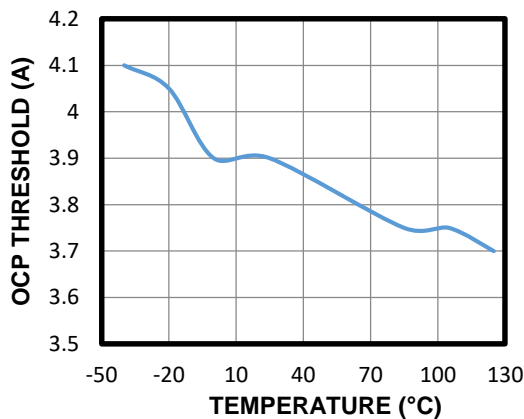
Operating Current vs. Temperature

$V_{IN} = 12V, \text{no load}$



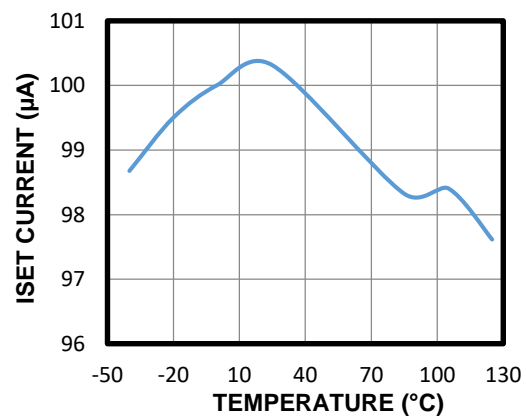
OCP Threshold vs. Temperature

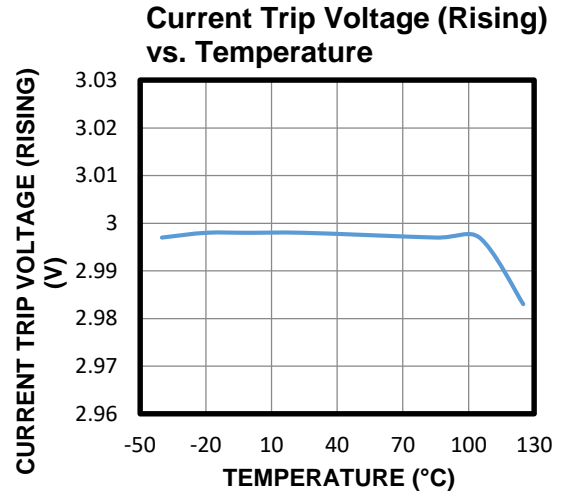
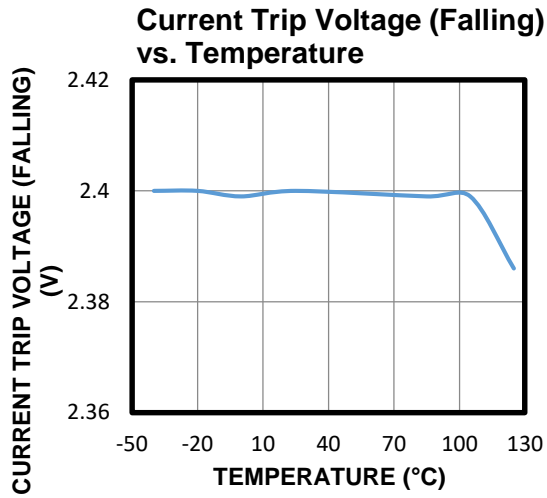
$V_{IN} = 12V$



ISET Current vs. Temperature

$V_{IN} = 12V, I_{OUT} = 1A$

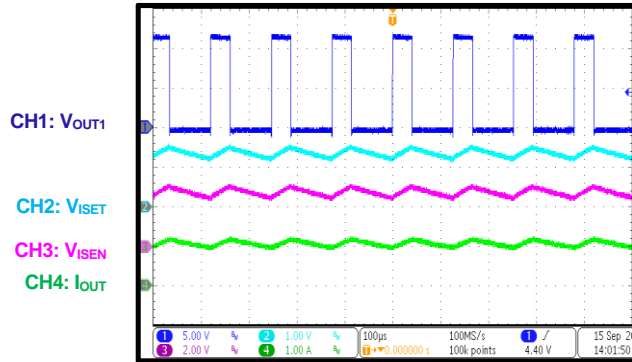


TYPICAL CHARACTERISTICS *(continued)*


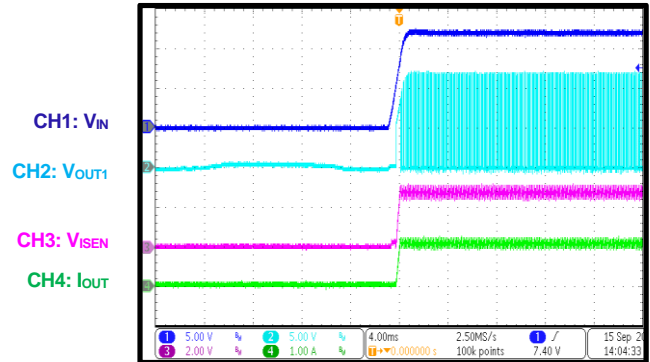
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$, $IN1 = 3.3V$, $IN2 = 0V$, $I_{OUT} = 1.2A$, output current configuring resistor = $12.5k\Omega$, $T_A = 25^\circ C$, resistor + inductor load: $3\Omega + 1.5mH$ between OUT1 and OUT2, unless otherwise noted.

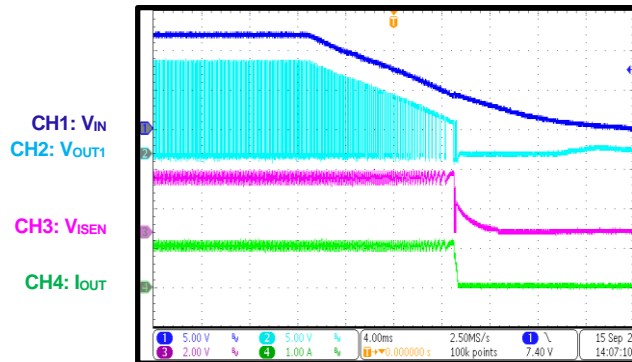
Steady State



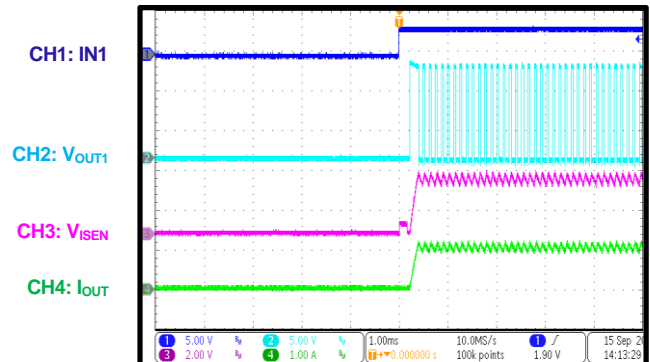
Power Ramping Up



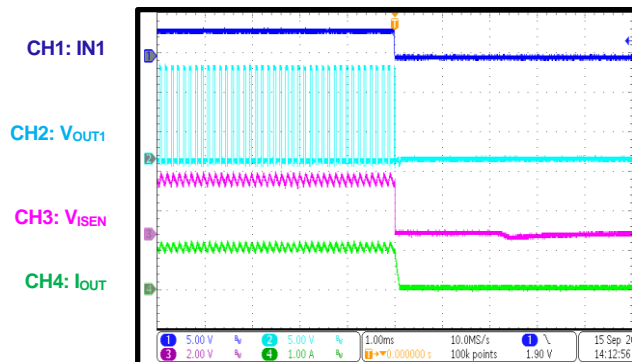
Power Ramping Down



Sleep Recovery



Sleep Entry



FUNCTIONAL BLOCK DIAGRAM

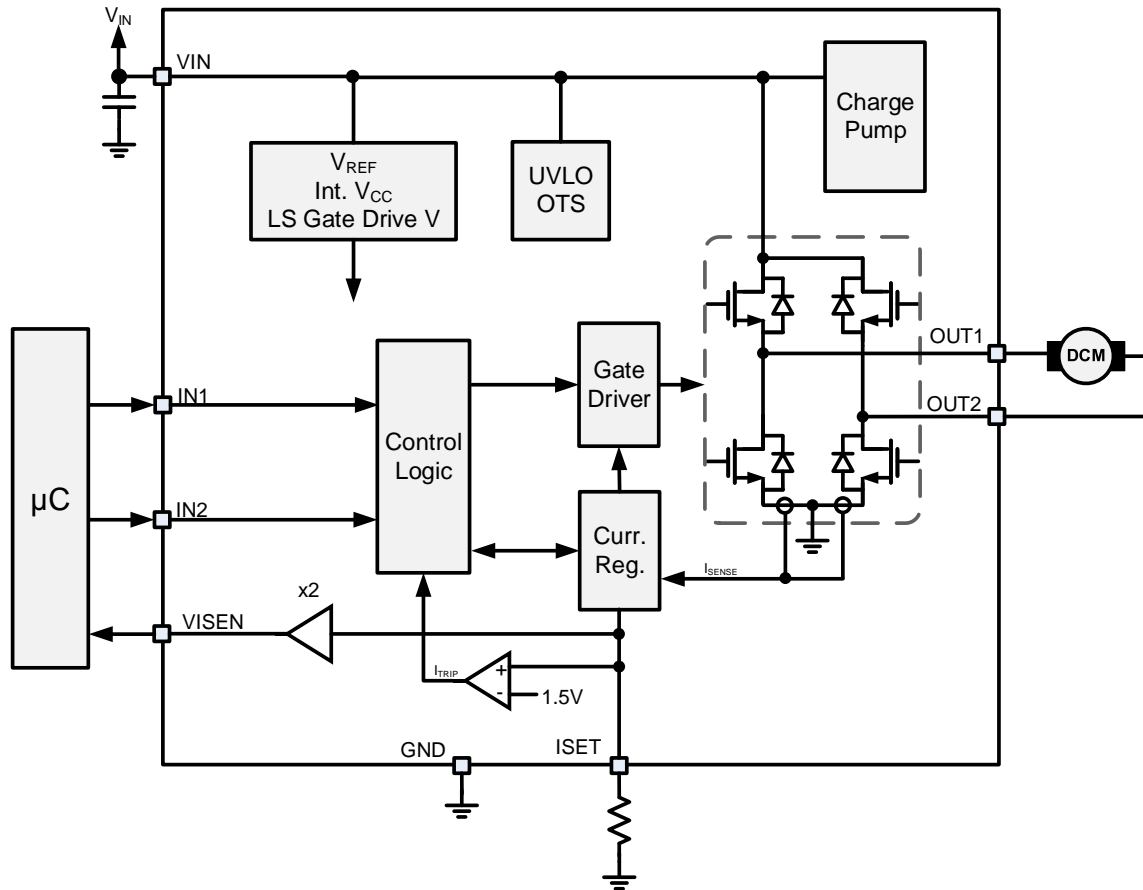


Figure 2: Functional Block Diagram

OPERATION

The MPQ6614-AEC1 is an H-bridge motor driver that integrates four N-channel power MOSFETs with 1.5A of continuous output current (I_{OUT}) capability. The MPQ6614-AEC1 operates across a wide 5V to 35V input voltage (V_{IN}) range and is designed to drive bipolar stepper motors, brushed DC motors, solenoids, and other loads.

Current Sensing

The current flowing in the two low-side MOSFETs (LS-FETs) is sensed with an internal current-sensing circuit. A voltage that is proportional to the output current (I_{OUT}) is sourced on VISEN.

The VISEN pin's output voltage is twice the value of the voltage on the ISET pin. The voltage on the ISET pin is set by a resistor connected between ISET and ground. For 1A of I_{OUT} , 100 μ A of current is sourced into the resistor connected to ISET. For example, if a 10k Ω resistor is connected between ISET and ground, the voltage on the ISET pin is 1V for every 1A (1V/A) of output current, and the output voltage on VISEN is 2V/A of output current.

The current is sensed when one of the LS-FETs is turned on, including during slow decay (brake) mode.

The load current applied to VISEN should be kept below 2mA, with no more than 500pF of capacitance.

Current Limit/Regulation

The current in the outputs is limited using constant-off-time pulse-width modulation (PWM) control circuitry. Figure 3 shows the operation sequence, which is described in

greater detail below.

1. A diagonal pair of MOSFETs turns on and drives current through the load.
2. The current increases in the load, which is then sensed by the internal current-sense circuit.
3. If the load current reaches the current trip threshold, the H-bridge switches to slow decay mode. Meanwhile, two LS-FETs turn on.
4. After a fixed off time (t_{ITRIP}), if the load current falls at least 20% below the current trip threshold (I_{TRIP}), the MOSFETs are re-enabled and the cycle repeats.
5. If the current still does not reach 20% below I_{TRIP} , t_{ITRIP} is extended until the current falls to 20% below I_{TRIP} .

The current limit threshold is reached when ISET reaches 1.5V. For example, with a 10k Ω resistor from ISET to ground, the ISET voltage is 1V/A of the output current. Therefore, when the current reaches 1.5A, the ISET voltage reaches 1.5V, and VISEN's output voltage reaches 3V, a current trip occurs.

Blanking Time

There is often a current spike during the start-up process, due to the body diode's reverse-recovery current or the load's shunt capacitance. This current spike requires filtering to prevent it from erroneously shutting down the high-side MOSFET (HS-FET). An internal, fixed blanking time blanks the output of the current-sense comparator when the outputs are switched. This blanking time also sets the minimum on time for the HS-FET.

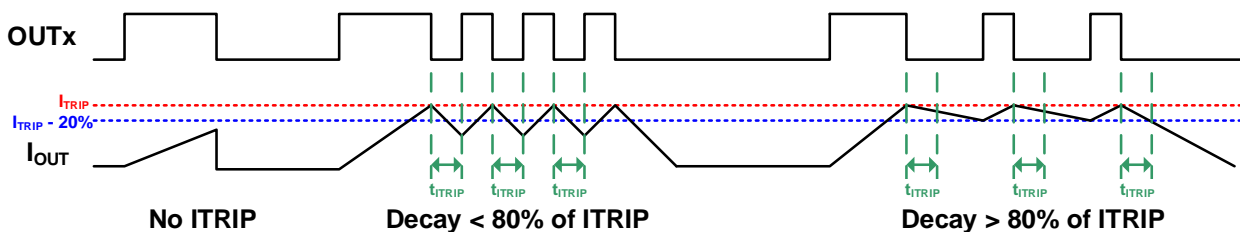


Figure 3: Current Limit/Regulation

Input Logic

The MPQ6614-AEC1 is controlled using a PWM input interface that is compatible with industry-standard devices. Table 1 shows the logic for the MPQ6614-AEC1.

Table 1: Output Control Pins

IN1	IN2	OUT1	OUT2	Function (DC Motor)
Low	Low	Hi-Z	Hi-Z	Coast (sleep entered after 2ms)
Low	High	Low	High	Reverse (current OUT2 to OUT1)
High	Low	High	Low	Forward (current OUT1 to OUT2)
High	High	Low	Low	Brake, LS-FET slow decay

nSLEEP Operation

If the input pins (IN1 and IN2) both stay at a low level for a certain time, then the MPQ6614-AEC1 enters a low-power sleep mode. In this state, all unnecessary internal circuitry shuts down. If the device starts up while both inputs are low, the device immediately enters sleep mode. If IN1 or IN2 are high for at least 50ns, the device resumes normal operation 250µs later.

Over-Current Protection (OCP)

The over-current protection (OCP) circuit limits the current through each MOSFET by reducing the gate drive to the MOSFET.

If the MOSFET remains at the current-limit condition for longer than the OC deglitch time, all MOSFETs in the H-bridge are disabled. The driver remains disabled for t_{OCR} , at which point it is re-enabled automatically.

OC conditions are sensed on both the HS-FETs and LS-FETs (e.g. a short to ground, supply, or across the motor winding) results in an OC shutdown.

Note that OCP does not use the current-sense circuitry that is used for PWM current control. OCP is independent of the ISET resistor value.

Junction Thermal Shutdown

If the IC junction temperature (T_J) exceeds its safe limits, the IC stops switching. Normal operation resumes once T_J falls to a safe level.

Input Under-Voltage Lockout (UVLO) Protection

If V_{IN} falls below its under-voltage lockout (UVLO) threshold, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes once V_{IN} exceeds the UVLO threshold.

APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the supply bypass capacitors as close as possible to the IC.
2. Place as many GND vias as possible near the input capacitors to improve thermal performance.

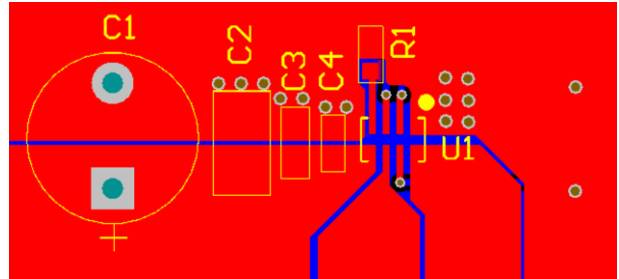


Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

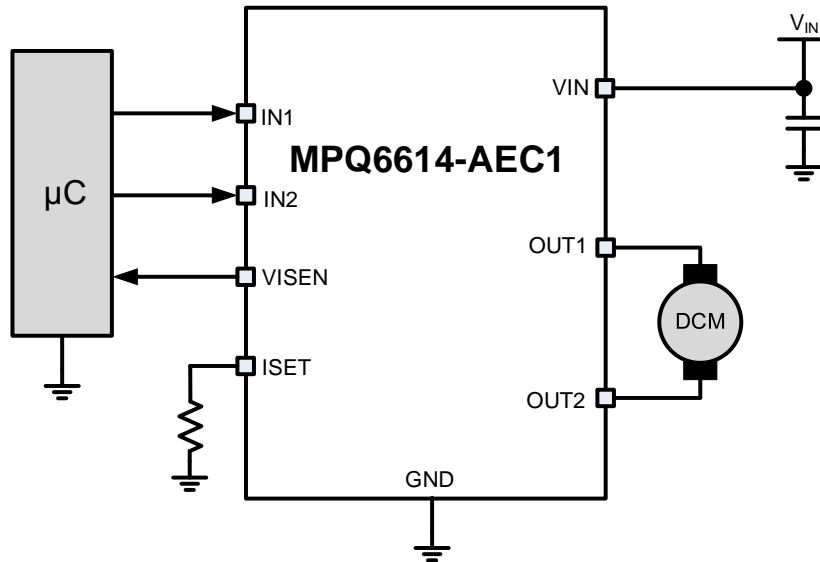
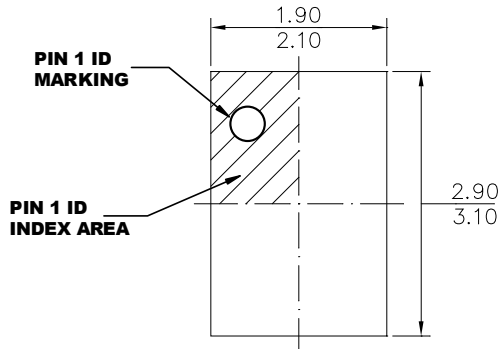


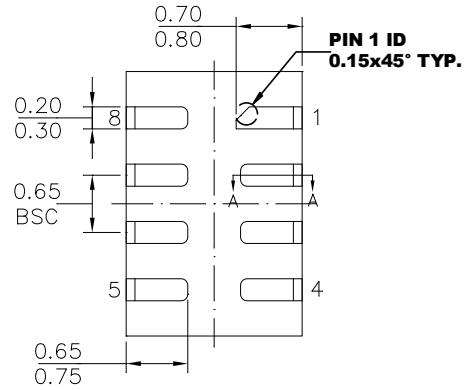
Figure 5: Typical Application Circuit

PACKAGE INFORMATION

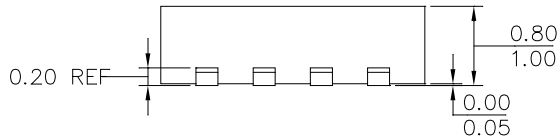
QFN-8 (2mmx3mm) Wettable Flank



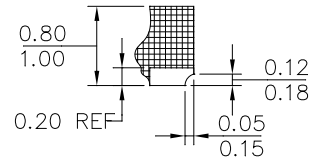
TOP VIEW



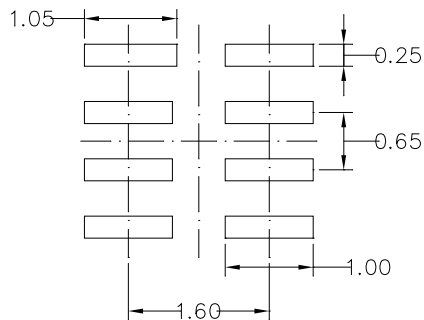
BOTTOM VIEW



SIDE VIEW



SECTION A-A

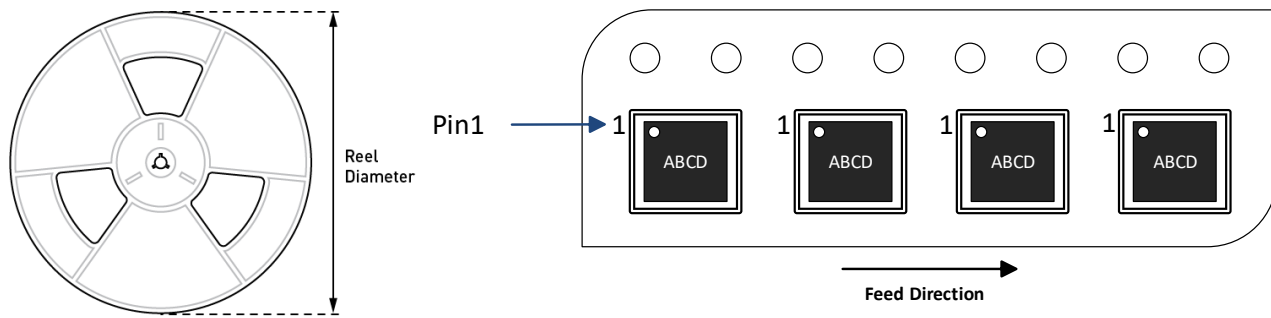


RECOMMENDED LAND PATTERN

NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6614GDE-AEC1-Z	QFN-8 (2mmx3mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/1/2023	Initial Release	-

Notice: The information in this document is subject to change without notice. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.