MPQ6653-AEC1

35V, Single-Phase BLDC Motor Driver with Embedded Hall Sensor, AEC-Q100 Qualified

DESCRIPTION

The MPQ6653-AEC1 is a single-phase brushless DC (BLDC) motor driver with integrated power MOSFETs and an embedded Hall sensor. It drives a single-phase BLDC motor, with up to 1.2A of phase peak current. The input voltage (V_{IN}) range is between 5.5V and 35V.

The MPQ6653-AEC1 controls the motor speed through the pulse-width modulation (PWM) signal or the DC voltage on the PWM pin. The device features configurable soft commutation and a Hall offset angle that can flexibly optimize performance.

The MPQ6653-AEC1 also provides rotational speed detection. The rotational speed detector (the FG/RD pin) is an open-drain output that outputs a high or low voltage relative to the internal Hall comparator's output.

Rich protections include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown protection.

The MPQ6653-AEC1 is available in TSOT23-6-SL and TSOT23-6 packages, and it is available in AEC-Q100 Grade 1.

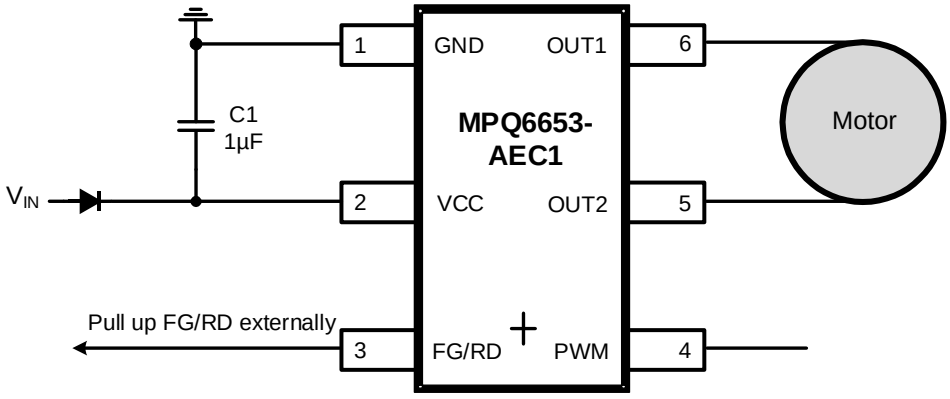
FEATURES

- 5.5V to 35V Operating Input Voltage (V_{IN}) Range
- On-Chip Hall Sensor
- Integrated High-Side MOSFET (HS-FET) and Low-Side MOSFET (LS-FET): 960mΩ
- Soft Commutation
- Starting Duty Set with Hysteresis
- Selectable Open-Loop or Closed-Loop Speed Control
- Configurable Soft Accelerate Time
- Configurable Hall Leading/Lag Angle
- Supports 50Hz to 100kHz Pulse-Width Modulation (PWM) Input Frequency or DC Input
- Automatic Reverse Current Block
- 24kHz PWM Output Frequency
- Configurable Current Limit
- Short-Circuit Protection (SCP)
- Over-Voltage Protection (OVP)
- Standby Mode
- Selectable FG and RD Output
- Available in TSOT23-6-SL and TSOT23-6 Packages
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Seat Fans
- Automotive Fans
- Cooling Fans
- General Fans

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ6653GJS-xxxx-AEC1**	TSOT23-6-SL	*See Below*	1
MPQ6653GJ-xxxx-AEC1**	TSOT23-6		

* For Tape & Reel, add suffix -Z (e.g. MPQ6653GJS-xxxx-AEC1-Z).

** “xxxx” is the configuration code identifier. The four digits of the suffix (“xxxx”) can be a hexadecimal value between 0 and F. “0000” is the default code. Work with an MPS FAE to create this unique number, even when ordering the “0000” code.

TOP MARKING (MPQ6653GJS-xxxx-AEC1)

BVVY
LLL

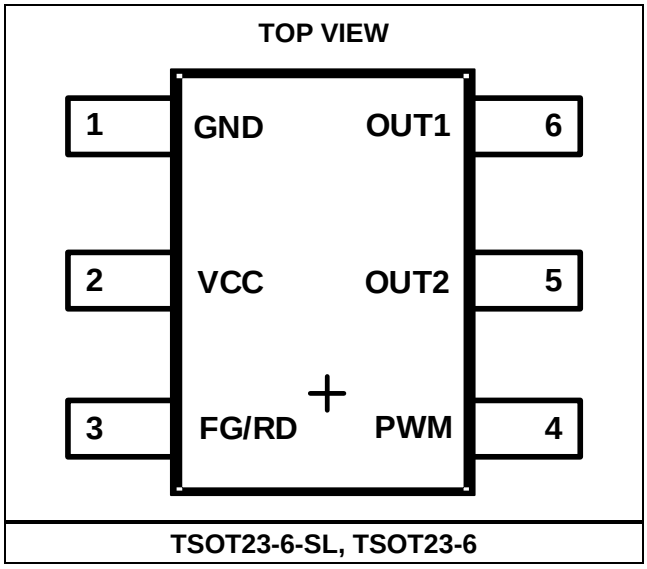
BVV: Product code
Y: Year code
LLL: Lot number

TOP MARKING (MPQ6653GJ-xxxx-AEC1)

| BVVY

BVV: Product code
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Ground.**
2	VCC	**Input power supply.** The VCC pin must be locally bypassed.
3	FG/RD	**Speed (FG) or rotor deadlock (RD) indicator output.** The FG/RD pin is an open-drain output. Pull up FG/RD externally.
4	PWM	**Speed control pulse-width modulation (PWM) input.** The PWM pin supports a 50Hz to 100kHz PWM input frequency or a 0V to 3V DC input. Pull PWM high internally by 100kΩ.
5	OUT2	**Motor driver output 2.** The OUT2 pin is connected to the mid-point of the internal N-channel MOSFET half-bridge.
6	OUT1	**Motor driver output 1.** The OUT1 pin is connected to the mid-point of the internal N-channel MOSFET half-bridge.

ABSOLUTE MAXIMUM RATINGS (1)

VCC, PWM, FG/RD .....-0.3V to +40V
OUT1, OUT2.....-0.3V to V_{CC} + 0.3V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Continuous power dissipation (2) 1.25W
Junction temperature (T_J) .....150°C
Supply voltage (V_{IN}) .....5.5V to 35V
Operating temperature..... -40°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....5.5V to 35V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6-SL, TSOT23-6 .....100……55...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

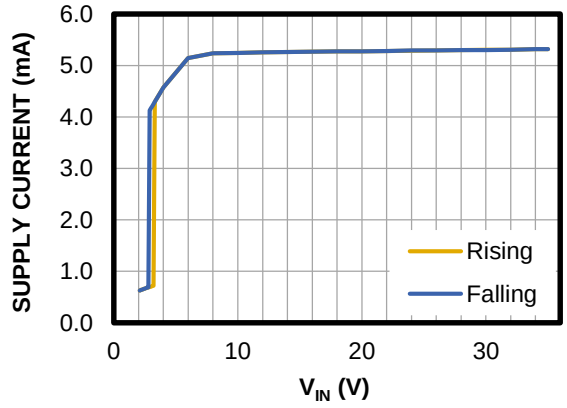
Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{CC} under-voltage lockout (UVLO) rising threshold	V_{UVLO_R1}	-40°C to +125°C		3.1	3.3	V
V_{CC} UVLO rising threshold	V_{UVLO_R2}	150°C		4.75		V
V_{CC} UVLO falling threshold	V_{UVLO_F}			2.8	3	V
Operating supply current	I_{CC}	PWM = high		5	7	mA
Standby current	I_{STD}	PWM = low		75		µA
Pulse-width modulation (PWM) input high threshold	V_{PWM_H}		2.2			V
PWM input low threshold	V_{PWM_L}				0.8	V
DC input high threshold	V_{DC_H}			3		V
DC input low threshold	V_{DC_L}			100		mV
PWM internal pull-up resistance	R_{PWM}			100		kΩ
Low-level FG/RD output	V_{FG_L}	$I_{FG/RD}$ = 3mA			0.43	V
Switching frequency	f_{SW}	T_A = 25°C		24		kHz
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 100mA		480		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	I_{OUT} = 100mA		480		mΩ
Cycle-by-cycle current limit	I_{OCP}	OCP_SEL = 1		1.2		A
Peak current limit	I_{LIMIT_PEAK}			1.8		A
Zero-current detection (ZCD) threshold	I_{ZCD}			0		mA
Soft-on commutation angle	θ_{SON}	SON[4:0] = 0x10		46.4		°
Soft-off commutation angle	θ_{SOFF}	SOFF[4:0] = 0x10		46.4		°
Hall lead/lag angle	θ_{HAL}	HAL_ANG[3:0] = 0xF		21.8		°
Rotor deadlock protection detection time	t_{RD}			0.6		sec
Rotor deadlock protection retry time	t_{RE}	LOCK_SEL = 0		3.6		sec
Over-voltage protection (OVP) threshold	V_{OVP_H}	OVP_DIS = 0, OVP_H = 1		31	34	V
	V_{OVP_L}	OVP_DIS = 0, OVP_H = 0		19	21	V
OVP hysteresis	V_{OVP_HYS}			2	3	V
Operation point	B_{OP}			1	2	mT
Release point	B_{RP}		-2	-1		mT
Thermal shutdown threshold	T_{ST}			165		°C
Thermal shutdown hysteresis	T_{ST_HYS}			20		°C

TYPICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

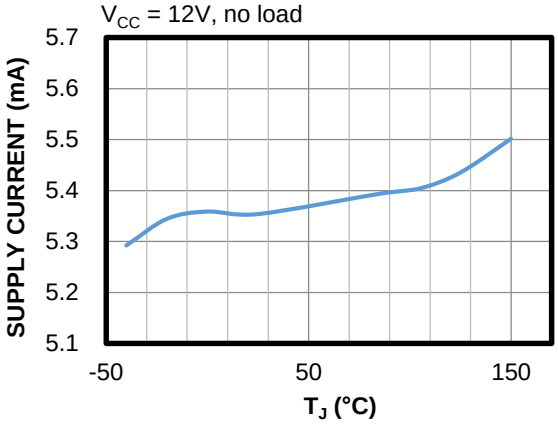
Supply Current vs. Input Voltage

V_{CC} = 2V to 35V, no load, T_J = 25°C

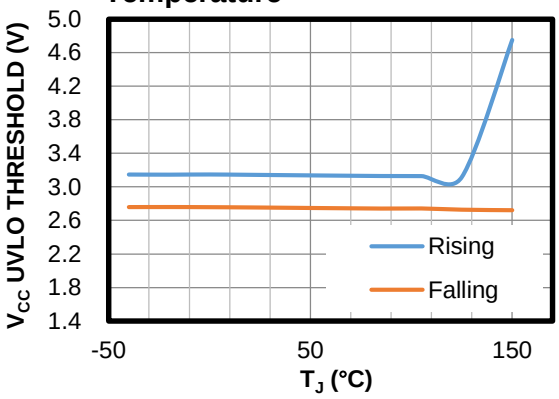


Supply Current vs. Junction Temperature

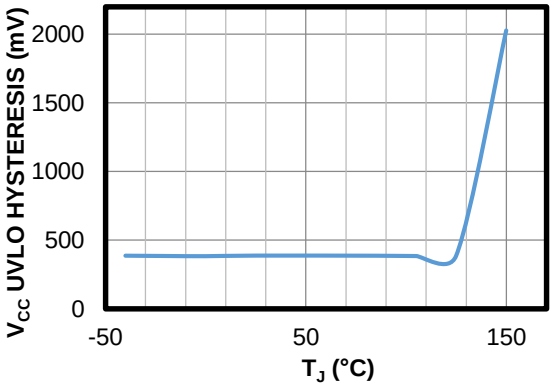
V_{CC} = 12V, no load



V_{CC} UVLO Threshold vs. Junction Temperature

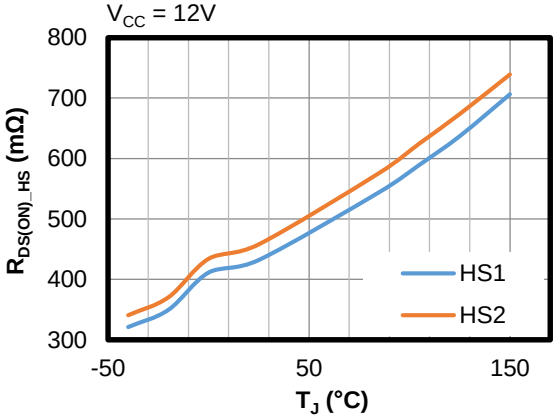


V_{CC} UVLO Hysteresis vs. Junction Temperature



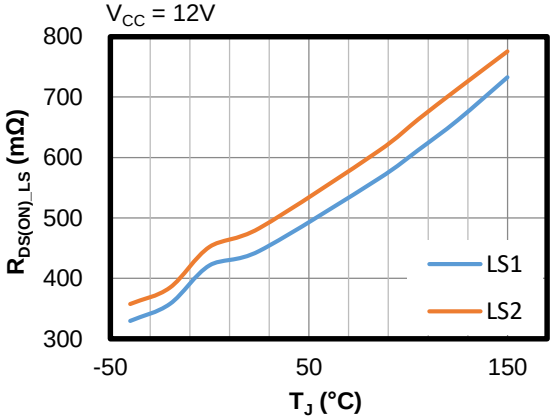
HS-FET On Resistance vs. Junction Temperature

V_{CC} = 12V



LS-FET On Resistance vs. Junction Temperature

V_{CC} = 12V

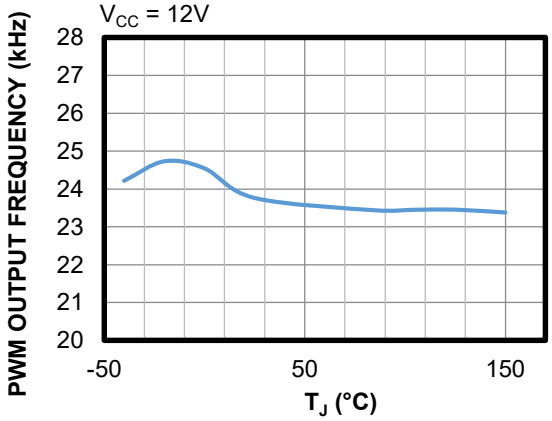


TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

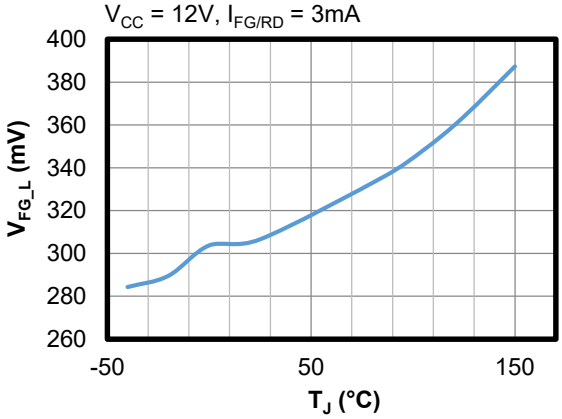
PWM Output Frequency vs. Junction Temperature

V_{CC} = 12V



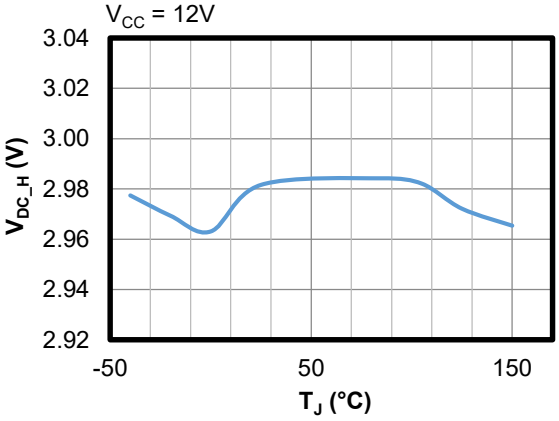
Low-Level FG/RD Output vs. Juntion Temperature

V_{CC} = 12V, $I_{FG/RD}$ = 3mA



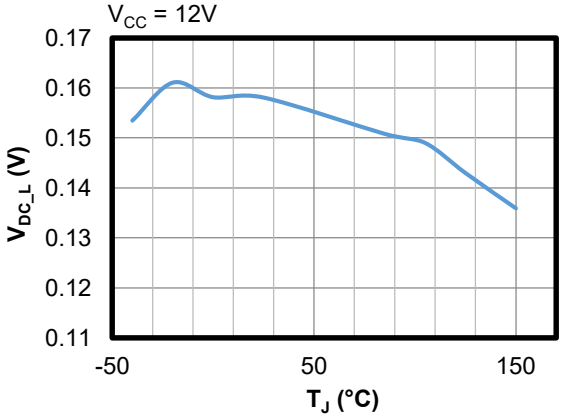
DC Input High Threshold vs. Junction Temperature

V_{CC} = 12V



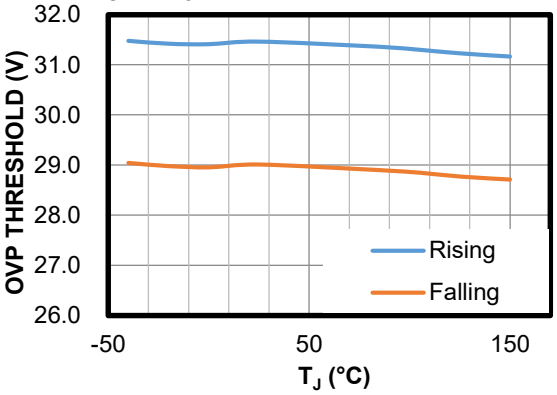
DC Input Low Threshold vs. Junction Temperature

V_{CC} = 12V



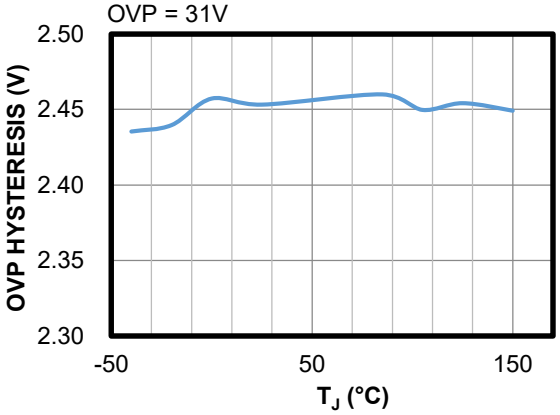
Over-Voltage Protection vs. Junction Temperature

OVP = 31V



OVP Hysteresis vs. Junction Temperature

OVP = 31V

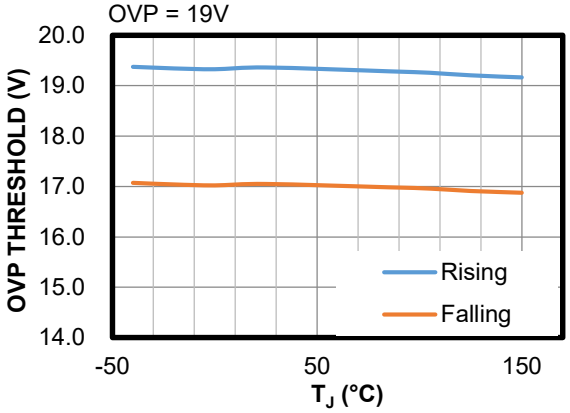


TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

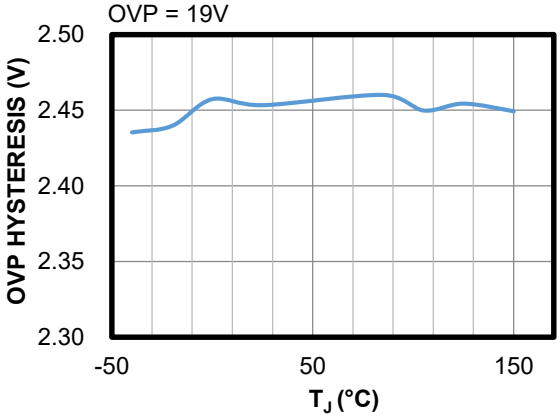
Over-Voltage Protection vs. Junction Temperature

OVP = 19V



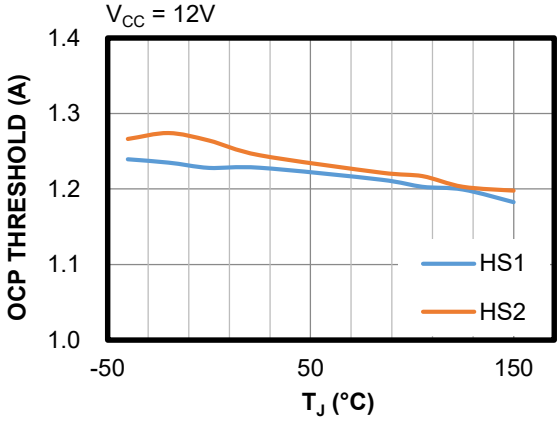
OVP Hysteresis vs. Junction Temperature

OVP = 19V



Over-Current Protection vs. Junction Temperature

V_{CC} = 12V

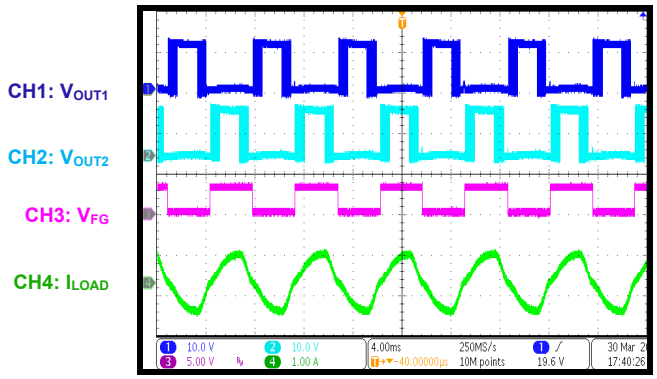


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, 450mA, 5000rpm, 8025 axial fan, T_A = 25°C, unless otherwise noted.

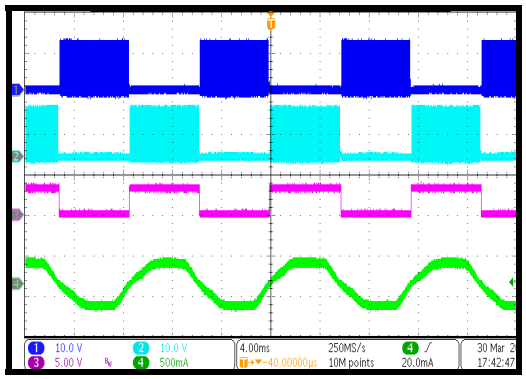
Steady State

PWM duty cycle = 100%



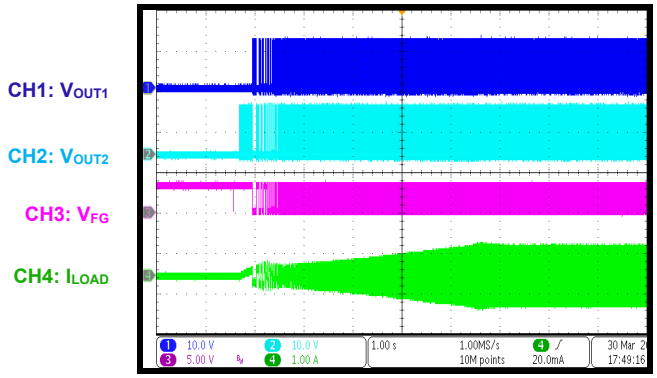
Steady State

PWM duty cycle = 50%



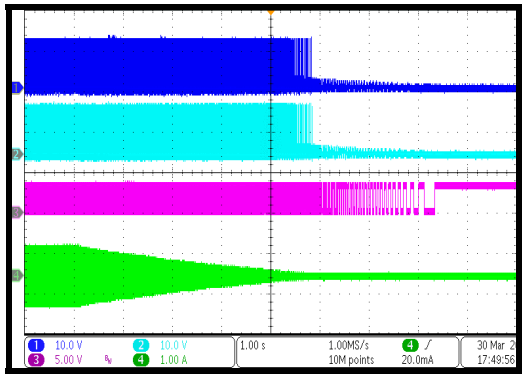
PWM On

PWM duty cycle = 0% to 100%



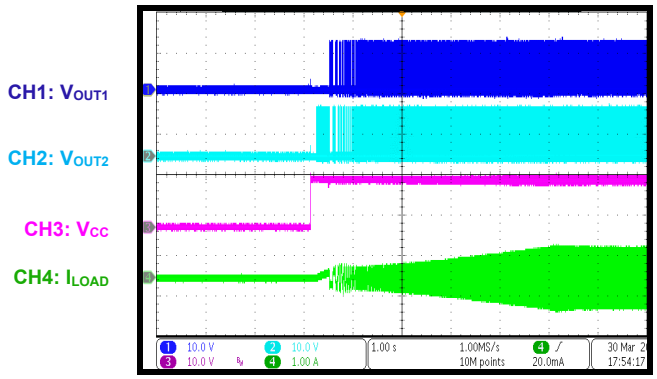
PWM Off

PWM duty cycle= 100% to 0%



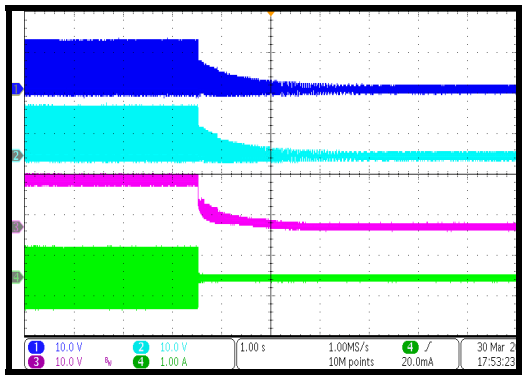
Start-Up through VCC

VCC power plugged in



Shutdown through VCC

VCC power not plugged in

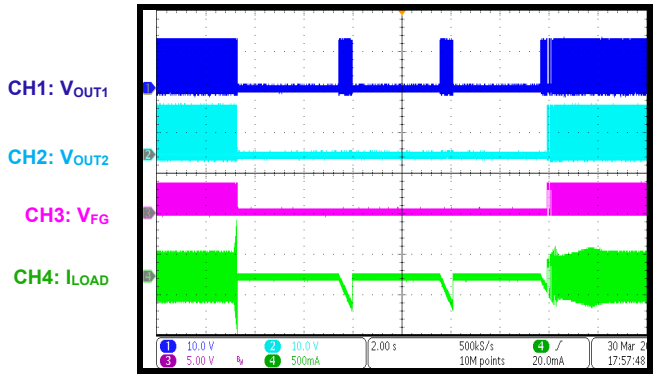


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, 450mA, 5000rpm, 8025 axial fan, T_A = 25°C, unless otherwise noted.

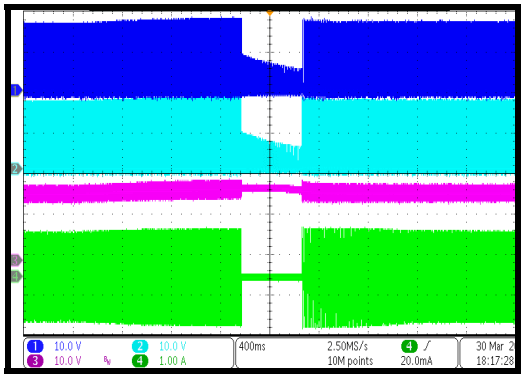
Locked-Rotor Protection

PWM duty cycle = 50%, lock rotor



Over-Voltage Protection

VCC ramps up, then ramps down,
OVP threshold = 19V



FUNCTIONAL BLOCK DIAGRAM

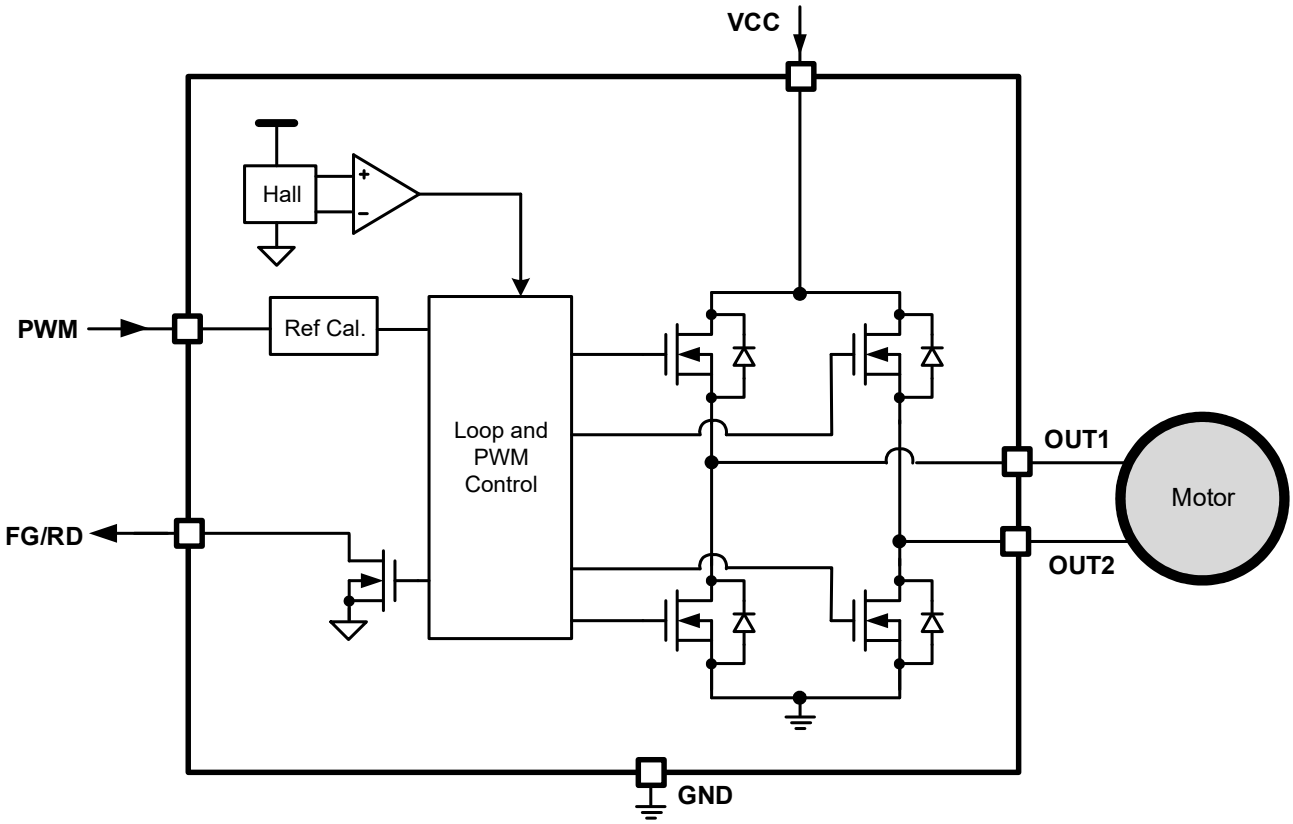


Figure 1: Functional Block Diagram

OPERATION

The MPQ6653-AEC1 is a single-phase brushless DC (BLDC) motor driver with integrated power MOSFETs and a Hall-effect sensor. The device controls the motor speed through the pulse-width modulation (PWM) signal or DC voltage on the PWM pin. It features configurable soft on/off commutation. The configurable Hall angle offset angle can flexibly optimize performance.

The MPQ6653-AEC1 also provides rotational speed detection. The rotational speed detector (the FG/RD pin) is an open drain that outputs a high or low voltage relative to the internal Hall comparator's output.

Rich protection includes input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown protection.

Speed Control

The PWM signal or DC voltage applied on the PWM pin controls the fan rotation speed. By default, the PWM signal is selected. A wide 50Hz to 100kHz PWM frequency (f_{PWM}) range is supported by the register setting.

If LOW_F = 0, the f_{PWM} range is between 1kHz and 100kHz. The PWM signal resolution is 163ns. If LOW_F = 1, the f_{PWM} range is between 50Hz and 2kHz. The PWM signal resolution is 2.6μs.

In PWM input mode, the input PWM duty cycle is detected, and the rotation speed is controlled by the input PWM duty cycle. In DC input mode, the DC input voltage is converted to a PWM duty cycle that controls the rotation speed.

The MPQ6653-AEC1 provides open-loop or closed-loop speed control, which is configured by the register setting. In open-loop speed control, the output duty cycle of OUT1 or OUT2 is adjusted based on the input PWM duty cycle or DC input voltage on the PWM pin.

In closed-loop speed control, the input PWM duty cycle or DC input voltage is detected, then converted to a reference speed. The motor's rotation speed is fed back to the control loop, and the output duty cycle is adjusted by the control loop to make the rotation speed equal to the reference speed.

Starting Duty

The D0[6:0] bits set the starting duty cycle. If the input duty cycle is below the starting duty, the IC does not switch, and the fan stops. Figure 2 shows the minimum speed of the starting duty.

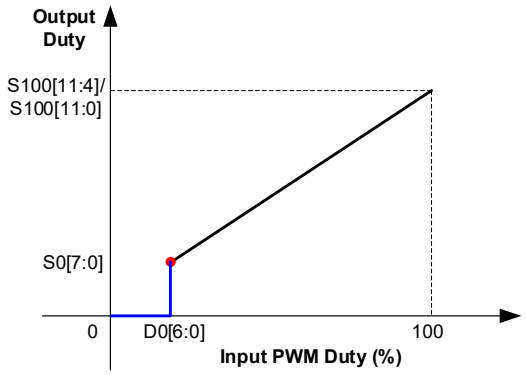


Figure 2: Minimum Speed of Starting Duty

Stop Duty

The MPQ6653-AEC1 stops the fan if the PWM duty cycle exceeds the stop duty cycle. Figure 3 shows the fan stopping at high duty cycle.

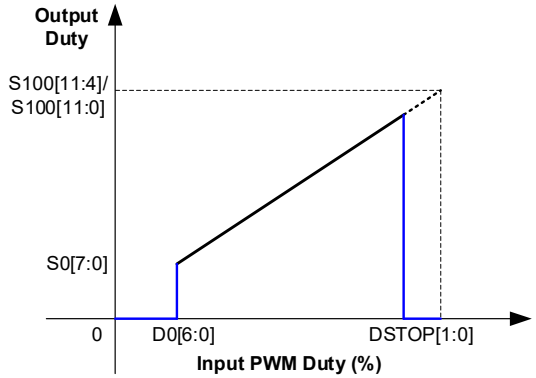


Figure 3: Fan Stopping at High Duty Cycle

The register bits configure the stop duty cycle, as described below:

- If DSTOP[1:0] = 00, there are no stops.
- If DSTOP[1:0] = 01, the stop duty cycle is 100%.
- If DSTOP[1:0] = 10, the stop duty cycle is 95%.
- If DSTOP[1:0] = 11, the stop duty cycle is 90%.

OUT1/OUT2 Normal Operation

In normal operation, the MPQ6653-AEC1 controls the switching of the H-bridge MOSFETs based on a set timing sequence (see Figure 4). This reduces the speed variation and increases system efficiency.

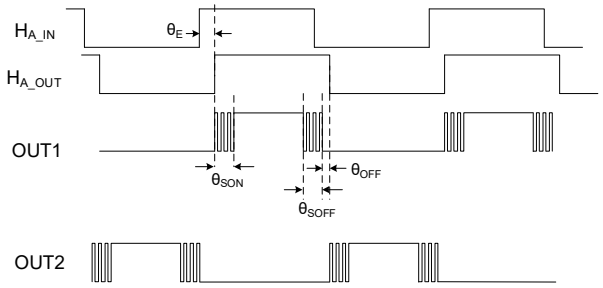


Figure 4: Operation with Hall Offset Angle

The operation sequence is based on the Hall signal coming from the embedded Hall sensor. H_{A_IN} is the original Hall from the embedded Hall. H_{A_OUT} is generated based on H_{A_IN} with a phase shift, and the shifted phase (θ_E) is configured by the Hall offset angle register.

If the H_{A_OUT} signal is high, OUT2 remains low constantly while OUT1 switches phases. If the H_{A_OUT} signal is low, OUT1 remains low constantly while OUT2 switches phases. The Hall offset angle is dependent on the following factors:

- The Hall offset angle is dependent on HAL_ANG[3:0].
- The Hall offset angle leading/lag direction is set by the HAL_FLAG bit.
- When HAL_ANG[3:0] = 0000, the Hall offset angle is 0.

Soft-On Commutation

During soft-on commutation (θ_{SON} in Figure 4), the switching phase's output duty cycle gradually increases from 0% to the target duty cycle, and the other phase keeps the low-side MOSFETs (LS-FETs) on.

The SON[4:0] bits set the soft-on commutation angle, which is between 0° and 90°. Note that the high soft-on commutation angle leads to a lower rotation speed under the same conditions.

Soft-Off Commutation

During soft-off commutation (θ_{SOFF} in Figure 4), the switching phase's output duty cycle gradually decreases from the target duty cycle to 0%, and the other phase keeps the LS-FETs on.

The SOFF[4:0] bits set the soft-off commutation angle, which is between 0° and 90°. Note that the larger soft-off commutation angle helps to eliminate the reverse current, but it also leads to a lower rotation speed under the same conditions.

Soft-On/Off Commutation Angle Linear Interpolation

The soft-on/off commutation angle can be set to linearly change as the output varies. The SON[4:0] and SOFF[4:0] bits set the soft-on and soft-off commutation angle when the output duty is 100%. The commutation angle linearly increases to 90° when the output duty cycle decreases to 0 (see Figure 5).

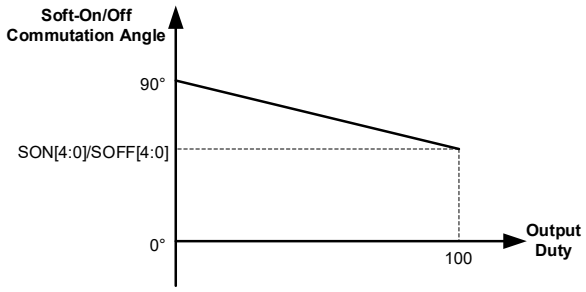


Figure 5: Soft-On/Off Commutation Angle Linear Interpolation

Curve Configuration

The MPQ6653-AEC1 provides curve configuration. The input duty cycle or the output duty cycle speed is configured by the corresponding register setting.

Four different configurable points are available, including the starting duty (D0[6:0]) and 100% input duty cycle. Figure 6 on page 14 shows the curve configuration, where the input duty cycle is set by Dx (where x = 0 for D0[6:0], 1 for D1[7:0], or 2 for D2[7:0]) and is calculated as Dx / 255.

In open-loop speed control, the corresponding output duty is set by Sx (where x = 0 for S0[7:0], 1 for S1[7:0], 2 for S2[7:0]), or 100 for S100[11:4]) and is calculated as Sx / 255.

In closed-loop speed control, S100[11:0] sets the maximum speed when the input duty cycle is 100%, and the other speed is set as S100[11:0] x (Sx / 255) (where x = 0 for S0[7:0], 1 for S1[7:0], or 2 for S2[7:0]).

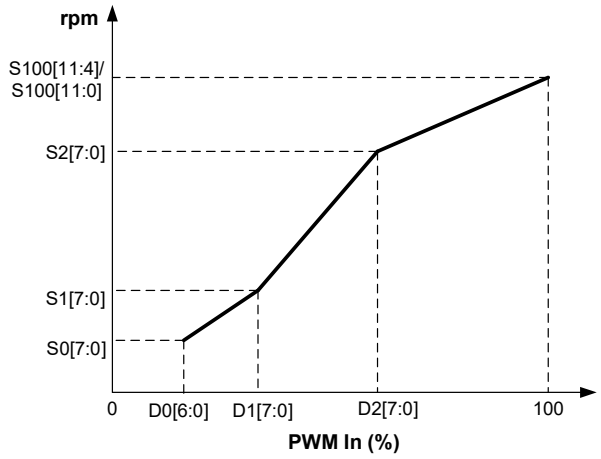


Figure 6: Curve Configuration

Standby Mode

If the voltage on the VCC pin (V_{CC}) exceeds the UVLO rising threshold and the PWM pin remains keeps low, then the IC enters standby mode. The IC exits this mode when the PWM input signal is high or power is cycled on the MPQ6653-AEC1.

Pre Start-Up

Once the input voltage (V_{IN}) exceeds the UVLO threshold or the input PWM duty exceeds the starting duty set by D0[6:0], the MPQ6653-AEC1 first enters pre start-up stage. The output duty increases with a set slope by ignoring the final steady-state output duty cycle. After several Hall cycles, the MPQ6653-AEC1 exits pre start-up and enters soft start (SS).

With different pre start-up timer configurations, the MPQ6653-AEC1 can provide sufficient torque to spin up the motor.

Soft Start (SS)

After pre start-up, SS is employed. The output duty cycle ramps up and down step by step with the TIME_SS[1:0] configuration.

To reduce the input inrush current during start-up, several configurations are available to meet the requirements of different applications. The dropping duty cycle can be configured as 1x or 2x of TIME_SS[1:0].

Rotor Speed Indicator (FG) or Rotor Deadlock Indicator (RD)

The speed indicator or rotor deadlock indicator can be output on the FG/RD pin with different configurations. The FGRD[2:0] bits set the FG/RD pin's output, with the different configurations described below:

- If FGRD[2:0] = 000, the FG/RD pin outputs one pulse every electrical cycle (1x).
- If FGRD[2:0] = 001, the FG/RD pin outputs one pulse every two electrical cycles (1/2x).
- If FGRD[2:0] = 010, the FG/RD pin outputs two pulses every electrical cycle (2x).
- If FGRD[2:0] = 011, the FG/RD pin outputs one pulse every electrical cycle during normal operation and outputs the RD signal in rotor deadlock protection. The RD signal output polarity is set by the RD_H_L bit.
- If FGRD[2:0] = 100, the FG/RD pin is set as the locked-rotor indicator. The RD signal output polarity is set by the RD_H_L bit.
- If FGRD[2:0] = 101, the FG/RD pin is set by the fault indicator to output a signal when a fault is detected.
- If FGRD[2:0] = 110, the FG/RD pin is set as the external Hall signal input. The external Hall sensor replaces the internal Hall sensor in operation.

Protection Circuits

The MPQ6653-AEC1 is fully protected against over-voltage (OV), under-voltage (UV), over-current (OC), and over-temperature (OT) events.

Cycle-by-Cycle Current Limiting (OCP)

During normal switching, if the current flowing through the high-side MOSFET (HS-FET) of the H-bridge exceeds the threshold set by the CL bit after a blanking time, then the HS-FET turns off. The HS-FET resumes switching in the next switching cycle. The OCP threshold is selectable via the OCP_SEL bit at 0.6A or 1.2A.

Peak Current Limit (SCP)

If the current is not limited by the cycle-by-cycle limit (I_{OCP}), there is also a peak current limit (I_{LIMIT_PEAK}). Once I_{LIMIT_PEAK} (typically 1.8A) is reached, all the MOSFETs turn off. The MOSFETs resume operation after a lock retry time.

Thermal Shutdown (TSD)

The MPQ6653-AEC1 provides thermal monitoring. If the temperature exceeds 165°C, the MOSFETs of the switching half-bridge turn off. Once the die temperature drops to a safe level, operation automatically resumes.

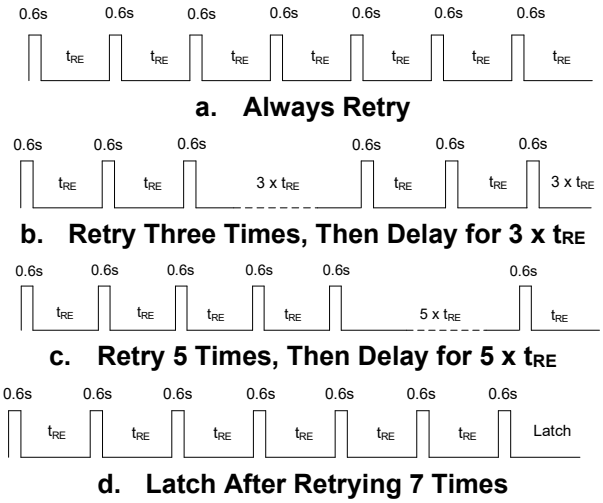
Under-Voltage Lockout (UVLO)

If V_{CC} drops below the UVLO falling threshold, all the circuitry in the device is disabled and the internal logic resets. Operation resumes once V_{CC} exceeds the UVLO rising threshold.

Rotor Deadlock Protection (RD)

The internal Hall signal is detected to determine whether rotor deadlock protection is triggered. If no Hall signal edge is detected during the 0.6s detection time, the rotor deadlock protection is triggered, and both LS-FETs of the H-bridge turn on. After a lock retry time (t_{RE}) set by the LOCK_SEL bit, the IC automatically tries again to start up. The lock retry time is configured as 3.6s or 8.4s.

The MPQ6653-AEC1 also supports retry several times until the lock retry time becomes longer via the LOCK_BHV[1:0] bit (see Figure 7).



a. Always Retry

b. Retry Three Times, Then Delay for 3 x t_{RE}

c. Retry 5 Times, Then Delay for 5 x t_{RE}

d. Latch After Retrying 7 Times

Figure 7: Rotor Deadlock Protection and Retry Time

The FG/RD pin releases only after the locked-rotor condition is released and three Hall signal edges are detected.

Over-Voltage Protection (OVP)

The MPQ6653-AEC1 provides two OVP thresholds for different applications.

If V_{CC} exceeds the OVP threshold (19V or 31V), the OUT1/OUT2 output is disabled. The OUT1/OUT2 output resumes normal operation once V_{CC} drops below the OVP falling threshold (17V or 28V), and the Hall edge is detected in the OVP interval.

Fault Diagnosis

Once the fault is triggered, the corresponding fault bit OCP, SCP, TSD, OVP, or RD is set, and all the fault bits can be read. The fault bit can be reset after the fault bit is read.

Test Mode and Factory Mode

To configure the internal register, the MPQ6653-AEC1 provides a test mode. In this test mode, the internal register can be set to read/write (R/W) operation. After the design is finalized, the register value can be configured to the non-volatile memory (NVM).

REGISTER MAP

Add	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	S0[7:0]							
01h (OTP/REG)	S1[7:0]							
02h (OTP/REG)	S2[7:0]							
03h (OTP/REG)	S100[11:4]							
04h (OTP/REG)	D1[7:0]							
05h (OTP/REG)	D2[7:0]							
06h (OTP/REG)	RD_H_L	D0[6:0]						
07h (OTP/REG)	OVP_H	FAST_DN	PWM_POL	SON[4:0]				
08h (OTP/REG)	SINE	SPD_SEL[1:0]		SOFF[4:0]				
09h (OTP/REG)	WAIT_DIS	T_PRE[1:0]		HAL_FLAG	HAL_ANG[3:0]			
0Ah (OTP/REG)	RESERVED	INT_EN	RESERVED	LOCK_SEL	OCP_SEL	RESERVED	PWM_WAIT	TADV_EN
0Bh (OTP/REG)	OVP_DIS	TADV[1:0]		TIME_SS[1:0]		FGRD[2:0]		
0Ch (OTP/REG)	PWM_DC	CLOSE	LOW_F	LOCK_BHV[1:0]		RESERVED	COA_SLOW	DN_SCAEL
0Dh (OTP/REG)	KI[6:0]							ZCD_POS
0Eh (OTP/REG)	RESERVED	FIX_ST	DSTOP[1:0]		S100[3:0]			
14h (REG)	OCP	SCP	OVP	TSD	RD	RESERVED		
15h (REG)	RESERVED	LOCK_DIS	RESERVED					
16h (REG)	RESERVED	OTP_PAGE[1:0]	RESERVED					

SPEED_CURVE_1 (00h)

The SPEED_CURVE_1 command configures the output duty or speed when the input pulse-width modulation (PWM) duty cycle is at D0[6:0].

Bits	Access	Bit Name	Default	Description
7:0	R/W	S0[7:0]	0x20	Sets the output duty or speed when the input PWM duty is at D0[6:0]. For open-loop control, set the output duty when the input PWM duty is at D0[6:0]. The output duty can be calculated with the following equation: Output Duty = S0[7:0] / 256 For closed-loop control, set the speed reference when the input PWM duty is at D0[6:0]. The speed can be calculated with the following equation: Speed = S0[7:0] / 256 x S100[11:0]

SPEED_CURVE_2 (01h)

The SPEED_CURVE_2 command configures the output duty or speed when the input PWM duty cycle is at D1[7:0].

Bits	Access	Bit Name	Default	Description
7:0	R/W	S1[7:0]	0x60	Sets the output duty or speed when the input PWM duty is at D1[7:0]. For open-loop control, set the output duty when the input PWM duty is at D1[7:0]. The output duty can be calculated with the following equation: Output Duty = S1[7:0] / 256 For closed-loop control, set the speed reference when the input PWM duty is at D1[7:0]. The speed can be calculated with the following equation: Speed = S1[7:0] / 256 x S100[11:0]

SPEED_CURVE_3 (02h)

The SPEED_CURVE_3 command configures the output duty or speed when the input PWM duty cycle is at D2[7:0].

Bits	Access	Bit Name	Default	Description
7:0	R/W	S2[7:0]	0xC0	Sets the output duty or speed when the input PWM duty is at D2[7:0]. For open-loop control, set the output duty when the input PWM duty is at D2[7:0]. The output duty can be calculated with the following equation: Output Duty = S2[7:0] / 256 For closed-loop control, set the speed reference when the input PWM duty is at D2[7:0]. The speed can be calculated with the following equation: Speed = S2[7:0] / 256 x S100[11:0]

SPEED_CURVE_4 (03h)

The SPEED_CURVE_4 command configures the output duty or speed when the input PWM duty cycle is at 100%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	S100[11:4]	0xFF	Sets the output duty or the 8 most significant bits (MSB) for the speed when the input PWM duty is at 100%. For open-loop control, set the output duty when the input PWM duty is at 100%. The output duty can be calculated with the following equation: Output Duty = S100[11:4] / 256 For closed-loop control, set the maximum speed reference when the input PWM duty is at 100%. Combined with S100[3:0], the maximum speed (electrical speed) can be calculated with the following equation: Max Speed = 16rpm / LSB

SPEED_CURVE_5 (04h)

The SPEED_CURVE_5 command configures input duty cycle 1 (D1).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D1[7:0]	0x60	Sets the input duty for curve configuration. The input PWM duty can be calculated with the following equation: Input PWM Duty = D1[7:0] / 256

SPEED_CURVE_6 (05h)

The SPEED_CURVE_6 command configures input duty cycle 2 (D2).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D2[7:0]	0xC0	Sets the input duty for curve configuration. The input PWM duty can be calculated with the following equation: Input PWM Duty = D2[7:0] / 256

RD_D0 (06h)

The RD_D0 command sets the RD/FT output polarity and starting corner duty.

Bits	Access	Bit Name	Default	Description
7	R/W	RD_H_L	0	Selects the RD/FT output polarity. 0: The output is low when the protection is triggered (default) 1: The output is high when the protection is triggered
6:0	R/W	D0[6:0]	0x20	Sets the starting corner duty for curve configuration. The starting corner PWM duty can be calculated with the following equation: Starting Corner PWM Duty = D0[6:0] / 256

CFR_1 COMMAND (07h)

The CFR_1 command is for control function register 1, which sets the over-voltage protection (OVP) threshold, fast off, input PWM polarity, and soft-on commutation angle.

Bits	Access	Bit Name	Default	Description
7	R/W	OVP_H	1	Selects the OVP threshold. 0:19V 1:31V (default)
6	R/W	FAST_DN	0	Enables fast off. 0: Disables fast off (default) 1: Enables fast off when PWM is off. The IC quickly stops switching when the input duty cycle drops below the starting duty
5	R/W	PWM_POL	0	Selects input PWM polarity. 0: Positive duty cycle (default) 1: Negative duty cycle
4:0	R/W	SON[4:0]	0x10	Sets the soft-on commutation angle. 00000: 2.9° 00001: 5.8° …. 11111: 90° The soft on angle can be calculated with the following equation: Soft On Angle = (SON[4:0] + 1) x 2.9° 2.9° per step

SOFF_CLK (08h)

The SOFF_CLK command sets soft on/off mode, the digital clock, and the soft-off commutation angle.

Bits	Access	Bit Name	Default	Description
7	R/W	SINE	0	Selects soft on/off mode. 0: Linear (default) 1: Sine
6:5	R/W	SPD_SEL[1:0]	00	Selects the digital clock. A higher frequency results in a higher calculated resolution; however, it also leads to a higher minimum speed. The bits listed below indicate the supported minimum electrical speeds: 00: 200rpm (default electrical speed) 01: 800rpm 10: 1600rpm 11: 3200rpm
4:0	R/W	SOFF[4:0]	0x10	Sets the soft-off commutation angle. 00000: 2.9° 00001: 5.8° …. 11111: 90° The soft off angle can be calculated with the following equation: Soft off angle = (SOFF[4:0] + 1) x 2.9° 2.9° per step

CFR_2 (09h)

The CFR_2 command is for control function register 2, which sets the waiting function, pre start-up timer, and Hall offset angle.

Bits	Access	Bit Name	Default	Description
7	R/W	WAIT_DIS	0	Disables the waiting function at start-up. 0: Enabled (default) 1: Disabled
6:5	R/W	T_PRE[1:0]	01	Selects the pre start-up timer. 00: 21.33ms/step 01: 10.67ms/step (default) 10: 5.36ms/step 11: 2.73ms/step
4	R/W	HAL_FLAG	0	Selects the Hall offset angle lag/lead. 0: Lag (default) 1: Lead
3:0	R/W	HAL_ANG[3:0]	0000	Sets the Hall offset angle. 0000: 0° (default) 0001: 1.4° … 1111: 21° The Hall offset angle can be calculated with the following equation: Hall Offset Angle = HAL_ANG[3:0] x 1.4° 1.4° per step.

CFR_3 (0Ah)

The CFR_3 command is for control function register 3, which sets the soft on/off angle, lock retry time, current limit, waiting function, and the advanced turn-off function.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6	R/W	INT_EN	0	Enables soft on/off commutation angle linear interpolation. 0: Disables the soft on/off commutation angle, which linearly increases to 90° when the duty drops (default) 1: Enables the soft on/off commutation angle, which linearly increases to 90° when the duty drops
5	R	RESERVED	1	Reserved.
4	R/W	LOCK_SEL	0	Selects the deadlock protection retry time. 0: 3.6s (default) 1: 8.4s
3	R/W	OCP_SEL	1	Selects the current limit threshold. 0: 0.6A 1: 1.2A (default)
2	R	RESERVED	0	Reserved.

1	R/W	PWM_WAIT	0	Enables the waiting function at PWM on start-up. 0: Disabled (default) 1: Enabled
0	R/W	TADV_EN	1	Enables advanced turn-off. 0: Disables advanced turn-off 1: Enables advanced turn-off (default)

CFR_4 (0Bh)

The CFR_4 command is for control function register 4, which sets the OVP function, advanced soft off angle, soft-start time (t_{SS}), and the FG/RD pin.

Bits	Access	Bit Name	Default	Description
7	R/W	OVP_DIS	0	Disables OVP. 0: Enables OVP (default) 1: Disables OVP
6:5	R/W	TADV[1:0]	00	Selects the advanced soft off angle. 00: Automatic (default) 01: 5.6° 10: 11.2° 11: 22.5°
4:3	R/W	TIME_SS[1:0]	01	Selects t_{SS}, the time during which the output duty transitions from 0% to 100%. 00: 2.73s 01: 5.46s (default) 10: 8.19s 11: 10.92s
2:0	R/W	FGRD[2:0]	000	Selects the FG/RD pin. 000: 1 x FG (default) 001: 0.5 x FG 010: 2 x FG 011: FG + RD, where the FG signal is output during normal operation, and the RD signal is output if deadlock protection is detected 100: RD, where the RD signal polarity is set by the RD_H_L register 101: FT, where the fault signal is output if a fault is detected. The FT polarity is set by the RD_H_L register 110: HALL_IN, where the FG/RD pin is set as the external Hall input pin

CFR_5(0Ch)

The CFR_5 command is for control function register 7, which sets the PWM/DC input, open-/closed-loop speed control, PWM frequency, deadlock protection mode, coasting down threshold, and output duty ramping down scale.

Bits	Access	Bit Name	Default	Description
7	R/W	PWM_DC	0	Selects the DC input or PWM input for the PWM/DC pin. 0: PWM input (default) 1: DC input
6	R/W	CLOSE	0	Enables closed-loop speed control. 0: Open-loop speed control (default) 1: Closed-loop speed control

5	R/W	LOW_F	0	Selects the low-frequency PWM input. 0: The high frequency is selected between 1kHz and 100kHz (default) 1: The low frequency is selected between 50Hz and 2kHz
4:3	R/W	LOCK_BHV[1:0]	00	Selects deadlock protection mode. 00: Always retries (default) 01: Retries for three times, then lock retry time is 3x 10: Retries for 5 times, then lock retry time is 5x 11: Retries for 7 times, then latches up
2	R	RESERVED	1	Reserved.
1	R/W	COA_SLOW	0	Selects the coasting down speed threshold (electrical speed). The IC remains coasting until the fan rotation's coasting down speed drops below the speed threshold during start-up. 0: 1400rpm (default) 1: 700rpm
0	R/W	DN_SCALE	0	Selects the PWM output duty ramping down scale as the output duty cycle drops from 100% to 0%. 0: 1 x TIME_SS[1:0] (default) 1: 2 x TIME_SS[1:0]

KI_ZCD COMMAND (0Dh)

The KI_ZCD command sets the integral parameter for closed-loop control and the zero-current detection (ZCD) active angle position.

Bits	Access	Bit Name	Default	Description
7:1	R/W	KI[6:0]	0x10	Sets the integral parameter for closed-loop speed control.
0	R/W	ZCD_POS	0	Selects the ZCD active angle position. 0: ZCD is active once soft-on commutation ends (default) 1: ZCD is active after 90°

FIX_DSTOP_S100 (0Eh)

The FIX_DSTOP_S100 command sets the initial output duty, stop input duty, and maximum speed reference.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6	R/W	FIX_ST	0	Selects the initial output duty at start-up. 0: The initial output duty is 0% (default) 1: The initial output duty is 12.5%
5:4	R/W	DSTOP[1:0]	00	Selects the stop input duty. The IC stops switching when the input PWM duty is equal to or exceeds the selected stop input duty. 00: Does not stop (default) 01: 100% 10: 95% 11: 90%

3:0	R/W	S100[3:0]	0000	Sets the maximum speed reference when the input PWM duty is at 100% for closed-loop control. Combined with S100[11:4], the maximum speed (electrical speed) can be calculated with the following equation: Max Speed = 16rpm / LSB

FAULT_BIT (14h)

The FAULT_BIT command indicates faults including the cycle-by-cycle current limit (I_{OCP}), peak current limit (I_{LIMIT_PEAK}), input over-voltage (OV) conditions, thermal shutdown, and rotor deadlock.

Bits	Access	Bit Name	Default	Description
7	R	OCP	0	Indicates an I_{OCP} fault. 0: I_{OCP} is not triggered 1: I_{OCP} is triggered
6	R	SCP	0	Indicates a I_{LIMIT_PEAK} fault. 0: I_{LIMIT_PEAK} is not triggered 1: I_{LIMIT_PEAK} is triggered
5	R	OVP	0	Indicates an input OV fault. 0: Input OVP is not triggered 1: Input OVP is triggered
4	R	TSD	0	Indicates a thermal shutdown fault. 0: Thermal shutdown protection is not triggered 1: Thermal shutdown protection is triggered
3	R	RD	0	Indicates a rotor deadlock fault. 0: Rotor deadlock protection is not triggered 1: Rotor deadlock protection is triggered
2:0	R	RESERVED	000	Reserved.

LOCK_DIS (15h)

The LOCK_DIS command disables the rotor deadlock protection.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6	R/W	LOCK_DIS	0	Disables rotor deadlock protection. 0: Rotor deadlock protection is enabled 1: Rotor dead lock protection is disabled
5:0	R	RESERVED	0x00	Reserved.

OTP_PAGE (16h)

The OTP_PAGE command is the one-time programmable (OTP) memory page indicator.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6:5	R	OTP_PAGE[1:0]	00	Sets the OTP page indicator (read-only). 00: No OTP page is configured 01: The first OTP page is configured 10: The second OTP page is configured
4:0	R	RESERVED	0x00	Reserved.

APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible to maintain a stable V_{IN} and reduce noise at the input. C_{IN} must have a low impedance at the switching frequency (f_{SW}).

Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics. The ceramic capacitance is dependent on the DC voltage rating. If the ceramic capacitor is biased to its DC voltage rating, then its capacitance drops below 50%.

Leave sufficient voltage rating margin when selecting the component. For most applications, a 1µF to 10µF ceramic capacitor is sufficient.

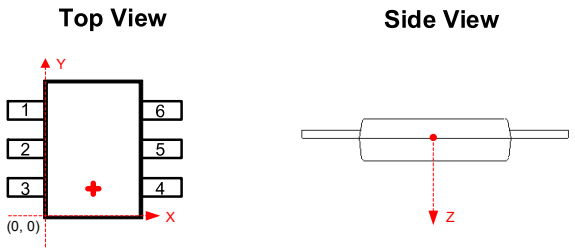
In some applications, an additional large, electrolytic capacitor may be required to absorb the motor's energy.

Selecting the Input Snubber

Due to the input capacitor's charge/discharge energy during phase commutation, I_{IN} has switching cycle ringing. If necessary, place an RC snubber (a 2Ω resistor in series with a 1µF capacitor) in parallel with C_{IN}. This effectively prevents switching cycle ringing.

Hall Sensor Position

Figure 8 shows the embedded Hall sensor location.



TSOT (X, Y, Z) = (800µm, 481µm, 80µm)

Figure 8: Hall Sensor Position

Selecting the Input-Clamping Circuit

A voltage-clamping circuit may be required to prevent V_{IN} from being charged by the energy stored in the motor. Typically, a 15V Zener diode or transient voltage suppressor (TVS) diode in a SOD-123 package is sufficient for most 12V applications. A higher clamping voltage is used if a higher V_{IN} range is applied.

Selecting the Reverse-Blocking Diode

If the fan experiences a reverse plug-in, or a reverse voltage is applied on the input terminal, then a reverse-blocking diode is required to avoid damage. The reverse-blocking diode prevents the bus voltage from charging via the fan's reverse current.

The blocking diode's reverse voltage rating must exceed the maximum operating voltage under all conditions.

System-Level ESD Testing

Some fan products must pass system-level ESD testing. System-level ESD follows the IEC 61000-4-2 standard. There are differences between human body model (HBM) ESD and system-level ESD (IEC 61000-4-2). Figure 9 shows the equivalent circuit of a HBM ESD circuit.

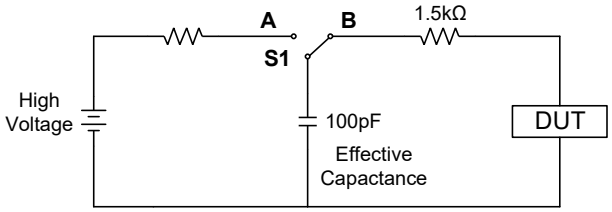


Figure 9: Equivalent Circuit of HBM ESD Circuit

Figure 10 shows the equivalent circuit of a system-level ESD circuit.

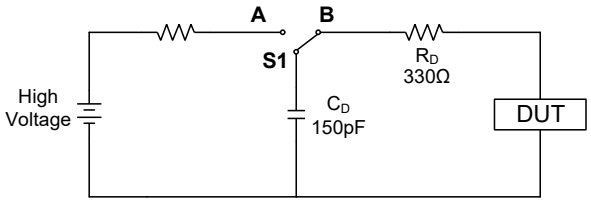


Figure 10: Equivalent Circuit of System-Level ESD

Compared to HBM ESD, the discharge capacitance exceeds the human body's effective capacitance, and the discharge resistance of IEC-level ESD is much smaller. As a result, the system-level ESD's discharging energy is much higher than HBM ESD.

There are two different modes for IEC 61000-4-2 ESD testing: air discharge and contact discharge. Contact discharge is the first choice for testing.

If a high-level ESD is required, then an external circuit may be required to enhance ESD capability.

Figure 11 shows an external ESD-enhanced circuit using a Zener or ESD diode.

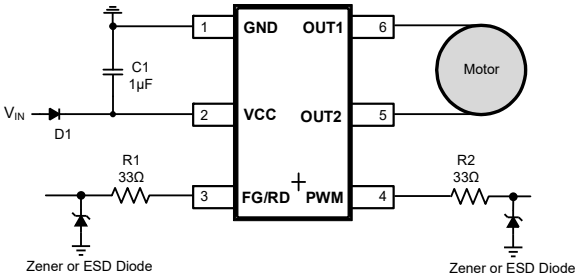


Figure 11: Enhanced ESD Using a Zener or ESD Diode

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 12 and follow the guidelines below:

1. To improve EMI performance, a capacitor (C2) with a 0402 package size is required.
2. Place C2 as close to the VCC and GND pins as possible.
3. Place the input capacitor (C1) close to the VCC and GND pins.

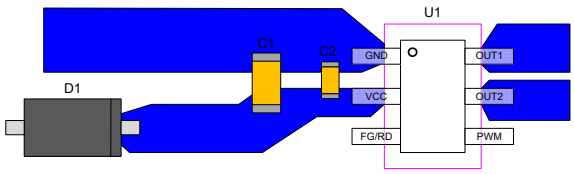


Figure 12: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

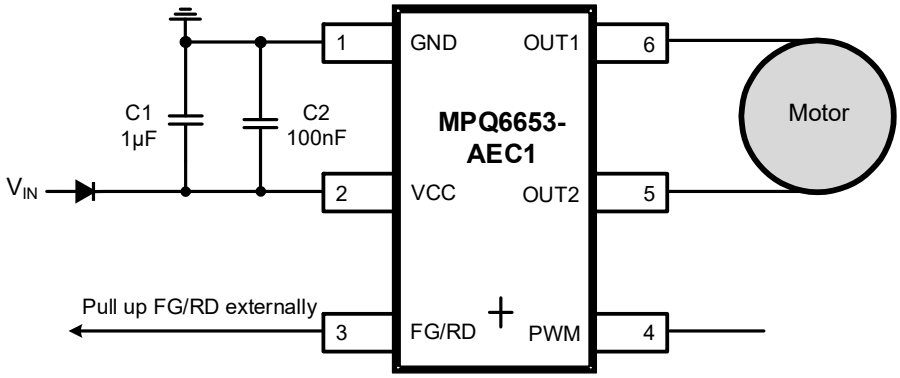


Figure 13: Typical Application Circuit

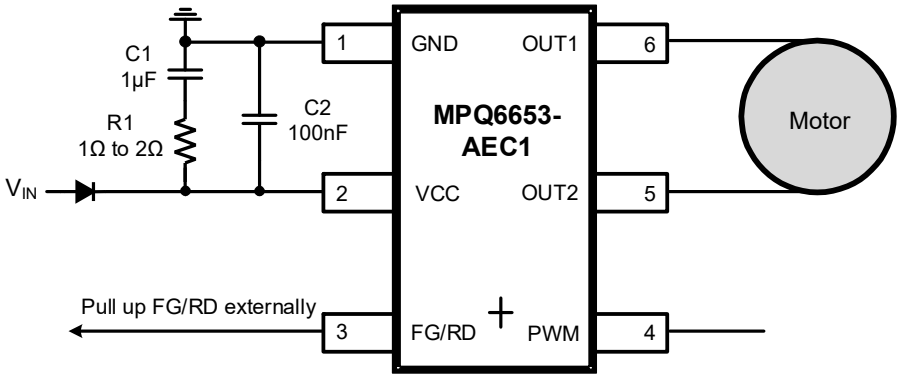


Figure 14: Typical Application Circuit (with RC Snubber)

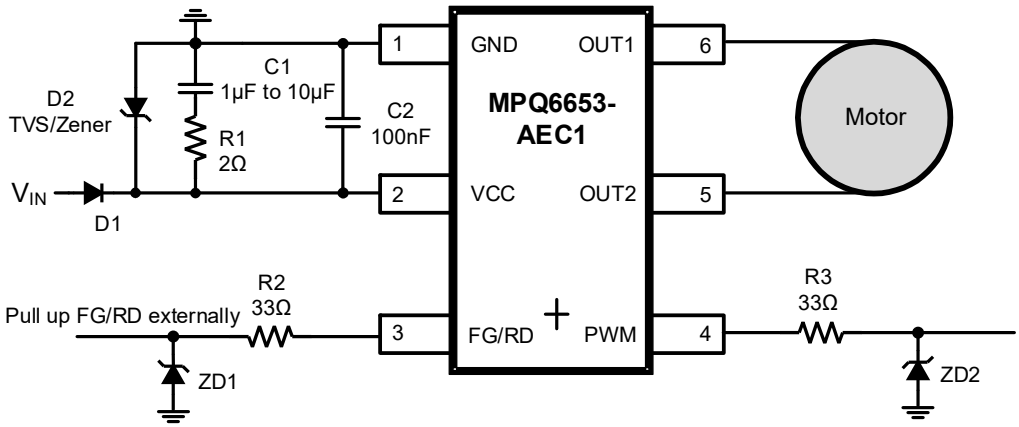
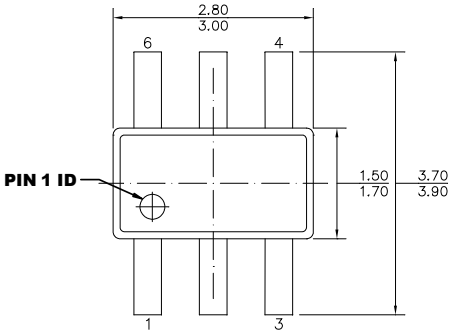


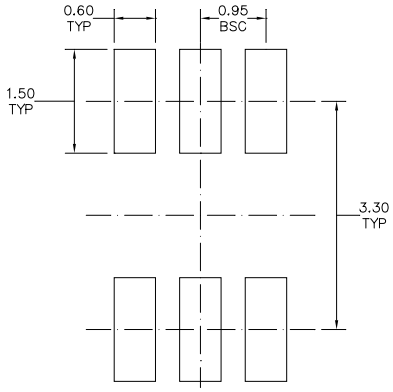
Figure 15: Typical Application Circuit (with Voltage Clamping and Enhanced ESD)

PACKAGE INFORMATION

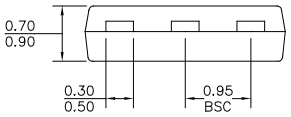
TSOT23-6-SL



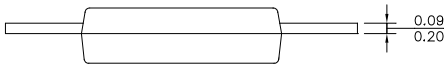
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



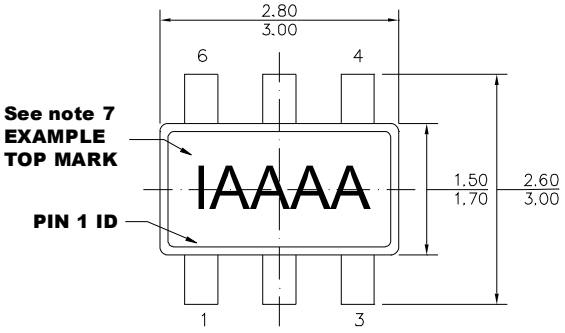
SIDE VIEW

NOTE:

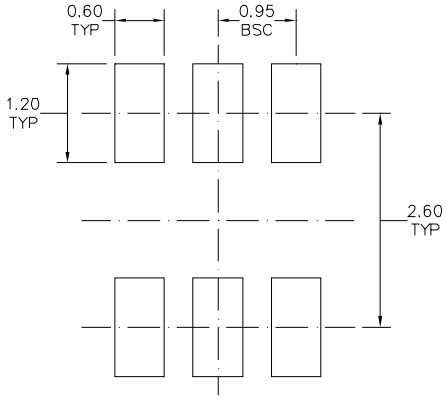
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE IS JEDEC MO-193.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

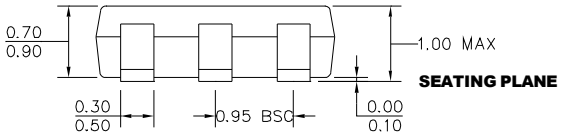
TSOT23-6



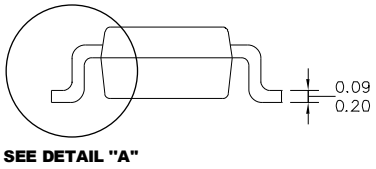
TOP VIEW



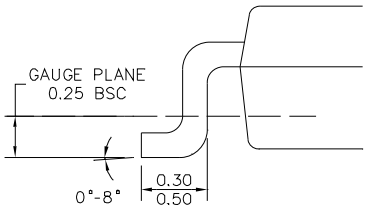
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

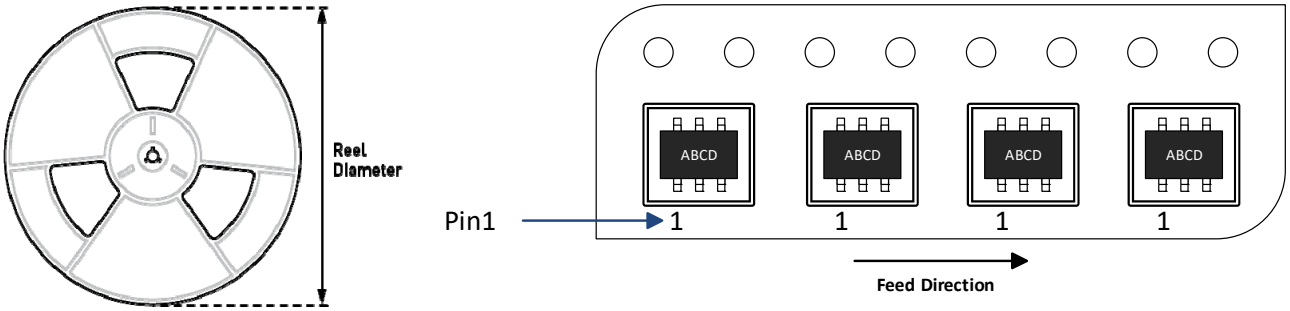


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6653GJS-xxxx-AEC1-Z	TSOT23-6-SL	5000	N/A	N/A	13in	12mm	8mm
MPQ6653GJ-xxxx-AEC1-Z	TSOT23-6	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/7/2024	Initial Release	-