MPQ7795

2.2MHz, Low-EMI, 24.5W, Mono BTL Class-D Audio Amplifier with Diagnostics, AEC-Q100 Qualified

DESCRIPTION

The MPQ7795 is an automotive-grade, low-EMI, differential analog input Class-D audio amplifier with I²C diagnostics. The device is a fully integrated audio amplifier that can drive a mono speaker in a bridge-tied load (BTL) configuration, and it significantly reduces the solution size.

The MPQ7795 utilizes a BTL structure capable of delivering 24.5W into 4Ω speakers with a 14.4V power supply (PV_{DD}). MPS's Class-D audio amplifiers exhibit the high fidelity of Class-AB amplifiers, as well as high efficiency.

The switching frequency (f_{SW}) can be set to 330kHz, 384kHz, 470kHz, or 2.2MHz. The MPQ7795's efficiency exceeds 90% during both 470kHz and 2.2MHz operation.

The MPQ7795 integrates a load diagnostic function that detects open load, short load, load-to-GND short, and load-to-PVDD short conditions. The diagnostics work when the device is enabled, which protects the load and the device.

In addition to over-current protection (OCP), under-voltage protection (UVP), and over-temperature protection (OTP), the MPQ7795 features an adjustable power limit (P_{LIMIT}) function. The P_{LIMIT} circuit sets a limit on the output's peak-to-peak voltage (V_{PK-PK}). This is accomplished by limiting the duty cycle to a fixed maximum value. This limit can be considered a virtual voltage rail, and it is below the supply connected to PVDD.

The device statuses can be reported to the microcontroller (MCU) via the I²C interface. The parameters can also be set via the I²C interface.

The MPQ7795 is available in a QFN-24 (4mmx4mm) package, and is AEC-Q100 qualified.

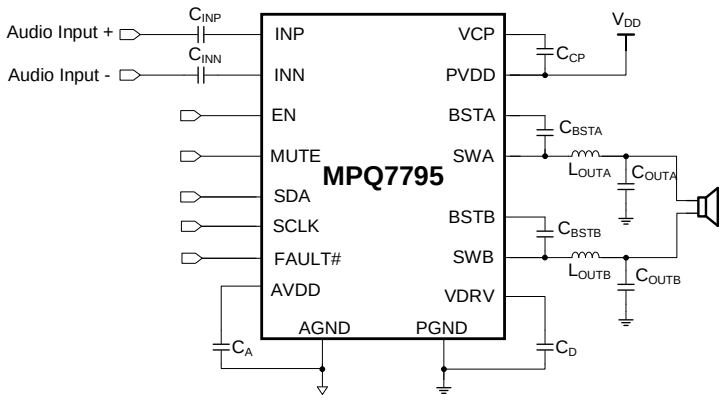
FEATURES

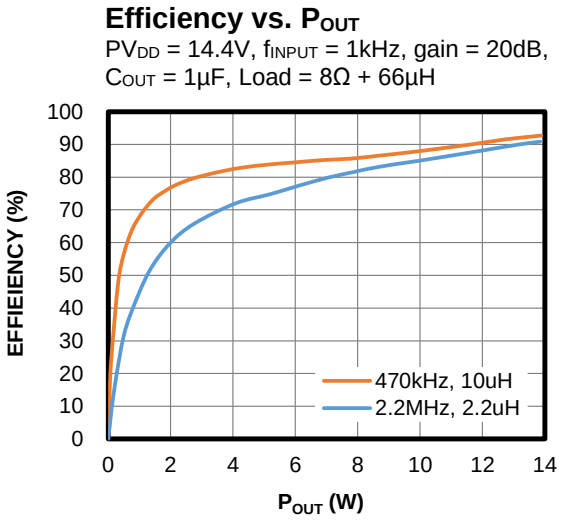
- Built to Handle Automotive Transients:
  - Load Dump Up to 42V
  - Cold Crank Down to 4.5V
- Cooler Thermals:
  - Deliver 24.5W into 4Ω Loads with 14.4V PV_{DD}
  - High Power Efficiency
    - Up to 92.6% for 8Ω Load
    - Up to 90.4% for 4Ω Load
  - Less than 20°C Junction Temperature (T_J) Rise at 8Ω, 14W/470kHz
  - Low-Ohmic BCD FET Technology
- Low EMI/EMC Noise:
  - Meet CISPR 25 Class 5
  - MeshConnect™ Flip-Chip Packaging
  - Operates Outside of AM Radio Band
- Extends Vehicle Battery Life:
  - 0.02μA Standby Current (I_{QSTBY})
  - 16mA Quiescent Current (I_Q)
- Additional Features:
  - Load Diagnostics:
    - Open Load or Short Load
    - Output Short to PVDD or Ground
  - Status Report with I²C and Fault Pin
  - Start-Up/Shutdown Pop Elimination
  - 150mΩ Power MOSFETs
  - 80dB PSRR at 100Hz
  - Selectable Voltage Gain
  - Adjustable Power Limiter
  - Communicates with MCU via I²C Interface
  - Supports 2Ω to 16Ω Speakers
  - Available in a QFN-24 (4mmx4mm) Package
  - Available in a Wettable Flank Package
  - Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive E-Call Systems
- Telematics Systems
- Infotainment Audio
- Cluster Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ7795GRE-AEC1***	QFN-24 (4mmx4mm)	*See Below*	1

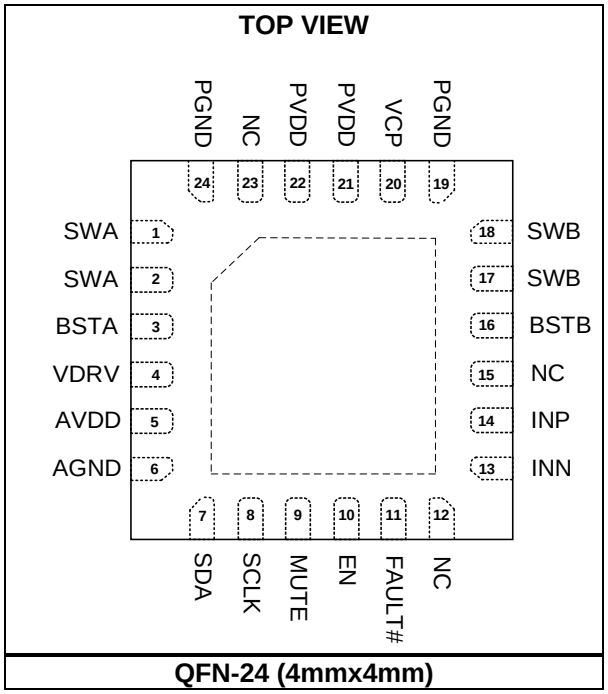
* For Tape & Reel, add suffix -Z (e.g. MPQ7795GRE-AEC1-Z).
** Moisture Sensitivity Level Rating
*** Wettable Flank

TOP MARKING (MPQ7795GRE-AEC1)

MPSYWW
MP7795
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP7795: Part number
LLLLLL: Lot number
E: Wettable Flank

PACKAGE REFERENCE



QFN-24 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 2	SWA	**Switched power output for amplifier A (the positive output).**
3	BSTA	**High-side MOSFET bootstrap input for amplifier A.** A capacitor connected from BSTA to SWA supplies the gate drive current to the internal high-side MOSFET (HS-FET).
4	VDRV	**Gate drive supply bypass.** The VDRV pin powers the internal circuitry, internal MOSFET gate drive, and the power limit (P_{LIMIT}) function. Bypass VDRV to AGND with a 4.7μF to 10μF capacitor.
5	AVDD	**Internal analog reference.** Connect a bypass capacitor from the AVDD pin to AGND.
6	AGND	**Analog ground.**
7	SDA	**I^2C data pin.**
8	SCLK	**I^2C clock pin.**
9	MUTE	**Mute control.** Drive the MUTE pin above 0.95V to disable output switching; drive MUTE below 0.8V to allow for switching.
10	EN	**Enable input.** Drive EN above 1.2V to turn on the amplifiers; drive EN below 1V to turn them off.
11	FAULT#	**Fault output.** The FAULT# pin has a low output to indicate whether the IC has detected a fault. This output is an open drain.
12, 15, 23	NC	**No connection.** Tie the NC pin to ground or leave it floating.
13	INN	**Negative audio input.** The INN pin is biased at 2V.
14	INP	**Positive audio input.** The INP pin is biased at 2V.
16	BSTB	**High-side MOSFET bootstrap input for amplifier B.** A capacitor connected from BSTB to SWB supplies the gate drive current to the internal HS-FET.
17, 18	SWB	**Switched power output for amplifier B (the negative output).**
19, 24	PGND	**Power ground for amplifier.**
20	VCP	**Charge pump output for boost capacitor.** Connect a capacitor from VCP to PVDD.
21, 22	PVDD	**Power supply input.** Bypass the PVDD pin to PGND with a 1μF, X7R capacitor (in addition to the main bulk capacitor), placed close to the PVDD and PGND pins.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (PV_{DD}).....-0.3V to +42V
V_{SWA}, V_{SWB}.....-1V to PV_{DD} + 1V
V_{EN} .....-0.3V to PV_{DD} + 0.3V
V_{VDRV} .....-0.3V to +5.5V
AVDD.....-0.3V to +5.5V
BS voltage (V_{BSTA}).....V_{SWA} - 0.3V to V_{SWA} +5.5V
BS voltage (V_{BSTB}).....V_{SWB} - 0.3V to V_{SWB} + 5.5V
V_{VCP}..... -0.3V to PV_{DD} + 5.5V
V_{VCP} to V_{BSTX} .....-0.3V to +40V
V_{BSTX} to V_{VDRV}.....-0.3V to +40V
AGND to PGND……-0.3V to +0.3V
All other pins .....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2) (6)
QFN-24 (4mmx4mm) …….....5.2W
Junction temperature……150°C
Lead temperature……..260°C
Storage temperature……...-65°C to +150°C

ESD Ratings

Human body model (HBM) ..... Class 2 (3)
Charged device model (CDM) ..... Class C2b (4)

Recommended Operating Conditions

Supply voltage (PV_{DD}).....4.5V to 36V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-24 (4mmx4mm)			
JESD51-7	42	9	°C/W (5)
EVQ7795-R-00A	24	6	°C/W (6)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002
4) Per AEC-Q100-011
5) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
6) Measured on MPS MPQ7795 standard EVB, 7.62cmx6.35cm, 2oz. thick copper, 4-layer PCB. The value of θ_{JC} shows the thermal resistance from junction-to-case top.

ELECTRICAL CHARACTERISTICS

PV_{DD} = 14.4V, V_{EN} = 5V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Operating Voltage and Current						
Standby current	I_{QSTBY}	V_{EN} = 0V, INN = INP = float		0.02	3	μA
Quiescent current (7)	I_Q	V_{EN} = 5V, V_{MUTE} = 0V, INN = INP = float, no load, with LC filter		16		mA
Output offset voltage	V_{OS}	Zero input, gain = 36dB, T_J = 25°C	-20	2	+20	mV
		Zero input, gain = 36dB, T_J = -40°C to +150°C	-50	2	+50	mV
MOSFETS						
SW on resistance	$R_{DS(ON)}$	I_{OUT} = 500mA, T_J = 25°C		150	180	mΩ
		I_{OUT} = 500mA, T_J = -40°C to +150°C		150	280	
Over-current limit	I_{LIM}	Sourcing and sinking	4	5		A
Operating Parameters						
Switching frequency	f_{SW}	F1 = 0, F0 = 0	290	330	370	kHz
		F1 = 0, F0 = 1	338	384	430	kHz
		F1 = 1, F0 = 0	413	470	527	kHz
		F1 = 1, F0 = 1	1825	2200	2375	kHz
Gain of input signal	G	G1 = 0, G0 = 0, T_J = 25°C	19	20	21	dB
		G1 = 0, G0 = 1, T_J = 25°C	25	26	27	
		G1 = 1, G0 = 0, T_J = 25°C	31	32	33	
		G1 = 1, G0 = 1, T_J = 25°C	35	36	37	
Input bias voltage	V_{BIAS}	V_{EN} = 5V		2.0		V
EN threshold voltage	V_{EN_R}	V_{EN} rising		1.2	1.5	V
	V_{EN_F}	V_{EN} falling	0.8	1.0		V
EN threshold hysteresis	V_{EN_HYS}			0.2		V
EN enable input current	I_{EN}	V_{EN} = 5V		2.2		μA
PV_{DD} under-voltage lockout (UVLO) rising threshold	V_{UVP_R}		3.6	4	4.4	V
PV_{DD} UVLO falling threshold	V_{UVP_F}		3.3	3.7	4.1	V
PV_{DD} UVLO threshold hysteresis	V_{UVP_HYS}			0.3		V
MUTE threshold voltage	V_{MUTE_R}	V_{MUTE} rising	0.7	0.95	1.2	V
	V_{MUTE_F}	V_{MUTE} falling	0.6	0.8	1	V
Time						
Turn-on time	t_{ON}			430		ms
Protection						
Thermal shutdown trigger (7)	T_{OTP_R}	T_J rising		170		°C
Thermal shutdown hysteresis (7)	T_{OTP_HYS}			20		°C
FAULT# low voltage	V_{FT}	I_{SINK} = 2mA		14		mV

Note:

7) Derived from the bench characterization. Not tested in production.

ELECTRICAL CHARACTERISTICS *(continued)*

PV_{DD} = 14.4V, V_{EN} = 5V, T_J= -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Load Diagnostics						
Short to PVDD resistance	R_{STB}			220		Ω
Short to ground resistance	R_{STG}			250		Ω
Open load detection threshold	R_{OPEN}			95		Ω
Short load detection threshold	R_{SHORT}			1.5		Ω
I^2C Parameters						
SCL/SDA input logic low	V_{IL}		0		0.4	V
SCL/SDA input logic high	V_{IH}		2.1			V
SCL/SDA output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data set-up time	t_{SU_DAT}		100			ns
Data hold time	t_{HD_DAT}		0		0.9	µs
Set-up time for repeated start	t_{SU_STA}		0.6			µs
Hold time for start	t_{HD_STA}		0.6			µs
Bus free time between a start and a stop command	t_{BUF}		1.3			µs
Set-up time for stop command	t_{SU_STO}		0.6			µs
Rising time of SCL/SDA	t_R				120	ns
Falling time of SCL/SDA	t_F				120	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

OPERATING CHARACTERISTICS (8)

PV_{DD} = 14.4V, V_{EN} = 5V, T_J = -40 to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition		Min	Typ	Max	Units
THD + noise (P_{OUT} = 1W, f_{INPUT} (9) = 1kHz)	THD + N	f_{SW} = 470kHz, load = 8Ω			0.09		%
		f_{SW} = 470kHz, load = 4Ω			0.27		%
		f_{SW} = 2.2MHz, load = 8Ω			0.2		%
		f_{SW} = 2.2MHz, load = 4Ω			0.38		%
Output power (f_{INPUT} (9) = 1kHz, THD + N = 10%)	P_{OUT}	f_{SW} = 470kHz, load = 8Ω			13.6		W
		f_{SW} = 470kHz, load = 4Ω			24.4		W
		f_{SW} = 2.2MHz, load = 8Ω			13.7		W
		f_{SW} = 2.2MHz, load = 4Ω			24.5		W
Efficiency (THD + N = 10%)	η	f_{SW} = 470kHz, load = 8Ω			92.6		%
		f_{SW} = 470kHz, load = 4Ω			90.4		%
		f_{SW} = 2.2MHz, load = 8Ω			90.8		%
		f_{SW} = 2.2MHz, load = 4Ω			86.8		%
Frequency response		Gain = 20dB, A-weighted, 20Hz to 22kHz				2	dB
Noise floor (f_{SW} = 470kHz, load = 8Ω)	V_N	A-weighted, 20Hz to 22kHz			115		μV_{RMS}
Signal-to-noise ratio (f_{SW} = 470kHz, load = 8Ω)	SNR	f_{INPUT} (9) = 1kHz, THD + N = 1%, A-weighted, T_J = 25°C			102		dB
Power supply rejection	PSRR	V_{RIPPLE} = 1V_{PP}, inputs AC-coupled to AGND, T_J = 25°C	100Hz		80		dB
			1kHz		66		dB

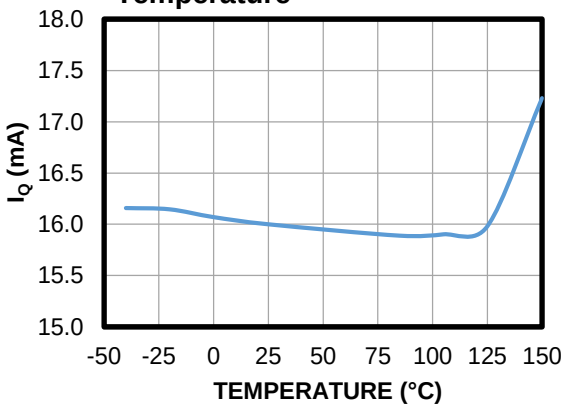
Note:

8) Operating specifications are for the typical application circuit (see Figure 12 on page 39). Not production tested.
9) f_{INPUT} is an external parameter referring to the input signal frequency. The 470kHz performance is based on Figure 12 on page 39. The 2.2MHz performance is based on Figure 13 on page 40.

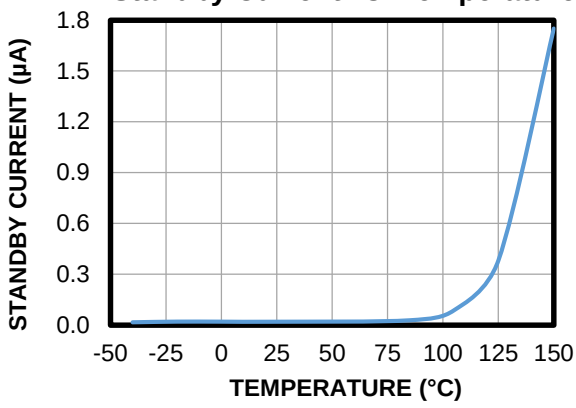
TYPICAL CHARACTERISTICS

PV_{DD} = 14.4V, T_J = 25°C, unless otherwise noted.

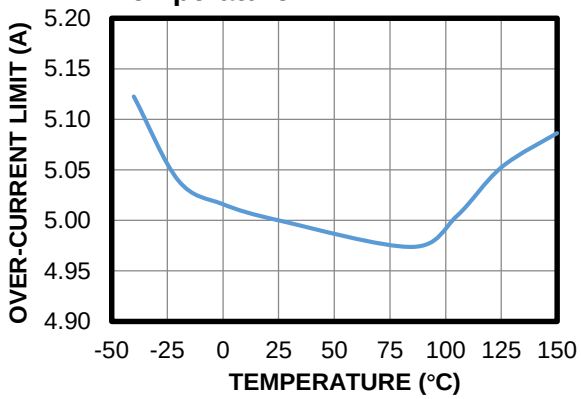
Quiescent Current vs. Temperature



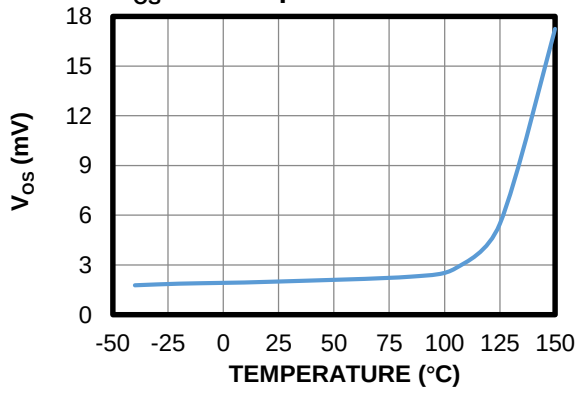
Standby Current vs. Temperature



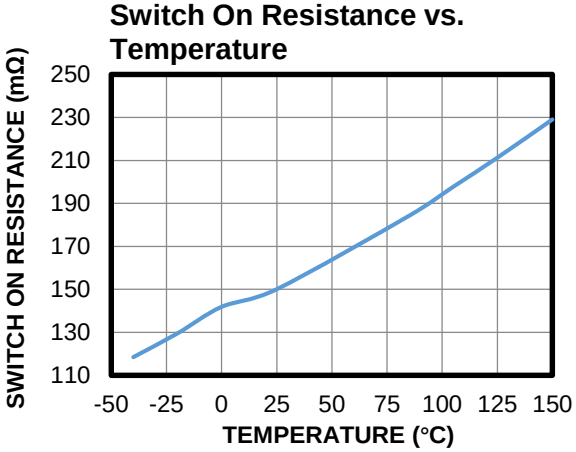
Over-Current Limit vs. Temperature



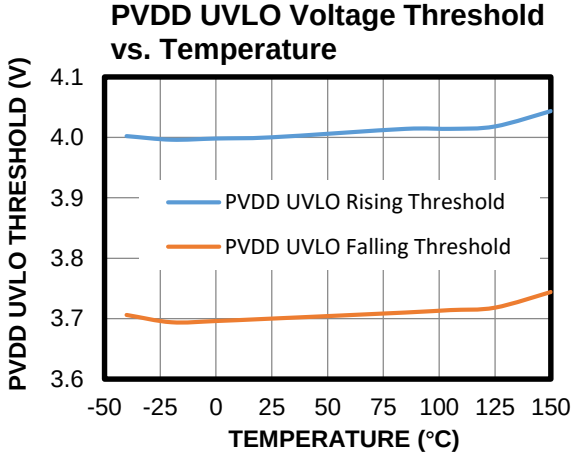
V_{OS} vs. Temperature



Switch On Resistance vs. Temperature



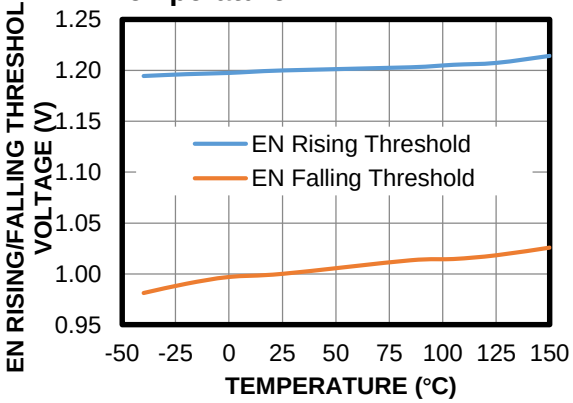
PVDD UVLO Voltage Threshold vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

PV_{DD} = 14.4V, T_J = 25°C, unless otherwise noted.

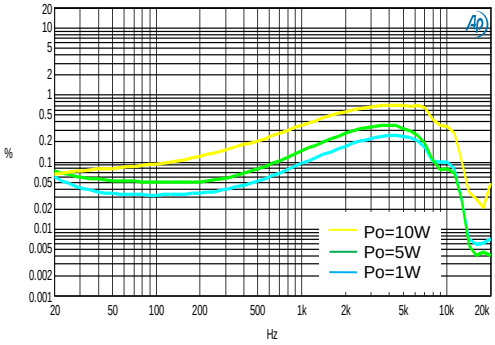
EN Rising/Falling Threshold vs. Temperature



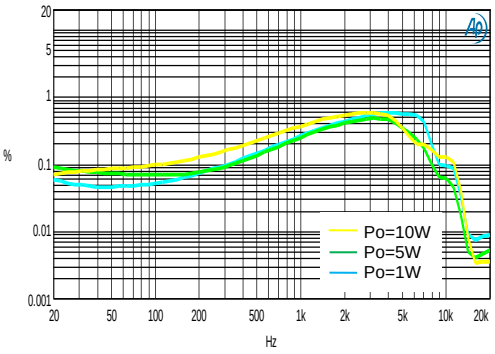
TYPICAL PERFORMANCE CHARACTERISTICS

PV_{DD}= 14.4V, f_{SW} = 470kHz, L_{OUT} = 10µH, C_{OUT} = 1µF, f_{INPUT} = 1kHz, Gain = 20dB, T_A = 25°C, unless otherwise noted.

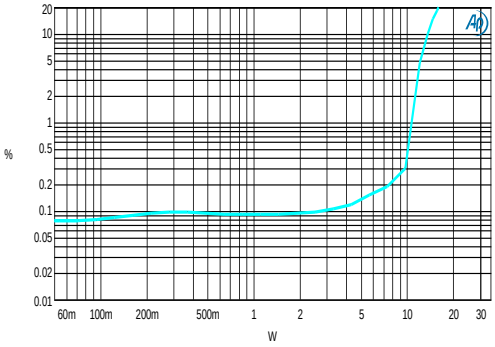
THD + N vs. Frequency
8Ω + 66µH



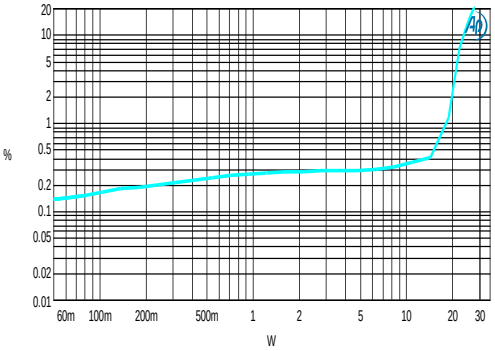
THD + N vs. Frequency
4Ω + 33µH



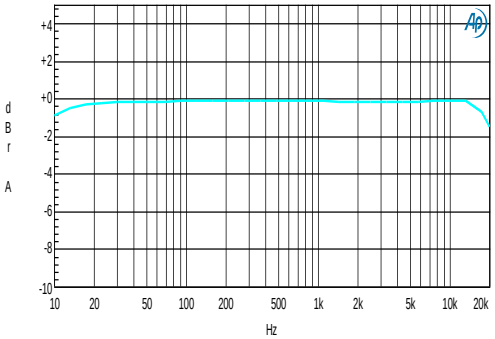
THD + N vs. P_{OUT}
8Ω + 66µH



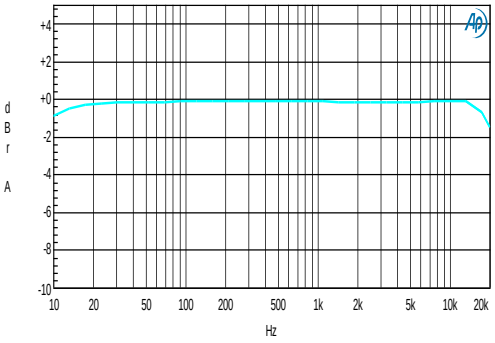
THD + N vs. P_{OUT}
4Ω + 33µH



Frequency Response
1W, 8Ω + 66µH



Frequency Response
1W, 4Ω + 33µH

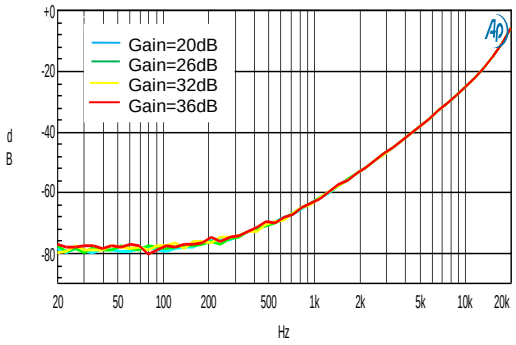


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD}= 14.4V, f_{SW} = 470kHz, L_{OUT} = 10µH, C_{OUT} = 1µF, f_{INPUT} = 1kHz, gain = 20dB, T_A = 25°C, unless otherwise noted.

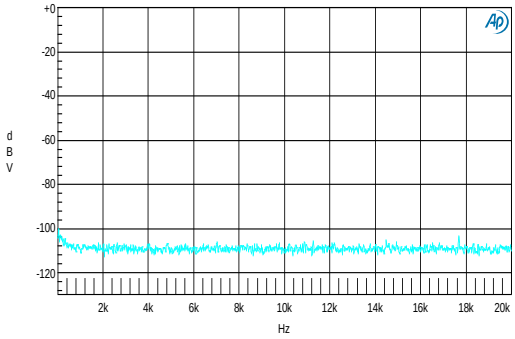
PSRR

V_{AC} ripple = $1V_{PP}$



FFT Noise Floor Test

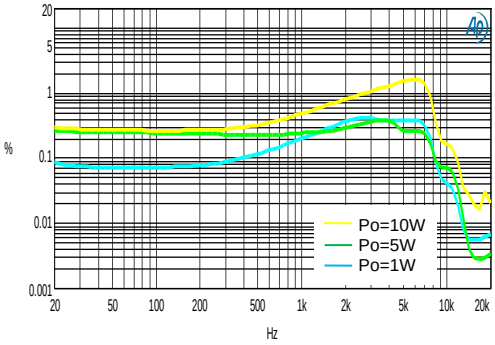
8Ω + 66µH



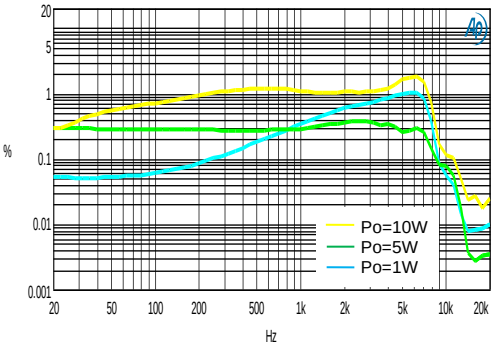
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD}= 14.4V, f_{SW} = 2.2MHz, L_{OUT} = 4.7µH, C_{OUT} = 1µF, f_{INPUT} = 1kHz, gain = 20dB, T_A = 25°C, unless otherwise noted.

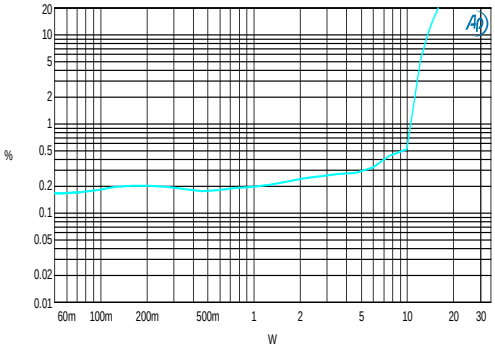
THD + N vs. Frequency
8Ω + 66µH



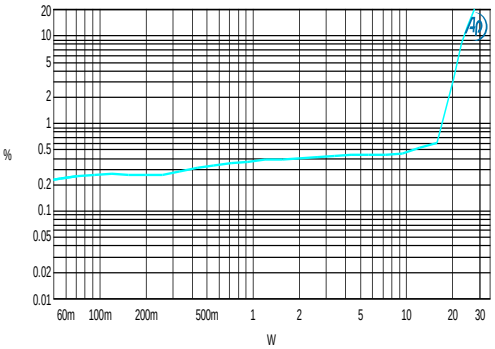
THD + N vs. Frequency
4Ω + 33µH



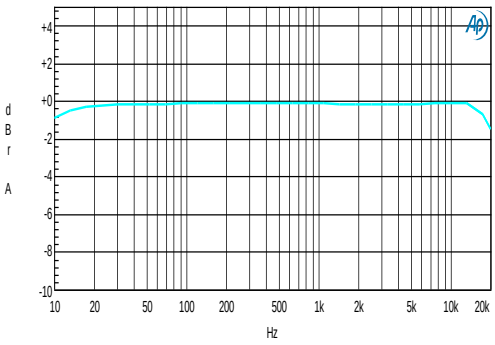
THD + N vs. P_{OUT}
8Ω + 66µH



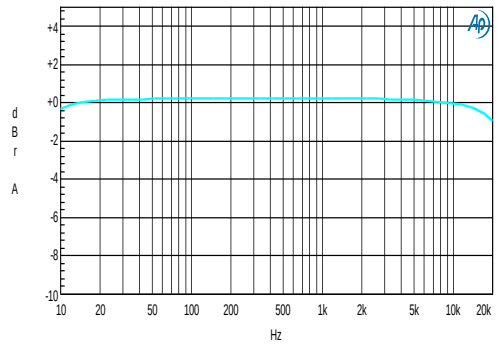
THD + N vs. P_{OUT}
4Ω + 33µH



Frequency Response
1W, 8Ω + 66µH



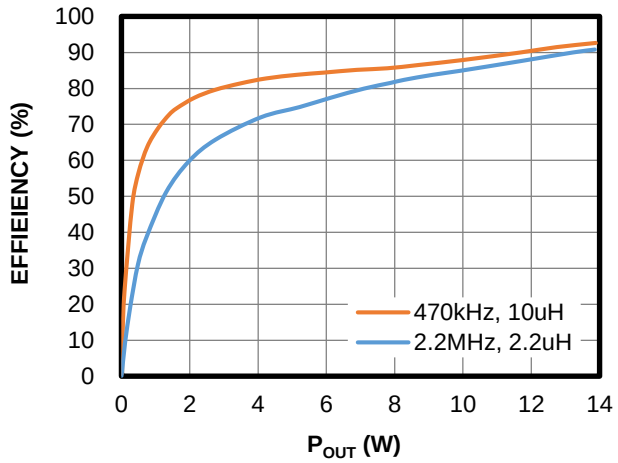
Frequency Response
1W, 4Ω + 33µH



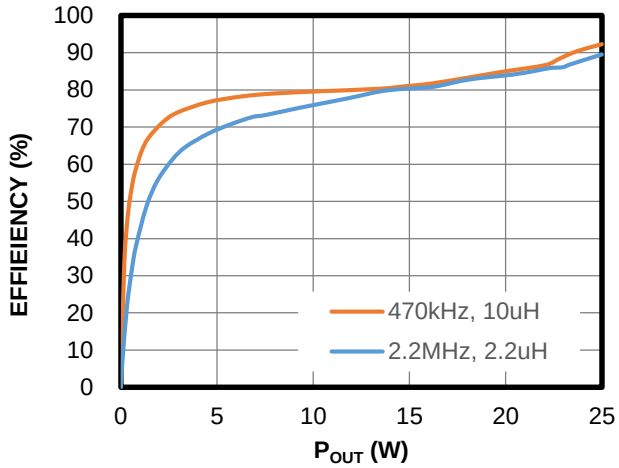
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD} = 14.4V, C_{OUT} = 1µF, f_{INPUT} = 1kHz, Gain = 20dB, T_A = 25°C, unless otherwise noted.

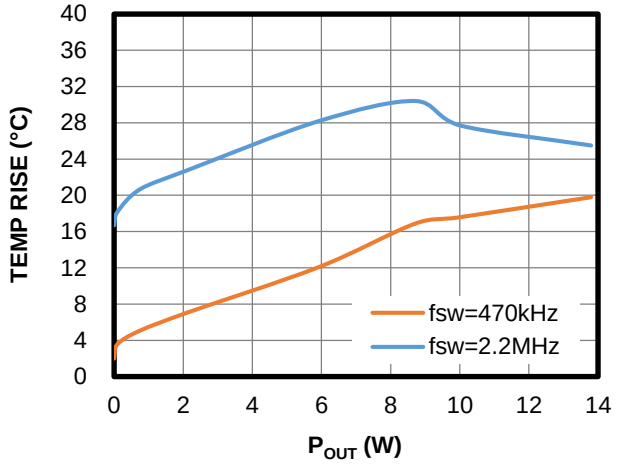
Efficiency vs. P_{OUT}
8Ω + 66µH (10)



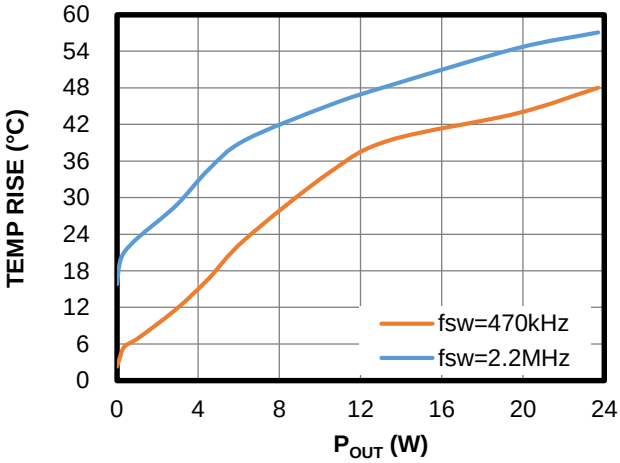
Efficiency vs. P_{OUT}
4Ω + 33µH (10)



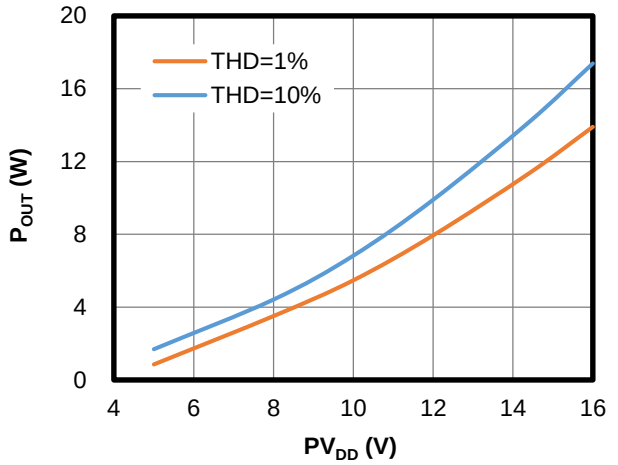
Temperature Rise vs. P_{OUT}
8Ω + 66µH



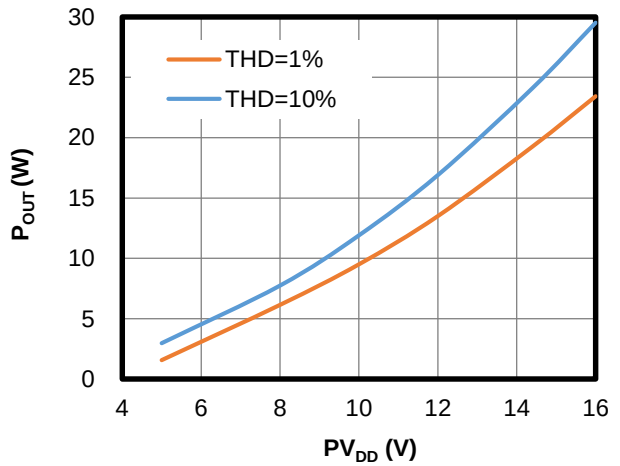
Temperature Rise vs. P_{OUT}
4Ω + 33µH



P_{OUT} vs. PV_{DD}
2.2MHz, 8Ω + 66µH



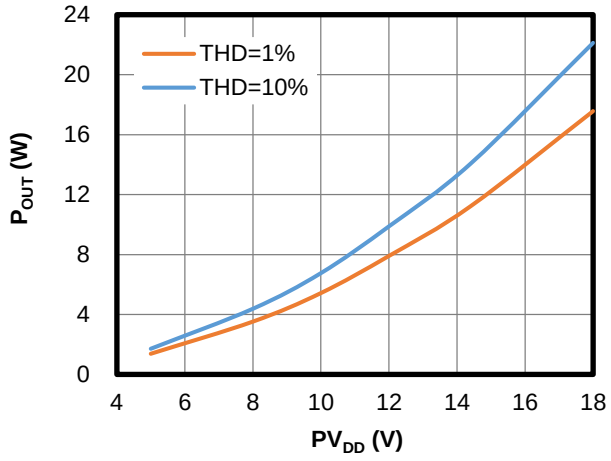
P_{OUT} vs. PV_{DD}
2.2MHz, 4Ω + 33µH



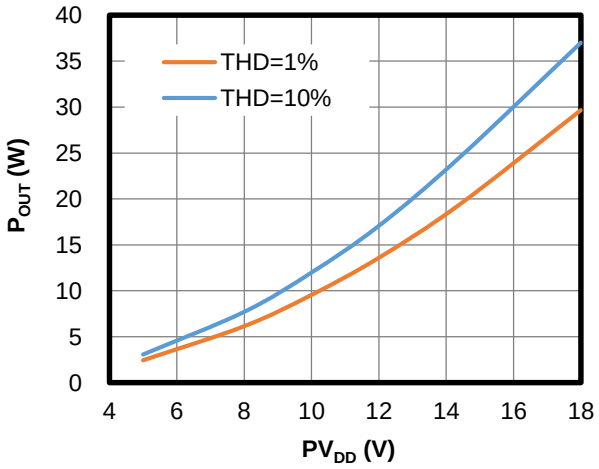
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD} = 14.4V, C_{OUT} = 1µF, f_{INPUT} = 1kHz, Gain = 20dB, T_A = 25°C, unless otherwise noted.

P_{OUT} vs. PV_{DD}
470kHz, 8Ω + 66µH



P_{OUT} vs. PV_{DD}
470kHz, 4Ω + 33µH



Note:

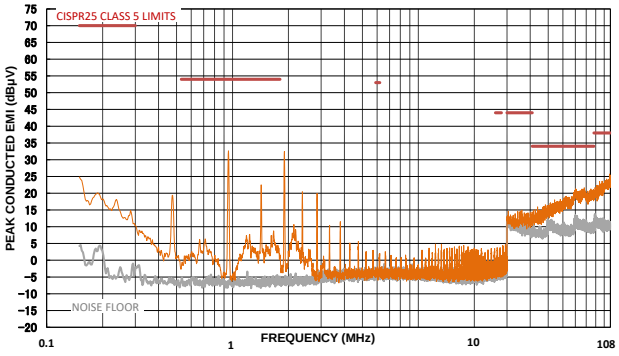
10) When f_{SW} = 470kHz, inductor information: XAL6060-103MEB, 10µH, DCR = 27mΩ. When f_{SW} = 2.2MHz, inductor information: XAL4030-222MEB, 2.2µH, DCR = 35.2mΩ.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD} = 12V, f_{SW} = 470kHz, L_{OUT} = 10µH (XEL5050-103MEC, 40.9mΩ, 3.6A), C_{OUT} = 1µF, f_{INPUT} = 1kHz, load = 4Ω, 1% THD + N, no output cable, gain = 20dB, T_A = 25°C, unless otherwise noted.

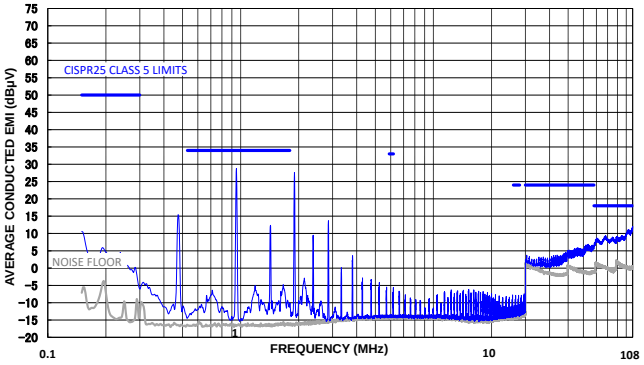
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



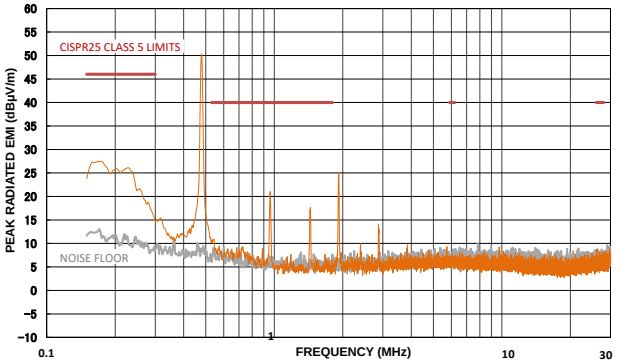
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



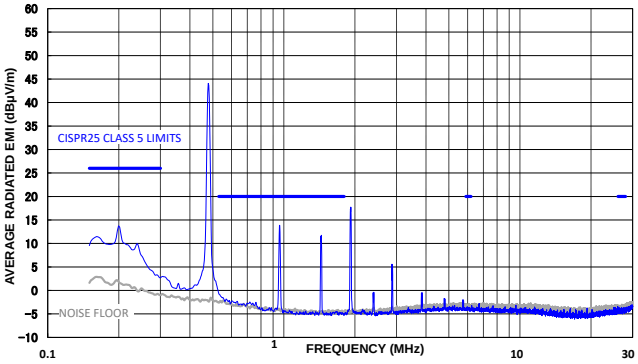
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



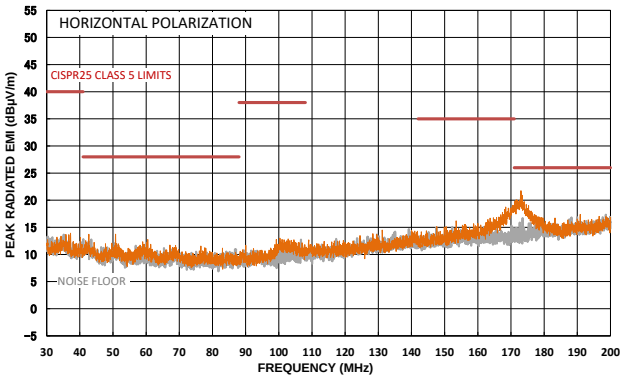
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



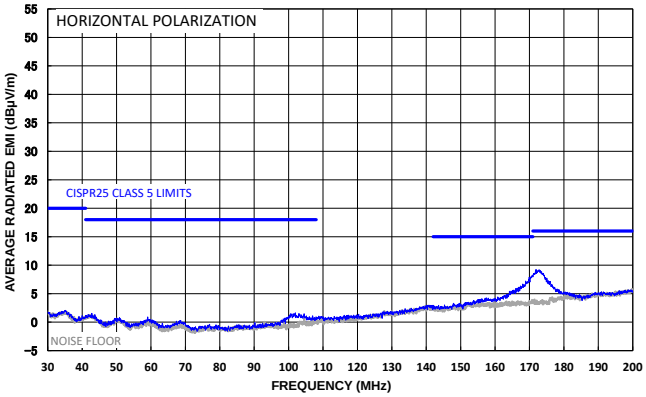
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz

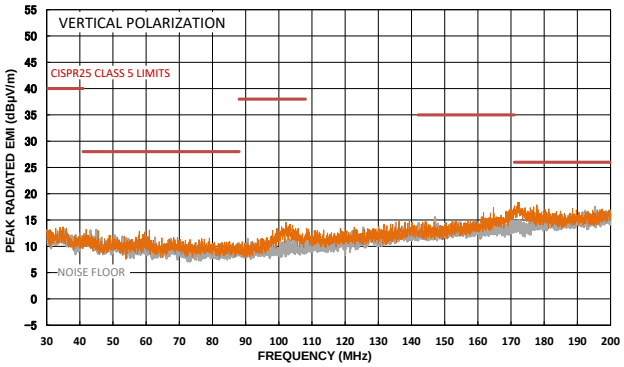


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD}= 12V, f_{SW} = 470kHz, L_{OUT} = 10µH (XEL5050-103MEC, 40.9mΩ, 3.6A), C_{OUT} = 1µF, f_{INPUT} = 1kHz, load = 4Ω, 1% THD + N, no output cable, gain = 20dB, T_A = 25°C, unless otherwise noted.

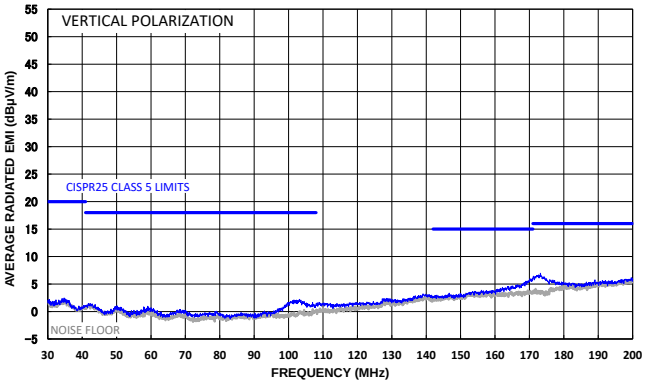
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



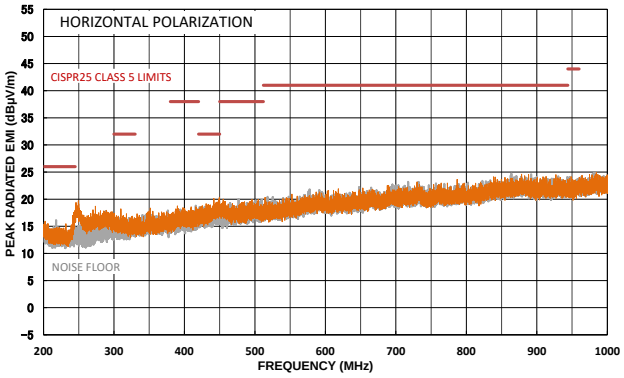
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



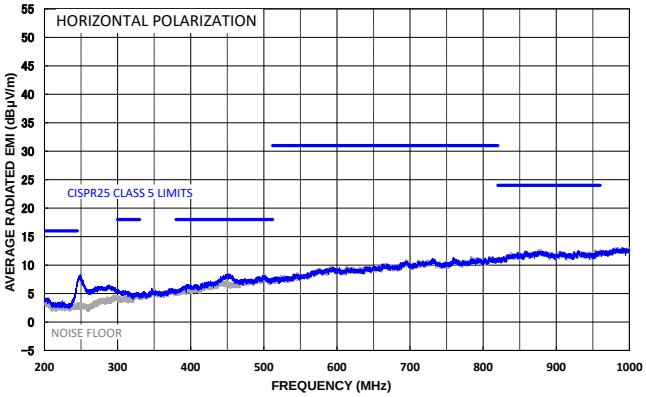
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



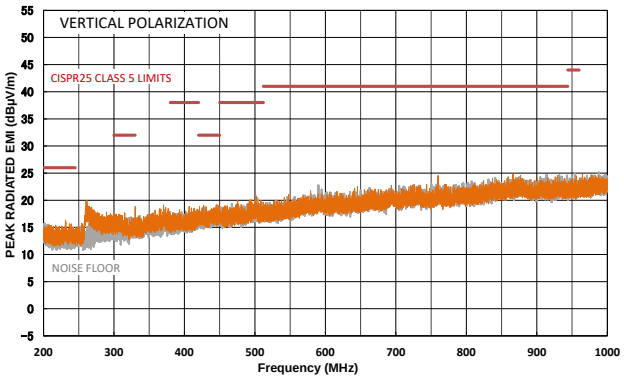
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



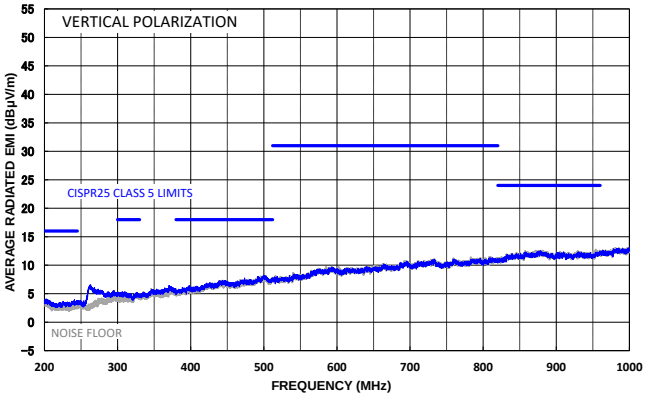
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz

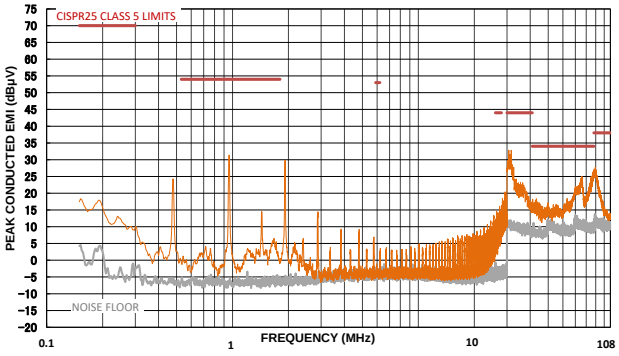


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD}= 12V, f_{SW} = 470kHz, L_{OUT} = 10µH (XEL5050-103MEC, 40.9mΩ, 3.6A), C_{OUT} = 1µF, f_{INPUT} = 1kHz, load = 4Ω, 1% THD + N, 2m output cable, gain = 20dB, T_A = 25°C, unless otherwise noted.

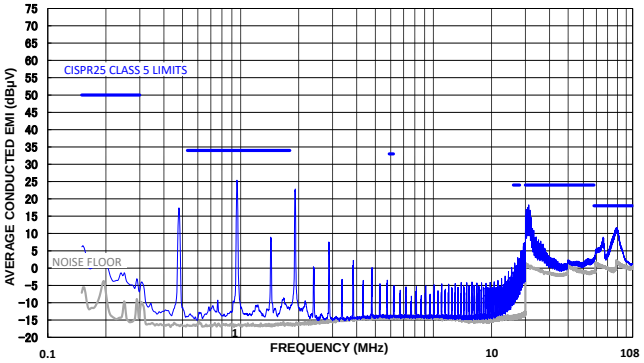
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



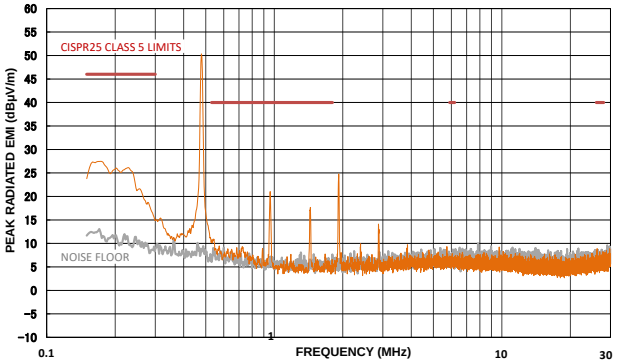
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



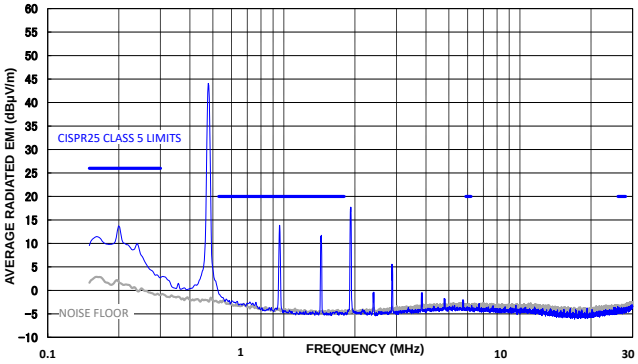
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



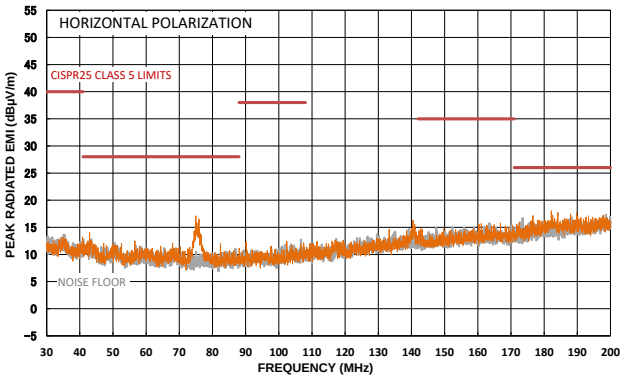
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



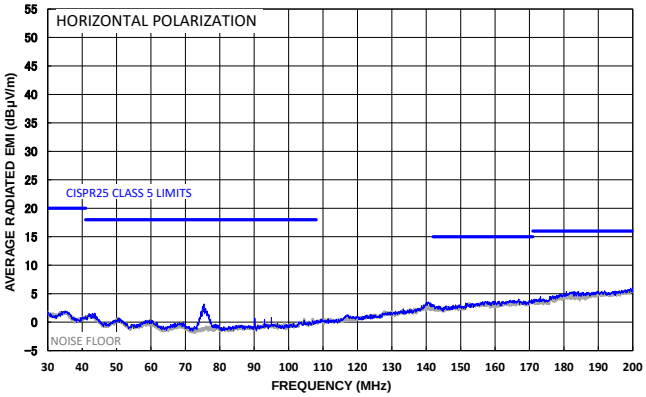
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz

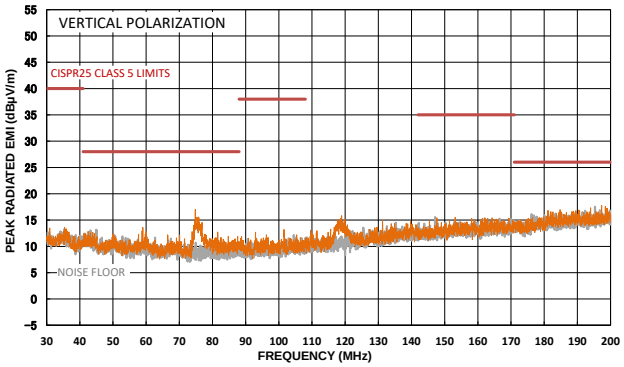


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD}= 12V, f_{SW} = 470kHz, L_{OUT} = 10µH (XEL5050-103MEC, 40.9mΩ, 3.6A), C_{OUT} = 1µF, f_{INPUT} = 1kHz, load = 4Ω, 1% THD + N, 2m output cable, gain = 20dB, T_A = 25°C, unless otherwise noted.

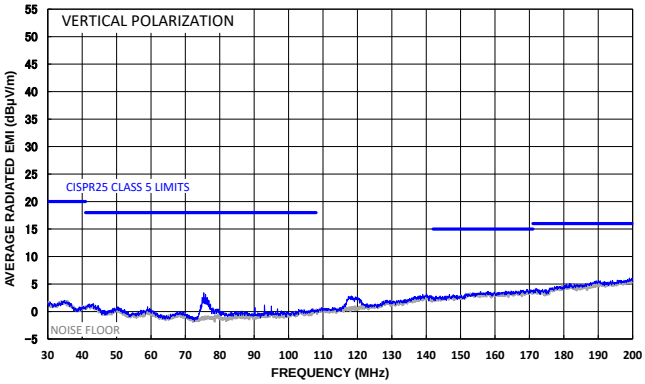
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



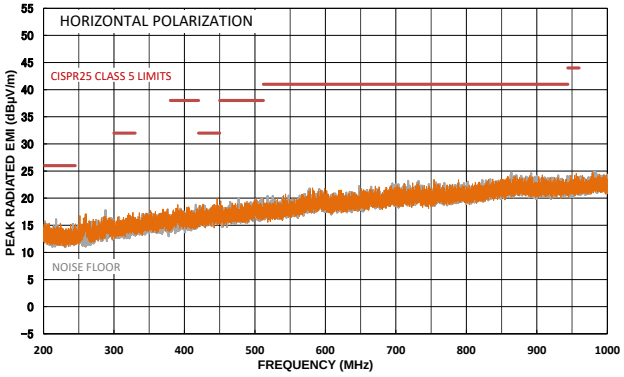
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



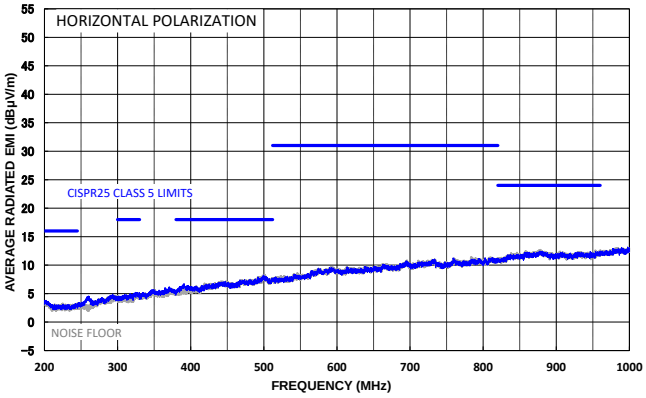
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



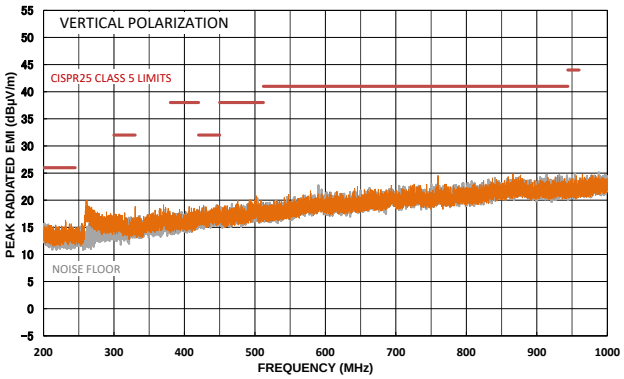
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



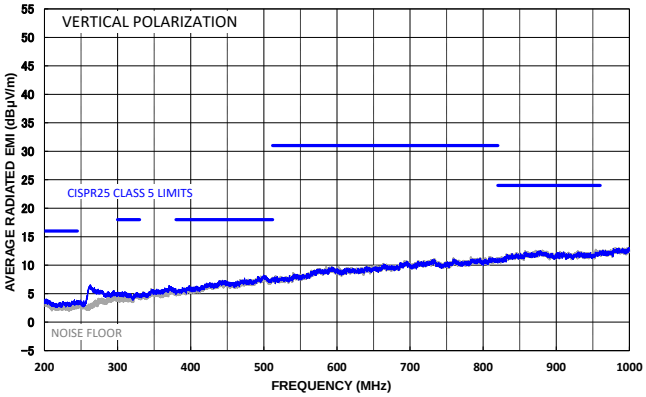
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

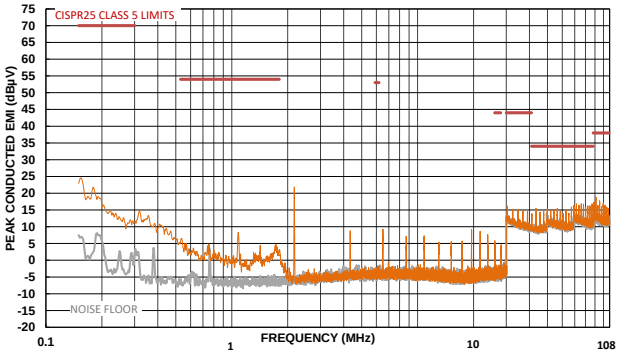
Vertical, 200MHz to 1GHz



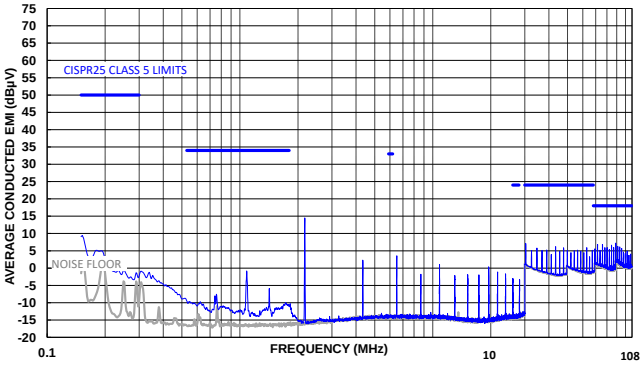
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD}= 12V, f_{SW} = 2.2MHz, L_{OUT} = 4.7µH (XAL5030-472MEB, 36mΩ, 5.9A), C_{OUT} = 1µF, f_{INPUT} = 1kHz, load = 4Ω, 10.5W, no output cable, with shielding, gain = 20dB, T_A = 25°C, unless otherwise noted.

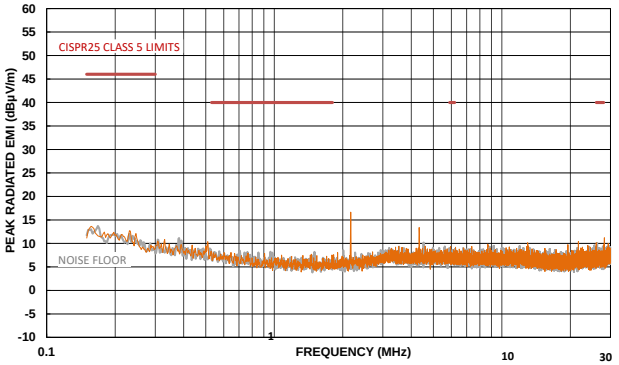
CISPR25 Class 5 Peak Conducted Emissions
150kHz to 108MHz



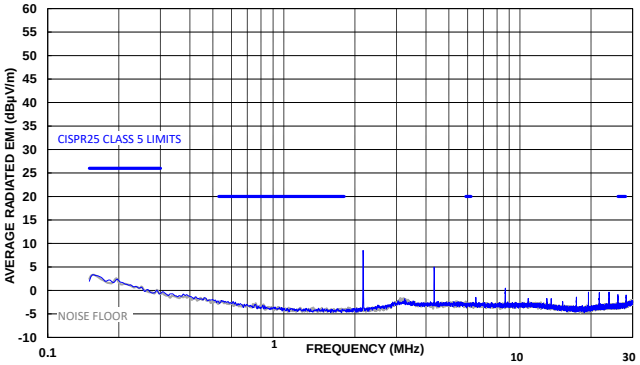
CISPR25 Class 5 Average Conducted Emissions
150kHz to 108MHz



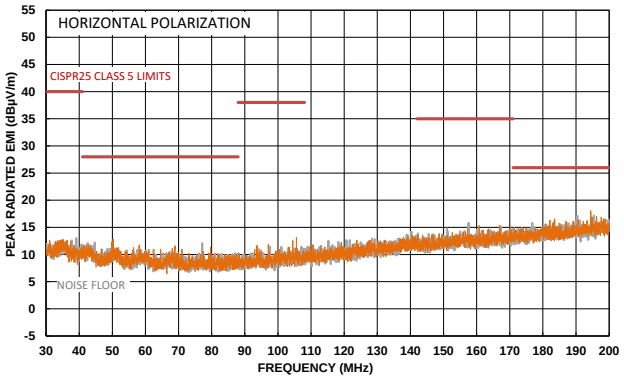
CISPR25 Class 5 Peak Radiated Emissions
150kHz to 30MHz



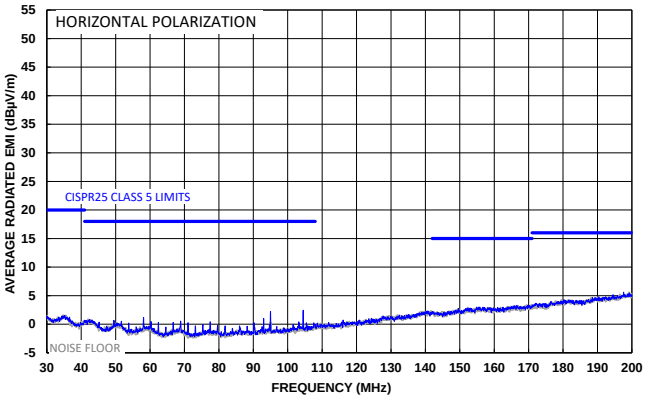
CISPR25 Class 5 Average Radiated Emissions
150kHz to 30MHz



CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions
Horizontal, 30MHz to 200MHz

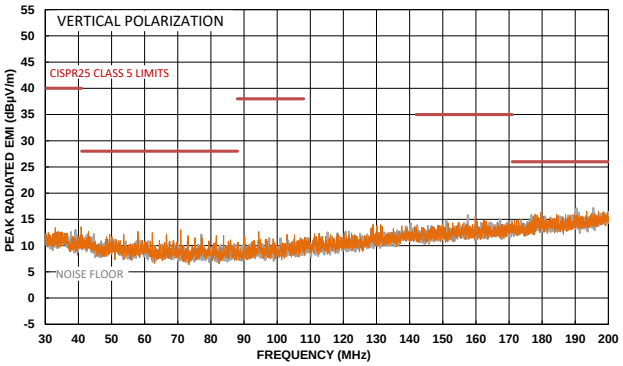


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD} = 12V, f_{SW} = 2.2MHz, L_{OUT} = 4.7µH (XAL5030-472MEB, 36mΩ, 5.9A), C_{OUT} = 1µF, f_{INPUT} = 1kHz, load = 4Ω, 10.5W, no output cable, with shielding, gain = 20dB, T_A = 25°C, unless otherwise noted.

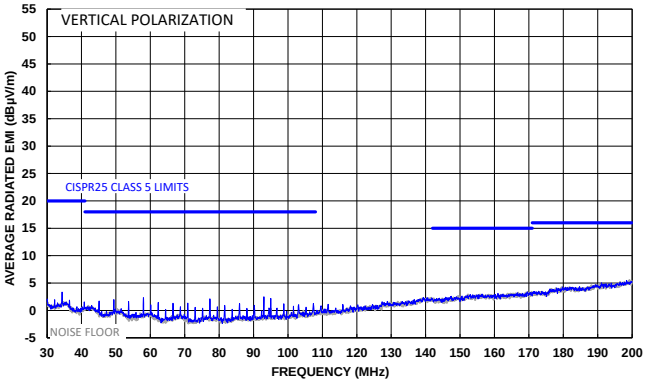
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



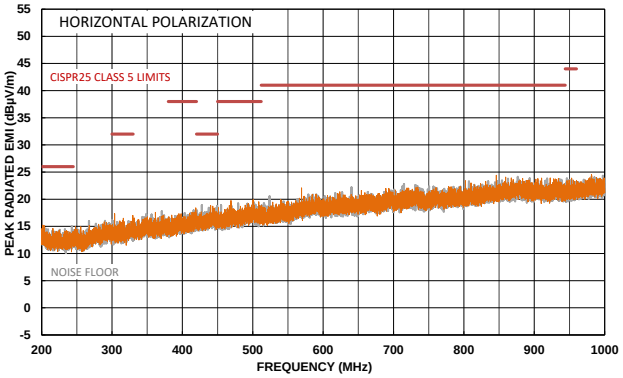
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



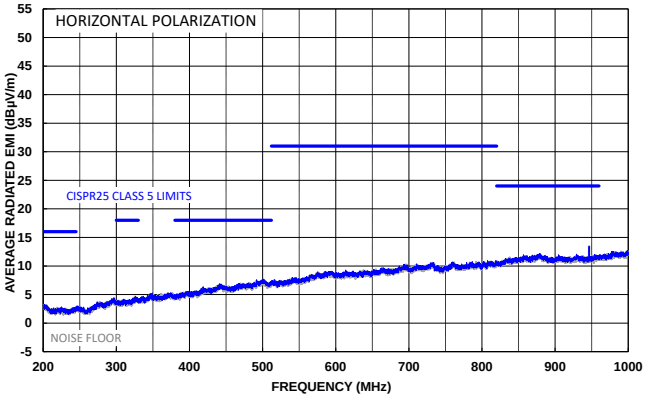
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



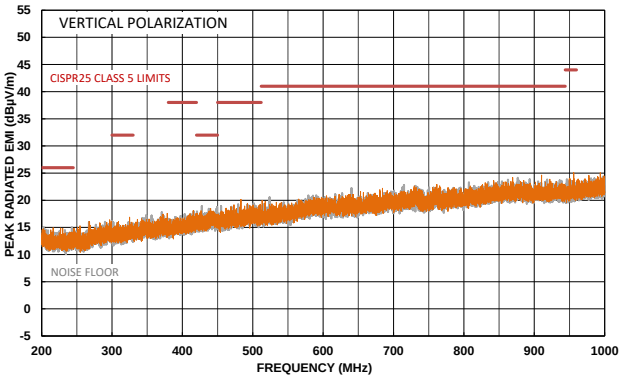
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



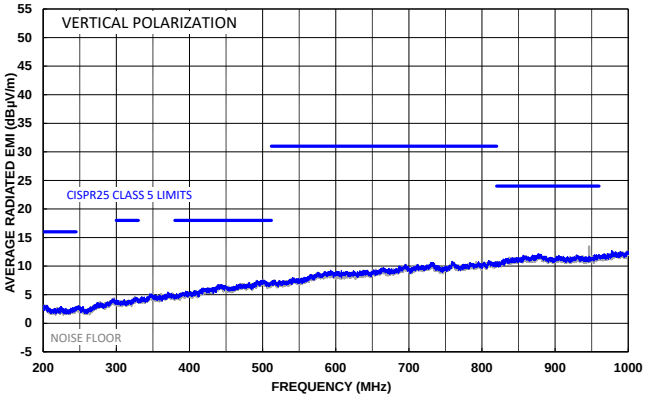
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz

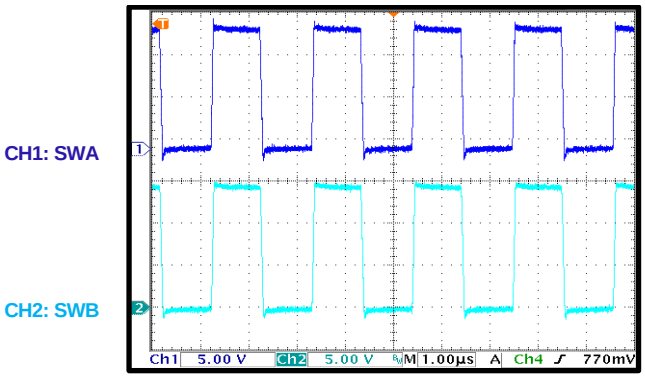


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD} = 14.4V, f_{SW} = 470kHz, L_{OUT} = 10µH, C_{OUT} = 1µF, f_{INPUT} = 1kHz, gain = 20dB, T_A = 25°C, unless otherwise noted.

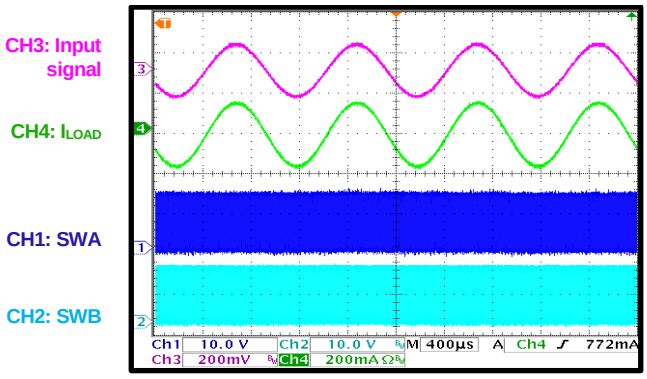
Steady State

8Ω + 66µH, no input signal



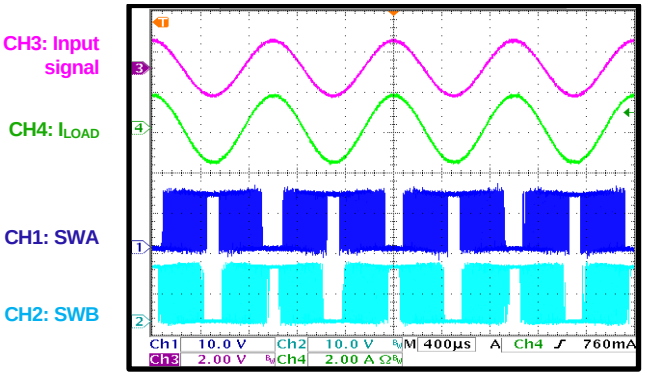
Steady State

8Ω + 66µH, THD = 0.1%, P_{OUT} = 94.5mW



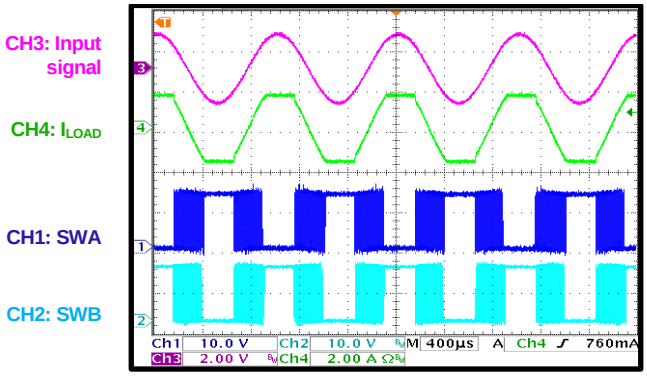
Steady State

8Ω + 66µH, THD = 1%, P_{OUT} = 11.3W



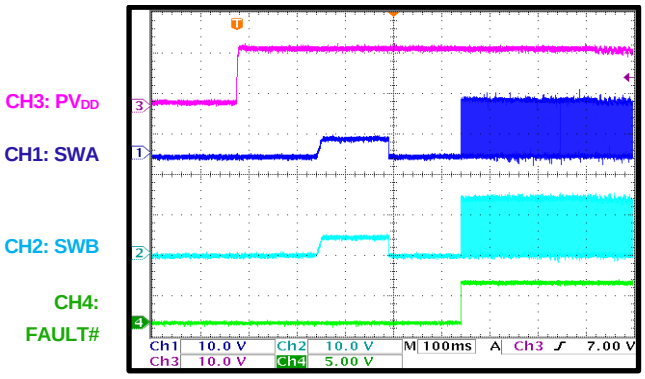
Steady State

8Ω + 66µH, THD = 10%, P_{OUT} = 13.6W



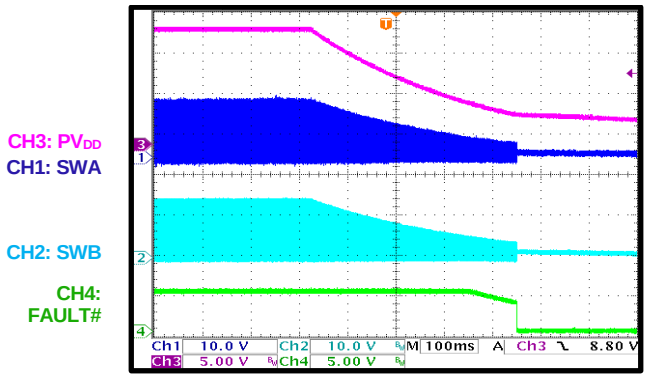
Start-Up through Input Voltage

8Ω + 66µH, THD = 1%, P_{OUT} = 11.3W



Shutdown through Input Voltage

8Ω + 66µH, THD = 1%, P_{OUT} = 11.3W

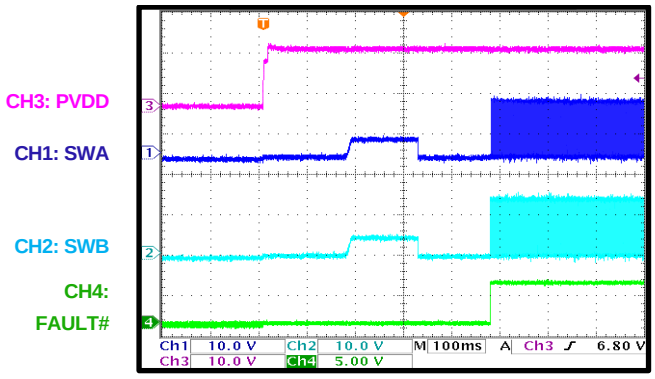


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD} = 14.4V, f_{SW} = 470kHz, L_{OUT} = 10µH, C_{OUT} = 1µF, f_{INPUT} = 1kHz, gain = 20dB, T_A = 25°C, unless otherwise noted.

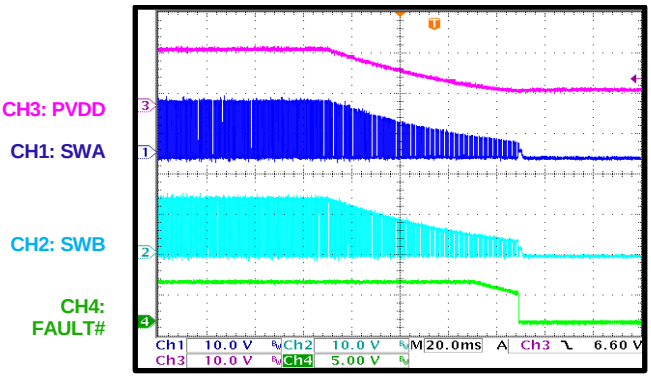
Start-Up through Input Voltage

8Ω + 66µH, THD = 10%, P_{OUT} = 13.6W



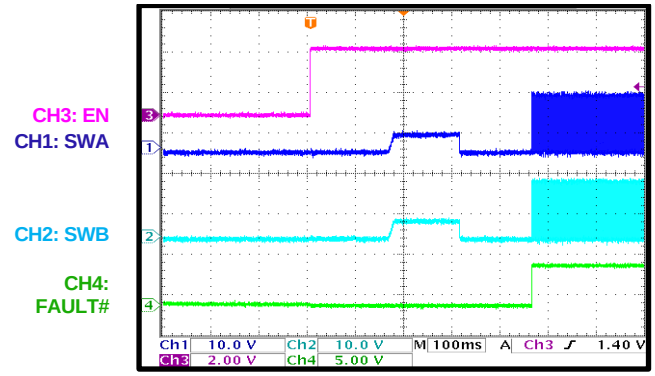
Shutdown through Input Voltage

8Ω + 66µH, THD = 10%, P_{OUT} = 13.6W



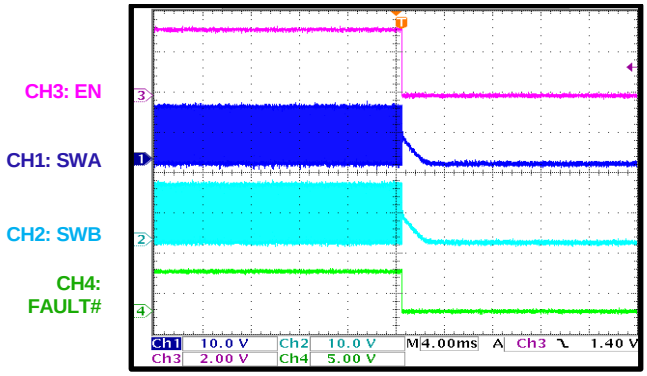
Start-Up through EN

8Ω + 66µH, THD = 1%, P_{OUT} = 11.3W



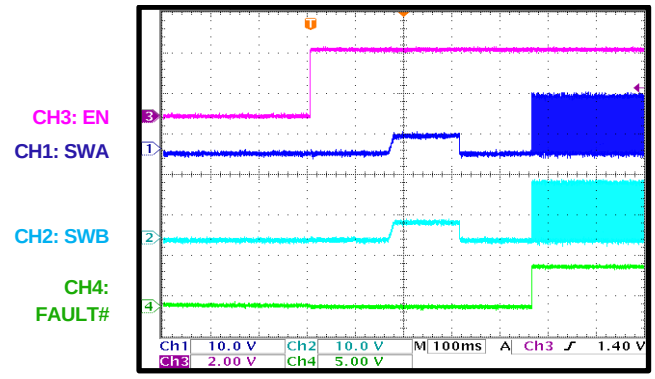
Shutdown through EN

8Ω + 66µH, THD = 1%, P_{OUT} = 11.3W



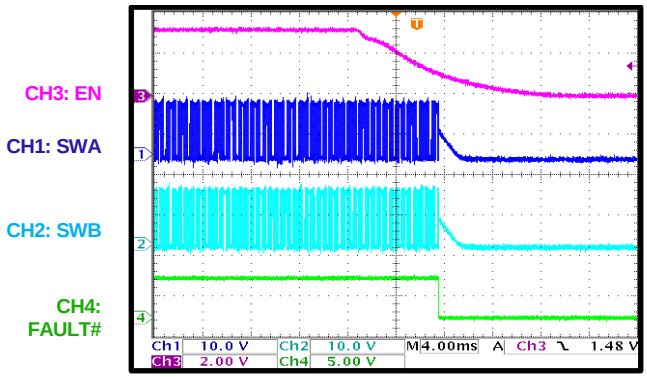
Start-Up through EN

8Ω + 66µH, THD = 10%, P_{OUT} = 13.6W



Shutdown through EN

8Ω + 66µH, THD = 10%, P_{OUT} = 13.6W

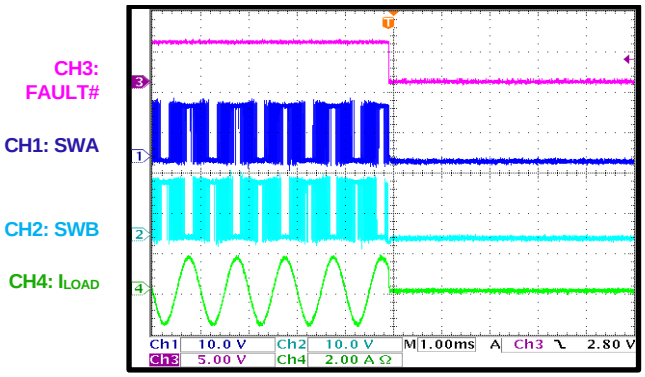


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD} = 14.4V, f_{SW} = 470kHz, L_{OUT} = 10µH, C_{OUT} = 1µF, f_{INPUT} = 1kHz, gain = 20dB, T_A = 25°C, unless otherwise noted.

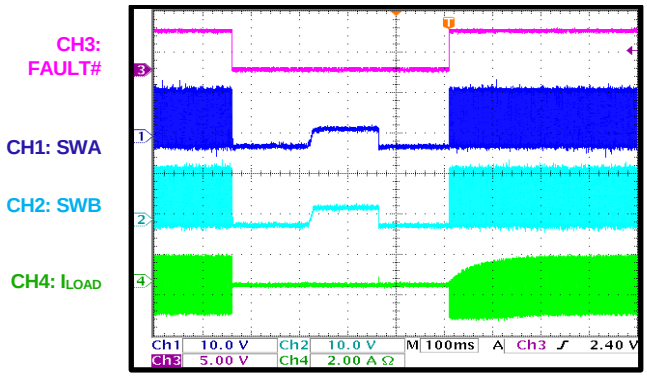
Short-Circuit Protection (SCP) Entry

OUT- short to GND, 8Ω + 66µH, THD = 1%,
P_{OUT} = 11.3W



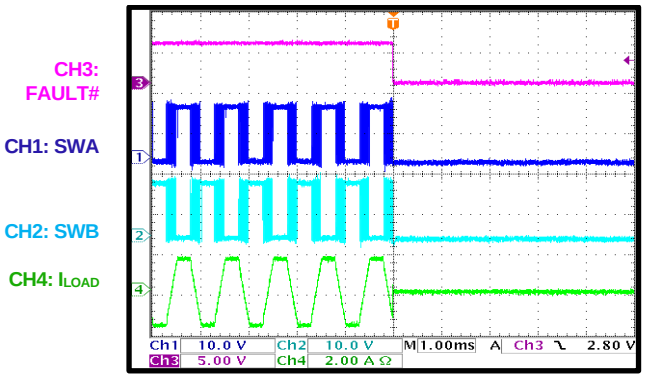
Short-Circuit Protection (SCP) Recovery

OUT- short to GND, 8Ω + 66µH, THD = 1%,
P_{OUT} = 11.3W



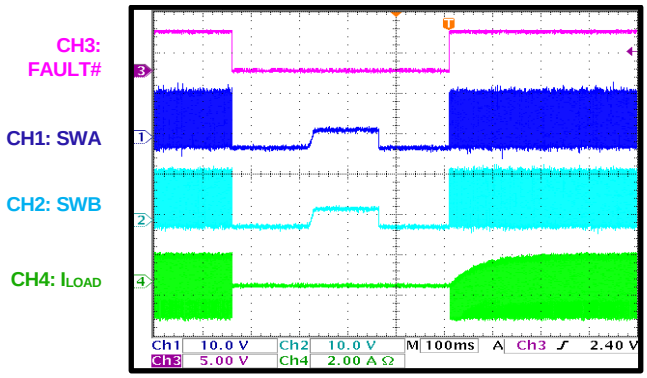
Short-Circuit Protection (SCP) Entry

OUT- short to GND, 8Ω + 66µH, THD = 10%,
P_{OUT} = 13.6W



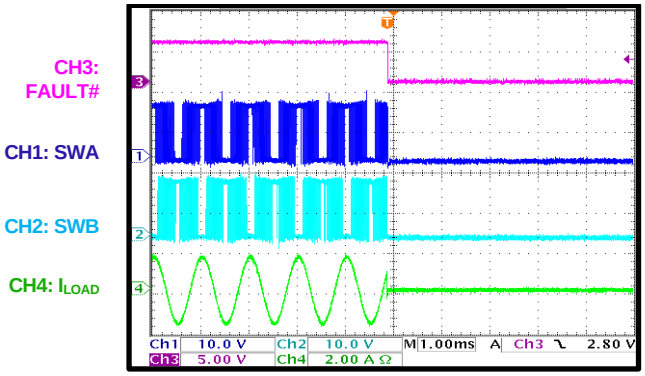
Short-Circuit Protection (SCP) Recovery

OUT- short to GND, 8Ω + 66µH, THD = 10%,
P_{OUT} = 13.6W



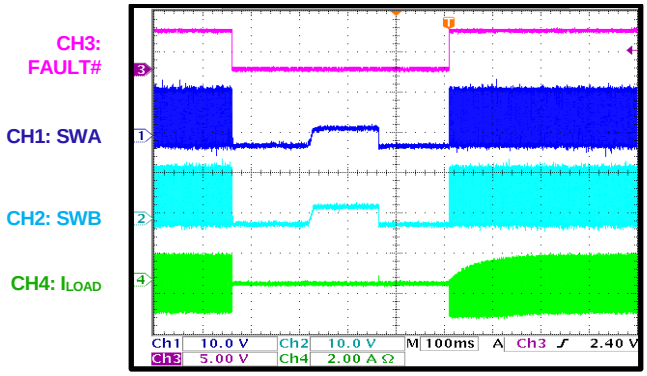
Short-Circuit Protection (SCP) Entry

OUT+ short to GND, 8Ω + 66µH, THD = 1%,
P_{OUT} = 11.3W



Short-Circuit Protection (SCP) Recovery

OUT+ short to GND, 8Ω + 66µH, THD = 1%,
P_{OUT} = 11.3W

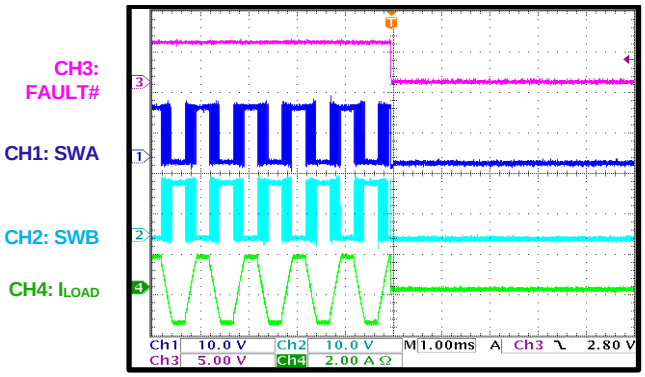


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD} = 14.4V, f_{SW} = 470kHz, L_{OUT} = 10µH, C_{OUT} = 1µF, f_{INPUT} = 1kHz, gain = 20dB, T_A = 25°C, unless otherwise noted.

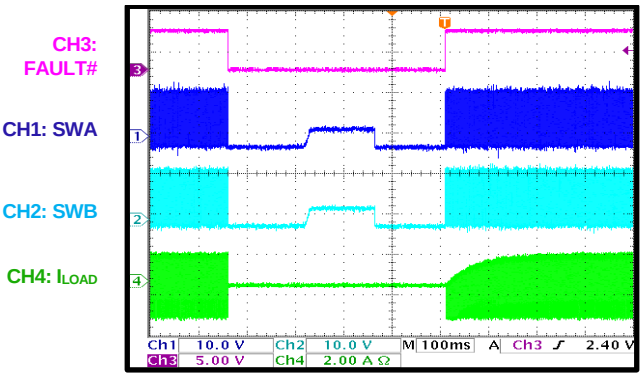
Short-Circuit Protection (SCP) Entry

OUT+ short to GND, 8Ω + 66µH, THD = 10%, P_{OUT} = 13.6W



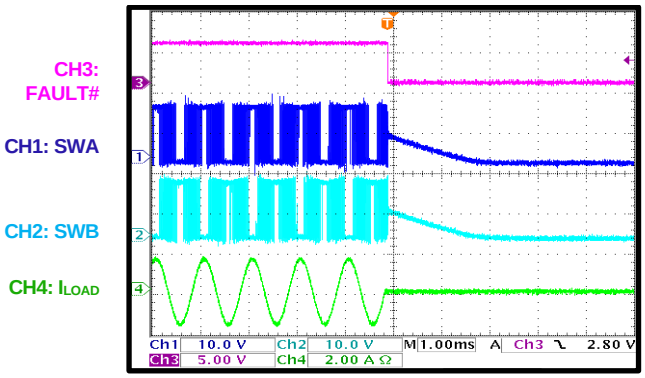
Short-Circuit Protection (SCP) Recovery

OUT+ short to GND, 8Ω + 66µH, THD = 10%, P_{OUT} =13.6W



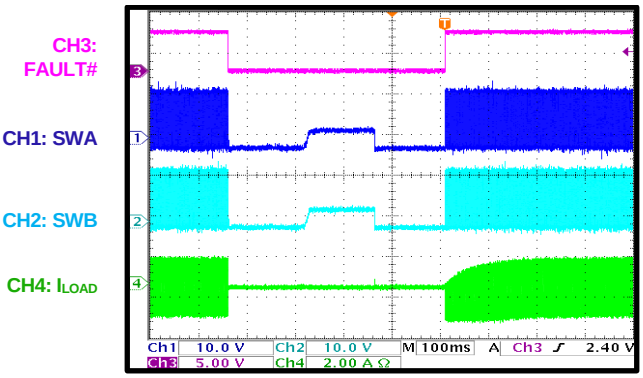
Short-Circuit Protection (SCP) Entry

OUT+ short to OUT-, 8Ω + 66µH, THD = 1%, P_{OUT} = 11.3W



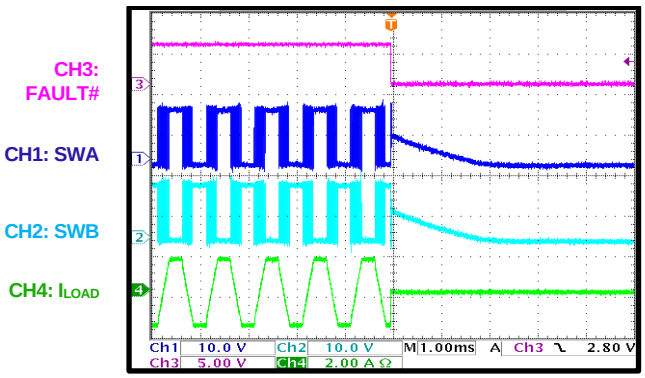
Short-Circuit Protection (SCP) Recovery

OUT+ short to OUT-, 8Ω + 66µH, THD = 1%, P_{OUT} = 11.3W



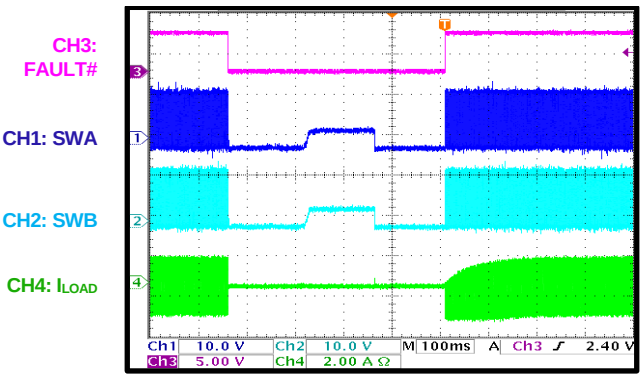
Short-Circuit Protection (SCP) Entry

OUT+ short to OUT-, 8Ω + 66µH, THD = 10%, P_{OUT} = 13.6W



Short-Circuit Protection (SCP) Recovery

OUT+ short to OUT-, 8Ω + 66µH, THD = 10%, P_{OUT} = 13.6W

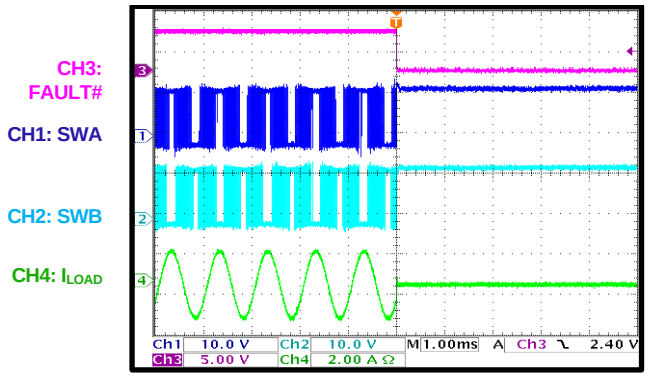


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD} = 14.4V, f_{SW} = 470kHz, L_{OUT} = 10µH, C_{OUT} = 1µF, f_{INPUT} = 1kHz, gain = 20dB, T_A = 25°C, unless otherwise noted.

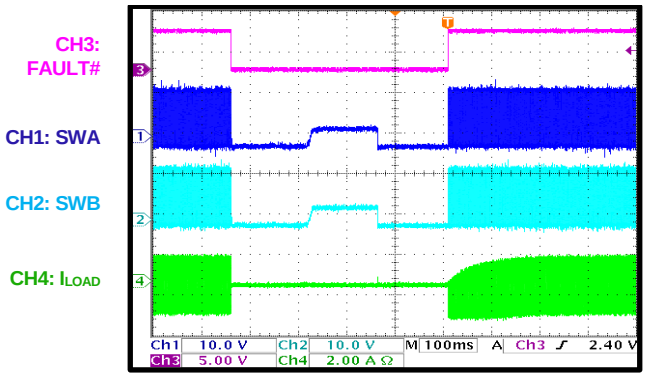
Short-Circuit Protection (SCP) Entry

OUT+ short to PVDD, 8Ω + 66µH, THD = 1%, P_{OUT} = 11.3W



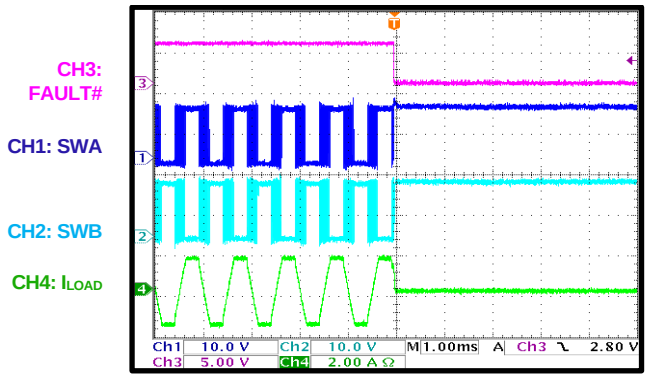
Short-Circuit Protection (SCP) Recovery

OUT+ short to PVDD, 8Ω + 66µH, THD = 1%, P_{OUT} = 11.3W



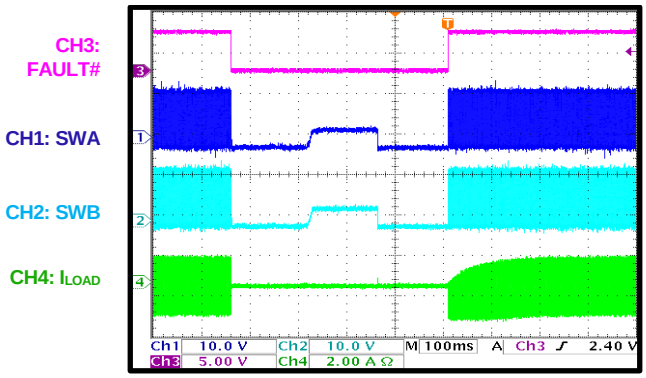
Short-Circuit Protection (SCP) Entry

OUT+ short to PVDD, 8Ω + 66µH, THD = 10%, P_{OUT} = 13.6W



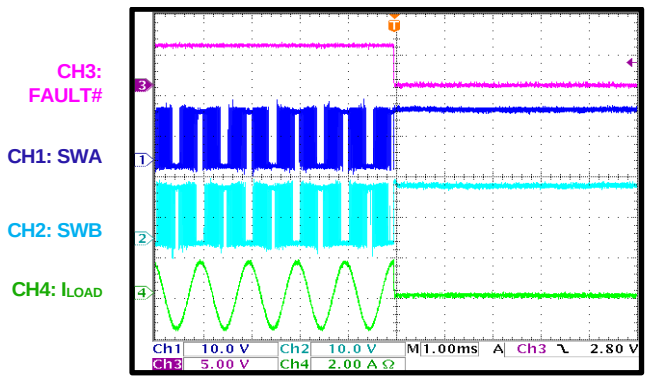
Short-Circuit Protection (SCP) Recovery

OUT+ short to PVDD, 8Ω + 66µH, THD = 10%, P_{OUT} = 13.6W



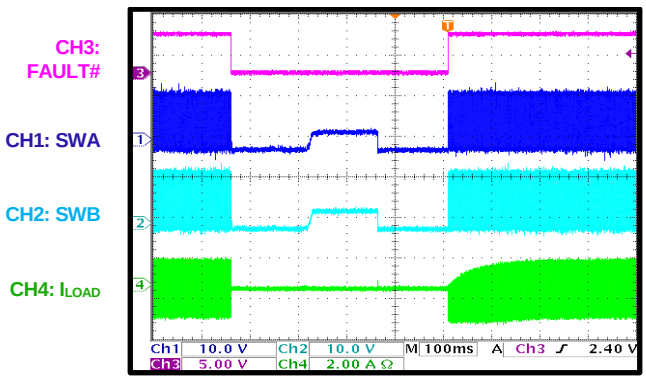
Short-Circuit Protection (SCP) Entry

OUT- short to PVDD, 8Ω + 66µH, THD = 1%, P_{OUT} = 11.3W



Short-Circuit Protection (SCP) Recovery

OUT- short to PVDD, 8Ω + 66µH, THD = 1%, P_{OUT} = 11.3W

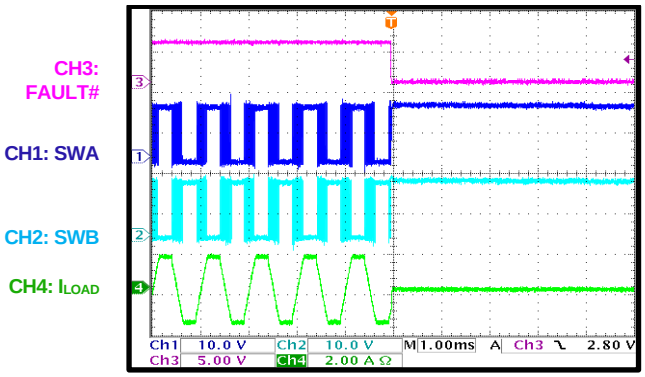


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

PV_{DD} = 14.4V, f_{SW} = 470kHz, L_{OUT} = 10µH, C_{OUT} = 1µF, f_{INPUT} = 1kHz, gain = 20dB, T_A = 25°C, unless otherwise noted.

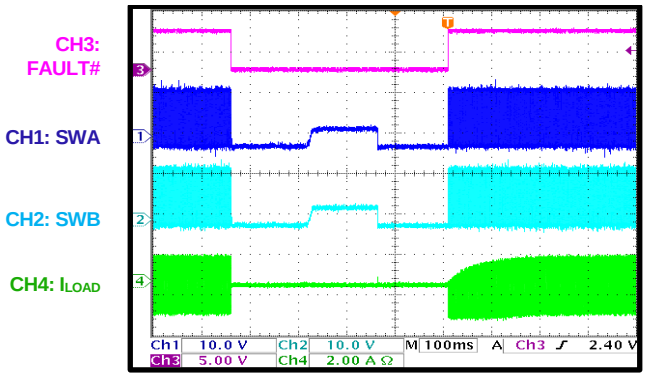
Short-Circuit Protection (SCP) Entry

OUT- short to PVDD, 8Ω + 66µH, THD = 10%, P_{OUT} = 13.6W



Short-Circuit Protection (SCP) Recovery

OUT- short to PVDD, 8Ω + 66µH, THD = 10%, P_{OUT} = 13.6W



FUNCTIONAL BLOCK DIAGRAM

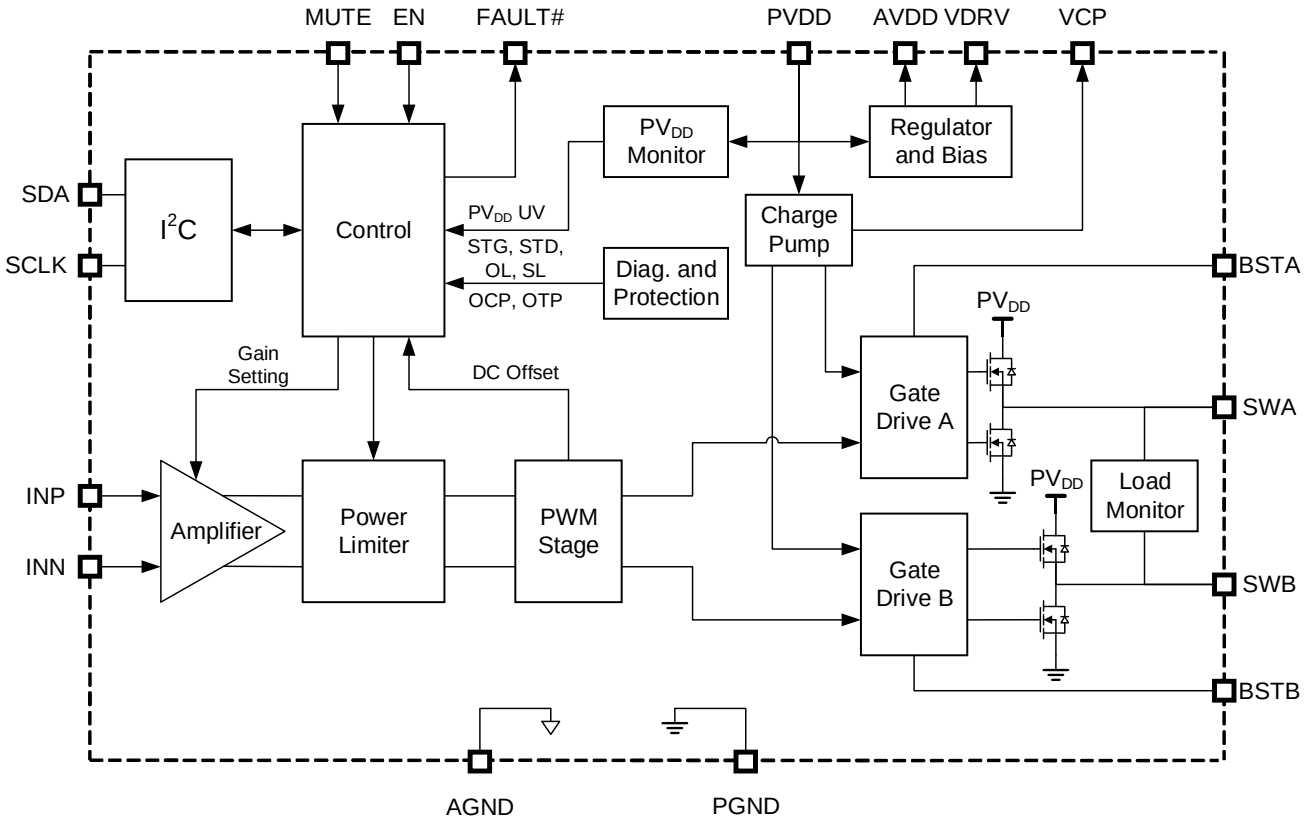


Figure 1: Functional Block Diagram

OPERATION

The MPQ7795 is a fully integrated Class-D mono BTL audio amplifier. Because of the switching Class-D output stage, power dissipation in the amplifier is drastically reduced when compared to Class-A, Class-B, or Class-A/B amplifiers, all while maintaining high fidelity and low distortion.

The MPQ7795 includes four high-power MOSFETs. For each half-bridge channel, the output driver stage uses two N-channel MOSFETs to deliver the pulses to the LC output filter, which in turn drives the load. To fully enhance the high-side MOSFET (HS-FET), the bootstrap capacitor between the OUTx and BSTx pins drives the gate to a voltage that exceeds the source. While the output is driven low, the bootstrap capacitor is charged by the power supply through an internal circuit. The HS-FET's gate is driven high by the voltage at the bootstrap supply, forcing the MOSFET gate to a voltage that exceeds the power supply voltage and allows the MOSFET to fully turn on. This process reduces the amplifier's power loss.

The MPQ7795's gain is set by the following I²C bits: G0 and G1. The actual gain settings are controlled by the ratios of the internal input and feedback resistors.

Enable (EN) and MUTE Function

The MPQ7795's EN input is an active-high enable control. To enable the MPQ7795, drive EN with a minimum 1.5V voltage. To disable the amplifier, drive EN below 0.4V. While the MPQ7795 is disabled, the PVDD operating current is about 0.02μA, and the output driver MOSFETs turn off. AVDD and VDRV are also disabled. When the device is enabled, the load is automatically detected.

The MUTE pin is also an active-high input pin. To enter mute mode, drive MUTE with a 3.3V or 5V voltage. When the MPQ7795 is muted, the output driver MOSFETs turn off, and the load diagnostics are executed while AVDD and VDRV are still enabled. When the device exits mute mode, load detection is not performed.

Adjustable Power Limit (P_{LIMIT})

The power limit (P_{LIMIT}) circuit sets a limit on the output's peak-to-peak voltage (V_{PK-PK}). The limit is set by limiting the duty cycle to a fixed maximum value (see Figure 2). This limit can be considered a virtual voltage rail that is below the supply connected to PVDD. This virtual voltage is set via the PL bits in the I²C. This output voltage (V_{OUT}) can be used to calculate the maximum output power (P_{OUT}) for a given maximum input voltage (V_{IN}) and speaker impedance.

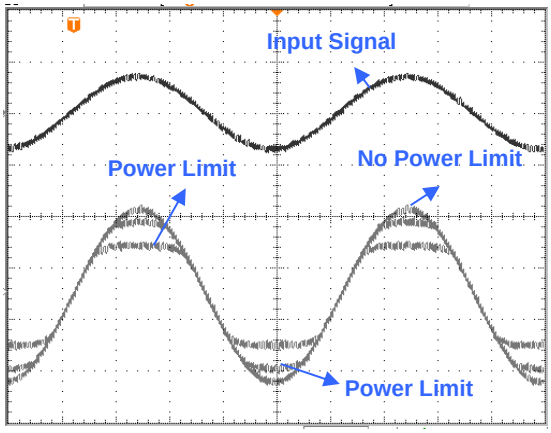


Figure 2: P_{LIMIT} Circuit Operation

The maximum output power (P_{OUT_MAX}) can be calculated with Equation (1):

$$P_{OUT\_MAX} = \frac{\left(\frac{R_L}{R_L + 2 \times R_S} V_P\right)^2}{2 \times R_L} \quad (1)$$

Where R_S is the total output series resistance (including $R_{DS(ON)}$ and the DCR of the output inductors), R_L is the load resistance, and V_P is the output voltage amplitude.

In addition, the output power at 10% THD + N ($P_{OUT@10\%THD+N}$) can be estimated with Equation (2):

$$P_{OUT@10\%THD+N} \approx 1.25 \times \text{unclamped } P_{OUT} \quad (2)$$

Table 1 on page 30 shows the P_{LIMIT} setting, and the typical max V_{OUT}, and P_{OUT} at 10% THD + N.

Table 1: Power Limit Typical Operation (11)

Power Limit Setting (V)	Max Output Voltage (V_{PK-PK})		P_{OUT} at 10% THD + N (W)	
	4Ω	8Ω	4Ω	8Ω
5	9.4	9.2	1.5	0.8
5.9	11.2	11	2.6	1.4
7	13.4	13	4.1	2.2
8.4	15.2	15	5.9	3.1
9.8	19.8	19.6	11.8	6.2
11.8	22.8	22.8	16.3	8.4
14	26.6	26.6	23.3	11.8
No limit	26.8	28.6	24.5	13.8

Note:

11) Test conditions: f_{SW} = 470kHz, 10µH inductor (XAL6060-103MEB, DCR = 27mΩ), T_A = 25°C, PV_{DD} = 14.4V, gain = 20dB.

Gain Setting

The MPQ7795's gain is set by the following I²C bits: G0 and G1. The actual gain settings are controlled by the ratios of the internal input and feedback resistors.

Table 2 shows the typical gain and single-ended (SE) input impedance for each setting.

Table 2: Gain Setting

G0	G1	Typ. GAIN (dB)	Typ. SE Input Impedance (kΩ)
0	0	20	70
1	0	26	50
0	1	32	30
1	1	36	20

Over-Temperature Shutdown

Thermal monitoring is integrated into the MPQ7795. If the die temperature exceeds 170°C, all switches turn off. The temperature must fall below 150°C before normal operation resumes, with the same start-up sequence used to prevent popping noise.

Overload and Short-Circuit Protection (SCP)

The MPQ7795 has internal overload and short-circuit protection (SCP). The currents flowing through the both the HS-FETs and low-side MOSFETs (LS-FETs) are monitored. When a short circuit is detected, all the MOSFETs go to high impedance for a fixed duration. After this fixed duration, the MPQ7795 restarts with load diagnostics to prevent the pop noise from occurring.

Typically, if a short circuit occurs in play mode with an input signal, the MPQ7795 triggers an overload then restarts load diagnostics to check which fault occurred. If the fault is consistent, the load diagnostics repeat until the fault disappears.

Load Diagnostics

When the device is enabled, the load diagnostics run before the part starts switching, or before entering a fault state. During diagnostics, the output is in a high-impedance state. The diagnostics typically take 480ms.

Step 1 (t_0 to t_1): SWA pulls low to detect whether there is a short circuit between SWA and PVDD.

Step 2 (t_1 to t_2): SWB pulls to detect whether there is a short circuit between SWB and PVDD.

Step 3 (t_2 to t_3): SWA pulls high to detect whether there is a short circuit between SWA and GND.

Step 4 (t_3 to t_4): SWB pulls high to detect whether there is a short circuit between SWB and GND.

Step 5 (t_4 to t_5): SWB pulls low, and SWA is pulled high by an internal current source to detect whether there is a short circuit between SWA and SWB (short load detection).

Step 6 (t_5 to t_6): SWB pulls low, and SWA is pulled high by an internal current source to detect whether there is an open circuit between SWA and SWB (open load detection).

Each step takes 80ms. At the end of step 4, SWA and SWB are pulled to GND. After 100µs, SWA is pulled to AVDD (5V). From step 1 to step 4, the undetected output is in a high-impedance state.

Figure 3 shows the load diagnostics when there is no load.

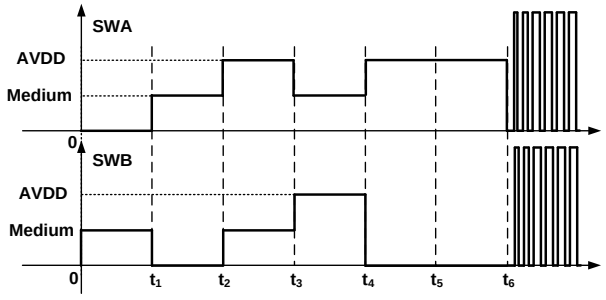


FIGURE 3: LOAD DIAGNOSTICS (NO LOAD)

Load diagnostics can detect open load, short load, output short to PVDD, and output short to ground conditions. See the Electrical Characteristics section starting on page 6 for the relevant thresholds. If any status mentioned above is detected, the I²C reports the status.

If the load diagnostics find a fault, the MPQ7795 restarts at step 1 after the current step is finished. For example, if an SWB-to-PVDD short condition is detected, the load diagnostics restart after step 2 finishes, then the MPQ7795 repeats step 1 and step 2 until the short is removed.

Fault Output

The MPQ7795 includes an open-drain, active-low fault indicator output on the FAULT# pin. A fault is trigged if any of the following faults occur: over-current (OC), PVDD under-voltage (UV), over-temperature shutdown, DC offset, shorted load, output short to PVDD, and output short to ground.

The FAULT# pin pulls low if a fault is detected on any channel, then the output goes into a high-impedance state. When the fault condition is removed, the MPQ7795 resumes normal operation. FAULT# remains asserted until the fault register is cleared. The fault register can be cleared by writing 0xFF to register 0x01.

Note that open load conditions are not reported via the FAULT# pin, nor does the output go to a high-impedance state. This condition is only indicated by the I²C registers.

I²C INTERFACE

I²C Serial Interface Description

The I²C bus is a 2-wire, bidirectional serial interface, consisting of a serial data line (SDA) and a serial clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. The MPQ7795 works as a slave-only device, which supports up to 400kbps of bidirectional data transfer in fast mode, adding flexibility to the power supply solution. The output voltage, transition slew rate, and additional converter parameters can be instantaneously controlled by I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 4).

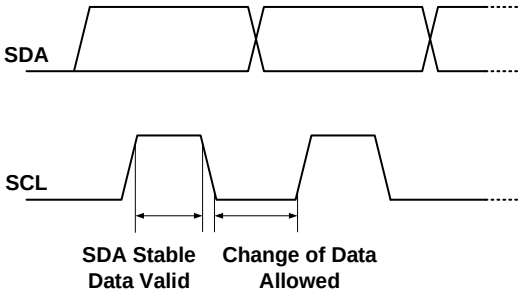


Figure 4: Bit Transfer on the I²C Bus

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start command is defined as the SDA signal transitioning from high to low while the SCL line is high. The stop command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 5).

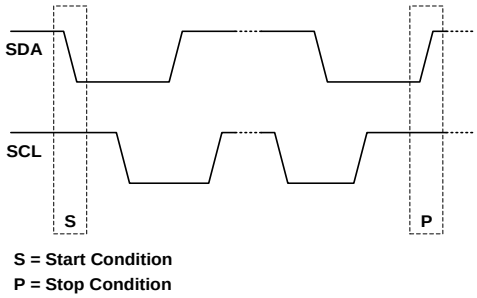


Figure 5: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is considered busy after the start command. The bus is considered free again a certain time after the stop command. The bus stays busy if a repeated start command is generated instead of a stop command. The start and repeated start commands are functionally identical.

Transfer Data

Every byte puts on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable low during the high period of the clock pulse.

Figure 6 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long followed by an eighth data direction bit (R/W). A “0” indicates a transmission (write), and a “1” indicates a request for data (read). A data transfer is always terminated by a stop command, which is generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

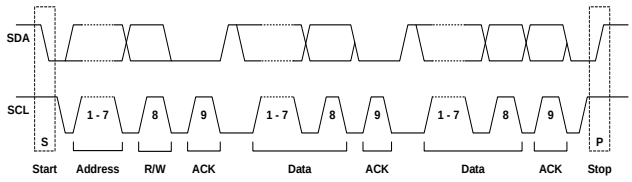


Figure 6: A Complete Data Transfer

Write Sequence

The typical write sequence requires a master's start command, a valid slave address, a register index byte, and a corresponding data byte.

After receiving each byte, the MPQ7795 acknowledges what it has received by pulling the SDA line low during the high period of a single clock pulse. A valid I^2C address selects the MPQ7795 (see Figure 7).

Read Sequence

The typical MPQ7795 read sequence requires a master's start command, then a valid slave address, followed by a register index byte. An additional start command comes with the re-broadcast of the slave address, with bit[1] indicating a read cycle. The following fourth byte contains the data being returned by the MPQ7795. The byte value in the data byte reflects the value of the register index that was previously queried (see Figure 8).

Chip Address

The MPQ7795's 7-bit address is 0x6C.

When the master sends the address as an 8-bit value, the 7-bit address should be followed by bit 0 or 1 to indicate write or read operation, respectively. For write operations, the first byte should be 0xD8; for read operations, the first byte should be 0xD9.

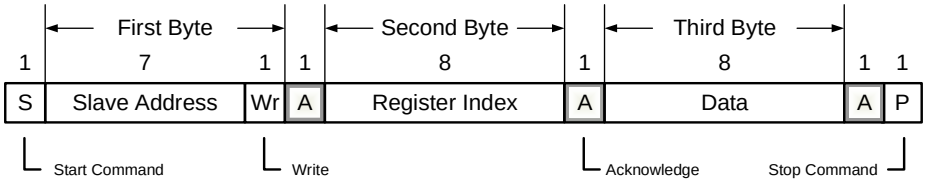


Figure 7: Write Sequence

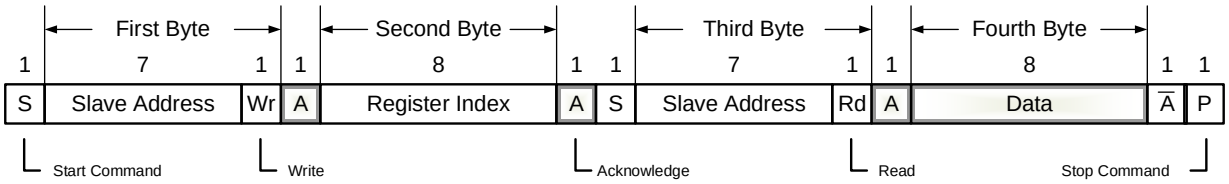


Figure 8: Read Sequence

REGISTER MAP

The default slave address is 0x6C. The MPQ7795-AEC1's detailed register map is described in the tables below.

FAULT_STATUS_DETECTION_1 (0x01)

The FAULT_STATUS_DETECTION_1 command indicates whether certain faults have occurred.

Command	FAULT_STATUS_DETECTION_1							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Function	OT	DC	UV	OCS	LF	BSTF	RESERVED	

Bits	Bit Name	Default	Description
7	OT	0b	Indicates whether over-temperature shutdown has occurred. 0: No over-temperature shutdown has occurred 1: Over-temperature shutdown has occurred
6	DC	0b	Indicates whether DC offset detection has occurred. 0: No DC offset fault has occurred 1: A DC offset fault has occurred
5	UV	0b	Indicates whether PV_{DD} under-voltage lockout (UVLO) has occurred. 0: No PV_{DD} UVLO has occurred 1: PV_{DD} UVLO has occurred
4	OCS	0b	Indicates whether over-current shutdown has occurred. 0: No over-current shutdown has occurred 1: Over-current shutdown has occurred
3	LF	0b	Indicates whether a load fault has occurred. 0: No load fault has occurred 1: A load fault has occurred
2	BSTF	0b	Indicates whether a boost capacitor fault has occurred. 0: No boost capacitor fault has occurred 1: A boost capacitor fault has occurred
1:0	RESERVED	-	Reserved.

FAULT_STATUS_DETECTION_2 (0x02)

The FAULT_STATUS_DETECTION_2 command indicates certain device statuses.

Command	FAULT_STATUS_DETECTION_2							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Function	PLY	MU	LD	FLT	SL	OL	GS	PS

Bits	Bit Name	Default	Description
7	PLY	0b	Indicates whether the MPQ7795 is in play mode. 0: Not in play mode 1: Currently in play mode

6	MU	0b	Indicates whether the MPQ7795 is in mute mode. 0: Not in mute mode 1: Currently in mute mode
5	LD	0b	Indicates whether the MPQ7795 is performing load diagnostics. 0: Not performing load diagnostics 1: Currently performing load diagnostics
4	FLT	0b	Indicates whether the MPQ7795 is in a fault state. 0: Not in a fault state 1: Currently in a fault state
3	SL	0b	Indicates whether a shorted load is present. 0: No shorted load is present 1: A shorted load is present
2	OL	0b	Indicates whether an open load is present. 0: No open load is present 1: An open load is present
1:0	GS	0b	Indicates whether an output short to ground is present. 0: No output short to ground is present 1: An output short to ground is present

PARAMETER_CONTROL_AND_SETTING (0x03)

The PARAMETER_CONTROL_AND_SETTING command sets certain device parameters.

Command	PARAMETER_CONTROL_AND_SETTING							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	G[1:0]		PL[2:0]				F[1:0]	

Bits	Bit Name	Default	Description
7:6	G[1:0]	00b	Sets the gain. 0h: 20dB 1h: 26dB 2h: 32dB 3h: 36dB
5:3	PL[2:0]	111b	Sets the power limit. 0h: 5V 1h: 5.9V 2h: 7V 3h: 8.4V
2	RESERVED	-	Reserved.
1:0	F[1:0]	10b	Sets the switching frequency (f_{SW}). 0h: 330kHz 1h: 384kHz 2h: 470kHz 3h: 2.2MHz

APPLICATION INFORMATION

Selecting the Input Coupling Capacitor

The input coupling capacitor transmits the AC signal from the source to the MPQ7795 while blocking the DC voltage. Choose an input coupling capacitor such that the corner frequency (f_{IN}) is below the passband frequency. The corner frequency can be calculated with Equation (3):

$$f_{IN} = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}} \quad (3)$$

The input resistor's impedance changes at different gain settings. At the same gain setting, the input impedance from part to part may shift by ±20% due to shifts in the actual resistance of the input resistors. Note that the gain variation between different parts is small.

For design purposes, the input network should be designed assuming an input impedance of 16kΩ, which is the MPQ7795's absolute minimum input impedance. At lower gains, the impedance can be as high as 90kΩ.

Power Source

The MPQ7795's power supply rejection is excellent, though power supply noise can pass to the output, so it is important to minimize power supply noise within the pass-band frequencies. Bypass the power supply with a large capacitor (typically aluminum electrolytic), along with two smaller 1μF and 1nF ceramic capacitors placed at the PVDD supply pins.

Output Short-to-Battery Protection

If the output is shorted to a voltage bus that exceeds PV_{DD}, the MOSFET's body diode turns on, and the power loss can generate excessive heat. If possible, it is recommended to place a reverse blocking diode or MOSFET in series with PVDD.

Input Signal

Considering the internal 2V biased voltage, the amplitude of INN and INP should be limited to a 2V peak. A greater value can cause distortion and damage the chip. If the external input signals (INN and INP) have another DC bias, this effect can be eliminated with a series of output capacitors.

Start-Up Sequence

The MPQ7795 has a soft-start function to eliminate the popping noise when the system starts up. Figure 9 on page 37 shows the recommended start-up sequence. Soft start takes about 100μs to set up V_{OUT}. Therefore, it is recommended to add an input signal 100μs after turning MUTE from high to low. Soft start occurs as long as the power stage starts switching, including when MUTE goes from high to low, overload or short-load recovery, or over-temperature recovery.

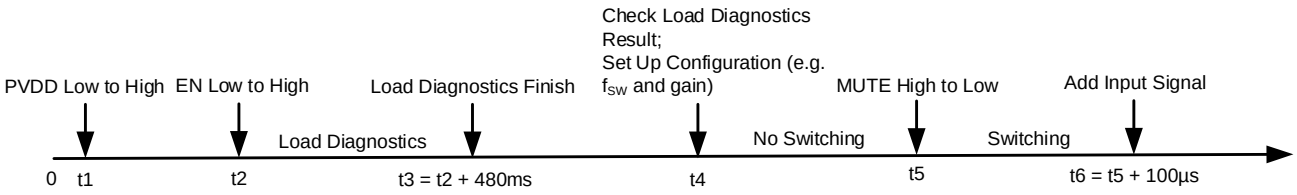


Figure 9: Recommended Start-Up Sequence

Shutdown Sequence

Generally, it is not required to wait between steps during the shutdown sequence. It is recommended to perform the load diagnostics before entering play mode again, as the open load and short load are not detected in play mode if the input signal is close to 0 (due to the synchronous switching of BTL channels). Figure 10 on page 37 shows the recommended shutdown sequence.

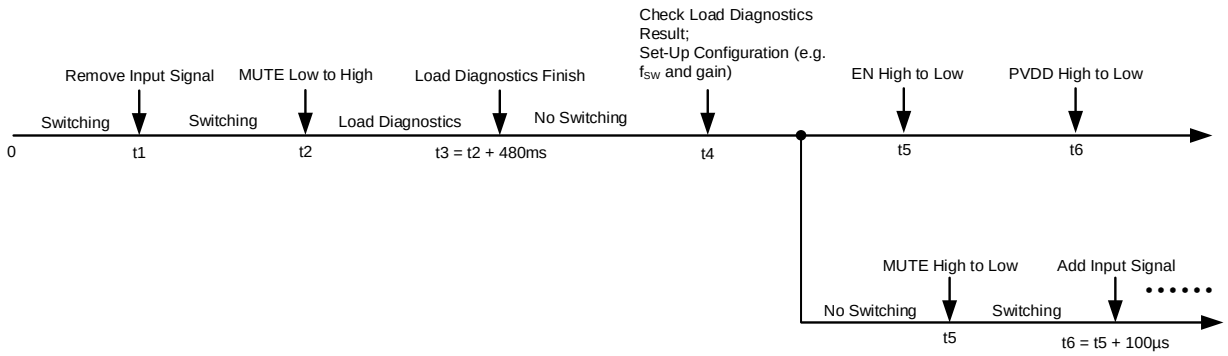


Figure 10: Recommended Shutdown Sequence

PCB Layout Guidelines (12)

An optimized PCB layout is very important for proper operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 11 on page 38 and follow the guidelines below:

1. Cut the top layer copper around IN to optimize EMI/EMC performance.
2. Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
3. Use large copper areas to minimize conduction loss and thermal stress.
4. Place the ceramic input capacitors as close to the IN and GND pins as possible to minimize high-frequency noise.
5. Route SW and BST away from sensitive analog areas.
6. Use multiple vias to connect the power planes to the inner layer.

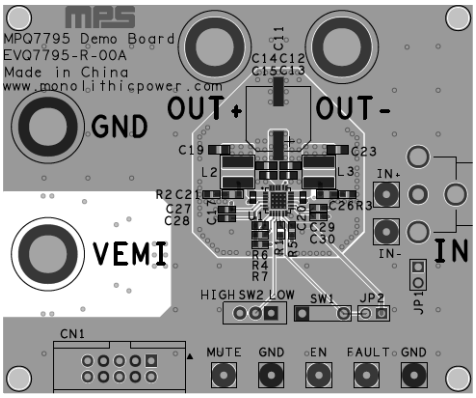
Note:

12) The recommended PCB layout is based on the circuit in Figure 13 on page 41.

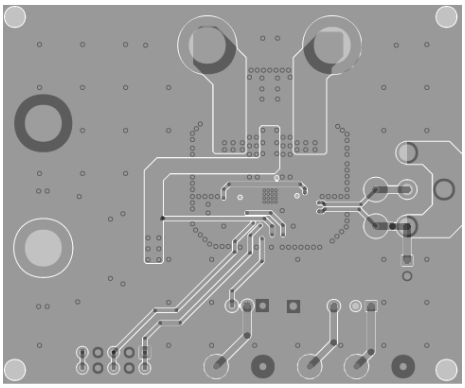
PCB Layout and EMI Considerations

The circuit layout is critical for optimal performance, low output distortion, and reduced noise. Duplicate the EVB layout for the best results. For additional layout changes, follow these guidelines below.

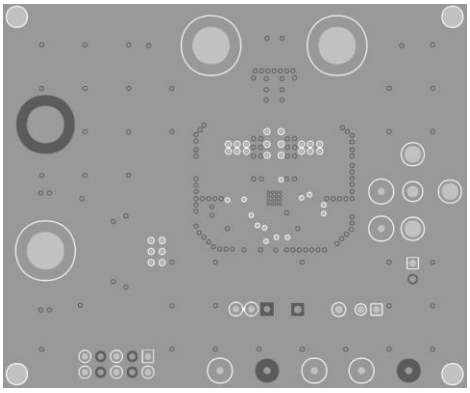
1. Place the following components as close to the MPQ7795 as possible:
   a. Bootstrap Capacitors (C_{BS}): C_{BS} supplies the gate drive's current to the internal HS-FET. Place C_{BS} as close to BST pin and SW pins as possible.
   b. Power Supply Bypass Capacitors (C_{BYP}): C_{BYP} carries the transient current for the switching power stage. To avoid overstressing the MPQ7795 and creating excessive output noise, place C_{BYP} as close to the PVDD pins as possible.
   c. Output Inductor (L_{OUT}): Place the output inductors close to MPQ7795 to minimize the size of the switching nodes SWA and SWB.
2. Minimize the size of high-current loops that carry rapidly changing currents.
3. Place the PVDD bypass capacitors are as close to the MPQ7795 as possible.
4. Route any traces carrying the switch node (SW) voltages far from any input signal traces. If the trace must run near the SW trace near the input, shield the input with a ground plane between the traces.
5. Minimize nodes that carry rapidly changing voltage, such as SW. If sensitive traces run near a trace connected to SW, place a ground shield between the traces.



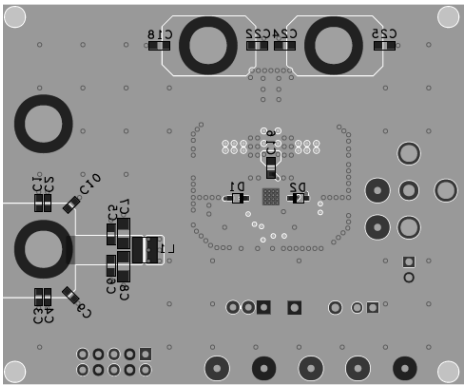
Top Layer and Top Silk



Inner Layer 2



Inner Layer 1



Bottom Layer and Bottom Silk

Figure 11: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

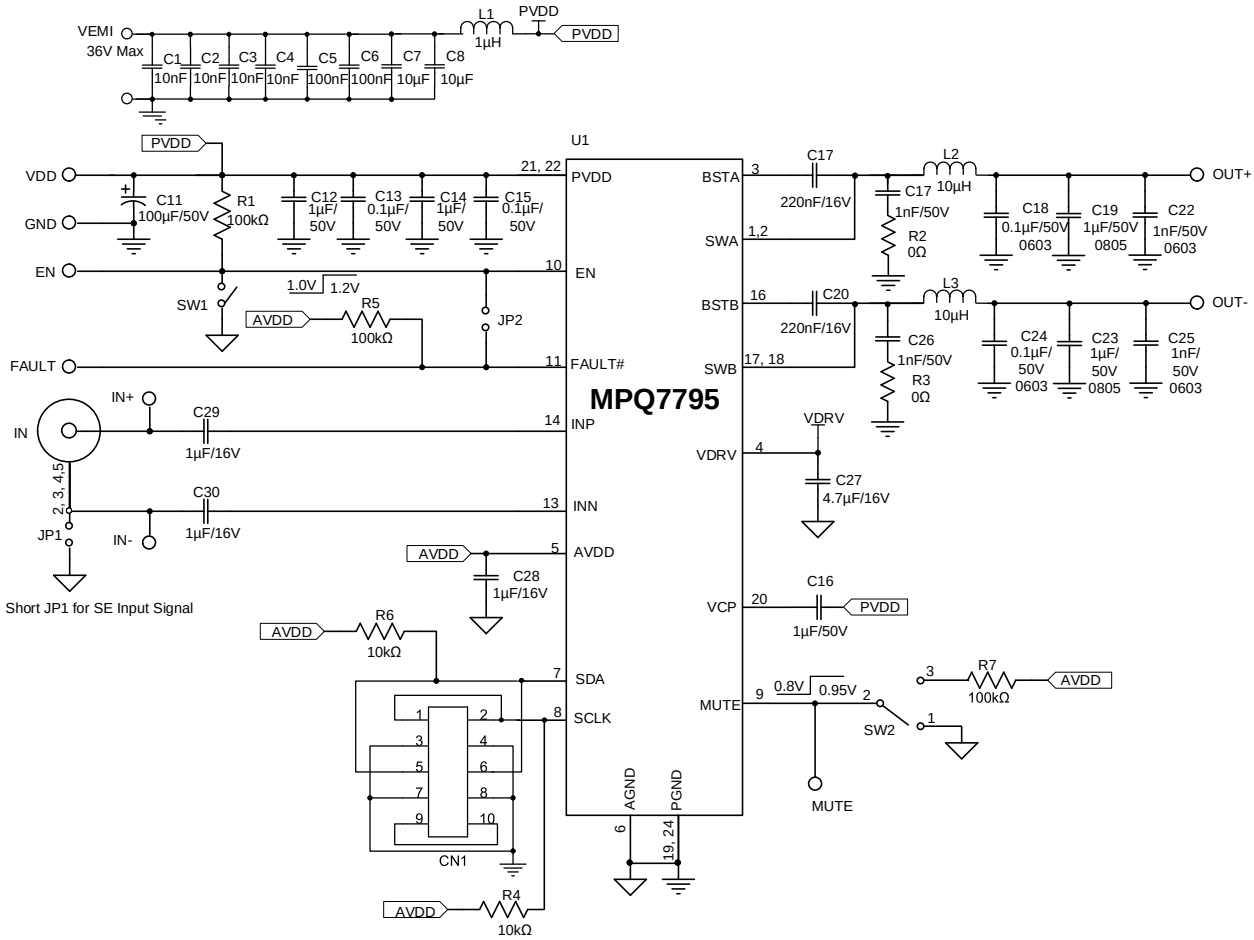


Figure 12: Typical Application Circuit with EMI Filters (470kHz Frequency)

TYPICAL APPLICATION CIRCUITS *(continued)*

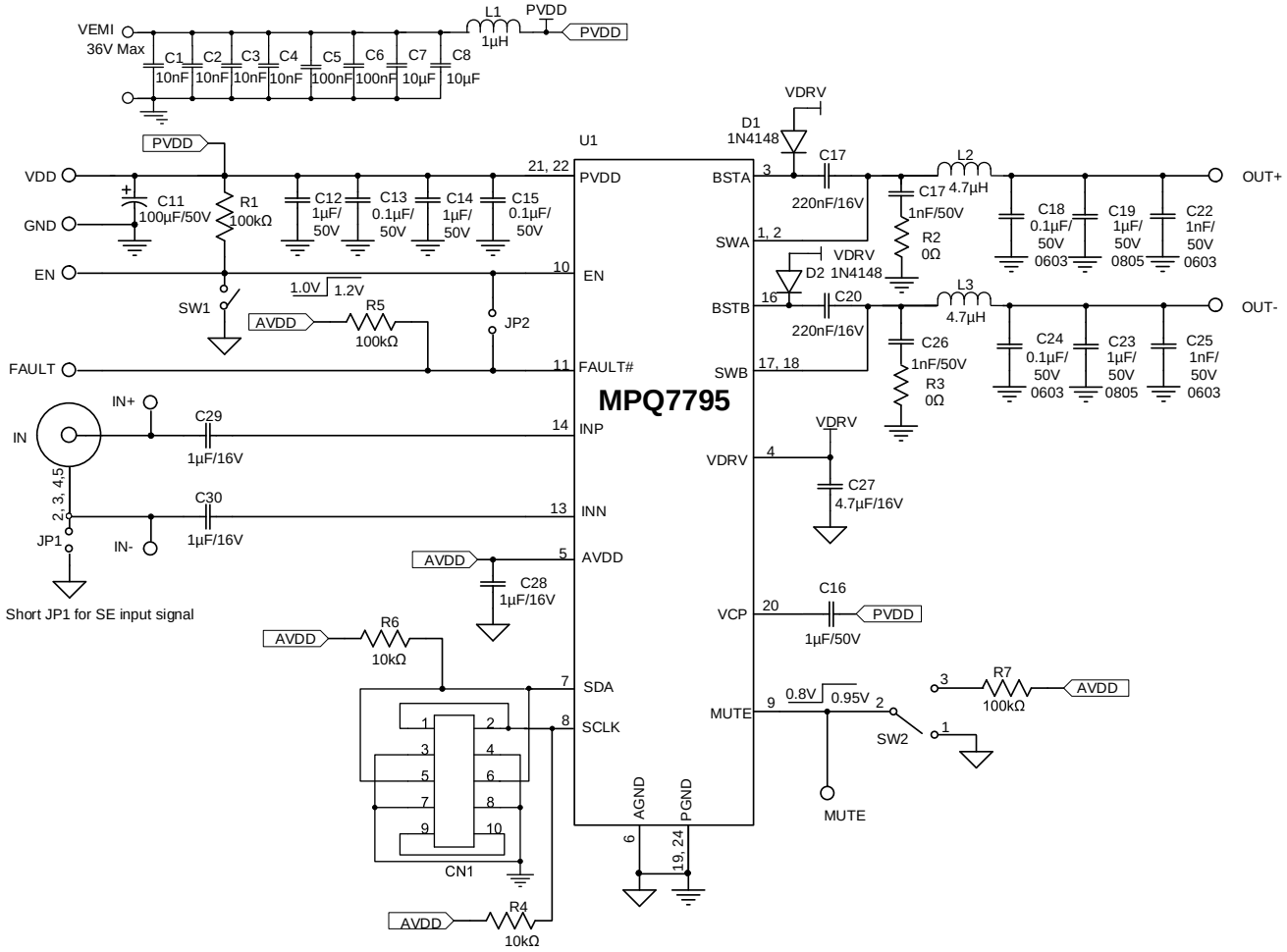
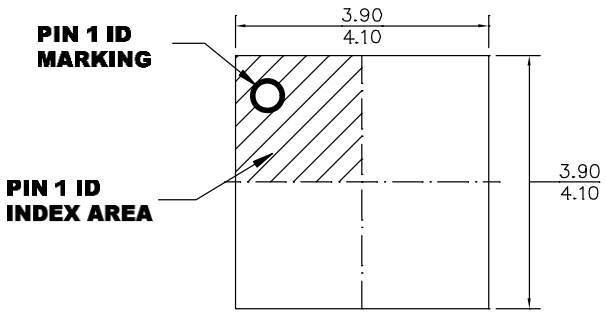


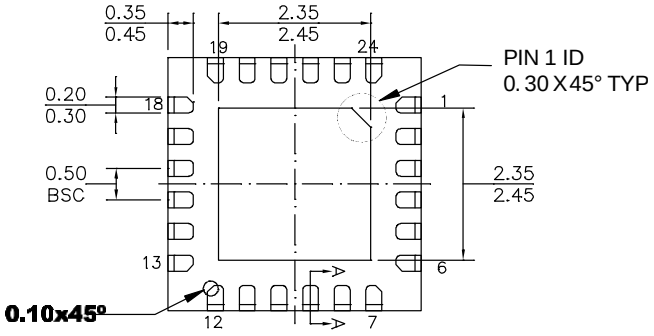
Figure 13: Typical Application Circuit with EMI Filters (2.2MHz Frequency)

PACKAGE INFORMATION

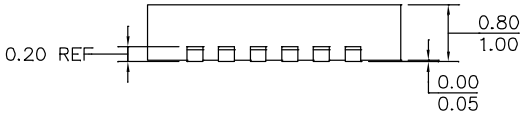
QFN-24 (4mmx4mm)



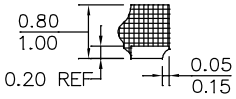
TOP VIEW



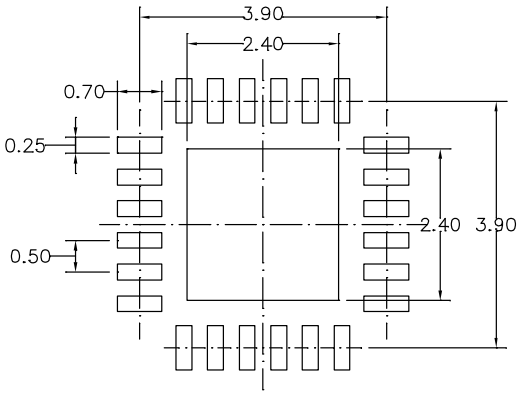
BOTTOM VIEW



SIDE VIEW



SECTION A-A

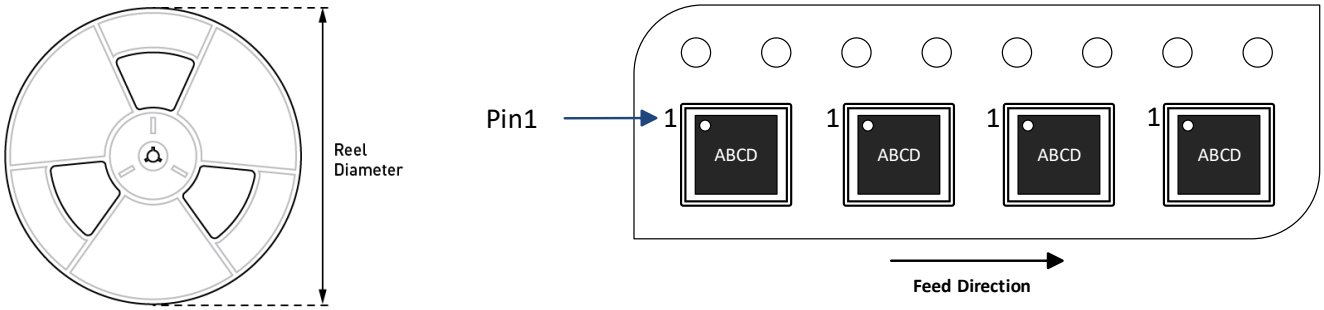


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE .
2) ALL DIMENSIONS ARE IN MILLIMETERS .
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ7795GRE-AEC1-Z	QFN-24 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/22/2023	Initial Release	-