MPQ8873

36V, 3A Continuous Output Current, Full Temperature, Four-Switch, Synchronous Buck-Boost Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ8873 is a 36V, monolithic, synchronous buck-boost DC/DC converter. Its wide 2.2V to 36V input voltage range makes the device well-suited to multi-purpose automotive and industrial applications. Proprietary constant-on-time (COT) control and a fully integrated, four-switch configuration allow the chip to flexibly change the converter topology between buck, boost, and buck-boost mode. This optimizes performance and efficiency at input voltages above, below, or equal to the output voltage. It also ensures seamless transitions between the adjacent operational regions.

The MPQ8873 is controlled via a standard I²C interface. The various parameters can be adjusted by writing the settings in the device, meaning that no hardware changes are required.

The switching frequency can be configured between 200kHz and 1MHz, or it can be synchronized between 250kHz and 1MHz via an external clock signal. In addition, the configurable frequency spread spectrum function can dither the switching frequency periodically for improved EMI performance.

Robust fault protections include input under-voltage lockout (UVLO), input over-voltage protection (OVP), cycle-by-cycle peak current limiting, output OVP, output short-circuit protection (SCP), and thermal shutdown. The built-in power good function can indicate whether the output voltage is regulated properly.

The MPQ8873 is available in a thermally enhanced QFN-34 (4mmx5mm) package.

FEATURES

- 2.2V to 36V Wide Input Voltage Range
- Up to 3A Continuous Output Current
- <25μA Shutdown Current
- 180μA Quiescent Current when V_{IN} = 12V
- Single-Channel, Four-Switch, Synchronous Buck-Boost Configuration:
  - Internal 10mΩ Buck High-Side Power MOSFET
  - Internal 25mΩ Buck Low-Side Synchronous Rectifier
  - Internal 10mΩ Boost Low-Side Power MOSFET
  - Internal 25mΩ Boost High-Side Synchronous Rectifier
- Proprietary Constant-On-Time (COT) Control for Seamless Transitions
- Internal Soft Start
- Smart Power Good Output
- Easy-to-Optimize Efficiency and EMI Performance:
  - Configurable 200kHz to 1MHz Switching Frequency
  - Synchronizable Switching Frequency from 250kHz to 1MHz
  - Switching Frequency Spread Spectrum
  - Configurable Switching Speed
- Protection Features:
  - Cycle-by-Cycle Current Limiting
  - Over-Current Protection (OCP)
  - Configurable Input Under-Voltage Lockout (UVLO)
  - Output Over-Voltage Protection (OVP)
  - Input Over-Voltage Protection (OVP)
  - Output Short-Circuit Protection (SCP)
  - Over-Temperature Shutdown

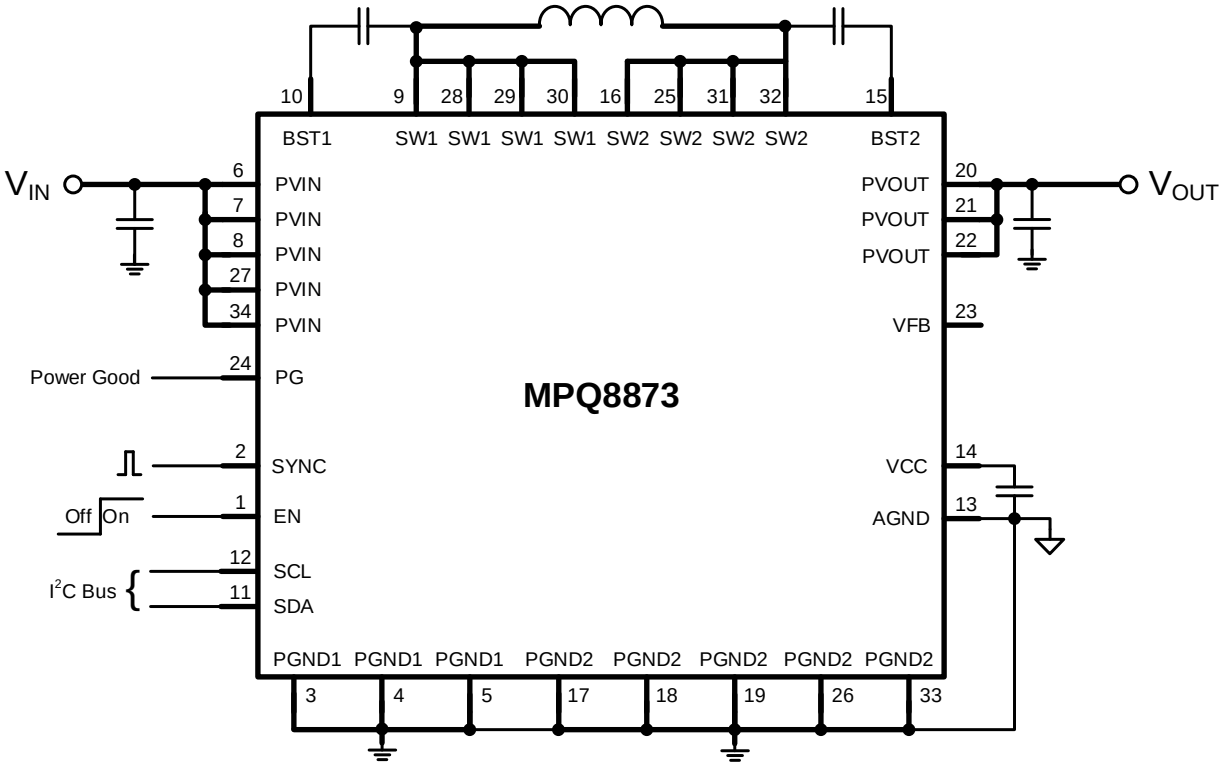
FEATURES *(continued)*

- Standard, Configurable I²C Interface:
  - Converter On/Off
  - Input Range Selection
  - Output Range from 0.5V to 30V for FCCM, 5V to 30V for DCM
  - Switching Frequency
  - Synchronized Input/Output Selection
  - Switching Slew Rate
  - Frequency Spread Spectrum Setting
  - Compensation Network
  - Ramp Compensation
  - Soft-Start Time
  - Dynamic Output Voltage Adjustment with Slew Rate Control
  - Converter Mode Transition Threshold
  - Discontinuous Conduction Mode (DCM) or Forced Continuous Conduction Mode (FCCM)
  - Constant-On-Time (COT) Control of the Boost Switch in Buck-Boost Mode
  - Input Over-Voltage Protection (OVP)
  - Output Over-Voltage Protection (OVP)
  - Cycle-by-Cycle Current Limit Threshold
  - Reverse Current Limit Threshold
  - Over-Current Protection (OCP)
  - Output Short-Circuit Protection (SCP)
  - Thermal Protection
  - Power Good (PG) Threshold
  - Junction Temperature Reading
- One-Time Programmable (OTP) Memory for Default Parameter Settings
- Available in QFN-34 (4mmx5mm) Package
- Available with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

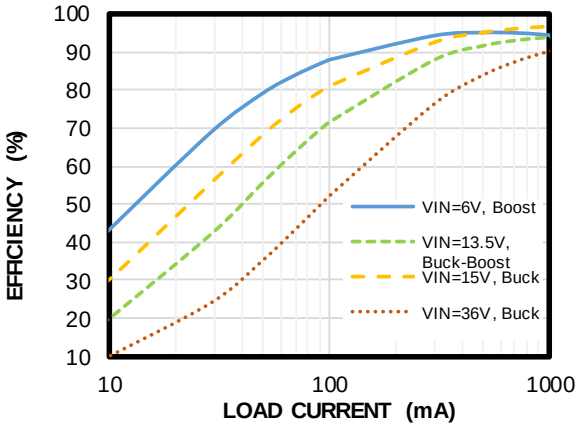
- Sensor Fusion Systems
- Camera Monitor System
- Infotainment Systems
- Automotive Applications

TYPICAL APPLICATION



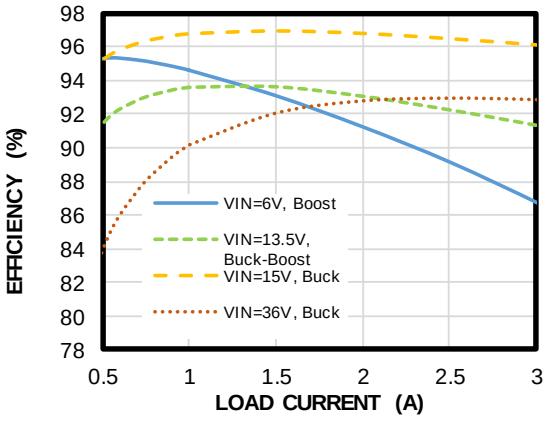
Efficiency vs. Load Current

V_{OUT} = 11.5V, f_{SW} = 450kHz, L = 10µH (23mΩ DCR), FCCM, I_{OUT} = 10mA to 1A



Efficiency vs. Load Current

V_{OUT} = 11.5V, f_{SW} = 450kHz, L = 10µH (23mΩ DCR), FCCM, I_{OUT} = 0.5A to 3A



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MPQ8873GVE-xxxx**, ****	QFN-34 (4mmx5mm)	*See Below*	1
MPQ8873GVE-xxxx-AEC1****	QFN-34 (4mmx5mm)		

* For Tape & Reel, add suffix –Z (e.g. MPQ8873GVE-xxxx–Z).

** "xxxx" is the configuration code identifier for the register settings stored in the OTP register. Each "x" can be a hexadecimal value between 0 and F. Contact an MPS FAE to create this unique number.

*** Moisture Sensitivity Level Rating

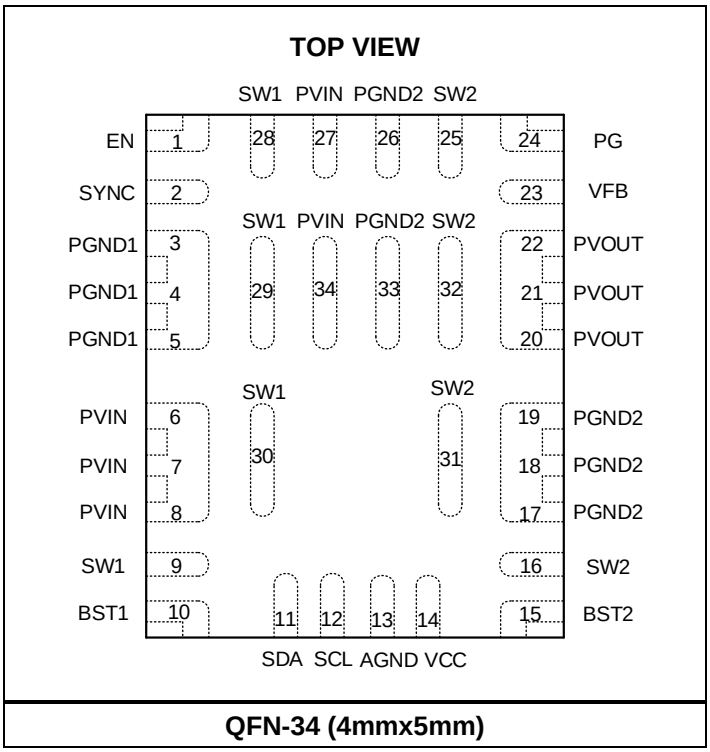
**** Wettable Flank

TOP MARKING

MPSYWW
MP8873
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP8873: Part number
LLLLLL: Lot number
E: Wettable Flank

PACKAGE REFERENCE



QFN-34 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	EN	**On/off control input and custom input UVLO setting.** The EN pin can be driven by an external logic signal to enable or disable the MPQ8873. Pull EN below the specified threshold (about 1.4V) to shut down the chip. Pull EN above the specified threshold (about 1.55V) to enable the chip. Connect a resistor divider from the input voltage (PVIN pin) to the EN pin to set a customer-accurate under-voltage lockout (UVLO) threshold for the input voltage. A 1.3µA internal pull-up current source is enabled when the EN voltage is above its high threshold (about 1.55V). A 1MΩ internal resistor pulls the EN pin low when it is floating. This means that the part is off by default when there is no external pull-up voltage.
2	SYNC	**Synchronization input or output.** The SYNC pin can be configured via the I²C to synchronization input or output mode. In synchronization input mode, the chip synchronizes its switching with the external clock connected to this pin. The external clock frequency must be 20% greater than the configured frequency set in the OTP register. In synchronization output mode, the chip outputs its clock signal to synchronize the other chip's switching clock. Float the SYNC pin if it is not used.
3, 4, 5	PGND1	**Power ground for the SW1 half-bridge.** The three PGND1 pins are connected inside the MPQ8873. These pins should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
6, 7, 8, 27, 34	PVIN	**Power input for converter.** Connect a large bulk input capacitor to PVIN for a stable power source, and connect bypass capacitors from PVIN to PGND1 to reduce noise. Inside the chip, three of the PVIN pins (pins 6, 7, and 8) are connected together. The two remaining PVIN pins (pins 27 and 34) are also connected together. Both sets of PVIN pins require a bypass capacitor. The bypass capacitors should be placed as close to the chip as possible. The input voltage (V_{IN}) is supplied by the PVIN pin.
9, 28, 29, 30	SW1	**Power switch output 1.** The four SW1 pins (pins 9, 28, 29, and 30) are connected together inside the chip. These pins should be connected to one side of the external power inductor.
10	BST1	**Bootstrap for SW1.** Place a capacitor between SW1 and BST1 to form a floating supply across the SW1 high-side MOSFET (HS-FET) driver. Generally, a 100nF ceramic capacitor is required to drive the SW1 HS-FET's gate above SW1's level.
11	SDA	**I²C bus serial data input/output.** This pin is an open-drain port. An external pull-up resistor is required to connect this pin to the I²C bus supply rail. If SDA is not used, it is recommended to connect SDA to the VCC pin through a resistor.
12	SCL	**I²C bus serial clock input.** This pin is an open-drain port. An external pull-up resistor is required to connect this pin to the I²C bus supply rail. If SCL is not used, it is recommended to connect SCL to the VCC pin through a resistor.
13	AGND	**Signal ground.** Ground for the internal logic and signal control blocks.
14	VCC	**5V internal regulator output.** VCC supplies power to the control blocks, I²C interface, and the power MOSFETs' gate driver. Bypass VCC to AGND with a 1µF to 10µF, external, low-ESR ceramic capacitor.
15	BST2	**Bootstrap for SW2.** Place a capacitor between SW2 and BST2 to form a floating supply across the SW2 HS-FET driver. A 100nF ceramic capacitor is typically required to drive the SW2 HS-FET's gate above SW2's level.
16, 25, 31, 32	SW2	**Power switch output 2.** The four SW2 pins (pins 16, 25, 31, and 32) are connected together inside the MPQ8873. These pins should be connected to one side of the external power inductor.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
17, 18, 19, 26, 33	PGND2	**Power ground for SW2 half-bridge.** Three of the PGND2 pins (pins 17, 18, and 19) are connected inside the MPQ8873. The two remaining PGND2 pins (pins 26 and 33) are also connected together. These five pins should be electrically connected to the system power ground plane through the shortest and lowest-impedance connection possible.
20, 21, 22	PVOUT	**Power output of converter.** The three PVOUT pins (pins 20, 21, and 22) are connected together inside the MPQ8873. The output capacitors should be placed as close to the chip as possible, with a short return path to the ground plane. In addition, connect a bypass capacitor from PVOUT to PGND2 to reduce noise. Place this capacitor as close to PVOUT as possible. The output voltage (V_{OUT}) is supplied by the PVOUT pin.
23	VFB	**Feedback input.** Two modes are available for the VFB pin via the I²C: 1. No connection. Leave this pin floating. 2. Tie this pin to the internal error amplifier's feedback input, which is also connected to the tap of the internal PVOUT resistor divider. To improve system stability, add an external RC compensation network from PVOUT to this pin. The external compensation network should be placed as close to the chip as possible. If the external compensation is not used, leave this pin floating.
24	PG	**Power good indicator**. This pin is an open-drain status pin that indicates if the output voltage (V_{OUT}) is within its allowable window. Connect PG to VCC with a resistor (e.g. 100kΩ). After soft start ends, the PG pin asserts low when V_{OUT} is not within the allowable window. Float this pin if it is not used.

ABSOLUTE MAXIMUM RATINGS (1)

PVIN, PVOUT (V_{IN}, V_{OUT}) ..... -0.3V to +42V
V_{SW1} ..... -0.3V to PVIN + 0.3V
V_{SW2} ..... -0.3V to PVOUT + 0.3V
V_{BST1} ..... (V_{SW1} - 0.3V) to (V_{SW1} + 5.5V)
V_{BST2} ..... (V_{SW2} - 0.3V) to (V_{SW2} + 5.5V)
All other pins ..... -0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-34 (4mmx5mm) 4W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Electrostatic Discharge (ESD) Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions

Supply voltage (V_{IN})
Normal input mode ..... 4.5V to 36V
Low input mode ..... 2.2V to 36V
Output voltage (V_{OUT}) in CCM ..... 0.5V to 30V
Output voltage (V_{OUT}) in DCM ..... 5V to 30V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***	
QFN-34 (4mmx5mm)			
JESD51-7 (3)	38	8	°C/W
EVQ8873-VE-00A (4)	31	3	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
4) Measured on EVQ8873-VE-00A, 4-layer, 9cmx9cm PCB, 2oz copper.

ELECTRICAL CHARACTERISTICS

Typical values are at V_{IN} = 12V, V_{EN} = 2V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition		Min	Typ	Max	Units
Input Supply Voltage							
Input operating range	V_{IN}	Normal input mode		4.5		36	V
		Low input mode, V_{CC} ≥ 2.5V		2.2		36	V
Input under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	Normal input mode, V_{IN} falling edge		3.2	3.6	4.2	V
		Low input mode, V_{IN} falling edge		1.8	2.0	2.2	V
Input UVLO hysteresis	$V_{IN\_UVLO\_HYS}$	Normal input mode			250		mV
		Low input mode			225		
Minimum input start-up voltage (7)	$V_{IN\_STARTUP}$	Low input mode, V_{IN} rising edge, VCC is powered from V_{IN}, I_{CC} = 10mA				3	V
Input Supply Current							
Shutdown current	I_{IN_SD}	V_{EN} = 0V, T_J = 25°C				5	µA
		V_{EN} = 0V, T_J = -40°C to +150°C				25	
Normal quiescent current	$I_{IN\_Q\_NOR}$	V_{IN} = 12V, no switching			180	500	µA
		V_{IN} = 24V, no switching			180	500	µA
Fault quiescent current	$I_{IN\_Q\_FLT}$	Fault latch condition			180	500	µA
Normal active current (6)	$I_{Q\_ACT\_NOR}$	V_{IN} = 12V, V_{OUT} = 11.5V, no load, buck-boost mode, SW1/SW2 switching	FCCM		33		mA
			DCM		0.31		
		V_{IN} = 24V, V_{OUT} = 11.5V, no load, buck mode, SW1 switching	FCCM		25		
			DCM		0.4		
VCC Regulator							
Regulator output voltage	V_{CC}	V_{IN} = 12V, V_{OUT} = 5V, I_{CC} = 1mA		4.85	5.1	5.35	V
		V_{IN} = 3V, V_{OUT} = 5V, I_{CC} = 1mA		4.65	4.85		V
VCC line regulation		V_{IN} = 5.5V to 36V, I_{CC} = 1mA		-0.5		+0.5	%
VCC load regulation		I_{CC} = 1mA to 30mA		-0.7		+0.7	%
Dropout voltage	VCC_{DRV}	V_{IN} = 2.7V, V_{OUT} = 2.5V, I_{CC} = 5mA			100	220	mV
		V_{OUT} = 2.7V, V_{IN} = 2.5V, I_{CC} = 5mA			80	500	mV
Short-circuit current limitation	I_{CC_MAX}	V_{CC} = 0V		40	60	100	mA

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at V_{IN} = 12V, V_{EN} = 2V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Regulator						
VCC UVLO threshold	VCC_{UVLO}	Normal input mode, VCC falling edge	3.2	3.4	3.6	V
		Low input mode, VCC falling edge	2.1	2.25	2.4	V
VCC UVLO hysteresis	VCC_{UVLO_HYS}			350		mV
Oscillator						
Switching frequency range (5)	f_{SW}		200		1000	kHz
Frequency PLL accuracy (6)		f_{SW} = default value in OTP register 0x03h, bits[5:0]	-15		+15	%
Minimum on time (7)	t_{ON_MIN}			100		ns
Minimum off time (7)	t_{OFF_MIN}	Buck mode		90		ns
		Boost mode		180		ns
Synchronization frequency range	f_{SYNC}	Sync clock input mode	250		1000	kHz
SYNC input logic high threshold	$V_{SYNC\_IN\_H}$	V_{SYNC} rising edge	1.4			V
SYNC input logic low threshold	$V_{SYNC\_IN\_L}$	V_{SYNC} falling edge			0.5	V
SYNC input minimal logic high pulse width	$t_{SYNC\_IN\_PW\_MIN}$		200			ns
SYNC output logic high (7)	$V_{SYNC\_OUT\_H}$			V_{CC}		
SYNC output logic low (7)	$V_{SYNC\_OUT\_L}$				0.3	V
SYNC output duty cycle	D_{SYNC_OUT}			50		%
Frequency Spread Spectrum						
Spread spectrum modulation frequency spread range (5)	f_{FSS}		±3%		±30%	f_{SW}
Spread spectrum modulation frequency range (5)	f_{FSSM}		0.25		8	kHz
Enable						
Logic enable threshold	V_{EN_LOGIC}		0.5	0.85	1.15	V
System enable threshold	V_{EN_ON}	V_{EN} rising edge	1.4	1.55	1.7	V
Pull-up hysteresis current	I_{EN_HYS}	After converter works		1.3		µA
Hysteresis voltage	V_{EN_SYS}			150		mV
Bootstrap						
Biased voltage for the high-side driver (Q1/Q3)	V_{BST1} - V_{SW1}	V_{CC} = 5V	4.3	4.7	5.1	V
	V_{BST2} - V_{SW2}					
	V_{BST1} - V_{SW1}	Low input mode, V_{CC} = 2.55V	1.6			
	V_{BST2} - V_{SW2}		1.4			
UVLO of BST	$V_{BST1/2\_UVLO}$	$V_{BST1/2}$ - $V_{SW1/2}$ falling edge	1.1	1.6	2.1	V
UVLO hysteretic of BST	$V_{BST1/2\_UVLO\_HYS}$			80		mV

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at V_{IN} = 12V, V_{EN} = 2V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power Switches						
Main switch (Q1/Q3) on resistance	$R_{DS(ON)\_MAIN}$	V_{CC} = 5V, T_J = 25°C		10	20	mΩ
		V_{CC} = 5V, T_J = -40°C to +150°C		10	25	
		Low input mode, V_{CC} = 2.55V, T_J = 25°C		15	20	mΩ
		Low input mode, V_{CC} = 2.55V, T_J = -40°C to +150°C		15	30	
Synchronous rectifier switch (Q2/Q4) on resistance	$R_{DS(ON)\_SR}$	V_{CC} = 5V, T_J = 25°C		25	40	mΩ
		V_{CC} = 5V, T_J = -40°C to +150°C		25	50	
		Low input mode, V_{CC} = 2.55V, T_J = 25°C		35	45	mΩ
		Low input mode, V_{CC} = 2.55V, T_J = -40°C to +150°C		35	60	
Switch leakage current	I_{SW_LKG}	$V_{SW1/SW2}$ = 36V, T_J = 25°C			1	µA
		$V_{SW1/SW2}$ = 36V, T_J = -40°C to +150°C			20	
Peak current limit range (5)	I_{LIMIT_PK}	I_L rising edge	2		7	A
Peak current limit accuracy (6)		I_{LIMT_PK} = 7A	7			A
Reverse current limit range (5)	I_{LIMIT_RV}	FCCM, I_L falling edge	-2.5		-4.7	A
Reverse current limit accuracy		I_{LIMT_RV} = -2.5A	-1.8	-2.5	-3.5	A
		I_{LIMT_RV} = -4.7A	-3.8	-4.7	-6.5	
Valley current limit range (5)	I_{LIMIT_VL}	OC fault triggers	1		6	A
Valley current limit accuracy (6)		I_{LIMT_VL} = 6A, I_{LIMT_RV} = -2.5A	4.64	6	7.36	A
		I_{LIMT_VL} = 6A, I_{LIMT_RV} = -4.7A	3.6	5	6.4	
Zero-current detection (ZCD) threshold	I_{ZCD}	DCM, I_L falling edge		100		mA
Switching slew rate range (5)	SR_R	$V_{SW1/2}$ rising edge	1		2	V/ns
	SR_F	$V_{SW1/2}$ falling edge	1		2	V/ns

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at V_{IN} = 12V, V_{EN} = 2V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Output Voltage Regulation						
Output voltage range	V_{OUT}		0.5		30	V
PVOUT leakage current	I_{OUT_LKG}	V_{IN} = V_{EN} = 0V, V_{OUT} = 12V		20	60	µA
Reference voltage range (5)	V_{REF}	Normal input mode	0.5		2.0	V
		Low-input mode	0.5		1.2	V
Reference voltage accuracy		V_{REF} = 0.5V, 1.2V, 1.5V, or 2V; T_J = 25°C	-2		+2	%
		V_{REF} = 0.5V, 1.2V, 1.5V, or 2V; T_J = -40°C to +125°C (7)	-2.5		+2.5	
		V_{REF} = 0.5V, 1.2V, 1.5V, or 2V; T_J = -40°C to +150°C	-3		+3	
Output divider ratio range (5)	V_{REF} / V_{OUT}		1/30		1	
Dynamic adjustment step interval range (5)	t_{DV_STEP}		20		166.67	µs
Dynamic adjustment step interval accuracy (6)		t_{DV_STEP} = default value in OTP register 0x01h, bits[4:3]	-15		+15	%
VFB current	I_{FB}	V_{FB} = 2V	-100		+100	nA

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at V_{IN} = 12V, V_{EN} = 2V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Buck-Boost Converter						
Boost out threshold range (5)	$V_{IN\_BST\_OUT}$	V_{IN} rising edge	0.7		0.9	V_{OUT}
Boost out threshold accuracy		V_{OUT} = 12V	-0.04		+0.04	V_{OUT}
Boost transition hysteresis range (5)	$V_{IN\_BST\_HYS}$		0.05		0.125	V_{OUT}
Boost transition hysteresis accuracy		V_{OUT} = 12V	-0.03		+0.03	V_{OUT}
Buck in threshold range (5)	$V_{IN\_BK\_IN}$	V_{IN} rising edge	1.1		1.3	V_{OUT}
Buck in threshold accuracy		V_{OUT} = 12V	-0.04		+0.04	V_{OUT}
Buck transition hysteresis range (5)	$V_{IN\_BK\_HYS}$		0.05		0.125	V_{OUT}
Buck transition hysteresis accuracy		V_{OUT} = 12V	-0.03		+0.03	V_{OUT}
Constant-on-time (COT) range of the boost switch in buck-boost mode (5) (7)	t_{BST_ON}		0.2		0.5	t_{SW}
Input Over-Voltage Protection (OVP)						
Input OVP threshold range (5)	V_{IN_OVP}	V_{IN} rising edge	11		33	V
Input OVP threshold accuracy			-10		+10	%
Input OVP hysteresis range (5)	$V_{IN\_OVP\_HYS}$		0.03		0.05	V_{IN}
Input OVP hysteresis accuracy			-0.02		+0.02	V_{IN}
Output OVP						
Output OVP threshold range (5)	V_{OUT_OVP}	V_{OUT} rising edge	1.1		1.3	V_{REF}
Output OVP threshold accuracy			-0.05		+0.05	V_{REF}
Output OVP recovery threshold range (5)	$V_{OUT\_OVP\_REC}$	V_{OUT} falling edge	1		1.05	V_{REF}
Output OVP recovery threshold accuracy			-0.04		+0.04	V_{REF}
Over-Current Protection (OCP)						
OC fault activation delay time range (5) (7)	t_{OCP_DELAY}	Consecutive switching count when COMP level is too high	32		256	t_{SW}
Output Under-Voltage Protection (UVP)						
Output under-voltage (UV) threshold range (5)	V_{OUT_UVP}	V_{OUT} falling edge	0.5		0.75	V_{REF}
Output UV threshold accuracy			-0.04		+0.04	V_{REF}
Output UV fault activation delay time (5) (7)	t_{UVP_DELAY}	Consecutive switching count when V_{OUT} < V_{OUT_UVP}	2		16	t_{SW}

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at V_{IN} = 12V, V_{EN} = 2V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Thermal Shutdown						
Thermal shutdown threshold range (5) (7)	T_{SD}	T_J rising	150		170	°C
Thermal shutdown hysteresis range (5) (7)	T_{HYS}		25		75	°C
Fault Recovery Timer						
Auto-recovery delay time range (5) (7)	t_{FLT_REC}	Fault recovery mode is activated, except T_{SD}	2		16	ms
Fault reset delay timer (7)	t_{FLT_RST}	After soft start ends during a recovery cycle, consecutive switching count when no fault is detected		30		µs
Power Good Indicator (Open-Drain)						
Power good (PG) high limit range (5)	$V_{OUT\_PG\_H}$	V_{OUT} rising edge	1.12		1.17	V_{REF}
PG high limit accuracy			-0.04		+0.04	V_{REF}
PG high limit hysteresis range (5)	$V_{OUT\_PG\_H\_HYS}$		0.04		0.06	V_{REF}
PG high limit hysteresis accuracy			-0.02		+0.02	V_{REF}
PG low limit range (5)	$V_{OUT\_PG\_L}$	V_{OUT} falling edge	0.85		0.9	V_{REF}
PG low limit accuracy (6)			0.86	0.9	0.94	V_{REF}
PG low limit hysteresis range (5)	$V_{OUT\_PG\_L\_HYS}$		0.04		0.06	V_{REF}
PG low limit hysteresis accuracy			-0.02		+0.02	V_{REF}
PG output low voltage	V_{PG_L}	I_{PG_SINK} = 200µA			0.4	V
PG leakage current	I_{PG_LKG}	V_{PG} = 5V			1	µA
PG flip-flop delay timer	t_{PG_DELAY}	After soft start ends, consecutive switching count when V_{OUT} is in or not in regulation		30		µs

Notes:

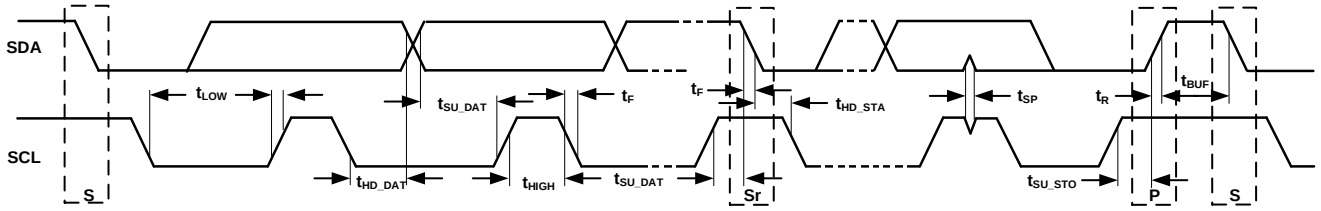
5) Configurable via the I²C interface.
6) Not tested across the entire range, and only guaranteed for the specified default option configured in the OTP register.
7) Guaranteed by design and characterization. Not tested in production.

I²C INTERFACE ELECTRICAL CHARACTERISTICS

Typical values are at V_{IN} = 12V, V_{EN} = 2V, T_J = 25°C. Minimum and maximum values are at V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, guaranteed by characterization. All voltages with respect to ground, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
SCL/SDA input logic low	V_{IL}		0		0.8	V
SCL/SDA input logic high	V_{IH}		1.5			V
SCL/SDA output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3		1.67	µs
Data set-up time	t_{SU_DAT}		100			ns
Data hold time	t_{HD_DAT}		0.25		0.9	µs
Set-up time for repeated start	t_{SU_STA}		0.6			µs
Hold time for start	t_{HD_STA}		0.6			µs
Bus free time between a start and stop condition	t_{BUF}		1.3			µs
Set-up time for stop condition	t_{SU_STO}		0.6			µs
SCL/SDA rise time	t_R		20 + 0.1 x C_B		300	ns
SCL/SDA fall time	t_F		20 + 0.1 x C_B		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

I²C-COMPATIBLE INTERFACE TIMING DIAGRAM



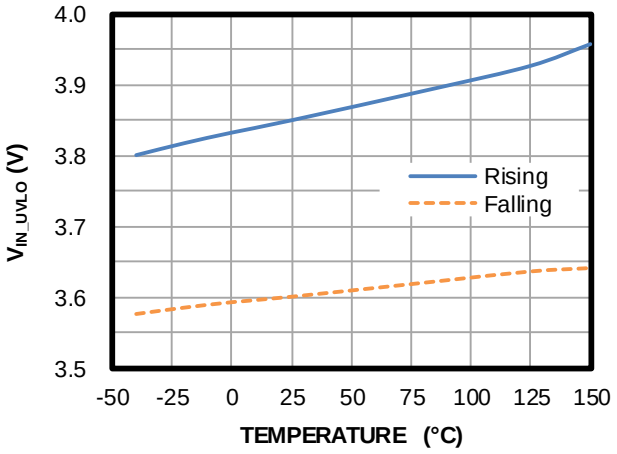
S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

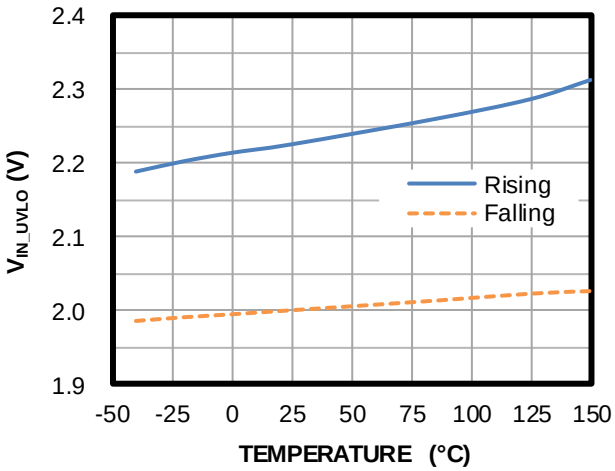
V_{IN} UVLO Threshold vs. Temperature

Normal input mode

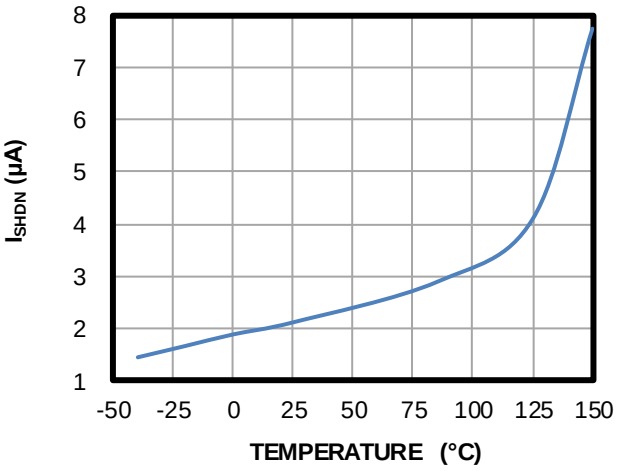


V_{IN} UVLO Threshold vs. Temperature

Low input mode

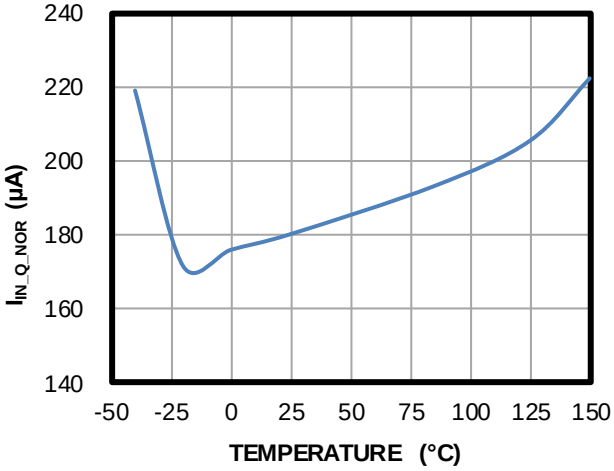


Shutdown Current vs. Temperature



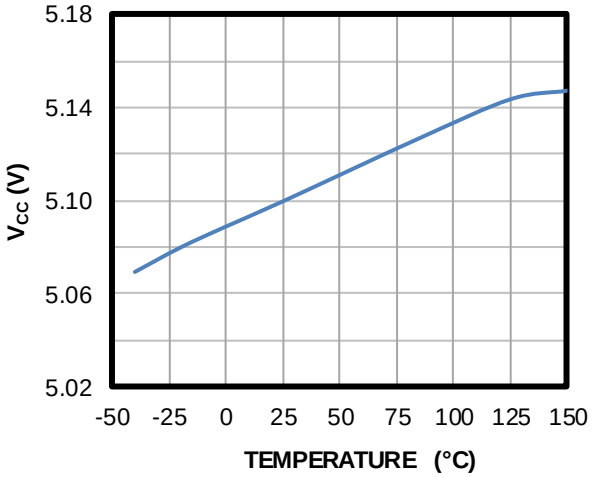
Quiescent Current vs. Temperature

No switching



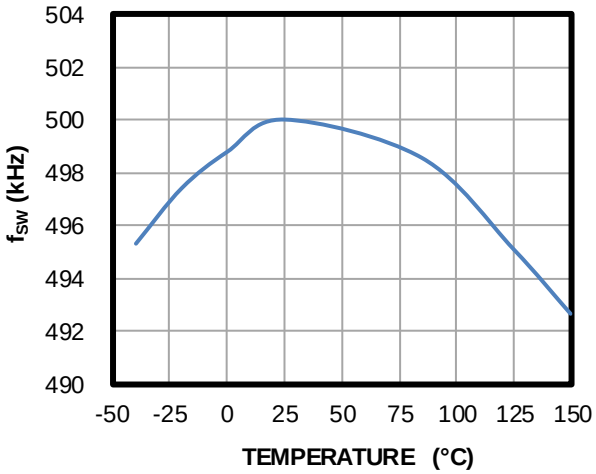
VCC Voltage vs. Temperature

V_{IN} = 12V



Frequency vs. Temperature

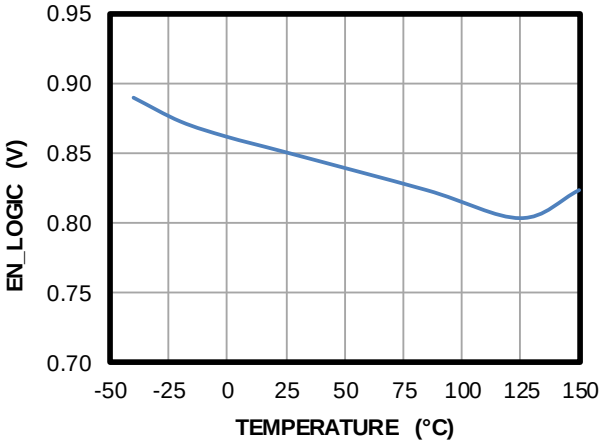
f_{SW} = 500kHz (Reg0x03, bits[5:0] = 0Ah)



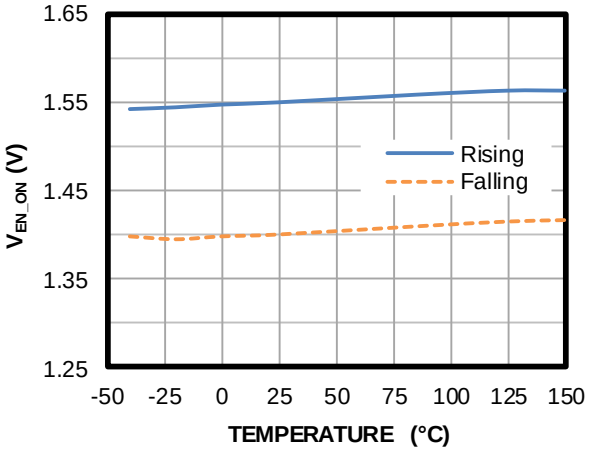
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

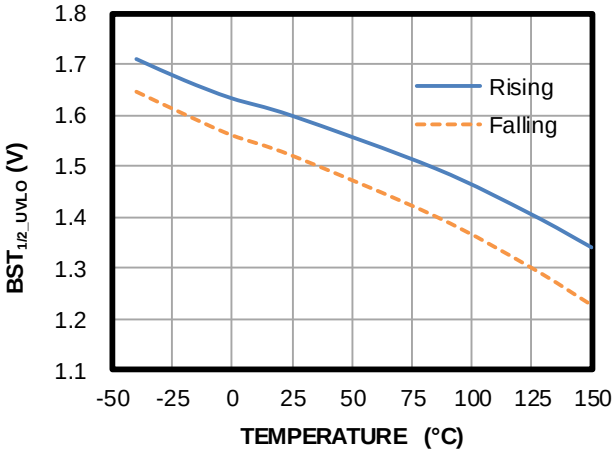
EN_LOGIC Rising vs. Temperature



System EN Threshold vs. Temperature

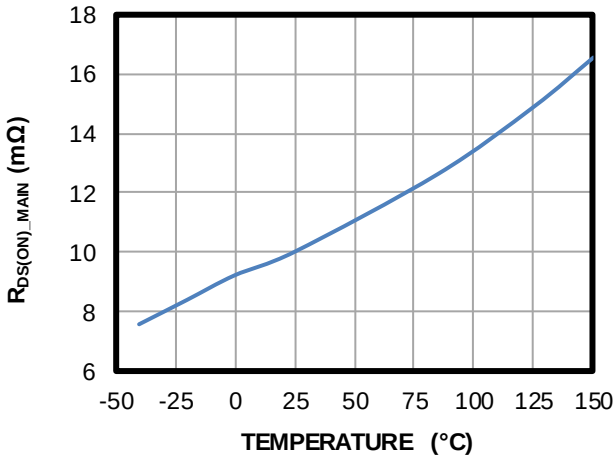


BST UVLO vs. Temperature



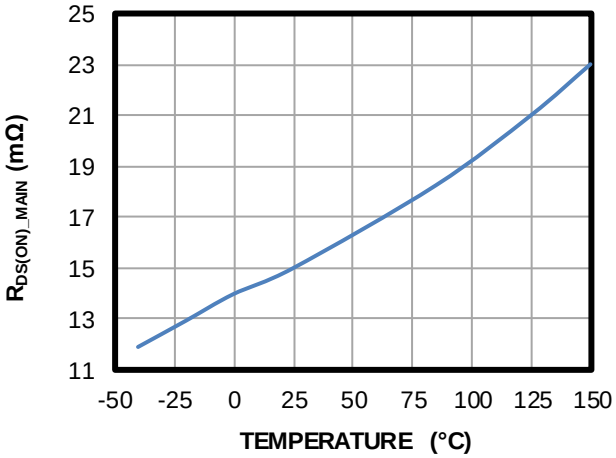
Main Switch (Q1/Q3) $R_{DS(ON)}$ vs. Temperature

V_{CC} = 5V



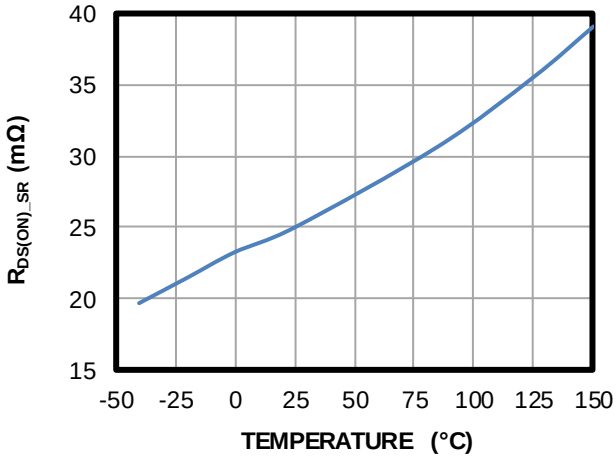
Main Switch (Q1/Q3) $R_{DS(ON)}$ vs. Temperature

V_{CC} = 2.55V



Synchronous Rectifier Switch (Q2/Q4) $R_{DS(ON)}$ vs. Temperature

V_{CC} = 5V

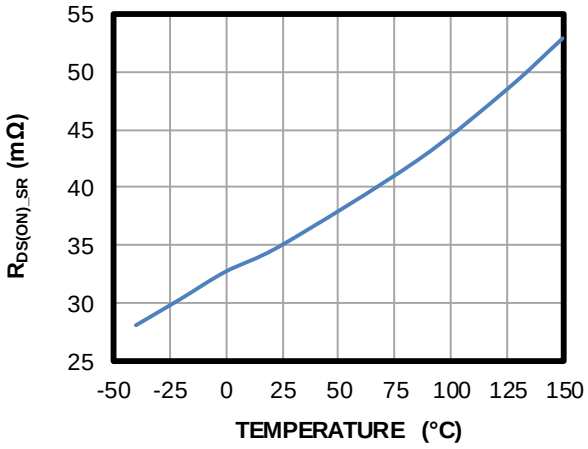


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

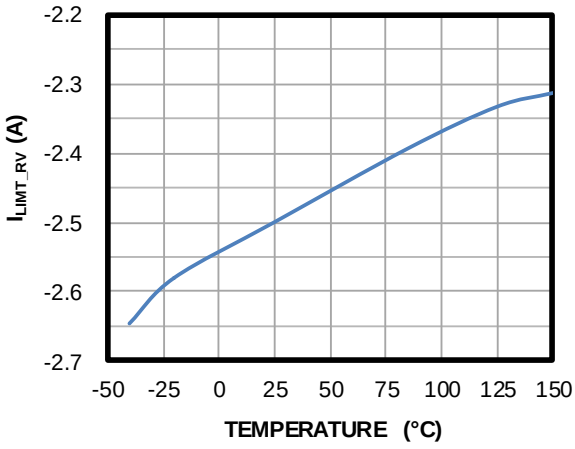
Synchronous Rectifier Switch (Q2/Q4) $R_{DS(ON)}$ vs. Temperature

V_{CC} = 2.55V



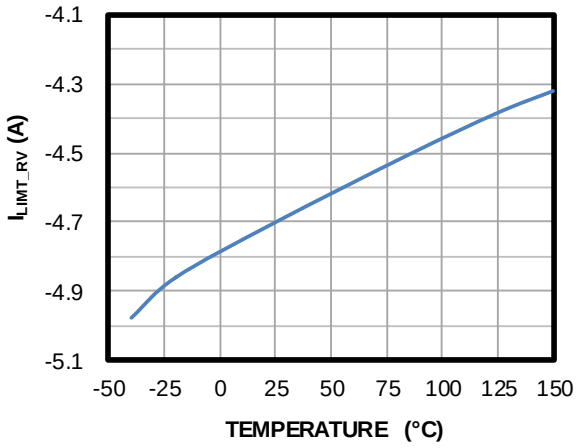
Reverse Current Limit vs. Temperature

I_{LIMT_RV} = -2.5A



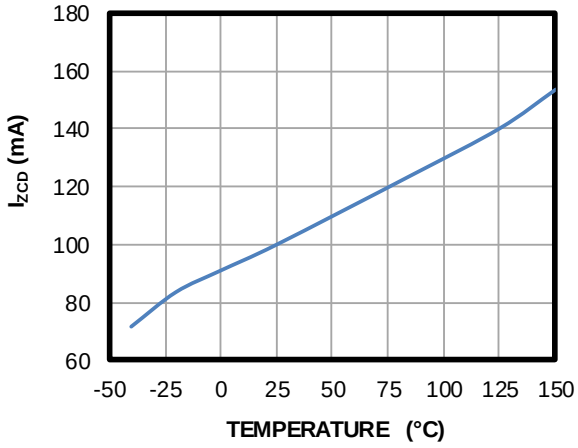
Reverse Current Limit vs. Temperature

I_{LIMT_RV} = -4.7A



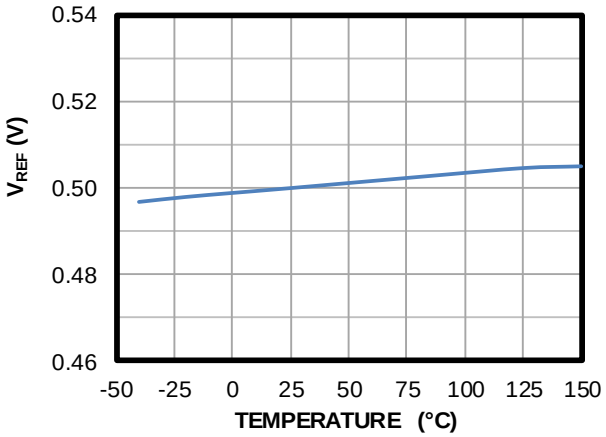
ZCD Current vs. Temperature

DCM



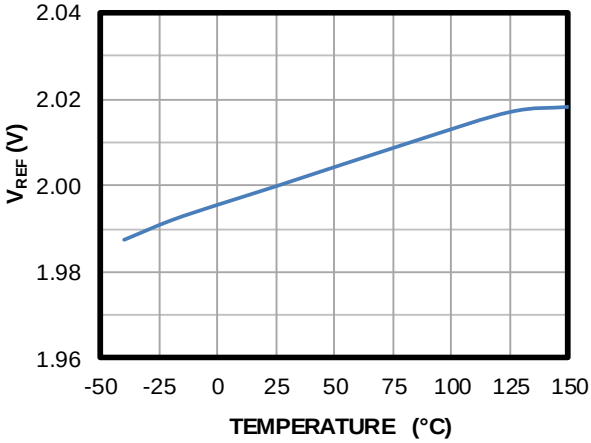
Reference Voltage vs. Temperature

V_{REF} = 0.5V



Reference Voltage vs. Temperature

V_{REF} = 2V

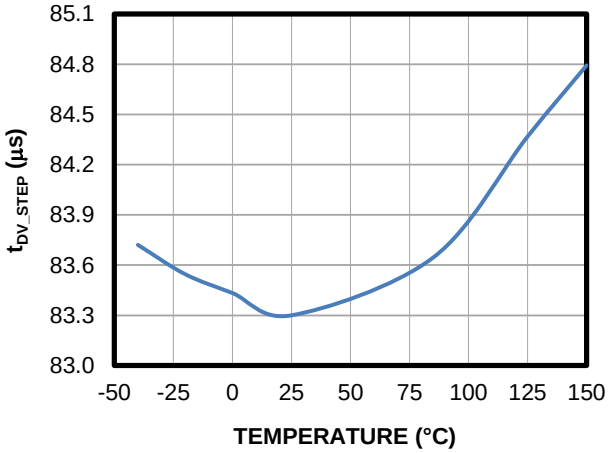


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

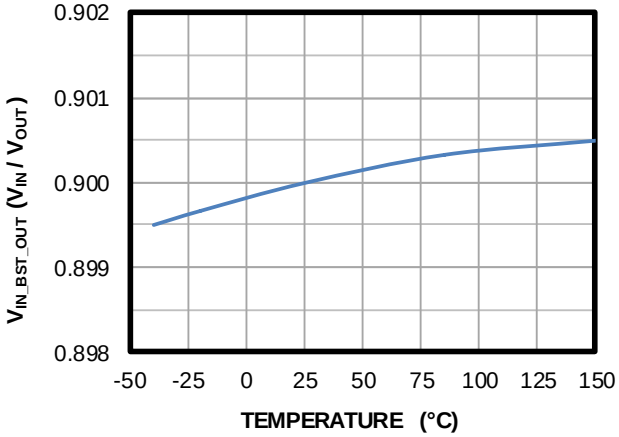
Dynamic Adjustment Step Interval vs. Temperature

t_{DV_STEP} = 83.3µs



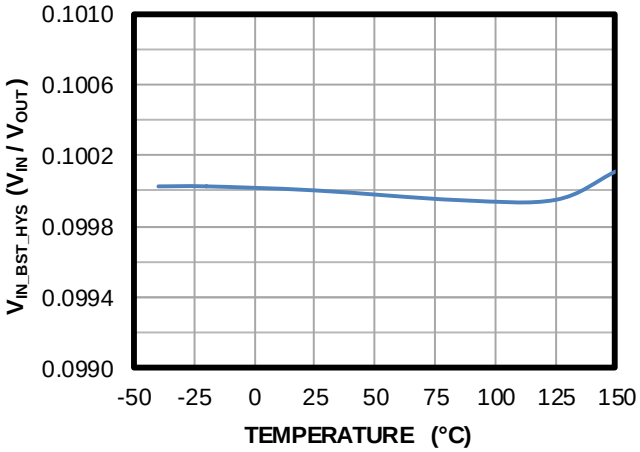
Boost Out Threshold vs. Temperature

$V_{IN\_BST\_OUT}$ = 90% $V_{IN\_BST\_HYS}$ = 7.5%



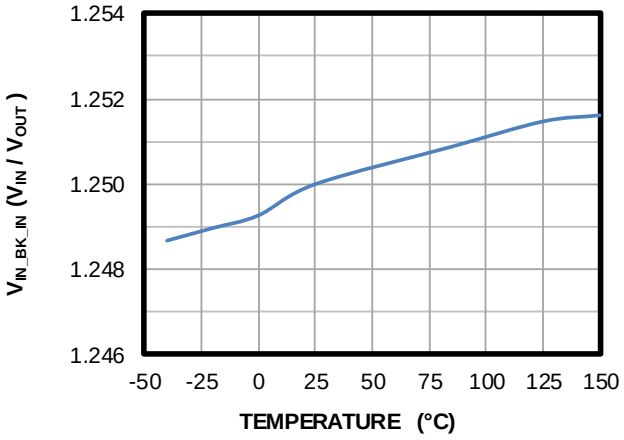
Boost Transition Hysteresis vs. Temperature

$V_{IN\_BST\_HYS}$ = 10%



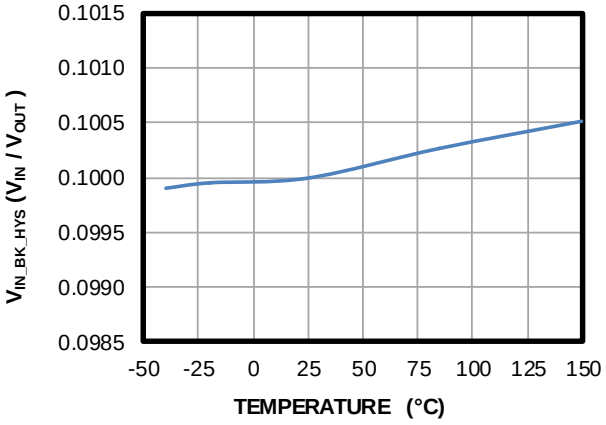
Buck In Threshold vs. Temperature

$V_{IN\_BK\_IN}$ / V_{OUT} = 125%, $V_{IN\_BK\_HYS}$ / V_{OUT} = 10%



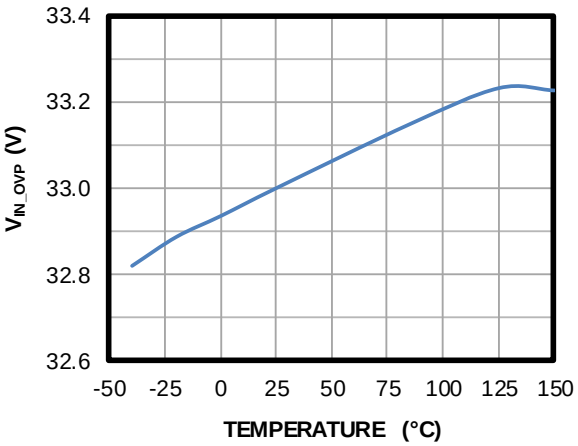
Buck Transition Hysteresis vs. Temperature

$V_{IN\_BK\_HYS}$ / V_{OUT} = 10%



Input OVP Threshold vs. Temperature

V_{IN_OVP} = 33V

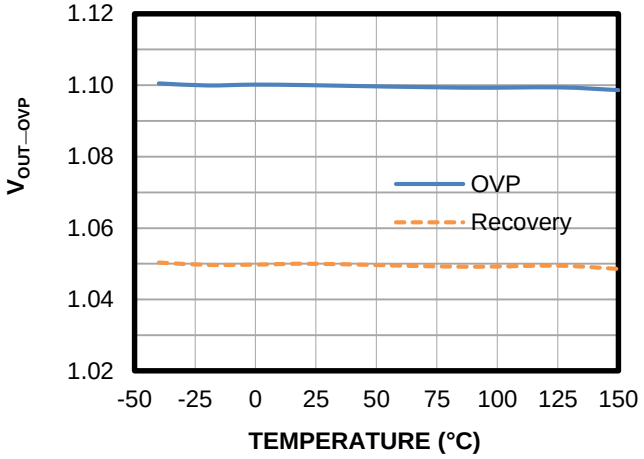


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

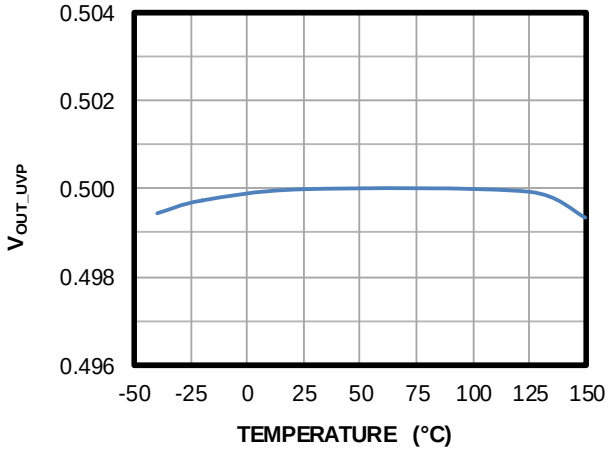
Output OVP Threshold vs. Temperature

V_{OUT_OVP} = 1.1, $V_{OUT\_OVP\_REC}$ = 1.05



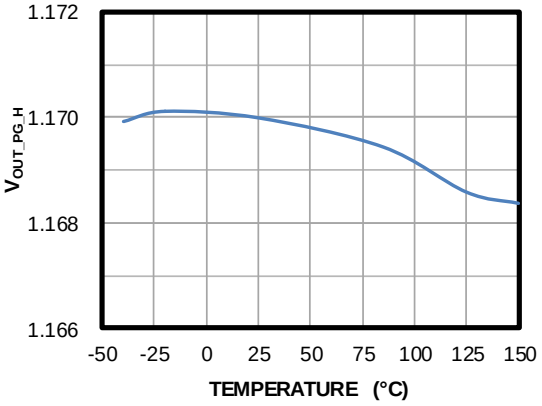
Output UVP Threshold vs. Temperature

V_{OUT_UVP} = 0.5



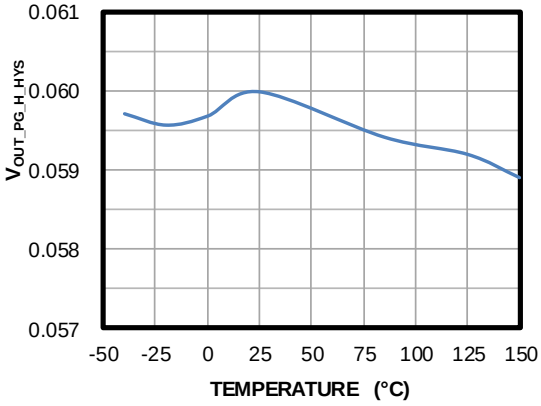
PG High Limit Threshold vs. Temperature

$V_{OUT\_PG\_H}$ = 1.17



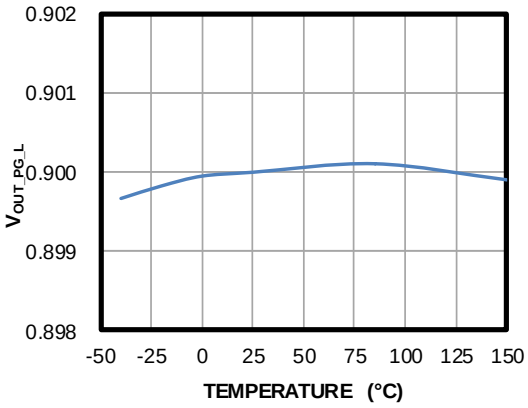
PG High Limit Hysteresis vs. Temperature

$V_{OUT\_PG\_H\_HYS}$ = 0.06



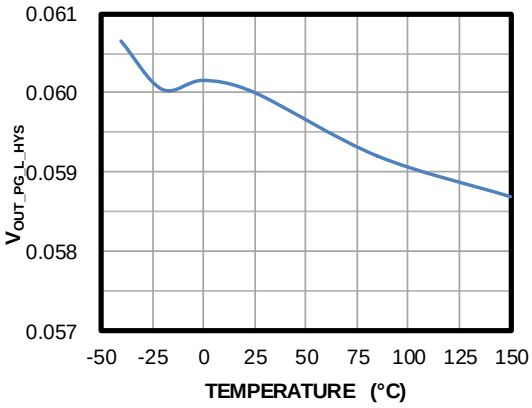
PG Low Limit Threshold vs. Temperature

$V_{OUT\_PG\_L}$ = 0.9



PG Low Limit Hysteresis vs. Temperature

$V_{OUT\_PG\_L\_HYS}$ = 0.06

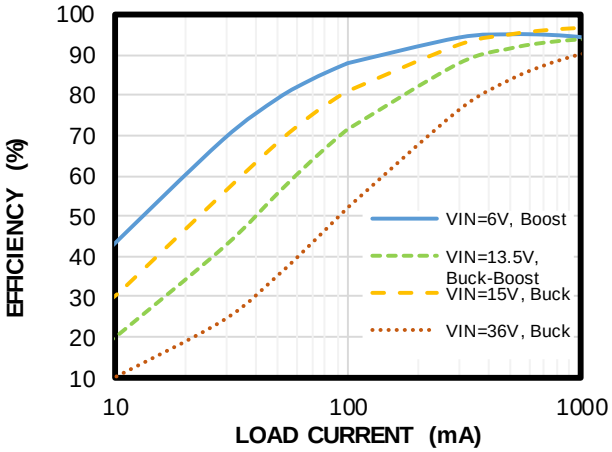


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 13.5V, V_{OUT} = 11.5V, L = 10µH, C_{OUT} = 40µF, f_{SW} = 450kHz, FCCM, T_A = 25°C, unless otherwise noted.

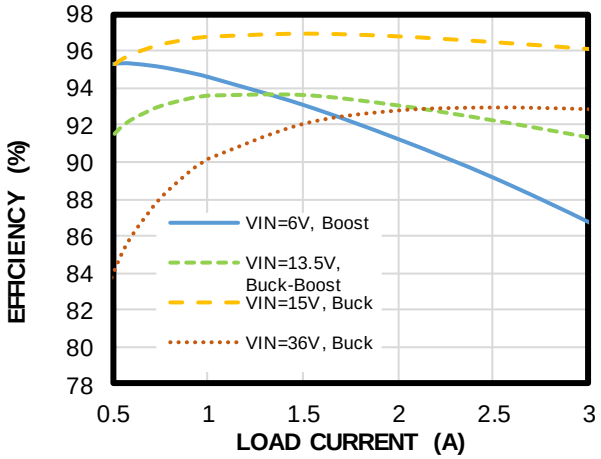
Efficiency vs. Load Current

V_{OUT} = 11.5V, FCCM, I_{OUT} = 10mA to 1A



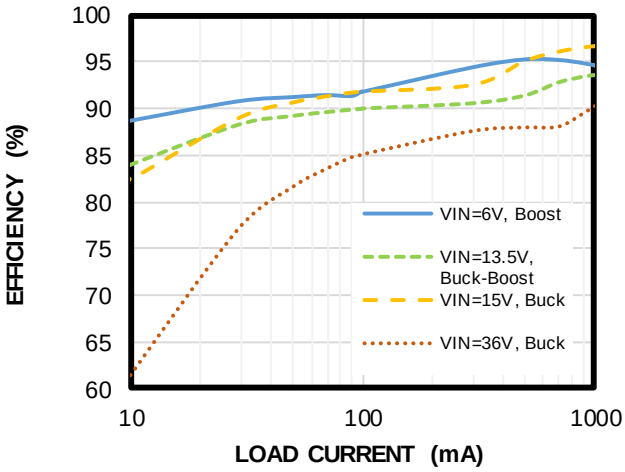
Efficiency vs. Load Current

V_{OUT} = 11.5V, FCCM, I_{OUT} = 0.5A to 3A



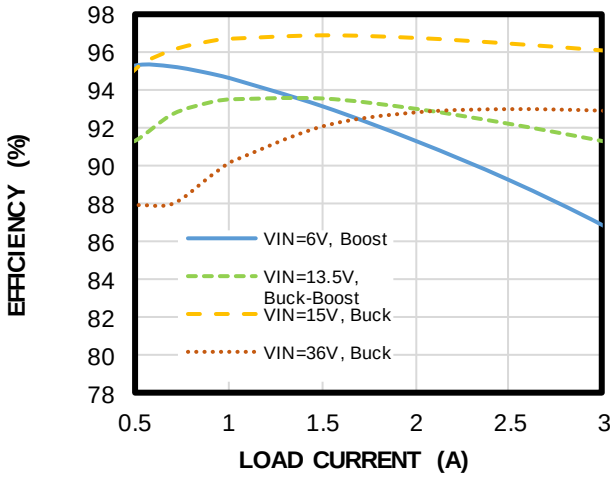
Efficiency vs. Load Current

V_{OUT} = 11.5V, DCM, I_{OUT} = 10mA to 1A



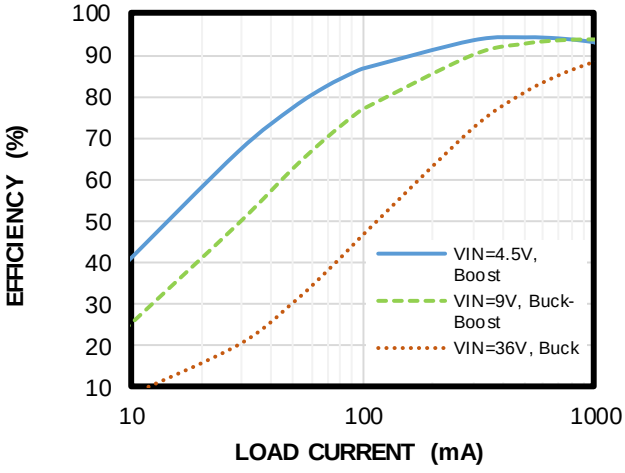
Efficiency vs. Load Current

V_{OUT} = 11.5V, DCM, I_{OUT} = 0.5A to 3A



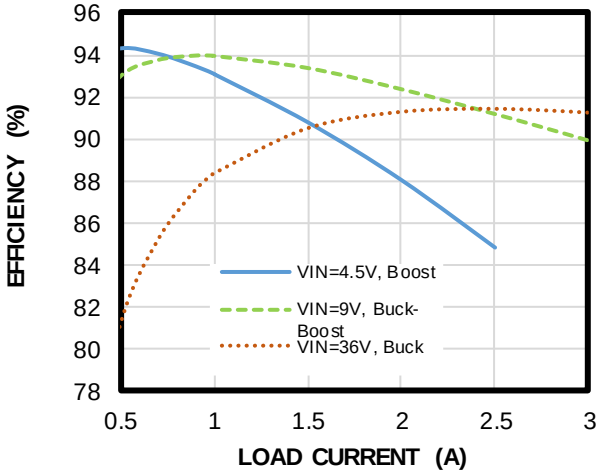
Efficiency vs. Load Current

V_{OUT} = 9V, FCCM, I_{OUT} = 10mA to 1A



Efficiency vs. Load Current

V_{OUT} = 9V, FCCM, I_{OUT} = 0.5A to 3A

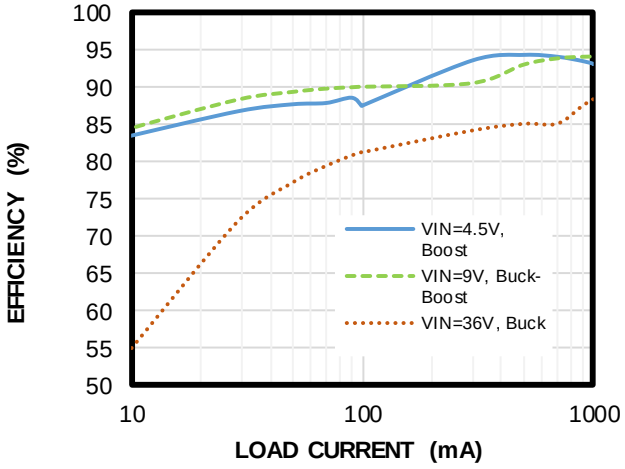


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 11.5V, L = 10µH, C_{OUT} = 40µF, f_{SW} = 450kHz, FCCM, T_A = 25°C, unless otherwise noted.

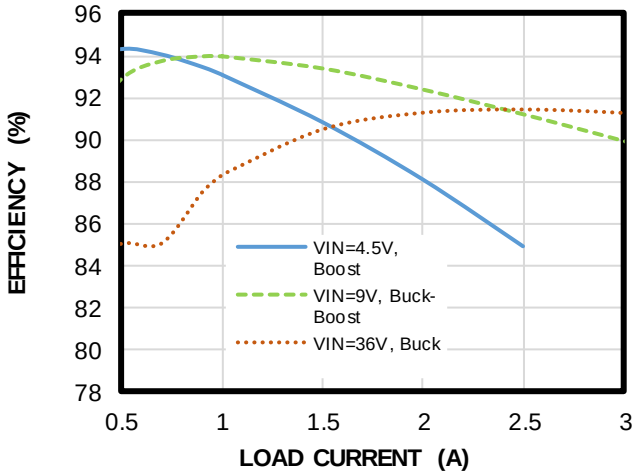
Efficiency vs. Load Current

V_{OUT} = 9V, DCM, I_{OUT} = 10mA to 1A



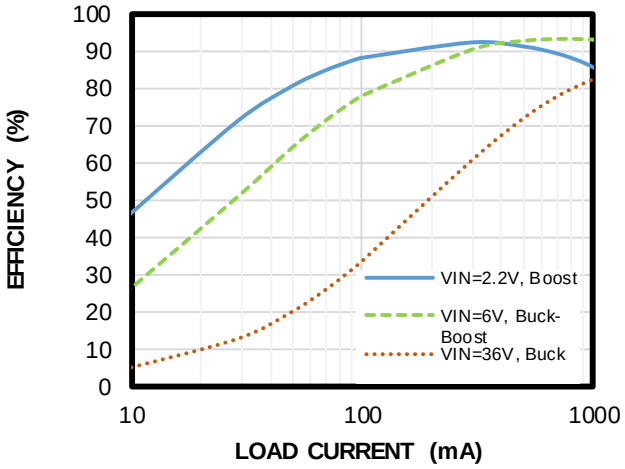
Efficiency vs. Load Current

V_{OUT} = 9V, DCM, I_{OUT} = 0.5A to 3A



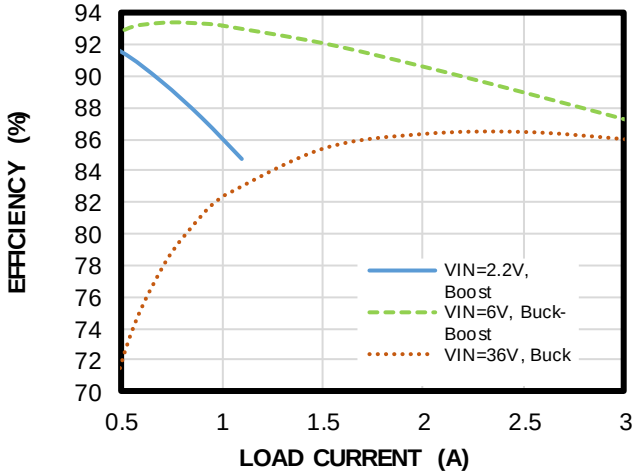
Efficiency vs. Load Current

V_{OUT} = 5V, FCCM, I_{OUT} = 10mA to 1A



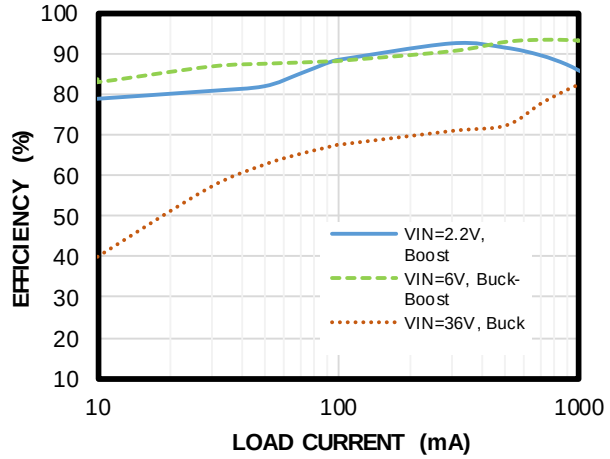
Efficiency vs. Load Current

V_{OUT} = 5V, FCCM, I_{OUT} = 0.5A to 3A



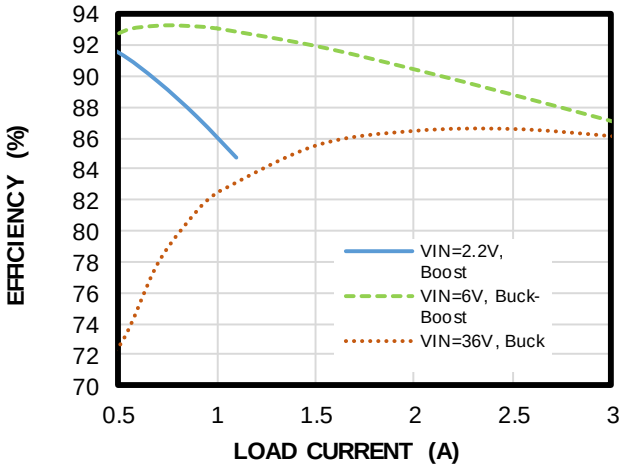
Efficiency vs. Load Current

V_{OUT} = 5V, DCM, I_{OUT} = 10mA to 1A



Efficiency vs. Load Current

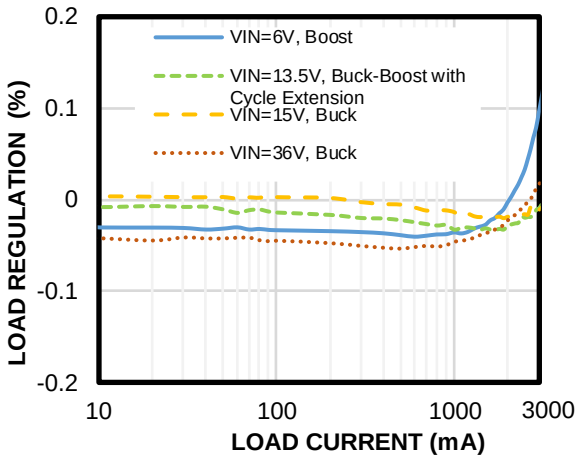
V_{OUT} = 5V, DCM, I_{OUT} = 0.5A to 3A



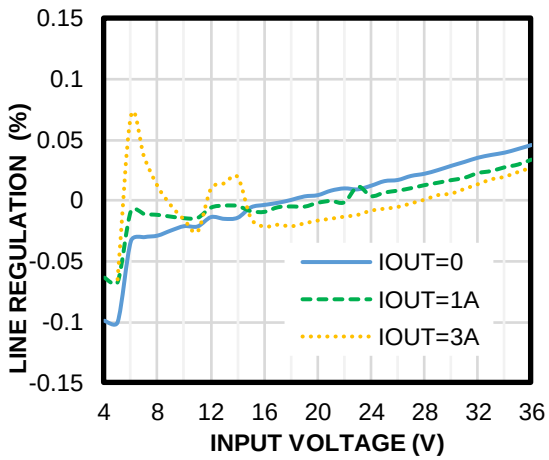
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 11.5V, L = 10µH, C_{OUT} = 40µF, f_{SW} = 450kHz, FCCM, T_A = 25°C, unless otherwise noted.

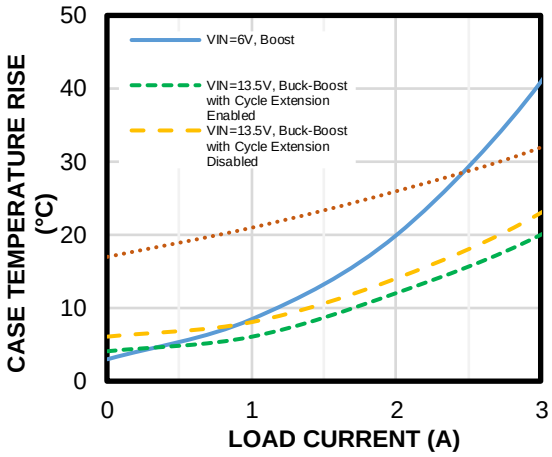
Load Regulation



Line Regulation



Case Temperature Rise vs. Load Current

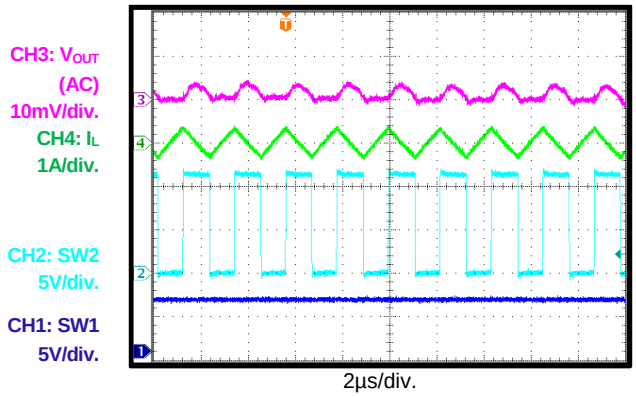


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 11.5V, L = 10µH, C_{OUT} = 40µF, f_{SW} = 450kHz, FCCM, T_A = 25°C, unless otherwise noted.

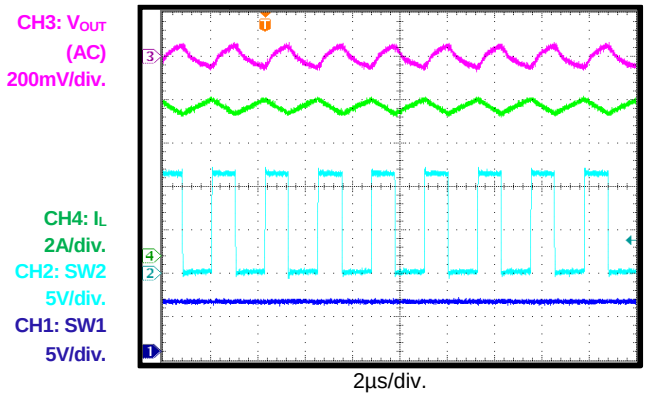
Steady State (Boost Mode)

V_{IN} = 6V, I_{OUT} = 0A



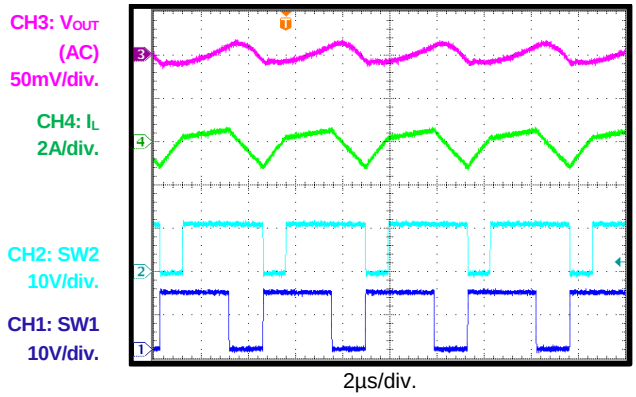
Steady State (Boost Mode)

V_{IN} = 6V, I_{OUT} = 3A



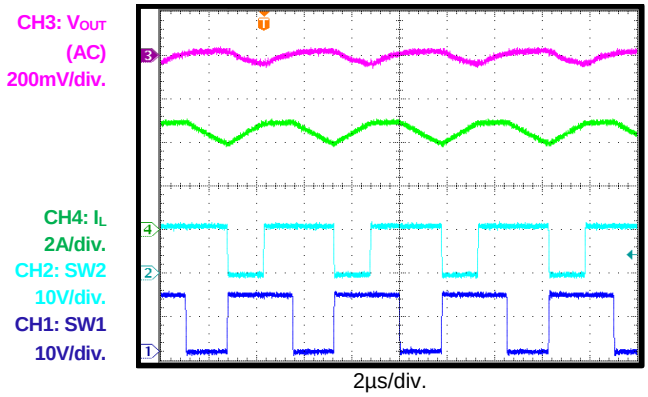
Steady State (Buck-Boost Mode)

V_{IN} = 13.5V, I_{OUT} = 0A



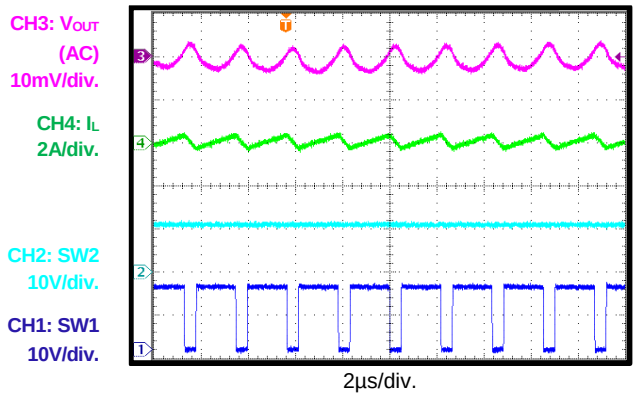
Steady State (Buck-Boost Mode)

V_{IN} = 13.5V, I_{OUT} = 3A



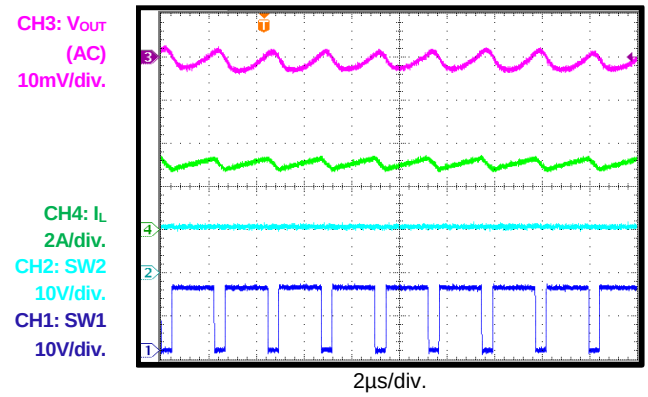
Steady State (Buck Mode)

V_{IN} = 15V, I_{OUT} = 0A



Steady State (Buck Mode)

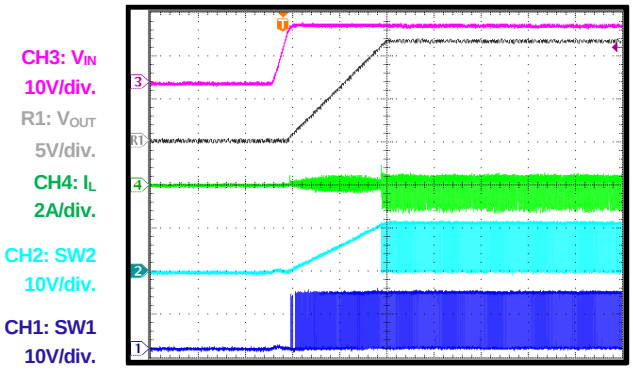
V_{IN} = 15V, I_{OUT} = 3A



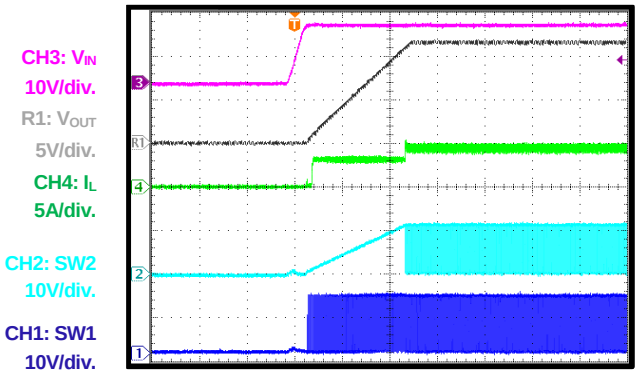
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 11.5V, L = 10µH, C_{OUT} = 40µF, f_{SW} = 450kHz, FCCM, T_A = 25°C, unless otherwise noted.

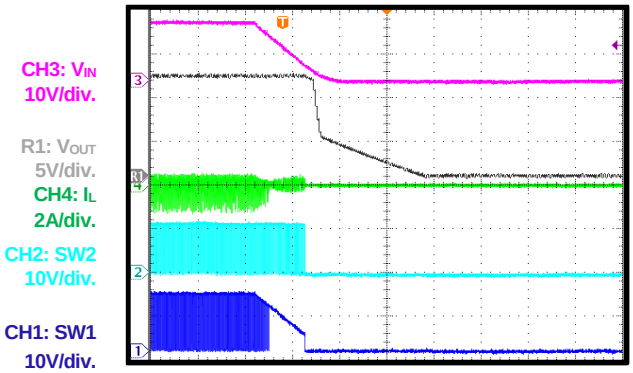
Start-Up through PVIN
I_{OUT} = 0A



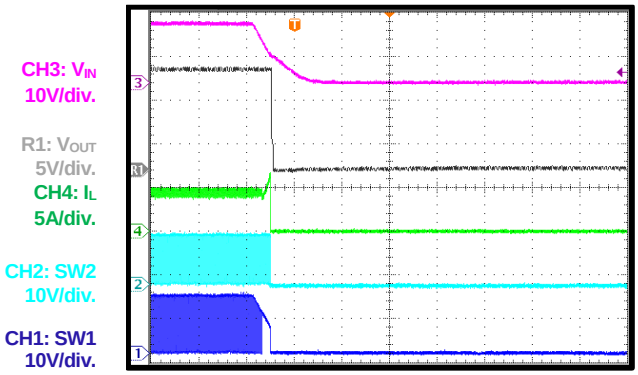
Start-Up through PVIN
I_{OUT} = 3A



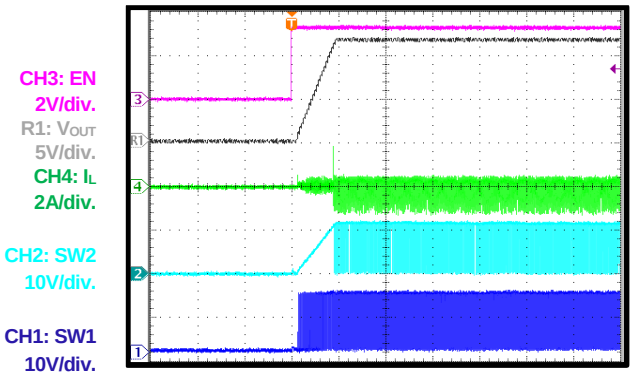
Shutdown through PVIN
I_{OUT} = 0A



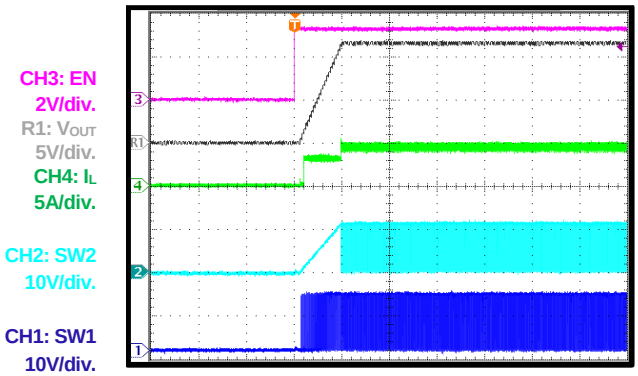
Shutdown through PVIN
I_{OUT} = 5A



Start-Up through EN
I_{OUT} = 0A



Start-Up through EN
I_{OUT} = 3A

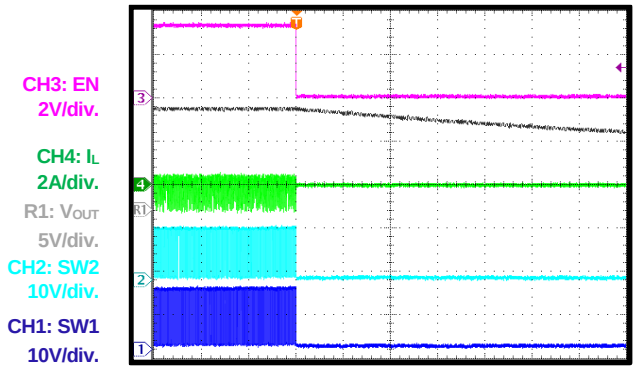


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 11.5V, L = 10µH, C_{OUT} = 40µF, f_{SW} = 450kHz, FCCM, T_A = 25°C, unless otherwise noted.

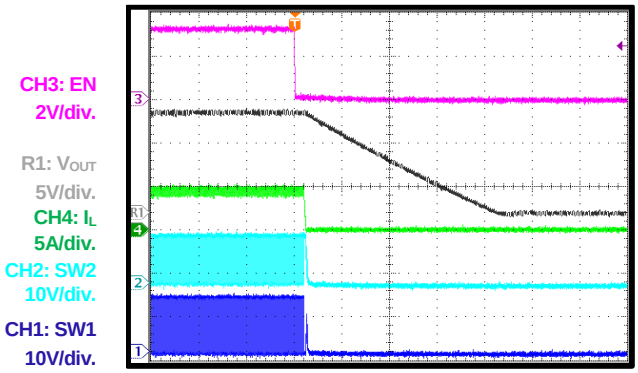
Shutdown through EN

I_{OUT} = 0A

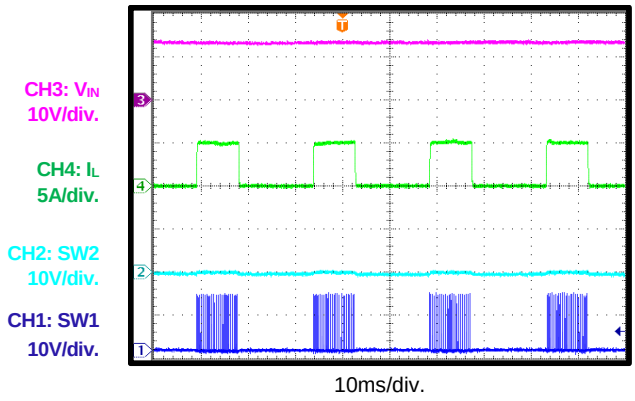


Shutdown through EN

I_{OUT} = 3A

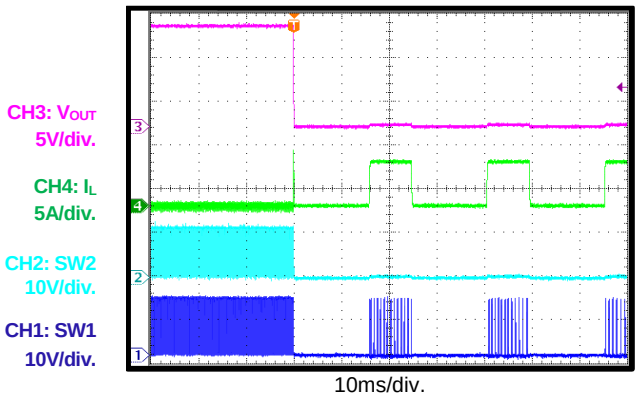


SCP Steady State



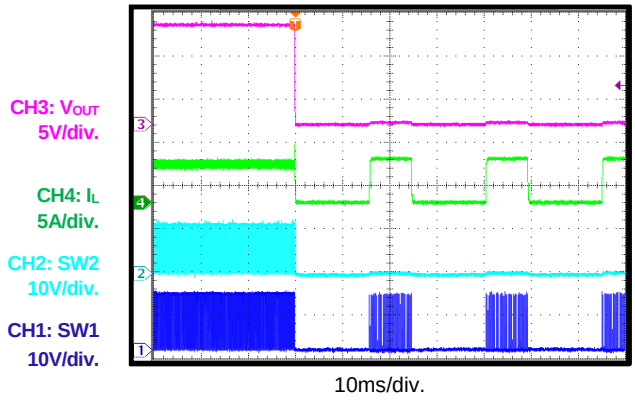
SCP Entry

I_{OUT} = 0A to short circuit



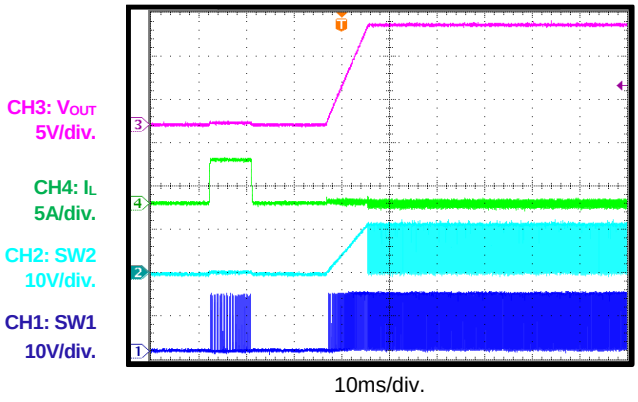
SCP Entry

I_{OUT} = 3A to short circuit



SCP Recovery

Short circuit to I_{OUT} = 0A

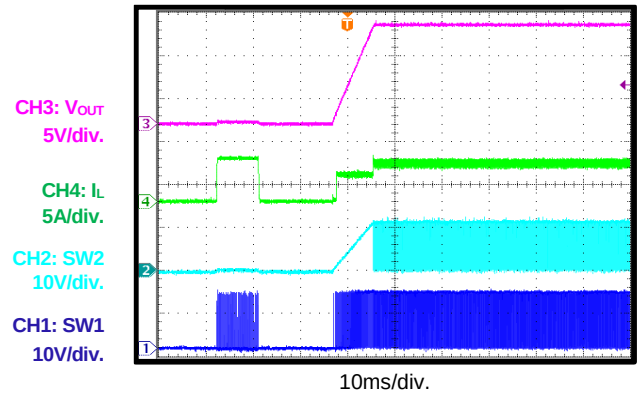


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 11.5V, L = 10µH, C_{OUT} = 40µF, f_{SW} = 450kHz, FCCM, T_A = 25°C, unless otherwise noted.

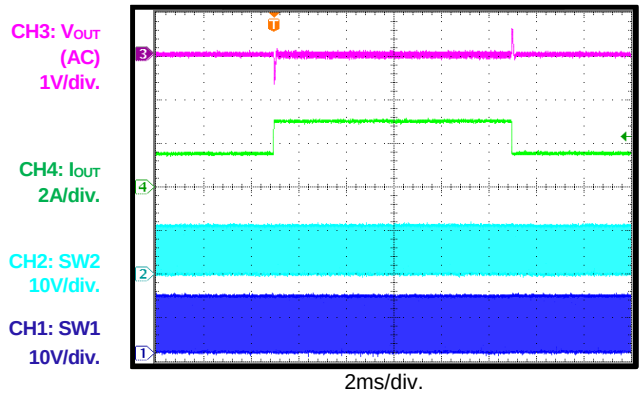
SCP Recovery

Short circuit to I_{OUT} = 3A



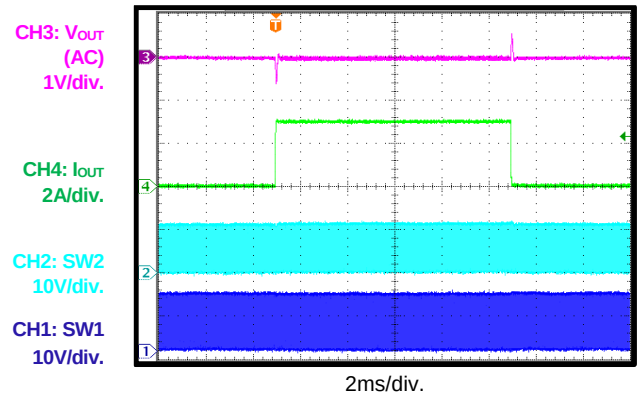
Load Transient

I_{OUT} = 1.5A to 3A, 1.6A/µs



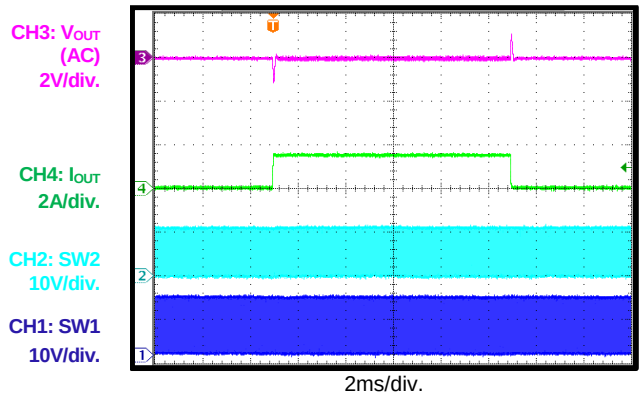
Load Transient

I_{OUT} = 0A to 1.5A, 2A/µs



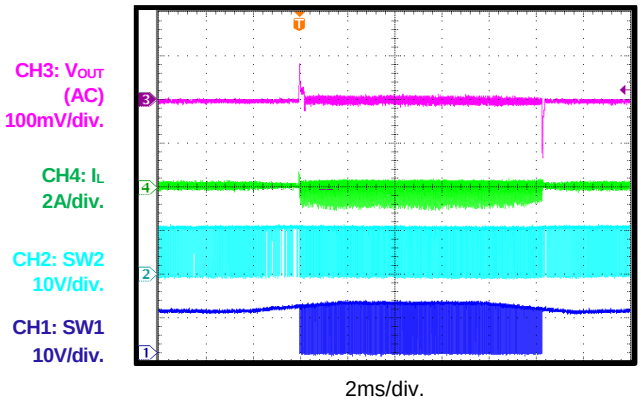
Load Transient

I_{OUT} = 0A to 3A, 2A/µs



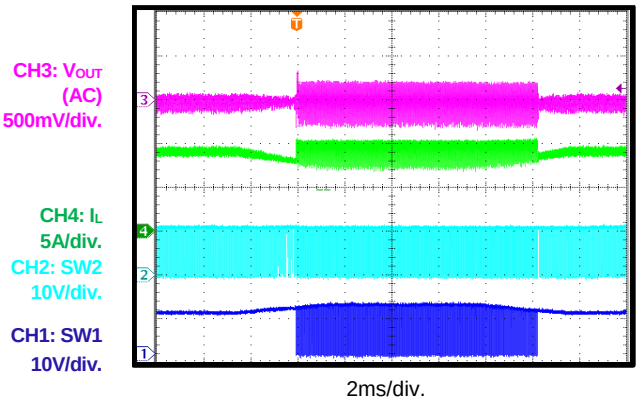
Mode Transient between Boost and Buck-Boost Modes

V_{IN} = 10V to 12V to 10V, I_{OUT} = 0



Mode Transient between Boost and Buck-Boost Modes

V_{IN} = 10V to 12V to 10V, I_{OUT} = 3A

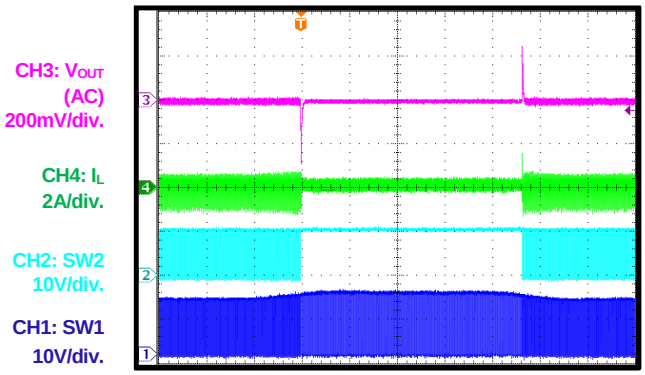


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 11.5V, L = 10µH, C_{OUT} = 40µF, f_{SW} = 450kHz, FCCM, T_A = 25°C, unless otherwise noted.

Mode Transient between Buck and Buck-Boost Modes

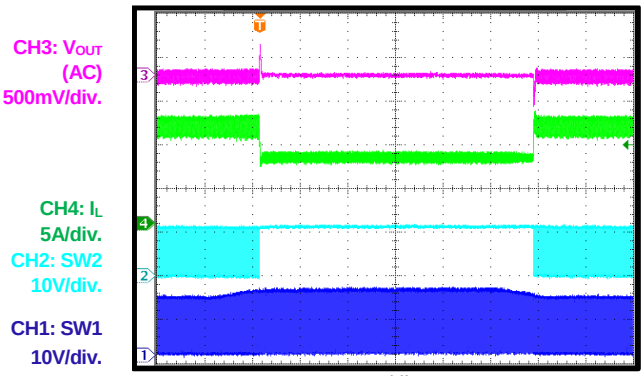
V_{IN} = 13.5V to 15V to 13.5V, I_{OUT} = 0A



2ms/div.

Mode Transient between Buck and Buck-Boost Modes

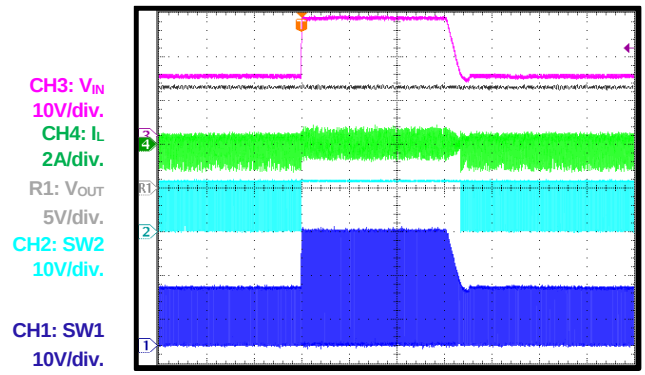
V_{IN} = 13.5V to 15V to 13.5V, I_{OUT} = 3A



2ms/div.

Load Dump

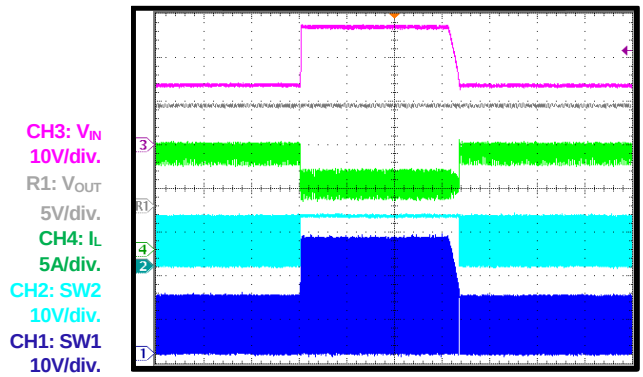
I_{OUT} = 0A



100ms/div.

Load Dump

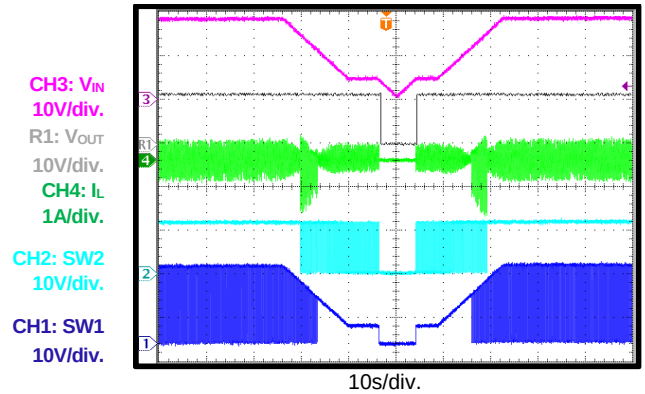
I_{OUT} = 3A



100ms/div.

V_{IN} Ramp Down and Up

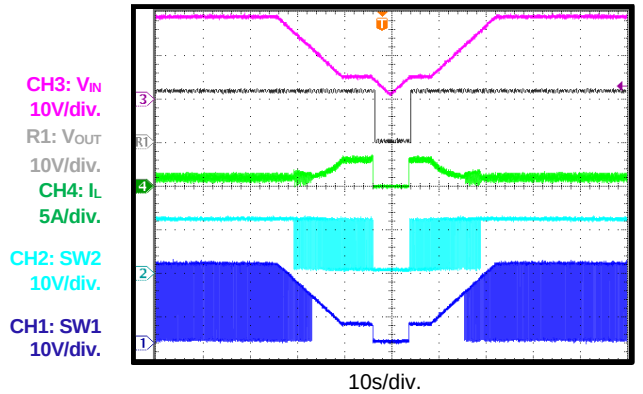
I_{OUT} = 0A



10s/div.

V_{IN} Ramp Down and Up

I_{OUT} = 1A



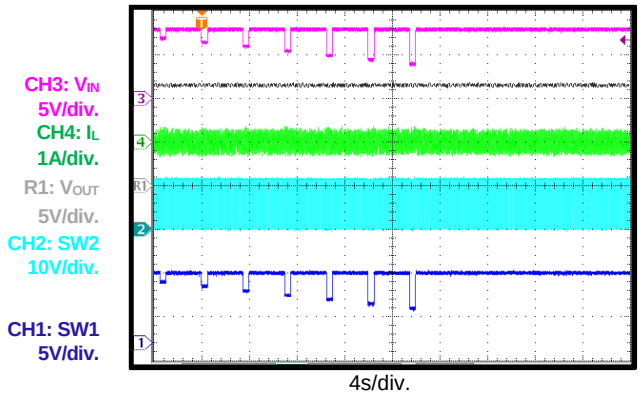
10s/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 11.5V, L = 10µH, C_{OUT} = 40µF, f_{SW} = 450kHz, FCCM, T_A = 25°C, unless otherwise noted.

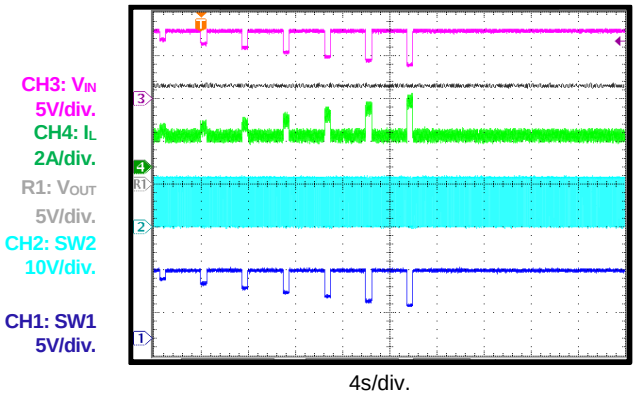
Reset Behavior

I_{OUT} = 0A



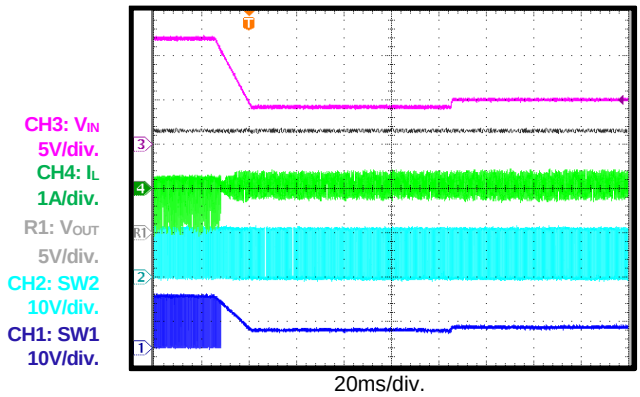
Reset Behavior

I_{OUT} = 1A



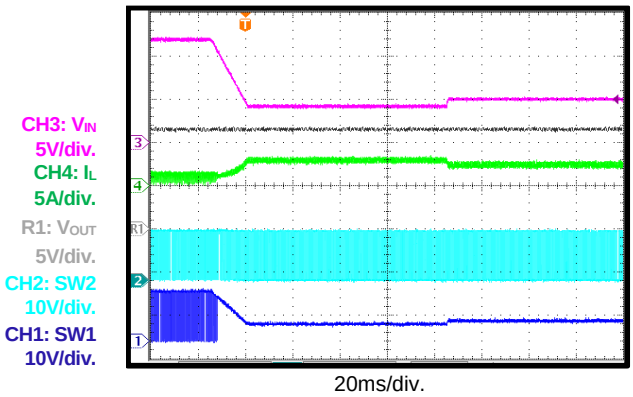
Cold Crank

I_{OUT} = 0A



Cold Crank

I_{OUT} = 1A

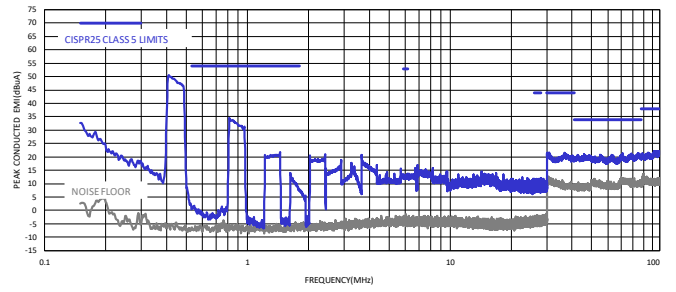


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 11.5V, I_{OUT} = 3A, L = 10µH, f_{SW} = 450kHz, in buck-boost mode, with EMI filters and FSS enabled, T_A = 25°C, unless otherwise noted. (8)

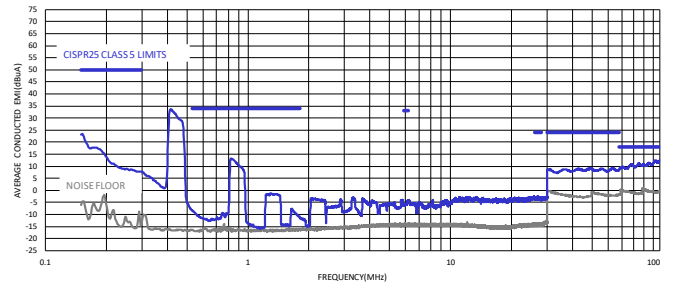
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



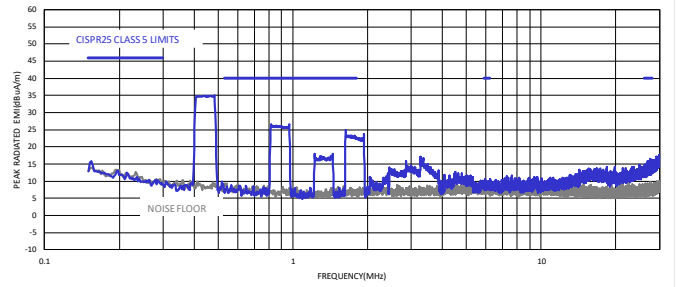
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



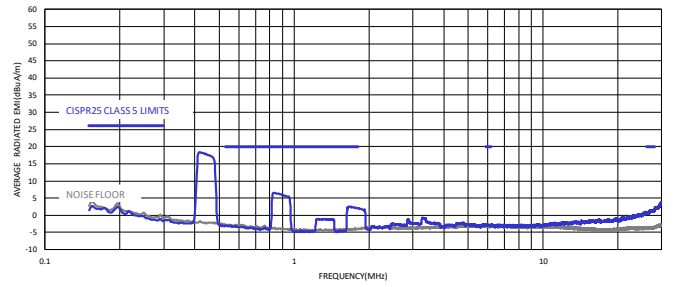
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



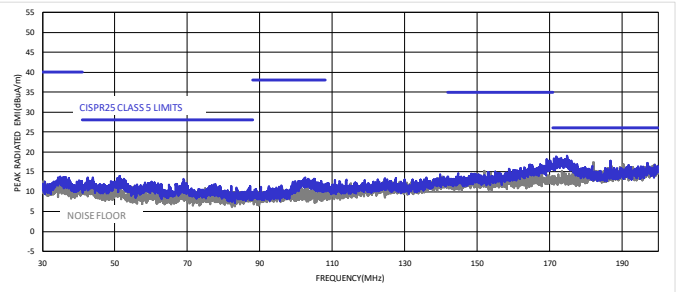
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



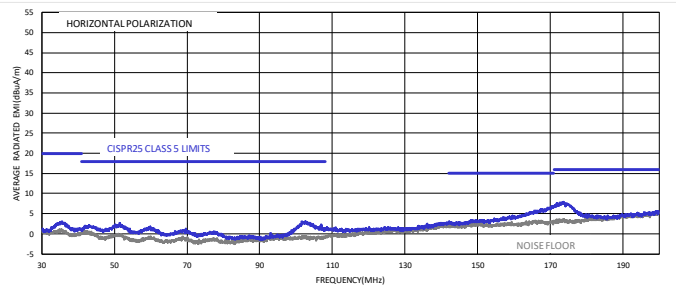
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz



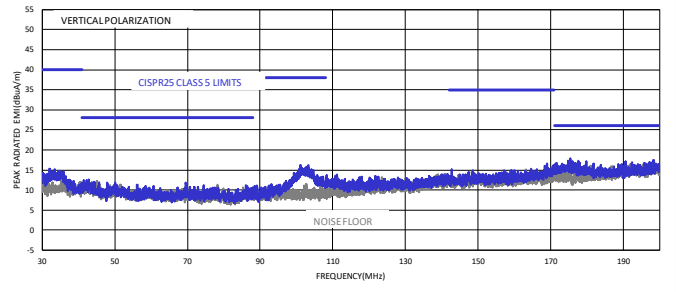
Notes:

8) The EMC test results are based on the application circuit with EMI filters (see Figure 34 on page 63).

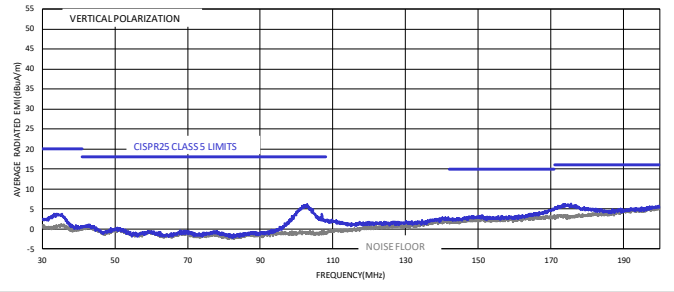
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 11.5V, I_{OUT} = 3A, L = 10µH, f_{SW} = 450kHz, in Buck-boost mode, with EMI filters and FSS enabled, T_A = 25°C, unless otherwise noted.

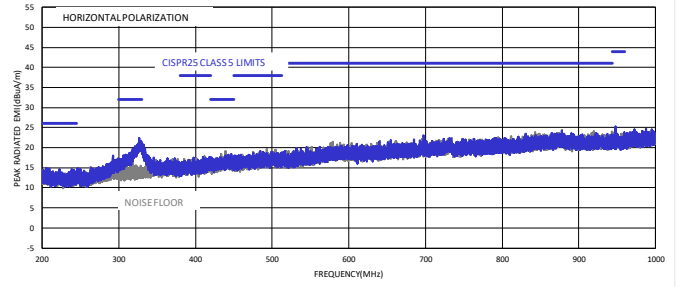
CISPR25 Class 5 Peak Radiated Emissions
Vertical, 30MHz to 200MHz



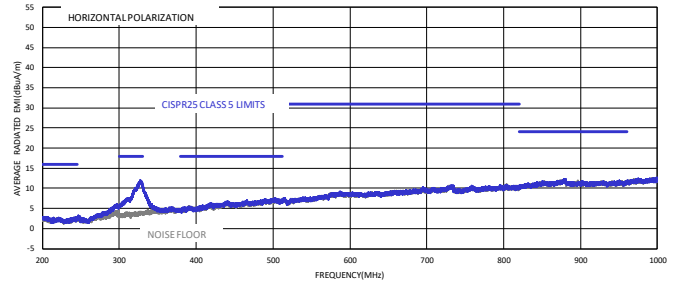
CISPR25 Class 5 Average Radiated Emissions
Vertical, 30MHz to 200MHz



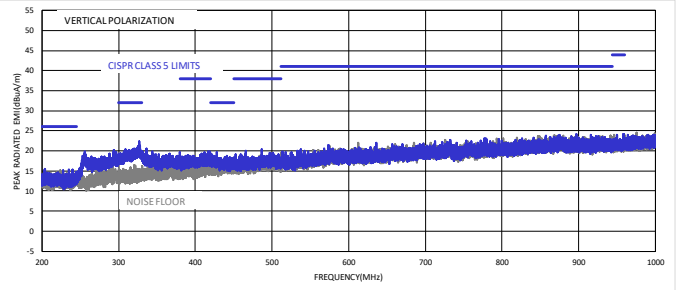
CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 200MHz to 1GHz



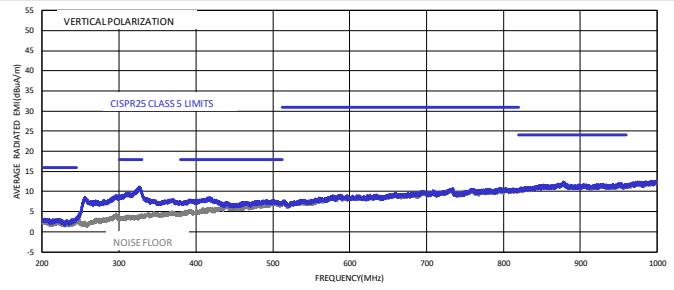
CISPR25 Class 5 Average Radiated Emissions
Horizontal, 200MHz to 1GHz



CISPR25 Class 5 Peak Radiated Emissions
Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions
Vertical, 200MHz to 1GHz



FUNCTIONAL BLOCK DIAGRAM

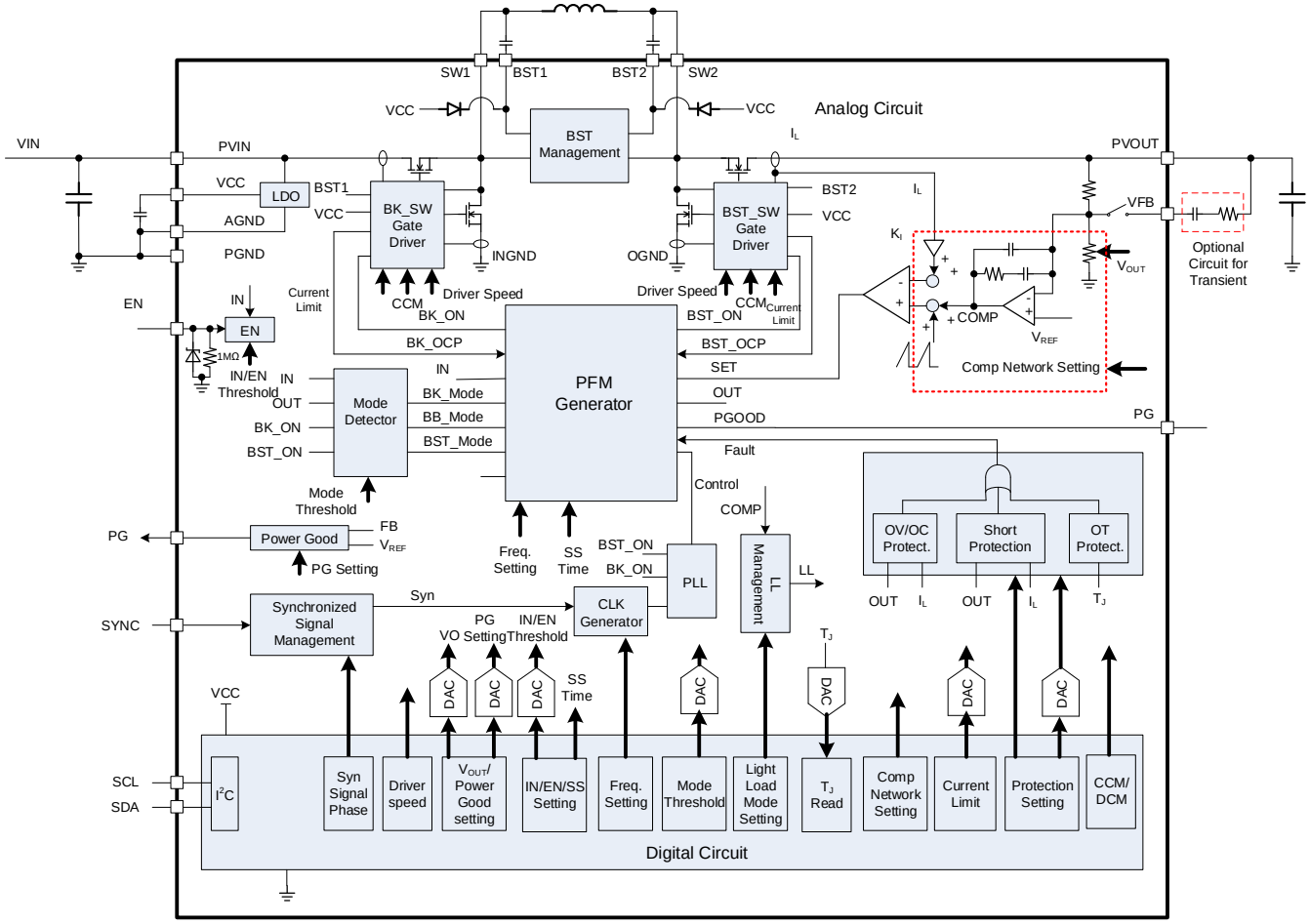


Figure 1: Functional Block Diagram

OPERATION

The MPQ8873 is a 36V, monolithic, synchronous buck-boost DC/DC converter with a 2.2V to 36V input voltage range. The wide input voltage (V_{IN}) range makes it well-suited to multi-purpose automotive and industrial applications.

Four integrated, low-resistance N-channel MOSFETs minimize the size of external circuitry. These N-channel MOSFETs also allow the converter to regulate the output voltage (V_{OUT}) when V_{IN} is above, below, or equal to V_{OUT}. The flexible topology transitions reduce power loss to maximize efficiency.

In addition, the proprietary constant-on-time (COT) control algorithm ensures seamless transitions between the adjacent operational regions. The MPQ8873 can operate across a wide 200kHz to 1MHz switching frequency range. This allows applications to be optimized for board size, efficiency, and EMI performance. Most of the electrical characteristics can be configured by accessing the related internal registers via the device's I²C interface.

VCC Regulator

In normal operation, an internal low-dropout (LDO) regulator outputs a nominal 5V VCC supply from PVIN. This supplies power to both control blocks and the four MOSFETs' gate drivers. The VCC regulator has a 60mA current limit to prevent short circuiting the VCC rail. Add a 1µF to 10µF, low-ESR ceramic capacitor to act as the bypass capacitor from VCC to AGND.

The VCC supply cannot maintain a 5V output once PVIN drops below 5V. If PVOUT is sufficient for the VCC power supply (e.g. in boost mode), the reserved 4.55V regulator takes over the VCC supply from PVOUT.

VCC must exceed 2.25V for applications where V_{IN} goes down to 2.2V.

Internal Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to avoid the chip (or some blocks) from operating at an insufficient supply voltage. The MPQ8873 incorporates three internal, fixed UVLO comparators to monitor PVIN, VCC, and BST.

There are two PVIN input ranges that can be selected by the I²C interface: 4.5V to 36V for normal input mode, and 2.2V to 36V for low input mode. The PVIN/VCC UVLO levels are not identical when there are different input voltage ranges.

The chip is disabled immediately if either the PVIN voltage (V_{IN}) or VCC voltage (V_{CC}) falls below its respective UVLO threshold. The I²C interface cannot work if VCC is not valid.

If V_{IN} falls below its UVLO threshold, all switching actions are disabled. Then the COMP voltage is pulled down until V_{IN} exceeds the start-up voltage.

Similarly, if V_{CC} drops below its UVLO threshold, chip stops switching and then the COMP voltage is pulled down until V_{CC} rises up again.

Since V_{CC} is the internal LDO output from PVIN (or PVOUT in some cases), the actual V_{CC} is determined by V_{IN} and the dropout voltage of the VCC regulator. The dropout voltage depends on the load current drawn from VCC. In scenarios with a higher switching frequency or larger FET driving capacity demand, the VCC regulator dropout voltage can rise. This means that V_{CC} can reach its UVLO threshold before the PVIN pin drops below its UVLO threshold.

BST UVLO indicates that there is inadequate driving capacity for the high-side MOSFET (HS-FET). Under this circumstance, the chip stops the HS-FET from switching and pulls down COMP. The bootstrap charger conducts the low-side MOSFETs (LS-FETs) to charge up the BST voltage. The converter restarts with soft start when the BST voltage (V_{BST}) exceeds its UVLO threshold.

On/Off Control and Custom Input Under-Voltage Lockout (UVLO)

When EN is driven above its logic threshold (typically 0.85V), the VCC regulator is activated. Once VCC exceeds the VCC UVLO threshold, it starts to provide power to the internal control circuitry. Then the integrated EN comparator begins working.

If the EN voltage exceeds the comparator's upper threshold (typically 1.55V), the converter is enabled and soft start begins. If EN drops below the comparator's lower threshold, the converter stops switching. The VCC regulator and control circuitry continue working until the EN pin is pulled below its logic threshold (<0.5V). Then the MPQ8873 shuts down and consumes very little input current. The total supply current is reduced to <25μA.

In addition to serving as normal on/off logic control, the integrated EN comparator can set the EN pin to a custom input UVLO threshold by adding an external resistor divider from PVIN to GND (see Figure 2).

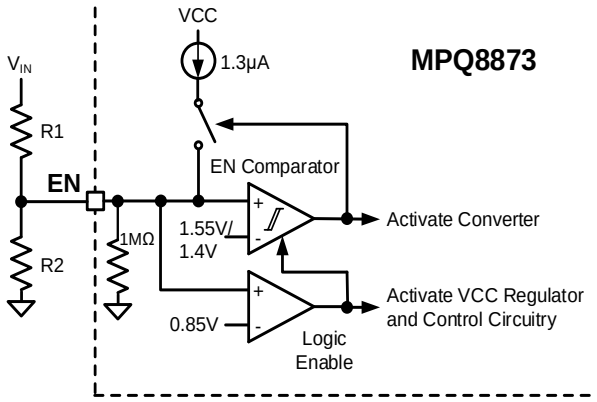


Figure 2: Custom Input UVLO Set by EN

The EN voltage is set via the resistor divider ratio from PVIN. When EN reaches 1.55V (the rising UVLO threshold of the integrated EN comparator), the converter starts switching. Meanwhile, an internal 1.3μA pull-up current source is enabled to source current from the EN pin.

To disable the converter when V_{IN} drops, the EN voltage must drop below the UVLO threshold of the EN comparator. This means V_{IN} must fall enough to overcome the hysteresis from the 1.3μA pull-up current, as well as the inherent 150mV hysteresis of the EN comparator. As a result, the actual hysteresis can be set independently without changing the rising UVLO threshold.

In addition to the EN logic, the converter can be turned on/off via the I²C interface. Set register 01h, bit[7] to 1 to turn the MPQ8873 on; set it to 0 to turn the MPQ8873 off.

Constant-On-Time (COT) Control

The MPQ8873 employs constant-on-time (COT) control to achieve fast load transient response. Figure 3 shows the COT control block diagram.

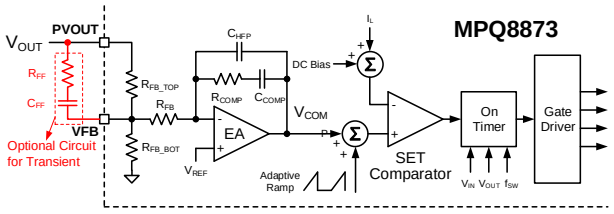


Figure 3: COT Control

The operational error amplifier (EA) corrects any error voltage between V_{FB} and V_{REF}. With the help of the EA, the MPQ8873 can provide excellent load regulation across the entire load range, regardless of whether the device operates in forced continuous conduction mode (FCCM) or discontinuous conduction mode (DCM). It also features internal ramp compensation. The adaptive internal ramp is optimized so that the converter is stable across the entire operating voltage range, with proper design of the external components. Figure 4 shows how the switching cycle is generated.

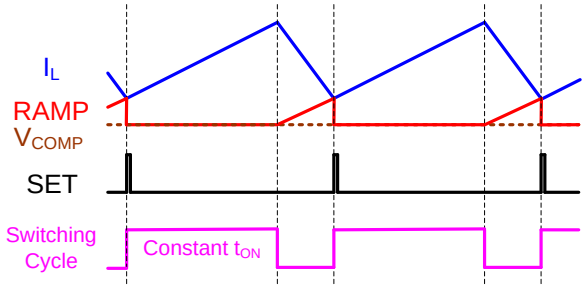


Figure 4: Switching Cycle Generation

The EA corrects the error between V_{FB} and V_{REF} to output a fairly smooth DC voltage (V_{COMP}). The internal ramp compensation is added to V_{COMP}. The combined V_{COMP} is compared to the inductor current (I_L).

When I_L drops below the combined V_{COMP}, the set comparator outputs a SET signal to begin a new switching cycle. The converter's on time is fixed and determined by V_{IN}, V_{OUT}, and the selected switching frequency (f_{SW}). Once the on interval elapses, the main MOSFET turns off. Then the coupled synchronous rectifier (SR) switch turns on after a dead time to avoid shoot-through.

In FCCM, the SR switch remains on until the next SET signal comes or the reverse current limit is triggered. By repeating this operation, the MPQ8873 regulates V_{OUT}.

Four-Switch Power Converter

Figure 5 shows the topology of the four-switch power converter, which is comprised of four N-channel MOSFETs. Q1 and Q3 work as the main switches, while Q2 and Q4 act as the SR switches. The switches are properly controlled so that transitions between buck, buck-boost, and boost mode are continuous according to V_{IN} and V_{OUT}.

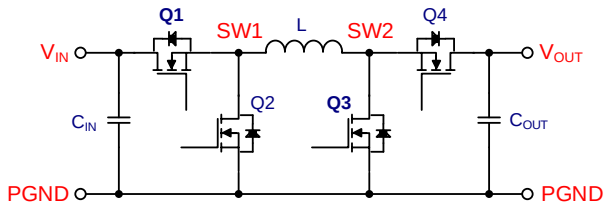


Figure 5: Four-Switch Power Converter

When stepping down from a higher V_{IN} to a lower V_{OUT}, the converter operates in buck mode (see Figure 6 and Figure 7). Q4 remains on and Q3 remains off for the entire switching cycle. Q1 and Q2 switch alternately, and behave like a typical synchronous buck converter. Q1's on time is fixed, and the off time can be adjusted via the control algorithm. Figure 6 shows buck mode in FCCM.

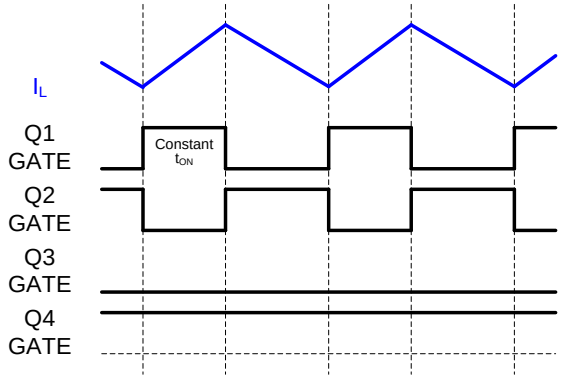


Figure 6: Buck Mode in FCCM

Figure 7 shows buck mode in DCM.

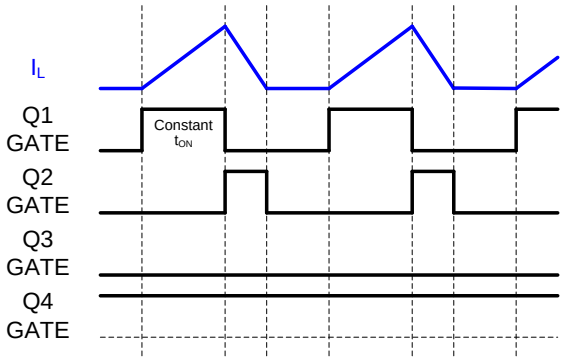


Figure 7: Buck Mode in DCM

If V_{IN} is close to V_{OUT}, the converter enters buck-boost mode (see Figure 8 and Figure 9). Q1 and Q2 still operate independently like a synchronous buck regulator. Q1's on time is fixed, and its off time can be adjusted by the control algorithm. Q3 switches on synchronously with Q1, and remains on for a constant duty cycle, which can be configured based on the switching frequency. Then Q3 turns off, and Q4 switches on.

When Q1 and Q4 are on at the same time, the voltage across inductor is the voltage difference between V_{IN} and V_{OUT}. This value is so low that I_L is smooth during this period.

Figure 8 shows buck-boost mode in FCCM when V_{IN} exceeds V_{OUT}.

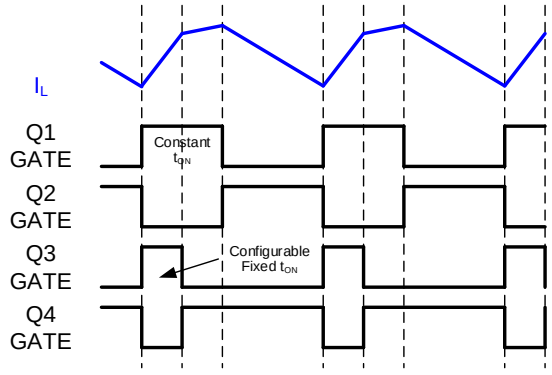


Figure 8: Buck-Boost Mode in Normal FCCM (V_{IN} > V_{OUT})

Figure 9 shows buck-boost mode in DCM when V_{IN} exceeds V_{OUT}.

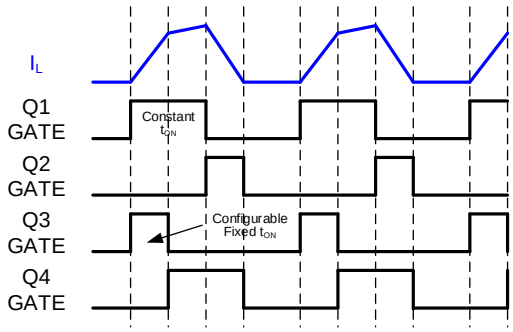


Figure 9: Buck-Boost Mode in Normal DCM (V_{IN} > V_{OUT})

Figure 10 shows buck-boost mode in FCCM when V_{OUT} exceeds V_{IN}.

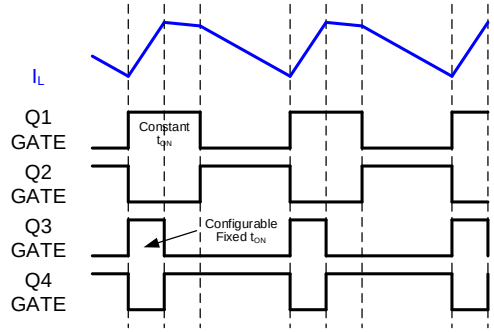


Figure 10: Buck-Boost Mode in Normal FCCM (V_{IN} < V_{OUT})

Figure 11 shows buck-boost mode in FCCM when V_{OUT} exceeds V_{IN}.

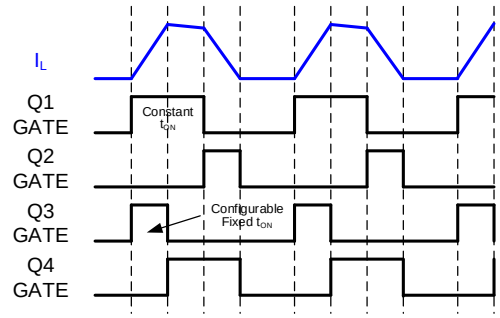


Figure 11: Buck-Boost Mode in Normal DCM (V_{IN} < V_{OUT})

If V_{IN} is below V_{OUT}, the MPQ8873 operates in boost mode (see Figure 12 and Figure 13). Q1 remains on and Q2 remains off for the entire switching cycle. Q3 and Q4 are modulated to switch alternately, behaving like a typical synchronous boost regulator. Q3's on time is fixed, and its off time can be adjusted by the control algorithm.

Figure 12 shows boost mode in FCCM.

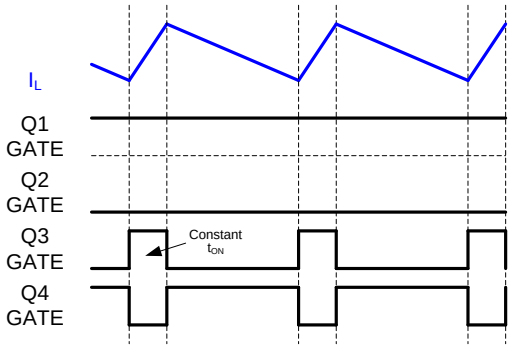


Figure 12: Boost Mode in FCCM

Figure 13 shows boost mode in DCM.

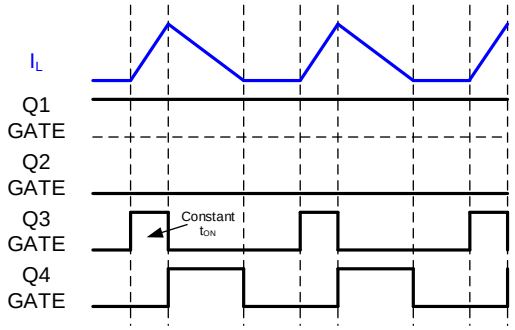


Figure 13: Boost Mode in DCM

The mode-to-mode transition is automatic by comparing the sensed V_{IN} and sensed V_{OUT}. Figure 14 shows the power converter's regions of operation.

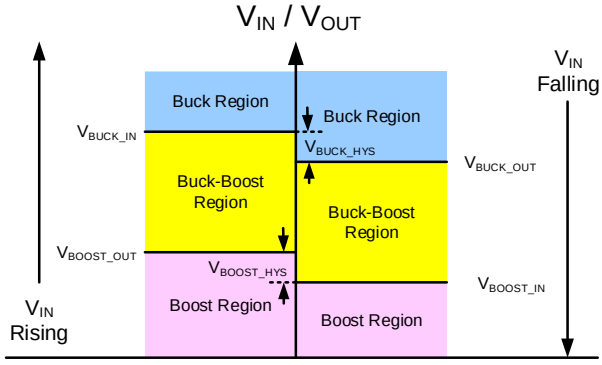


Figure 14: Regions of Operation

If V_{IN} is significantly lower than the sensed V_{OUT}, the MPQ8873 works in boost mode. When V_{IN} exceeds V_{BOOST_OUT}, the device transitions to buck-boost mode. If V_{IN} reaches V_{BUCK_IN}, then buck mode is activated. Alternately, if V_{IN} drops from a higher value to a lower one, the converter operates in buck mode, buck-boost mode, and boost mode successively.

To avoid unexpected, repetitive mode transitions when V_{IN} is close to the critical status between adjacent regions, there is a transition threshold hysteresis.

Bootstrap and Floating Driver

The bootstrap circuitry drives the high-side N-channel MOSFETs (Q1 and Q4). The external flying capacitors are charged up to maintain a sufficient driving voltage above SW via the internal bootstrap regulators.

At start-up, the bootstrap pre-charge process starts before the converter is ready for normal operation. Both LS-FETs (Q2 and Q3) turn on to force SW1 and SW2 low, allowing the bootstrap regulators to charge the flying capacitors from the VCC supply via the BST1 and BST2 pins, respectively. If the current limit is triggered, the LS-FETs turn off. The LS-FETs may switch several times before building up enough driving voltage across the flying capacitors. Then soft start begins.

If the converter is operating in buck-boost mode, the flying BST capacitor can be charged while the corresponding LS-FET is conducted.

However, in buck mode and boost mode, one HS-FET remains on, and its relevant LS-FET remains off for the entire switching cycle. Under this condition, the BST capacitors can charge each other through the internal charge regulator.

Error Amplifier

The MPQ8873 integrates a high-performance operational amplifier to implement control loop compensation for stable V_{OUT} regulation (see Figure 15).

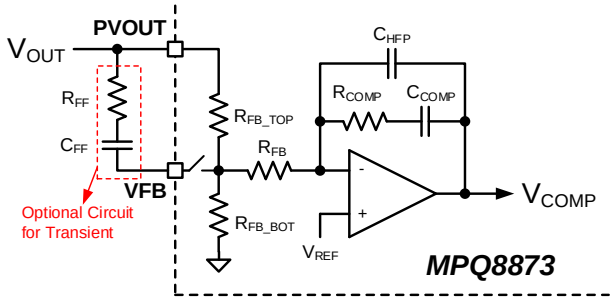


Figure 15: Compensation Network

Figure 15 shows the typical Type II compensation network that is fully integrated into the MPQ8873. Component values can be configured via the I²C interface. Neither an external V_{OUT} sensing resistor divider or compensation network components are required.

To optimize the converter's transient response, a Type III compensation network is also available. The Type III compensation network is comprised of the internal, existing Type II compensation network, plus an external RC compensation network tied between the PVOUT and VFB pins (see Figure 15). If a Type III compensation network or an external output voltage sensing resistor divider is required, set register 0Dh, bit[1] to 1.

Oscillator and Synchronization Input/Output

The MPQ8873 converter's switching frequency can be configured to be between 200kHz and 1MHz via the I²C interface. The COT control algorithm determines the on time based on V_{IN}, V_{OUT}, and the operating switching frequency.

For EMI-sensitive applications, the switching clock can be synchronized to an external clock signal applied to the SYNC pin if synchronization input mode is enabled. The synchronization clock frequency ranges between 250kHz and 1MHz, and must be 20% greater than the configured frequency set in the one-time programmable (OTP) memory. The square-wave amplitude should have a peak above 1.4V and a valley below 0.5V. The width of the synchronization pulse should be >200ns.

The MPQ8873 can operate in the designated switching frequency (via the I²C interface or external clock signal) in CCM or FCCM. Once the converter enters DCM, the switching frequency is self-adjusting based on the control algorithm.

The SYNC pin can also be configured to synchronized output mode. The MPQ8873 can output the internal clock with a 0° or 180° phase shift. For example, for a two-device system sharing a common input power supply, one MPQ8873 can output its clock signal with a 180° phase shift to synchronize to the other device's switching clock.

As a result, both devices can operate in the same frequency, but with a 180° phase difference to reduce the total input voltage/current ripple.

This allows a lower-value input bypass capacitor to be used. The output synchronization clock's duty cycle is constant at 50%.

Frequency Spread Spectrum (FSS)

To further optimize EMI performance, the MPQ8873 features frequency spread spectrum (FSS) (see Figure 16).

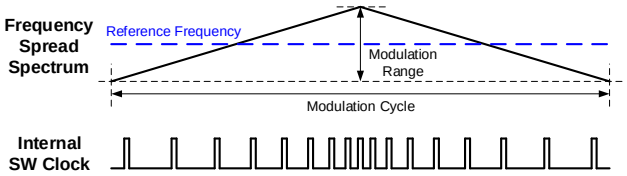


Figure 16: Frequency Spread Spectrum

The reference frequency, as well as the FSS modulation range and cycle, are all set via the I²C interface. Once FSS is enabled, triangular frequency modulation varies the switching frequency between the same ratio, which is both higher and lower than the reference value. During a full modulation cycle, the switching frequency varies from the lowest to the highest value, then drops back to the lowest value.

If an external clock signal is applied to the SYNC pin in synchronized input mode, the FSS mechanism is invalid. Therefore, FSS is unavailable in synchronization input mode.

Discontinuous Conduction Mode (DCM) and Forced Continuous Conduction Mode (FCCM) under Light Loads

In normal operation, the converter works in forced continuous conduction mode (FCCM) under heavier loads. I_L never drops to 0A during the switching cycle. f_{SW} is fairly constant, and can be configured via the I²C interface.

When the load current drops or there is no load, the converter experiences a light-load or no-load condition. The MPQ8873 can operate in discontinuous conduction mode (DCM) or FCCM under light-load conditions.

DCM is applied to optimize efficiency under light-load or no-load conditions. While the synchronous rectifier (SR) turns on, the inductor current falls linearly. When the load current continues to decrease, the I_L valley reaches 0A. If DCM is employed, the active SR switch stops switching once I_L reaches 0A (see Figure 17).

This means that I_L cannot drop to the negative value, and the output capacitor cannot be discharged further.

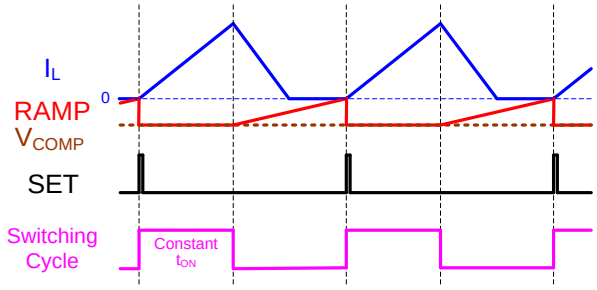


Figure 17: DCM under Light-Load Conditions

Based on the COT control algorithm, I_L stops falling, but the combined V_{COMP} can rise up continually with the ramp compensation. When the combined V_{COMP} reaches I_L, a SET signal initiates a new switching cycle. In DCM, f_{SW} is self-adjusting and does not follow the switching frequency setting until the converter resumes FCCM with load increments.

When FCCM is enabled, I_L can drop to the negative value as long as the reverse current limit is not triggered (see Figure 18). The converter acts as it would with a heavy load, and can maintain f_{SW} to regulate V_{OUT}, regardless of the output current. FCCM results in a smaller output ripple, but has lower efficiency under light-load conditions.

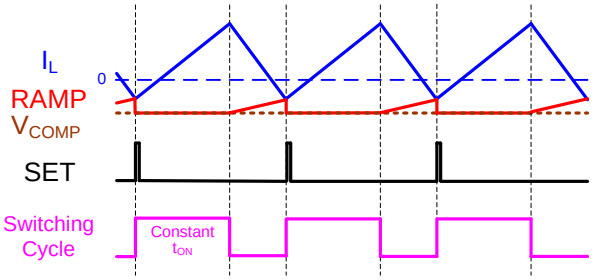


Figure 18: FCCM under Light-Load Conditions

Soft Start

Once PVIN, VCC, and EN are all enabled, the converter begins switching, and the internal soft start is implemented.

The MPQ8873's built-in soft start (SS) ramps up the internal reference voltage (V_{REF}) from 0V to the expected value with a controlled slew rate. This slew rate can be configured via the I²C interface. V_{OUT} can ramp up slowly to prevent the converter's V_{OUT} from overshooting during start-up.

Dynamic Output Voltage Adjustment

If the MPQ8873 operates in its normal input range (4.5V to 36V), V_{REF} can be adjusted from 0.5V to 2.0V with a 10mV resolution. The converter features dynamic V_{OUT} adjustments by changing V_{REF} from the current value to the set value. V_{REF} falls and rises in 10mV steps (see Figure 19 and Figure 20).

By controlling the time between steps using the I²C interface, the reference voltage variation slew rate can be adjusted. A longer time between steps results in a slower slew rate. Conversely, the slew rate increases by using a shorter time between steps. Figure 19 shows how V_{REF} is adjusted while it increases.

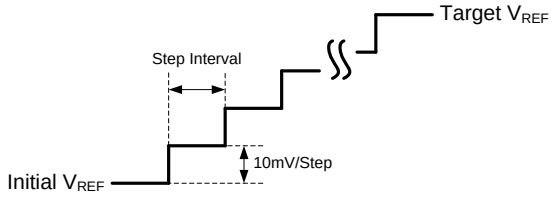


Figure 19: V_{REF} Adjustment (V_{REF} Increasing)

Figure 20 shows how V_{REF} is adjusted while it decreases.

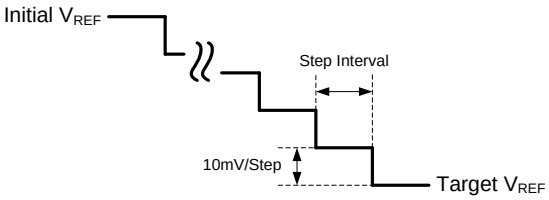


Figure 20: V_{REF} Adjustment (V_{REF} Decreasing)

V_{OUT} regulation is implemented by the converter control loop. The V_{OUT} adjustment, like the V_{REF} alteration, is dependent on the control loop stability. A slower slew rate helps achieve a smooth, monotonic V_{OUT} adjustment.

Power Good (PG) Indicator

The PG pin is connected to the open drain of an internal MOSFET. PG should be connected to a voltage source through an external pull-up resistor to act as the power good (PG) indicator. The PG pin is pulled down to ground during soft start, or if V_{OUT} is not within the allowable window. When V_{OUT} is in regulation, the PG MOSFET turns off, and the PG pin can be pulled high to indicate a good output status. There is a delay time of about 30µs if the PG status flip flops.

The PG threshold and hysteresis can be configured via the I²C interface.

Input Over-Voltage Protection (OVP)

If input over-voltage protection (OVP) is required, the chip can provide an input OVP threshold at 11V, 22V, or 33V. Once V_{IN} exceeds this threshold, the converter stops switching immediately and sets the input over-voltage (OV) fault flag. Once V_{IN} returns to within the normal range, the MPQ8873 automatically resumes normal operation.

The user can enable input OVP and select the threshold/recovery hysteresis via the I²C interface.

Output Over-Voltage Protection (OVP)

The MPQ8873 monitors V_{OUT} with the PVOUT pin. The VFB pin is connected to the tap of the internal output feedback resistor divider. If V_{OUT} exceeds the output OVP threshold, the converter stops switching immediately and an output OV fault is recorded.

There are two types of the optional output OVP modes: recoverable mode and latch-off mode.

The output OVP mode, threshold, and recovery hysteresis can be selected via the I²C interface.

Over-Current Protection (OCP)

The MPQ8873 provides a peak/valley current limit scheme designed to limit the peak/valley I_L to ensure that the switching currents remain within the device capabilities during overload conditions or during an output short circuit.

When the main power switch turns on, the chip monitors the increased I_L through the relevant operating main power switch. Once the peak I_L exceeds the peak current limit threshold, the relevant operating main power switch turns off immediately, and the relevant operating SR switch turns on to conduct and decrease I_L. The operating main power switch does not turn on again until I_L falls below the valley current limit threshold. This peak/valley current limit scheme ensures that I_L decreases sufficiently when the relevant operating main power switch is off. As a result, the average I_L is limited to a safe range.

If the internal EA's output level triggers the high clamp limit consecutively in a settled cycle, an over-current (OC) fault is recorded and over-current protection (OCP) is activated. There are

three optional OCP schemes: recoverable, latch-off, and no-response mode. The OC fault counter is screened during soft start.

When the SR switch is conducting, I_L drops. In some conditions (e.g. FCCM under light loads), the converter can actively conduct current away from the output. When I_L falls below 0A, a reverse inductor current occurs. To prevent damage to the part due to excessive reverse current, the MPQ8873 monitors the current entering the relevant operating SR switch from the output. If this current exceeds the reverse current limit threshold, the relevant operating SR switch turns off and the relevant operating main switch conducts to reduce the reverse current.

The OCP mode, peak/valley current limit threshold, and reverse current limit threshold can all be selected via the I²C interface.

Under-Voltage Protection (UVP) and Short-Circuit Protection (SCP)

A short circuit is the worst overload condition. In addition to OCP, the MPQ8873 provides short-circuit protection (SCP) in the event of a hard output short. SCP is triggered if V_{OUT} falls below the under-voltage (UV) threshold for a set period. Then an output UV fault is triggered, and the converter stops immediately. There are three optional output SCP/UVP modes: recoverable, latch-off, and no response mode. Output UV detection does not work during soft start.

The output UVP mode, threshold, and detection time can all be selected via the I²C interface.

Thermal Shutdown

Thermal shutdown is implemented to prevent the MPQ8873 from operating at exceedingly high temperatures. When the silicon die temperature exceeds the thermal shutdown threshold, an over-temperature (OT) fault is triggered and the whole chip shuts down. Thermal shutdown is auto-recoverable. Once the die temperature drops below its upper threshold, the chip starts up again and resumes normal operation.

The thermal shutdown threshold and recovery hysteresis can selected via the I²C interface. In addition, the MPQ8873 provides instantaneous die temperature information by reading the relevant register.

Fault Response

Once a fault status is confirmed, the converter turns off the main switches (Q1 and Q3) immediately after the minimum on time ends. The SR switches (Q2 and Q4) conduct I_L until it reaches 0A, regardless of whether the device is in DCM or FCCM. Finally, all four switches stop.

After a fault occurs, the converter operates based on the corresponding fault mode setting. There are three operating schemes: recoverable, latch-off, and no response mode.

In recoverable mode, the chip attempts to restart the converter. After the converter completely shuts down, a fault recovery timer starts. After a configurable delay time, the converter attempts to soft start automatically. If the fault condition is not removed, the converter reinitiates the fault protection and repeats the auto-recovery process in hiccup mode. If the fault condition is removed once soft start ends and the converter operates normally for a consecutive 30µs, then the fault status resets.

Latch-off mode stops the converter until power is recycled on the input supply or EN.

For OCP and UVP, no response mode can be selected. In this mode, the converter maintains switching in the peak/valley current limit unless thermal shutdown is triggered.

One-Time Programmable (OTP) Memory

The MPQ8873 provides a one-time programmable (OTP) memory for setting the custom default parameters.

MPS provides a GUI and I²C tool to configure the MPQ8873 during the development process. To configure in applications, contact an MPS FAE.

There are three OTP pages, each of which can be written once. The OTPCNT bit records the remaining OTP pages.

I²C INTERFACE

I²C Serial Interface Description

The I²C bus is a two-wire, bidirectional serial interface, consisting of a serial data line (SDA) and a serial clock line (SCL). The lines are externally pulled to a bus voltage when they are idle.

When connected to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. The MPQ8873 works as a slave-only device, which supports up to 400kbs of bidirectional data transfer in fast mode. This adds flexibility to the power supply solution. The output voltage, transition slew rate, and other converter parameters can be instantaneously controlled via the I²C interface.

The I²C interface uses VCC as its power source. If VCC cannot exceed its UVLO threshold, the SDA and SCL lines go to a high-impendence status and the I²C interface stops working.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 21).

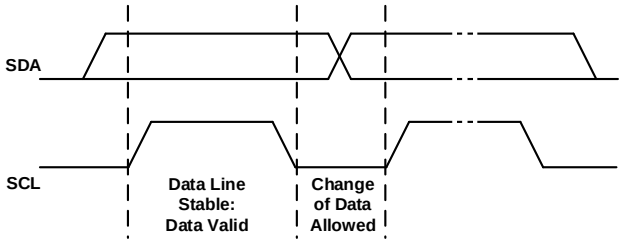


Figure 21: Bit Transfer on the I²C Bus

Start and Stop Conditions

The start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. A start command is defined as the SDA signal transitioning from high to low while the SCL line is high. A stop command is defined as the SDA signal transitioning from low to high while the SCL line is high (see Figure 22).

Start and stop commands are always generated by the master. The bus is considered busy after the start command. The bus is considered free again after a delay following a stop command. The bus stays busy if a repeated start (Sr) command is generated instead of a stop command. The start and repeated start commands are functionally identical.

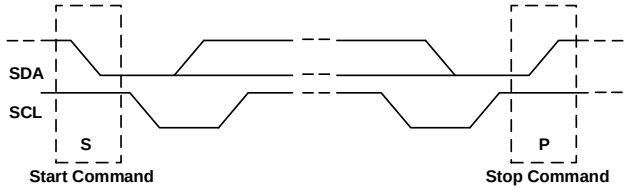


Figure 22: Start and Stop Conditions

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable (low) during the high period of the clock pulse.

Figure 23 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a write transmission, and a 1 indicates a read or a request for data. A data transfer is always terminated by a stop command generated by the master. However, if a master must communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

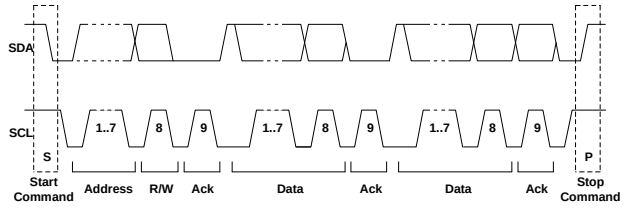


Figure 23: Complete Data Transfer

Write Sequence

A write sequence for the MPQ8873 requires a start command, a valid slave address, a register index byte, and a corresponding data byte for a single data update.

After receiving each byte, the MPQ8873 acknowledges this transfer by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPQ8873. The MPQ8873 then performs an update on the falling edge of the LSB byte.

Read Sequence

The typical MPQ8873 read sequence is 4 bytes long. It begins with a start command from the master, then a valid slave address followed by a register index byte. The read sequence differs from the write sequence in that a master's start command comes again. The bus direction then turns around with the rebroadcast of the slave address, with bit 1 indicating a read cycle. The following 4th byte contains the data being returned by the MPQ8873. That byte value in the data byte reflects the value of the register index that was queried before.

Chip Address

The MPQ8873 supports 16 different addresses from 00h to 0Fh, which can be preset in register 08h via the I²C bus.

When the master sends the address as an 8-bit value, the 7-bit address should be followed by a 0 or 1 to indicate a write or read operation, respectively. Figure 24 shows a write sequence, and Figure 25 shows a read sequence.

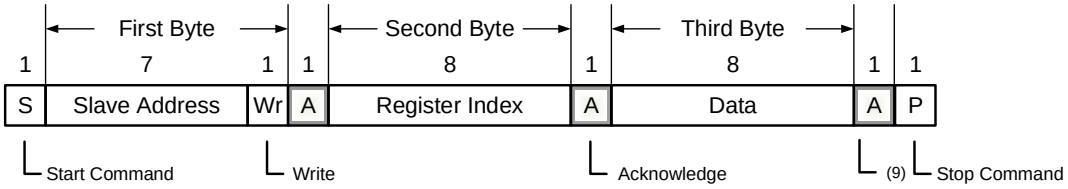


Figure 24: Write Sequence (9)

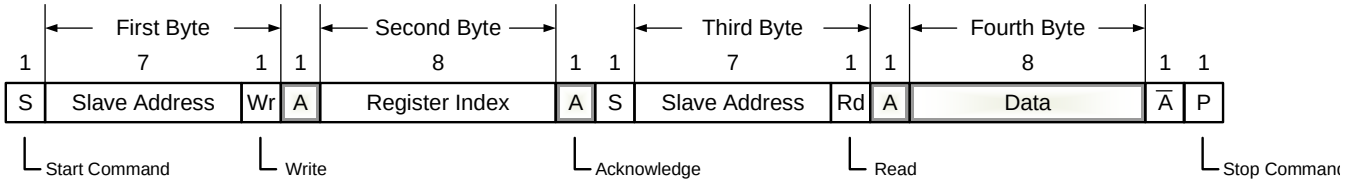


Figure 25: Read Sequence (9)

Note:

9) A dark gray outline is used during cycles in which the MPQ8873 owns or drives the SDA line. The master device drives all other cycles.

REGISTER MAP

Register Index	Default (10)	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
00h	32h	Reference Voltage							
01h	84h	Power Converter On/Off	RSVD (11)	RSVD (11)	V_{OUT} Dynamic Adjustment Step Time		V_{OUT} Divider Ratio		
02h	00h	SW1 Switching Rising Slew Rate		SW1 Switching Falling Slew Rate		SW2 Switching Rising Slew Rate		SW2 Switching Falling Slew Rate	
03h	08h	Synchronization Mode		Switching Frequency					
04h	00h	Frequency Spread Spectrum On/Off	Frequency Spread Spectrum Modulation Range			RSVD (11)	Frequency Spread Spectrum Modulation Cycle		
05h	7Fh	DCM/FCCM	Reverse Current Limit	Valley Current Limit			Peak Current Limit		
06h	00h	R_{FB} Compensation Network			R_{COMP} Compensation Network				
07h	00h	C_{HFP} Compensation Network			C_{COMP} Compensation Network				
08h	00h	I^2C Address				Cycle Extension in Buck-Boost On/Off	RSVD (11)	Constant-On-Time of Boost Switch in Buck-Boost Mode	
09h	EEh	Transition Hysteresis Between Buck and Buck-Boost		Threshold of Buck-Boost Transitioning to Buck		Transition Hysteresis between Boost and Buck-Boost		Threshold of Boost Transitioning to Buck-Boost	
0Ah	00h	Gain for Inductor Current Sense	DC Bias for Inductor Current Sense		Ramp Compensation Peak-to-Valley		Ramp Compensation		
0Bh	00h	Power-Good High Limit Hysteresis	Power-Good High Limit	Power-Good Low Limit Hysteresis	Power-Good Low Limit	Over-Current Counter		OCP Mode	
0Ch	60h	Fault Protection Mode	Delay Time for Fault Recovery		FB Threshold for UVP	Under-Voltage Counter		UVP Mode	
0Dh	04h	V_{IN} OVP Hysteresis	V_{IN} Over-Voltage Threshold		V_{OUT} OVP Hysteresis	V_{OUT} Over-Voltage Threshold		ENFBO	OVP Mode
0Eh	0Ah	RSVD (11)	Junction Temperature Range			Thermal Shutdown Hysteresis		Thermal Shutdown Threshold	
0Fh	00h	OTP Counter		Power Good Status	Input Over-Voltage Status	RSVD (11)	RSVD (11)	RSVD (11)	Thermal Shutdown Status
10h		Manufacturer Code [4:0]					Silicon Rev [2:0]		

Notes:

10) Initial factory defaults. The default value can be redefined if the OTP function is available.
11) This bit is not defined and reserved for future use. The reserved bits always read as 0. For compatibility with future devices, reserved bits should be written to “0” if accessed.

REGISTER DESCRIPTIONS

Register 00h							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0

Bit Field Definitions

Bits	Field Name	Description
[7:0]	REF[7:0]	Sets the reference voltage, calculated with the following equation: V_{REF} = REF[7:0] x 10mV (resolution: 10mV) In low input mode, REF[7:0] is invalid.

Register 01h							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
PWRCVTEN	INMD	RESERVED	DVSTEP1	DVSTEP0	FBDR2	FBDR1	FBDR0

Bit Field Definitions

Bits	Field Name	Description
7	PWRCVTEN	Enables power converter on/off control. 0: Disabled 1: Enabled
6	INMD	Selects normal mode or low-input mode. 0: Normal input mode 1: Low input mode
5	RESERVED	Reserved.
[4:3]	DVSTEP [1:0]	Sets the time of each step during soft start and output voltage dynamic adjustment mode (in µs). **00h**: 20; **01h**: 41.67 **02h**: 83.33; **03h**: 166.67
[2:0]	FBDR[2:0]	Sets the divider ratio for the reference voltage and output voltage. **00h**: 1; **01h**: 1/2 **02h**: 1/3; **03h**: 1/5 **04h**: 1/10; **05h**: 1/20 **06h/ 07h**: 1/30; -: - For example, if FBDR[2:0] = 04h, then V_{FB} = 1/10 x V_{OUT}.

REGISTER DESCRIPTIONS *(continued)*

Register 02h							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
SW1RSR1	SW1RSR0	SW1FSR1	SW1FSR0	SW2RSR1	SW2RSR0	SW2FSR1	SW2FSR0

Bit Field Definitions

Bits	Field Name	Description
[7:6]	SW1RSR [1:0]	Controls the switching rising slew rate for SW1. 00h: 1V/ns 01h: 2V/ns 02h: Reserved 03h: Reserved
[5:4]	SW1FSR [1:0]	Controls the switching falling slew rate for SW1. 00h: 1V/ns 01h: 2V/ns 02h: Reserved 03h: Reserved
[3:2]	SW2RSR [1:0]	Controls the switching rising slew rate for SW2. 00h: 1V/ns 01h: 2V/ns 02h: Reserved 03h: Reserved
[1:0]	SW2FSR [1:0]	Controls the switching falling slew rate for SW2. 00h: 1V/ns 01h: 2V/ns 02h: Reserved 03h: Reserved

Register 03h							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
SYNC1	SYNC0	FSW5	FSW4	FSW3	FSW2	FSW1	FSW0

Bit Field Definitions

Bits	Field Name	Description
[7:6]	SYNC[1:0]	Sets the synchronization mode. 00h: Disabled 01h: Synchronized clock input 02h: Synchronized clock output (with 0° phase shift) 03h: Synchronized clock output (with 180° phase shift)
[5:0]	FSW[5:0]	Sets the switching frequency (f_{SW}) of the converter. Although FSW[5:0] can be set up to 2.2MHz, the maximum f_{SW} supported by MPQ8873 is 1MHz. 00h to 03h: Reserved 04h to 2Ch: f_{SW} = FSW[5:0] x 50kHz (resolution: 50kHz) 2Dh to 3Fh: f_{SW} = 2.2MHz

REGISTER DESCRIPTIONS *(continued)*

Register 04h							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3]**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
FSSEN	FSSMR2	FSSMR1	FSSMR0	RESERVED	FSSMC2	FSSMC1	FSSMC0

Bit Field Definitions

Bits	Field Name	Description
7	FSSEN	Controls frequency spread spectrum (FSS). 0: Disabled 1: Enabled
[6:4]	FSSMR[2:0]	Sets the FSS modulation range (in 1‰ of f_{SW}). **00h** ±30 **01h** ±50 **02h** ±100 **03h** ±125 **04h** ±200 **05h** Reserved **06h/ 07h** ±300 - - For example, if FSSMR[2:0] = 02h and the switching frequency is configured to 450kHz, FSS mode modulates the oscillator between 405kHz and 495kHz (±10% x f_{SW}).
3	RESERVED	Reserved.
[2:0]	FSSMC[2:0]	Sets the FSS modulation frequency (in Hz). **00h** 250 **01h** 600 **02h** 1000 **03h** 1900 **04h** 2800 **05h** 3600 **06h** 7000 **07h** 8000

REGISTER DESCRIPTIONS *(continued)*

Register 05h							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
CCMEN	RVCLMT	VLCLMT2	VLCLMT1	VLCLMT0	PKCLMT2	PKCLMT1	PKCLMT0

Bit Field Definitions

Bits	Field Name	Description
7	CCMEN	Selects DCM or FCCM operation. 0: DCM 1: FCCM
6	RVCLMT	Sets the reverse current limit of the synchronous rectifier MOSFET. The reverse current limit is disabled in DCM. 0: -2.5A 1: -4.7A
[5:3]	VLCLMT[2:0]	Sets the valley current limit (in A). **00h** 1 **01h** 2 **02h** 3 **03h** 4 **04h** 5 **05h** 6 **06h** - **07h** - If the valley current limit set value exceeds the peak current limit, the valley current limit is invalid.
[2:0]	PKCLMT[2:0]	Sets the peak current limit (in A). **00h** 2 **01h** 3 **02h** 4 **03h** 5 **04h** 6 **05h** 7 **06h** - **07h** -

REGISTER DESCRIPTIONS *(continued)*

Register 06h							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
RFB2	RFB1	RFB0	RCOMP4	RCOMP3	RCOMP2	RCOMP1	RCOMP0

Bit Field Definitions

Bits	Field Name	Description
[7:5]	RFB[2:0]	Selects R_{FB}, calculated with the following equation: R_{FB} = 50kΩ + RFB[2:0] x 30kΩ
[4:0]	RCOMP[4:0]	Selects R_{COMP} (in kΩ).

00h	50	**01h**	173
02h	297	**03h**	420
04h	544	**05h**	667
06h	791	**07h**	914
08h	1038	**09h**	1161
0Ah	1284	**0Bh**	1408
0Ch	1531	**0Dh**	1655
0Eh	1778	**0Fh**	1902
10h	2025	**11h**	2148
12h	2272	**13h**	2395
14h	2519	**15h**	2642
16h	2766	**17h**	2889
18h	3012	**19h**	3136
1Ah	3259	**1Bh**	3383
1Ch	3506	**1Dh**	3630
1Eh	3753	**1Fh**	3877

Figure 26 shows the MPQ8873 control loop compensation network. Use Figure 26 to set values for register 06h and 07h.

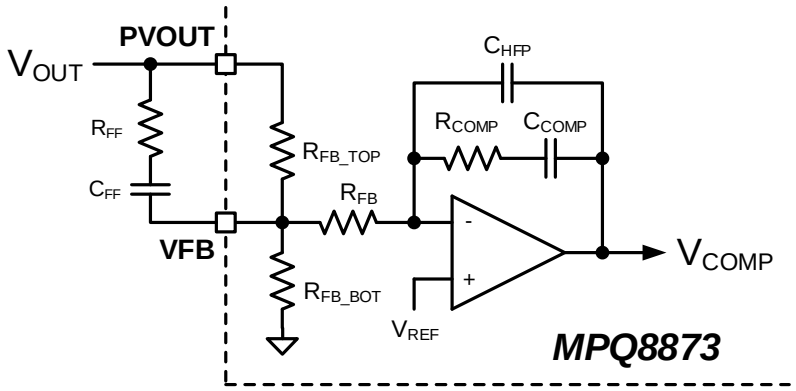


Figure 26: Control Loop Compensation Network

REGISTER DESCRIPTIONS *(continued)*

Register 07h							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
CHFP2	CHFP1	CHFP0	CCOMP4	CCOMP3	CCOMP2	CCOMP1	CCOMP0

Bit Field Definitions

Bits	Field Name	Description
[7:5]	CHFP[2:0]	Selects C_{HFP} (in pF). **00h** 0.5 **01h** 1 **02h** 3 **03h** 5 **04h** 6 **05h** 8 **06h** 9 **07h** 10
[4:0]	CCOMP[4:0]	Selects C_{COMP}, which can be set between 5pF and 160pF. 00h to 1Fh: C_{COMP} = (CCOMP[3:0] + 1) x 5pF

Register 08h							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
ADDR3	ADDR2	ADDR1	ADDR0	CYCEXTEN	RESERVED	BSTONT1	BSTONT0

Bit Field Definitions

Bit#	Field Name	Description
[7:4]	ADDR[3:0]	Sets the I²C bus address. The valid address is effective immediately once a write command is accepted.
3	CYCEXTEN	Enables cycle extension in buck-boost mode. If this bit is enabled, the switching frequency is half of its value set in buck-boost mode. 0: Disabled 1: Enabled
2	RESERVED	Reserved.
[1:0]	BSTONT[1:0]	Sets the COT percentage of the boost switch in buck-boost mode (in t_{SW}). **00h** 20% **01h** 30% **02h** 40% **03h** 50%

REGISTER DESCRIPTIONS *(continued)*

Register 09h							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
BKHYS1	BKHYS0	BKIN1	BKIN0	BSTHYS1	BSTHYS0	BSTOUT1	BSTOUT0

Bit Field Definitions

Bits	Field Name	Description
[7:6]	BKHYS[1:0]	Sets the transition hysteresis between buck and buck-boost mode. 00h: V_{IN} = 5% of V_{OUT} 01h: V_{IN} = 7.5% of V_{OUT} 02h: V_{IN} = 10% of V_{OUT} (invalid when BKIN[1:0] is set to 00h) 03h: V_{IN} = 12.5% of V_{OUT} (invalid when BKIN[1:0] is set to 00h)
[5:4]	BKIN[1:0]	Sets the threshold at which buck-boost mode transitions to buck mode when V_{IN} rises. 00h: V_{IN} = 110% of V_{OUT} 01h: V_{IN} = 120% of V_{OUT} 02h: V_{IN} = 125% of V_{OUT} 03h: V_{IN} = 130% of V_{OUT}
[3:2]	BSTHYS[1:0]	Sets the transition hysteresis between boost and buck-boost mode. 00h: V_{IN} = 5% of V_{OUT} 01h: V_{IN} = 7.5% of V_{OUT} 02h: V_{IN} = 10% of V_{OUT} 03h: V_{IN} = 12.5% of V_{OUT}
[1:0]	BSTOUT[1:0]	Sets the threshold at which boost mode transitions to buck-boost mode when V_{IN} rises. 00h: V_{IN} = 70% of V_{OUT} 01h: V_{IN} = 80% of V_{OUT} 02h: V_{IN} = 85% of V_{OUT} 03h: V_{IN} = 90% of V_{OUT}

Figure 27 shows MPQ8873 regions of operation. Use Figure 27 to set the values for register 09h.

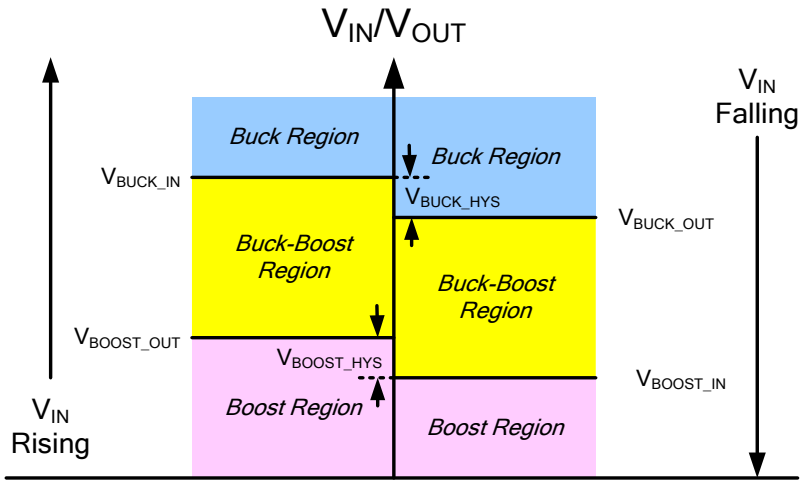


Figure 27: Regions of Operation

REGISTER DESCRIPTIONS *(continued)*

Register 0Ah							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
ILGAIN	ILBIAS1	ILBIAS0	RAMPPV1	RAMPPV0	RAMP2	RAMP1	RAMP0

Bit Field Definitions

Bits	Field Name	Description
7	ILGAIN	Sets the gain for the inductor current sense. 0: 13A/V 1: 10.4A/V
[6:5]	ILBIAS[1:0]	Sets the biased voltage for the inductor current sense (in mV). **00h** 200 **01h** 260 **02h** 320 **03h** 380
[4:3]	RAMPPV [1:0]	Sets the ramp compensation peak value to valley value (in mV). **00h** 40 **01h** 60 **02h** 80 **03h** 100
[2:0]	RAMP[2:0]	Sets the ramp compensation level (in mV/µs), calculated with the following equation: Ramp slope = (f_{SW} x 30) / (RAMP[2:0] + 1) Where f_{SW} is the switching frequency (in MHz).

REGISTER DESCRIPTIONS *(continued)*

Register 0Bh							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
PGVOHHYS	PGVOH	PGVOLHYS	PGVOL	OCCNT1	OCCNT0	OCPMD1	OCPMD0

Bit Field Definitions

Bits	Field Name	Description
7	PGVOHHYS	Sets the PG high limit hysteresis. 0: 4% of V_{REF} 1: 6% of V_{REF}
6	PGVOH	Sets the PG high limit (V_{OUT} rising edge). 0: V_{FB} = 112% of V_{REF} 1: V_{FB} = 117% of V_{REF}
5	PGVOLHYS	Sets the PG low limit hysteresis. 0: 4% of V_{REF} 1: 6% of V_{REF}
4	PGVOL	Sets the PG low limit (V_{OUT} falling edge). 0: V_{FB} = 90% of V_{REF} 1: V_{FB} = 85% of V_{REF}
[3:2]	OCCNT[1:0]	Sets the over-current (OC) counter for an OC fault (in t_{SW}, where t_{SW} = 1 / f_{SW}). **00h** 32 **01h** 64 **02h** 128 **03h** 256 The counter must count continuously. If the OC condition recovers while counting, the OC counter begins a recount. The OC counter is invalid during soft start, and the peak/valley current limit is valid.
[1:0]	OCPMD[1:0]	Selects the over-current protection (OCP) mode. 00h: Recoverable mode. If OCP is triggered, switching stops for some time (determined by the set delay time value). Then the part tries to soft start. If OCP is triggered again, the part enters hiccup mode 01h: Latch-off mode. If OCP is triggered, the part shuts down. Recycle the power on EN to restart the part 02h or 03h: No response mode. The part keeps switching, and uses the peak/valley current limit unless over-temperature protection (OTP) occurs The OC counter is invalid during soft start, and the peak/valley current limit is valid. OCP mode selection is only valid when OCP is triggered. If UVP and OCP are both triggered, UVP has a higher priority and OCP is invalid.

REGISTER DESCRIPTIONS *(continued)*

Register 0Ch							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
FLTMD	HCPTIME1	HCPTIME0	UVFB	UVCNT1	UVCNT0	UVPMD1	UVPMD0

Bit Field Definitions

Bits	Field Name	Description
7	FLTMD	Selects the fault protection mode. 0: Auto-reset mode. Once the fault is removed, the fault bits in Register 0Fh reset after 30µs 1: Latch-off mode. The power on EN must be cycled to reset the fault bits
[6:5]	HCPTIME [1:0]	Sets the delay time for fault recovery (in ms). **00h**: 2 **01h**: 4 **02h**: 8 **03h**: 16 This is only valid in hiccup mode. All fault recoveries (e.g. OCP delay) must have a delay.
4	UVFB	Sets the value of V_{FB} for under-voltage protection (UVP) (V_{OUT} falling edge). 0: V_{FB} = 50% of V_{REF} 1: V_{FB} = 75% of V_{REF}
[3:2]	UVCNT[1:0]	Sets the counter for under-voltage protection (UVP) (in t_{SW}, where t_{SW} = 1 / f_{SW}). **00h**: 2 **01h**: 4 **02h**: 8 **03h**: 16 The counter must count continuously. If the UV condition recovers while counting, the UV counter requires a recount. The UV counter should be shorter than the OC counter. UVP is invalid during soft start, and the peak/valley current limit is valid.
[1:0]	UVPMD[1:0]	Selects the UVP mode. 00h: Recoverable mode. If UVP is triggered, switching stops for a set time (determined by the set delay time value). Then the part tries to soft start. If UVP is triggered again, the part enters hiccup mode 01h: Latch-off mode. If UVP is triggered, the part shuts down. Recycle the power on EN to restart the part 02h or 03h: No response mode. The part keeps switching, and uses the peak/valley current limit unless over-temperature protection (OTP) occurs OCP mode selection is only valid when OCP is triggered. If UVP and OCP are both triggered, UVP has a higher priority and OCP is invalid.

REGISTER DESCRIPTIONS *(continued)*

Register 0Dh							
Bit[7] (R/W)	**Bit[6] (R/W)**	**Bit[5] (R/W)**	**Bit[4] (R/W)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1]**	**Bit[0] (R/W)**
VINOVHYS	VINOV1	VINOV0	VOUTOVHYS	VOUTOV1	VOUTOV0	ENFBO	OVPMD

Bit Field Definitions

Bits	Field Name	Description
7	VINOVHYS	Sets the V_{IN} over-voltage (OV) hysteresis. 0: 3% of V_{IN} 1: 5% of V_{IN}
[6:5]	VINOV[1:0]	Sets the V_{IN} OV threshold (rising edge) (in V). **00h** Disable **01h** 11 **02h** 21 **03h** 33
4	VOUTOVHYS	Sets the V_{OUT} OV recovery threshold. 0: 105% of V_{REF} 1: 100% of V_{REF}
[3:2]	VOUTOV [1:0]	Sets the V_{OUT} OV threshold (rising edge) (in V_{REF}). **00h** 110% **01h** 115% **02h** 120% **03h** 130%
1	ENFBO	Selects the VFB pin connection mode. 0: Disconnected from the internal circuit 1: Connect VFB to the internal error amplifier's feedback input
0	OVPMD	Selects the output over-voltage protection (OVP) mode. This bit is only valid for output OVP since input OVP recovers automatically. 0: Recoverable mode. If OVP is triggered, switching stops for a set time (determined by the delay time set value). Then the part tries to soft start. If OVP is triggered again, the part enters hiccup mode 1: Latch-off mode. If OVP is triggered, the part shuts down. Recycle the power on EN to restart the part

REGISTER DESCRIPTIONS *(continued)*

Register 0Eh							
Bit[7]	**Bit[6] (R)**	**Bit[5] (R)**	**Bit[4] (R)**	**Bit[3] (R/W)**	**Bit[2] (R/W)**	**Bit[1] (R/W)**	**Bit[0] (R/W)**
RESERVED	TJ2	TJ1	TJ0	THSHYS1	THSHYS0	THSTEMP1	THSTEMP0

Bit Field Definitions

Bits	Field Name	Description
7	RESERVED	Reserved.
[6:4]	TJ[2:0]	Sets the junction temperature (T_J) range (in °C). These bits are read-only. **00h** <25 **01h** 25 to 50 **02h** 50 to 75 **03h** 75 to 100 **04h** 100 to 125 **05h** 125 to 150 **06h** 150 to 160 **07h** 160 to 170
[3:2]	THSHYS[1:0]	Sets the thermal shutdown hysteresis (in °C). **00h** 25 **01h** 50 **02h/ 03h** 75 - -
[1:0]	THSTEMP [1:0]	Sets the thermal shutdown T_J threshold (rising edge) (in °C). **00h** 150 **01h** 160 **02h/ 03h** 170 - -

REGISTER DESCRIPTIONS *(continued)*

Register 0Fh							
Bit[7] (R)	**Bit[6] (R)**	**Bit[5] (R)**	**Bit[4] (R)**	**Bit[3] (R)**	**Bit[2] (R)**	**Bit[1] (R)**	**Bit[0] (R)**
OTPCNT1	OTPCNT0	PGOOD	VINOVP	RESERVED	RESERVED	RESERVED	THS

Bit Field Definitions

Bits	Field Name	Description
[7:6]	OTPCNT [1:0]	Indicates the number of available one-time programmable (OTP) pages. These bits are read-only. 00h: 0 OTP pages available 01h: 1 OTP page available 02h: 2 OTP pages available 03h: 3 OTP pages available
5	PGOOD	Indicates the power good status. This bit is read-only. 0: Power not good 1: Power good
4	VINOVP	Indicates the V_{IN} over-voltage (OV) status. This bit is read-only. 0: No V_{IN} OV condition has occurred 1: A V_{IN} OV condition has occurred
[3:1]	RESERVED	Reserved.
0	THS	Indicates the thermal shutdown status. This bit is read-only. 0: No thermal shutdown has occurred 1: Thermal shutdown has occurred

Register 10h							
Bit[7] (R)	**Bit[6] (R)**	**Bit[5] (R)**	**Bit[4] (R)**	**Bit[3] (R)**	**Bit[2] (R)**	**Bit[1] (R)**	**Bit[0] (R)**
MFG4	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0

Bit Field Definitions

Bits	Field Name	Description
[7:3]	MFG[4:0]	Manufacturer code. These bits are read-only.
[2:0]	REV[2:0]	Silicon revision code. These bits are read-only.

APPLICATION INFORMATION

Figure 28 shows the typical application circuit for the MPQ8873.

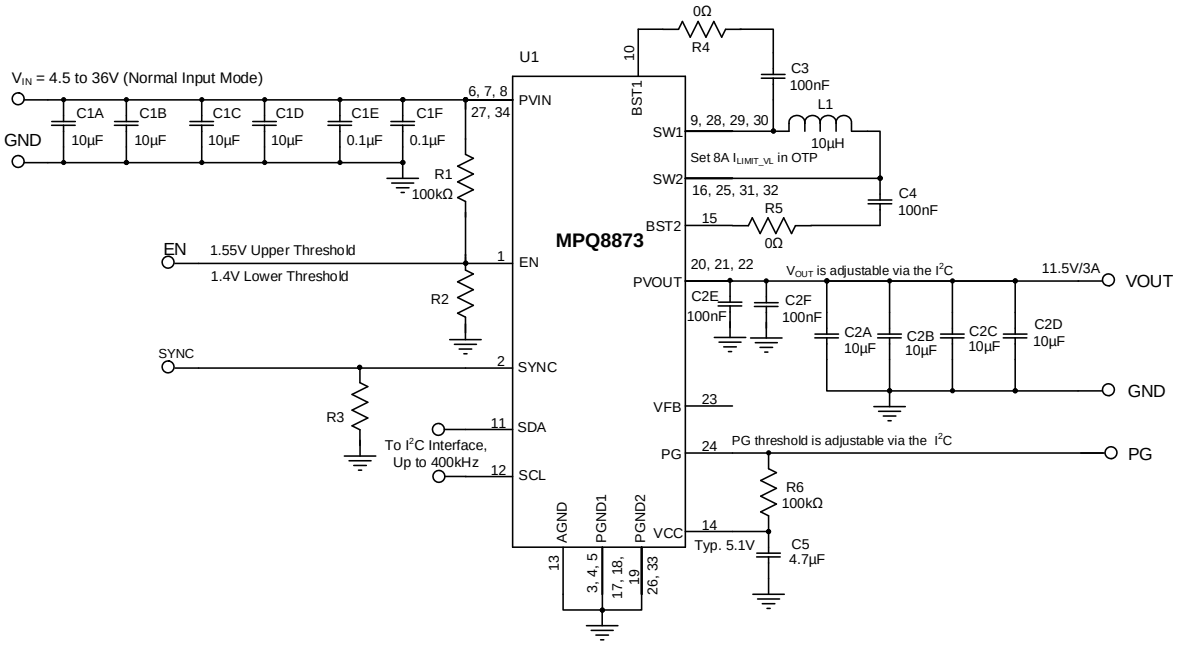


Figure 28: Typical Application Circuit

Table 1: Design Guide Index

Pin #	Name	Components	Design Guide Index
1	EN	R1	V_{IN} Under-Voltage Lockout (UVLO) Setting (EN, Pin 1)
2	SYNC	-	Synchronization Input/Output (SYNC, Pin 2)
3, 4, 5	PGND1	-	GND Connection (PGND1, Pins 3, 4, and 5; AGND, Pin 13; PGND2, Pins 17, 18, 19, 26, and 33)
6, 7, 8, 27, 34	PVIN	C1A, C1B, C1C, C1D, C1E, C1F	Selecting the Input Capacitors (PVIN, Pins 6, 7, 8, 27, and 34)
9, 28, 29, 30	SW1	L1	Selecting the Inductor (SW1, Pins 9, 28, 29, and 30; SW2, Pins 16, 25, 31, and 32)
10	BST1	C3	Floating Driver and Bootstrap Charging (BST1, Pin 10; BST2, Pin 15)
11	SDA	-	I²C Interface (SDA, Pin 11; SCL, Pin 12)
12	SCL	-	I²C Interface (SDA, Pin 11; SCL, Pin 12)
13	AGND	-	GND Connection (PGND1, Pins 3, 4, 5; AGND, Pin 13; PGND2, Pins 17, 18, 19, 26, and 33)
14	VCC	C5	Internal VCC (VCC, Pin 14)
15	BST2	C4	Floating Driver and Bootstrap Charging (BST1, Pin 10; BST2, Pin 15)
16, 25, 31, 32	SW2	L1	Selecting the Inductor (SW1, Pins 9, 28, 29, and 30; SW2, Pins 16, 25, 31, and 32)
17, 18, 19, 26, 33	PGND2	-	GND Connection (PGND1, Pins 3, 4, and 5; AGND, Pin 13; PGND2, Pins 17, 18, 19, 26, and 33)
20, 21, 22	PVOUT	C2A, C2B, C2C, C2D, C2E, C2F	Selecting the Output Capacitors (PVOUT, Pins 20, 21, and 22)
23	VFB	-	Setting the Feedback (VFB, Pin 23)
24	PG	R2	Power Good Indicator (PG, Pin 24)

V_{IN} Under-Voltage Lockout (UVLO) Setting (EN, Pin 1)

Enabled by External Logic High/Low Signal

EN is a digital control pin that turns the regulator on and off. Drive EN above its 0.85V logic threshold to activate the VCC regulator. Once VCC exceeds its under-voltage lockout (UVLO) threshold, VCC begins powering the internal control circuitry, and the integrated EN comparator works. Drive EN above its upper system threshold (1.55V) to enable the converter and initiate soft start. If EN is pulled below the lower system threshold (1.4V), the converter stops switching. The VCC regulator and control circuitry continue working until EN is pulled below its logic threshold (<0.5V).

Since EN has a 1MΩ pull-down resistor, float EN to shut down the chip. EN can be connected to a high-voltage bus (e.g. the PVIN pin) through a pull-up resistor. EN's maximum sink current is about 400μA, and it is recommended to use a 100kΩ pull-up resistor.

Configurable V_{IN} UVLO Threshold

The MPQ8873 has an internal, fixed UVLO threshold. In the normal input range, the rising threshold is about 3.6V, while the falling threshold is about 3.35V. For applications that require a higher UVLO point, place an external resistor divider between the PVIN and EN pins to raise the equivalent UVLO threshold (see Figure 29).

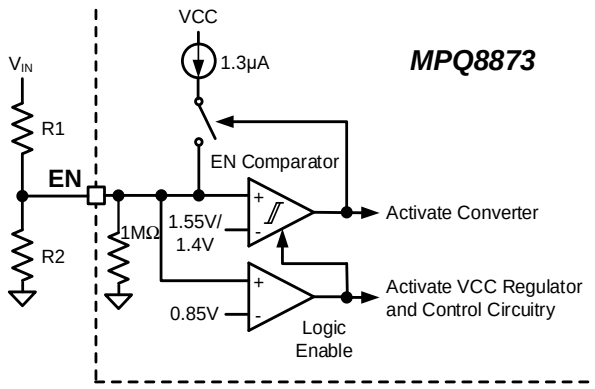


Figure 29: Adjustable UVLO Using EN Divider

The UVLO rising and falling thresholds can be calculated with Equation (12) and Equation (13), respectively:

$$V_{IN\_R} = \left(1 + \frac{R_1}{R_2 \,||\, 1M\Omega}\right) \times V_{EN\_R} \qquad (12)$$

$$V_{IN\_F} = \left(1 + \frac{R_1}{R_2 \,||\, 1M\Omega}\right) \times V_{EN\_F} - 1.3\mu A \times R_1 \qquad (13)$$

Where V_{EN_R} = 1.55V, and V_{EN_F} = 1.4V.

Synchronization Input/Output (SYNC, Pin 2)

The SYNC pin can be configured to synchronized input mode, synchronized output mode, or no response mode by Reg03h, bits[7:6]. If the SYNC pin is not used, float SYNC or pull it down to GND via a resistor (e.g. 100kΩ).

If synchronized input mode is enabled, the synchronization clock frequency ranges between 250kHz and 1MHz, and it must be 20% greater than the configured frequency set in the OTP register. The square-wave amplitude should have a peak above 1.4V, and a valley below 0.5V. The width of the synchronization pulse should exceed 200ns.

If synchronized output mode is enabled, the MPQ8873 can output the internal clock with a 0° or 180° phase shift. The output synchronization clock's duty cycle is constant at 50%.

Selecting the Input Capacitors (PVIN, Pins 6, 7, 8, 27, and 34)

The converter has a discontinuous input current when it operates in buck and buck-boost mode, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

It is strongly recommended to use another, lower-value capacitor (e.g. 0.1μF) with a small package size (0603) to absorb high-frequency switching noise. Place the small-sized capacitor as close to PVIN and GND as possible. Place two bypass capacitors on pins 6, 8, and 27.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating.

The RMS current in the input capacitor for buck mode and buck-boost mode can be estimated with Equation (14) and Equation (15), respectively:

$$I_{CIN\_BUCK} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (14)$$

$$I_{CINRMS\_BUCK\text{-}BOOST} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (\frac{1}{1-D_{Q3}} - \frac{V_{OUT}}{V_{IN}})} \quad (15)$$

Where D_{Q3} is the Q3 switch duty cycle. D_{Q3} is a fixed value set via register 08h.

The maximum RMS current for buck mode and buck-boost mode can be calculated with Equation (16) and Equation (17), respectively:

$$I_{CINRMS\_BUCK\_MAX} = \frac{I_{LOAD}}{2} \quad (16)$$

$$I_{CINRMS\_BUCK-BOOST\_MAX} = \frac{I_{LOAD}}{2 \times \sqrt{1-D_{Q3}}} \quad (17)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance for buck mode and buck-boost mode can be estimated with Equation (18) and (19), respectively:

$$\Delta V_{IN\_BUCK} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (18)$$

$$\Delta V_{IN\_BUCK\_BOOST} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \times (1 - D_{Q3})\right) \quad (19)$$

Selecting the Output Capacitors (PVOUT, Pins 20, 21, and 22)

The converter also has a discontinuous output current in boost and buck-boost mode, and requires a capacitor to supply AC current to the load while maintaining the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. The output capacitor's characteristics also affect regulatory control system's stability.

For the best results, use low-ESR capacitors to keep the output voltage ripple low. It is strongly recommended to use other, lower-value capacitors (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the small capacitors as close to the PVOUT and GND pins as possible.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple for boost mode and buck-boost mode can be estimated with Equation (20) and Equation (21), respectively:

$$\Delta V_{OUT\_BOOST} = I_{LOAD} \times \frac{1 - \frac{V_{IN}}{V_{OUT}}}{f_{SW} \times C_{OUT}} \quad (20)$$

$$\Delta V_{OUT\_BUCK-BOOST} = I_{LOAD} \times \frac{D_{Q3}}{f_{SW} \times C_{OUT}} \quad (21)$$

Where D_{Q3} is the Q3 switch duty cycle. D_{Q3} is a fixed value set in register 08h.

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The output ripple for boost mode and buck-boost mode can be estimated with Equation (22) and Equation (23), respectively:

$$\Delta V_{OUT\_BOOST} = I_{LOAD} \times (\frac{1 - \frac{V_{IN}}{V_{OUT}}}{f_{SW} \times C_{OUT}} + \frac{V_{OUT}}{V_{IN}} \times R_{ESR}) \quad (22)$$

$$\Delta V_{OUT\_BUCK-BOOST} = I_{LOAD} \times (\frac{D_{Q3}}{f_{SW} \times C_{OUT}} + \frac{1}{1-D_{Q3}} \times R_{ESR}) \quad (23)$$

Since C_{OUT} absorbs the output switching current, it requires an adequate ripple current rating. The RMS current in the output capacitor for boost mode and buck-boost mode can be estimated with Equation (24) and Equation (25), respectively:

$$I_{COUTRMS\_BOOST} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (24)$$

$$I_{COUTRMS\_BUCK\text{-}BOOST} = I_{LOAD} \times \sqrt{\frac{D_{Q3}}{1-D_{Q3}}} \quad (25)$$

Selecting the Inductor (SW1, Pins 9, 28, 29, and 30; SW2, Pins 16, 25, 31, and 32)

Connect an inductor between SW1 and SW2. A 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum inductor current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage. However, larger-value inductors also have a larger physical size, higher series resistance, and lower saturation current.

A good rule to determine the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum average inductor current. The inductance values for buck and boost mode can be calculated with Equation (26) and Equation (27), respectively:

$$L_{BUCK} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (26)$$

$$L_{BOOST} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (27)$$

The inductance value for buck-boost mode when $V_{IN} \geq V_{OUT}$ can be calculated with Equation (28):

$$L_{BUCK-BOOST,V_{IN} \geq V_{OUT}} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - t_1 \times f_{SW}) \quad (28)$$

The inductance value for buck-boost mode when $V_{IN} < V_{OUT}$ can be calculated with Equation (29):

$$L_{BUCK-BOOST,V_{IN} < V_{OUT}} = \frac{V_{IN}}{f_{SW} \times \Delta I_L} \times t_3 \times f_{SW} \quad (29)$$

Where ΔI_L is the peak-to-peak inductor ripple current, t_1 is the MOSFET Q1 turn-on time, and t_3 is the MOSFET Q3 turn-on time.

Choose the largest calculated result from the above equations to use as the inductance value.

The MPQ8873's internal peak current limit should be considered when selecting the inductor. The inductor's saturation current (I_{SAT}) minimum value should exceed the peak current limit, so that the inductor is never saturated.

Floating Driver and Bootstrap Charging (BST1, Pin 10; BST2, Pin 15)

The BST1 and BST2 capacitors (C3 and C4) range between 0.1µF and 1µF. A 0.1µF ceramic capacitor with a 0603 package size is recommended for most applications.

Place a resistor in series with the BST capacitor to reduce the SW rising rate and voltage spikes. This enhances EMI performance and reduces voltage stress at a high V_{IN}. Greater resistance is better for switching spike reduction but compromises efficiency. A tradeoff should be made between EMI and efficiency.

I²C Interface (SDA, Pin 11; SCL, Pin 12)

The MPQ8873 works as a slave-only device, which supports up to 400kbs of bidirectional data transfer in fast mode, adding flexibility to the power supply solution. Refer to the I²C Interface section on page 40 for details.

If the I²C interface is not used, it is recommended to connect these pins to the VCC pin through a resistor (e.g. 100kΩ).

Internal VCC (VCC, Pin 14)

The VCC capacitor (C5) should be between 1µF and 10µF. A 2.2µF or 4.7µF ceramic capacitor is typically recommended.

Most of the internal circuitry is powered by the internal 5V VCC regulator. This regulator uses V_{IN} as its input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, VCC is in full regulation and supplied by V_{IN}. When V_{IN} is below 5V, but V_{OUT} exceeds 5V, VCC is supplied by V_{OUT}, and regulates to about 4.85V. When both V_{IN} and V_{OUT} are below 5V, the VCC output drops.

Setting the Output Voltage

The MPQ8873 does not require an external resistor divider to set V_{OUT}. OTP registers 00h and 01h set V_{OUT} (see the Register Descriptions section on page 43).

Write the EA reference voltage in register 00h, REF[7:0]. The V_{OUT} divider ratio is configured by register 01h, bits FBDR[2:0]. V_{OUT} can be calculated with Equation (30):

$$V_{OUT} = \frac{REF[7:0] \times 10mV}{FBDR[2:0]} \quad (30)$$

For example, if REF[7:0] is set to 73h and FBDR[2:0] is set to 04h, then V_{OUT} = 115 x 10mV / (1/10) = 11.5V.

Setting the Feedback (VFB, Pin 23)

The VFB pin is disconnected from the internal circuit by default. Float VFB if it is not used.

VFB optimizes the converter's transient response. Set register 0Dh, bit[1] to 1, then connect VFB to the tap of the internal FB resistor divider.

A Type III compensation network is comprised of the internal existing Type II compensation network and an external RC compensation network tied between the PVOUT and VFB pins (see Figure 30 on page 60). The external RC network value is based on the detailed application and internal Type II compensation set-up.

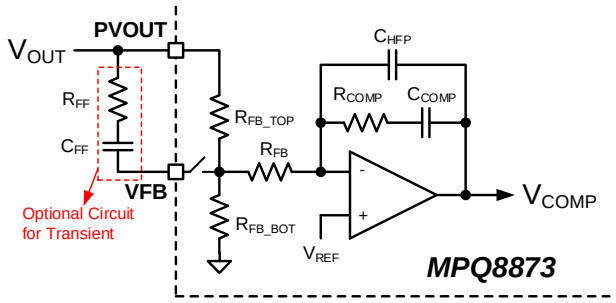


Figure 30: Control Loop Compensation Network

Even if VFB is enabled and connected to the internal EA, V_{OUT} can only be set by changing the I²C register, and cannot be set by adding an external resistor divider to the VFB pin. This is because the V_{OUT} / V_{FB} divider ratio changes after adding an external resistor divider. The MPQ8873's converter mode transition, power good (PG), over-voltage protection (OVP), and under-voltage protection (UVP) functions are related to the FB divider ratio. If the ratio is changed externally, the MPQ8873 cannot operate normally.

Power Good Indicator (PG, Pin 24)

The R_{PG} resistance (R2) value is recommended to be about 100kΩ.

The PG pin is connected to the open drain of an internal MOSFET. It should also be connected to a voltage source through an external pull-up resistor for power good indication. The PG pin is pulled down to ground during soft start, or if V_{OUT} is not within the allowable window. The PG threshold and hysteresis can be programmed via the I²C interface.

Float PG if it is not used.

GND Connection (PGND1, Pins 3, 4, and 5; AGND, Pin 13; PGND2, Pins 17, 18, 19, 26, and 33)

See the PCB Layout Guidelines section on page 61 for more details.

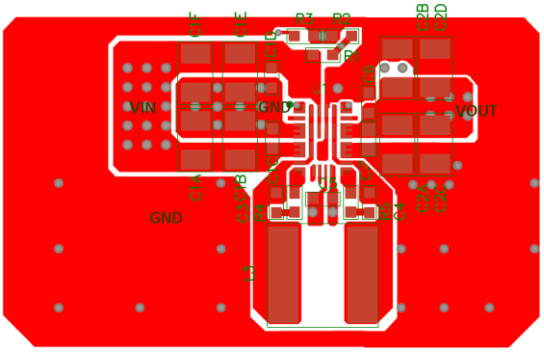
PCB Layout Guidelines [12]

Efficient PCB layout (especially input capacitor placement) is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 31 and follow the guidelines below:

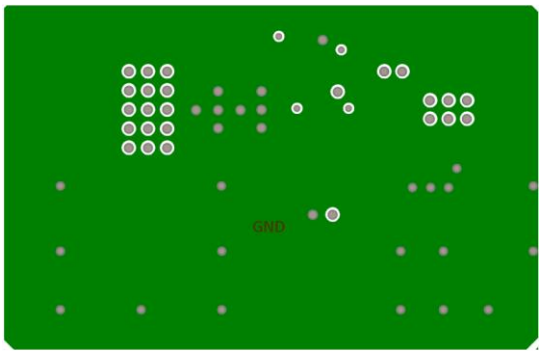
1. Place symmetric input/output capacitors and as close as possible to the PVIN and GND pins.
2. Use a large ground plane to connect directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
3. Ensure that the high-current paths (e.g. GND and PVIN/PVOUT) have short, direct, and wide traces.
4. Place the ceramic input capacitor — especially the small package size (0603) input/output bypass capacitor — as close to the PVIN/PVOUT and PGND pins as possible to minimize high-frequency noise.
5. Keep the connection between the input/output capacitor and PVIN/PVOUT as short and wide as possible.
6. Place bypass capacitors close to pins 6 and 8 (PVIN), pin 27 (PVIN), and all PVOUT pins.
7. Place the VCC capacitor as close to the VCC and GND pins as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Place the feedback resistors (if required) close to the chip to ensure that the trace connected to the FB pin is as short as possible.
10. Use multiple vias to connect the power planes to internal layers.

Note:

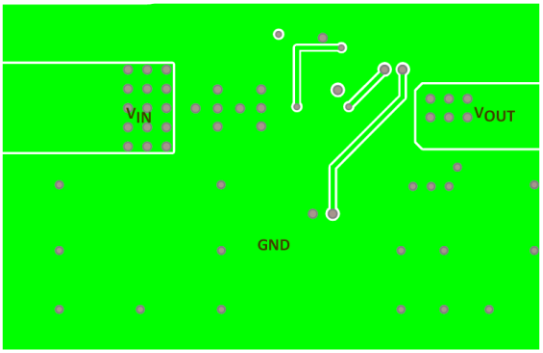
12) The recommended PCB layout is based on Figure 32 on page 62.



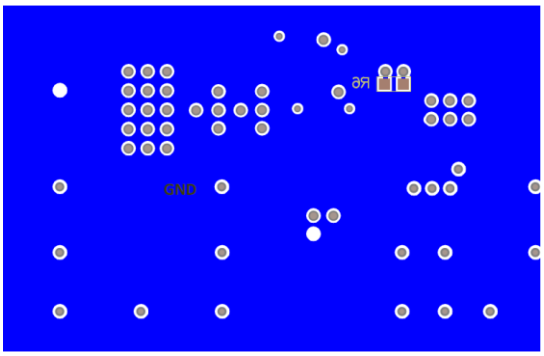
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 31: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

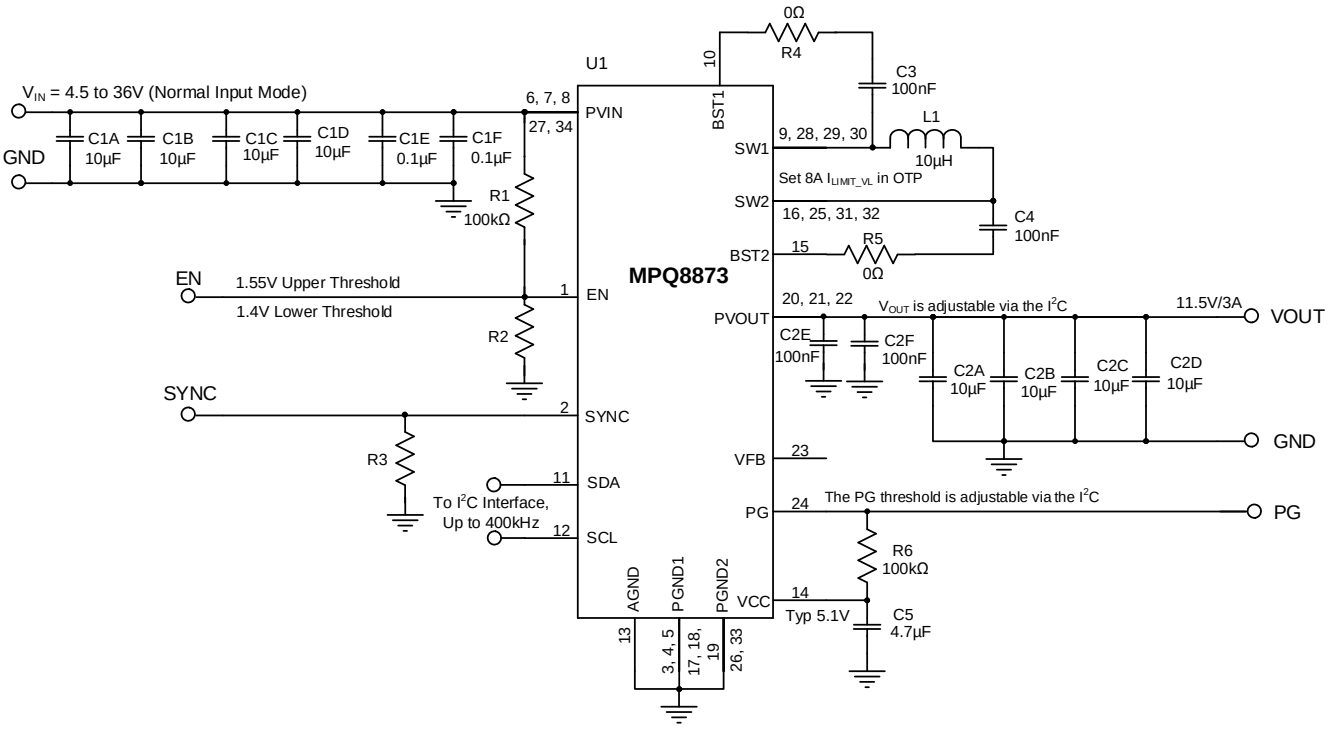


Figure 32: V_{OUT} = 11.5V, f_{SW} = 450kHz

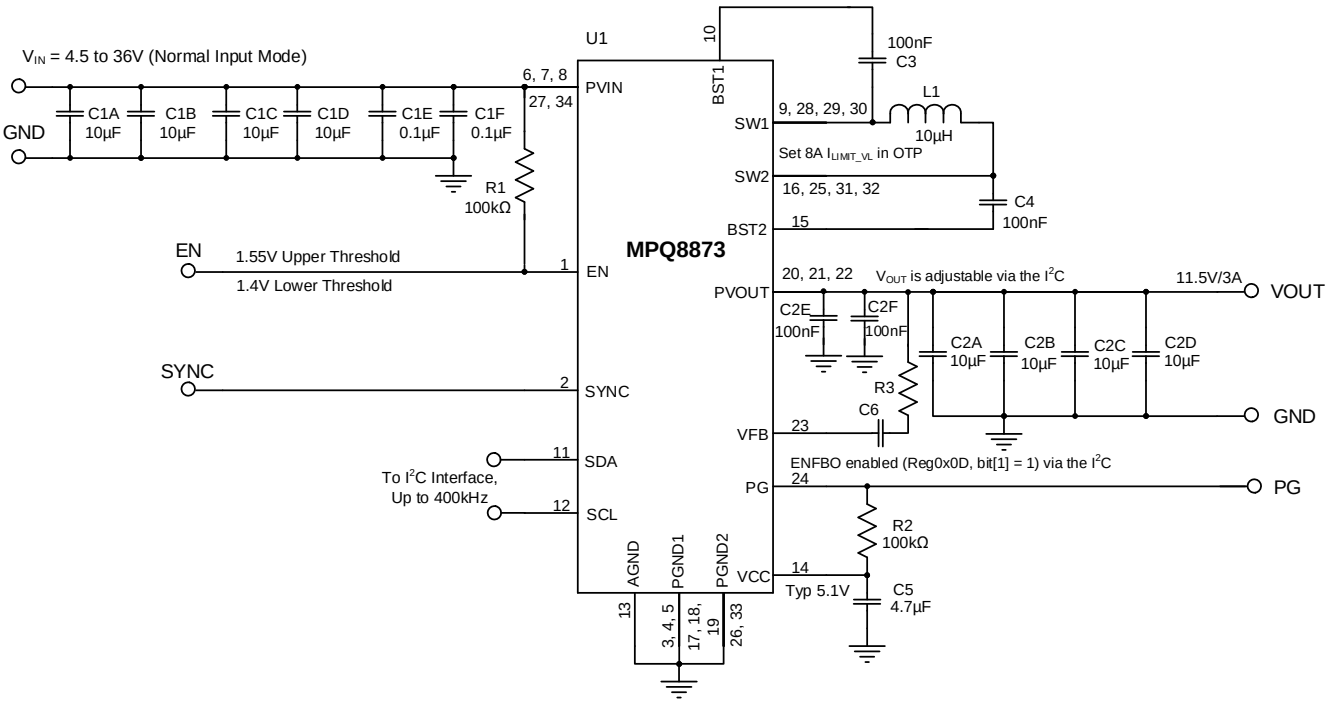


Figure 33: V_{OUT} = 11.5V, f_{SW} = 450kHz with External Forward RC Compensation

TYPICAL APPLICATION CIRCUITS *(continued)*

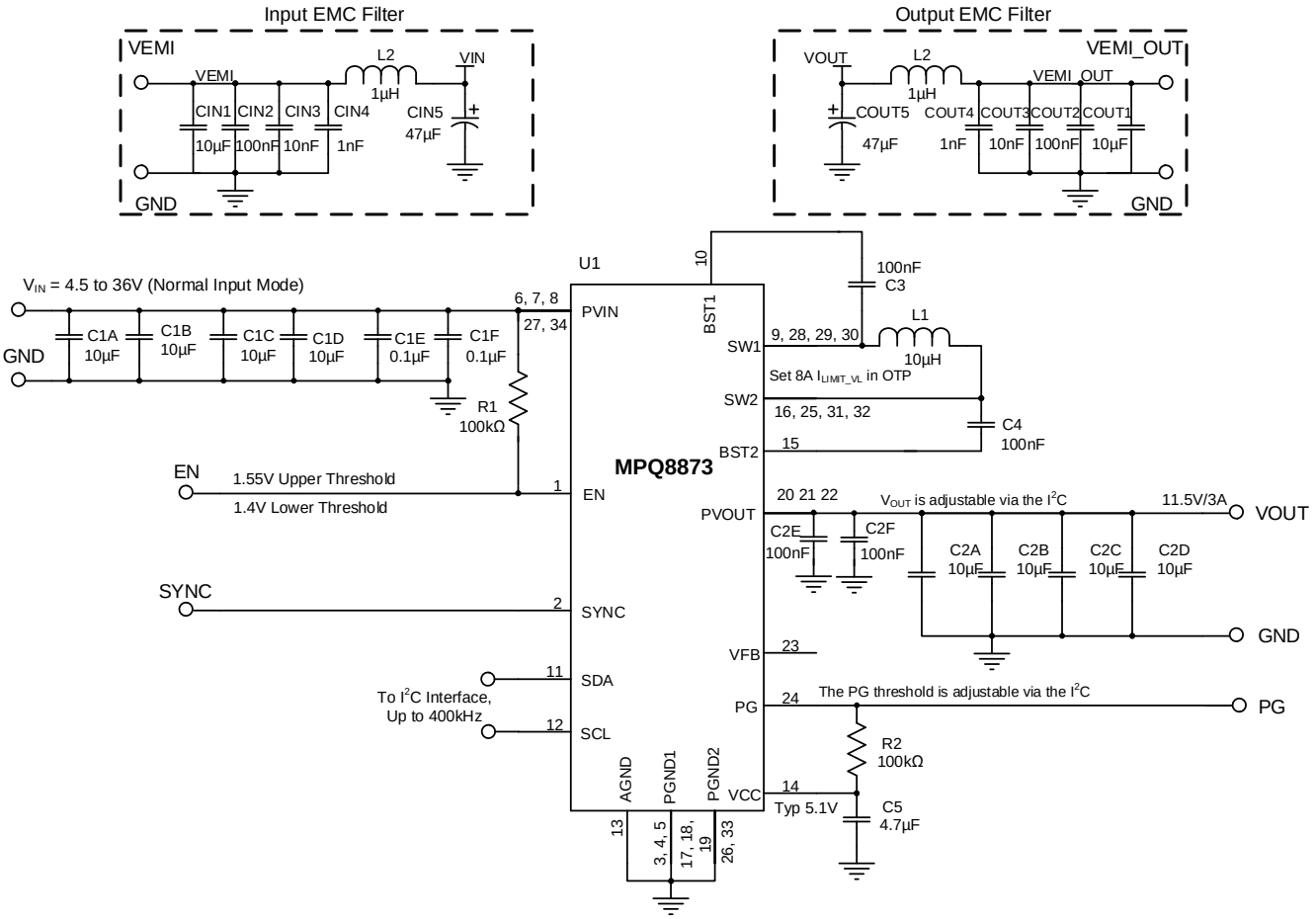
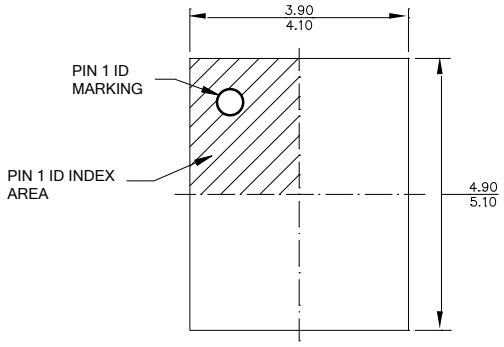


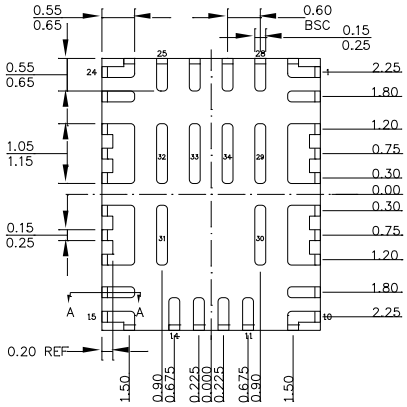
Figure 34: V_{OUT} = 11.5V, f_{SW} = 450kHz, with EMI Filters

PACKAGE INFORMATION

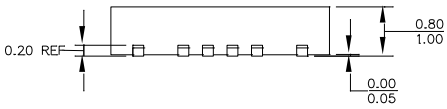
QFN-34 (4mmx5mm)
Wettable Flank



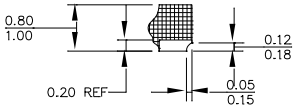
TOP VIEW



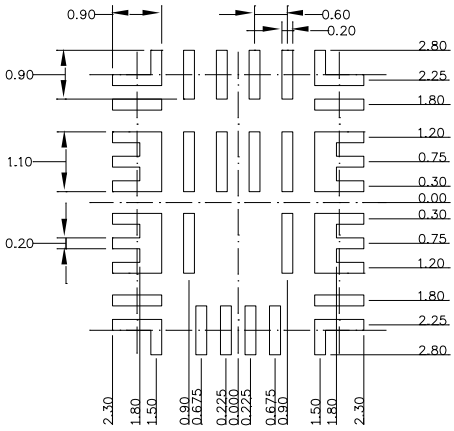
BOTTOM VIEW



SIDE VIEW



SECTION A-A

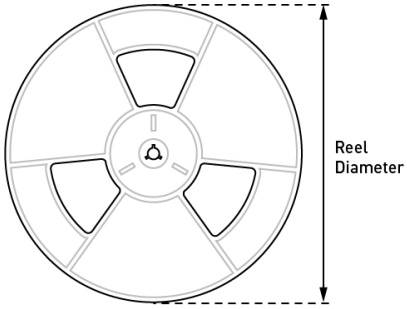


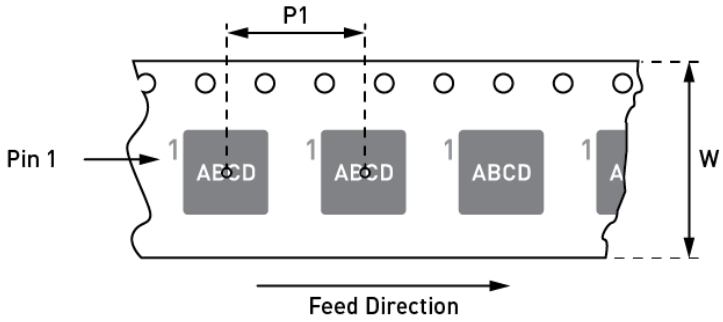
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ8873GVE-xxxx–Z	QFN-34 (4mmx5mm)	5000	13in	12mm	8mm
MPQ8873GVE-xxxx-AEC1–Z					

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/15/2021	Initial Release	-