commodore semiconductor group

CMOS

MPS

23C32

STATIC READ ONLY MEMORY
(4096x8)

23C32 STATIC READ ONLY MEMORY (4096x8)

DESCRIPTION

The 23C32 high performance read only memory is organized 4096 words by 8 bits with access times of less than 450 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations.

The 23C32 operates totally asynchronously. No clock input is required. The two programmable chip select inputs allow four 32K ROMS to be OR-tied without external decoding.

Designed to replace two 2716 16K EPROMS, the 23C32 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMS after prototyping with EPROMS.

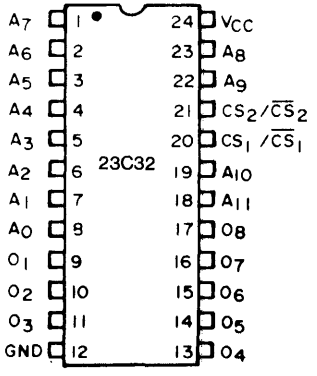
- 400mV Noise Immunity on Inputs
- 4096 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 450 ns
- Totally Static Operation
- TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- Pin Compatible with 2716 & 2532 EPROM
- Replacement for 2716
- 2708/2716 EPROMS Accepted as Program Data Inputs

ORDERING INFORMATION:

MXS 23C32

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	°C to +70°C
Storage Temperature	−65 C to +150°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
Applied Output Voltage	−0.5V to +7.0V
Applied Input Voltage	−0.5V to +7.0V

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D. C. CHARACTERISTICS (T_A = 0 C to +70 C, V_{CC} = 5.0V ± 5%, unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_{CC}	Power Supply Current		17	mA	F = 1 MHz
I_{CCS}	Stand-by Power Supply Current		10	μA	Chip Deselected
I_O	Output Leakage Current		10	μA	Chip Deselected
I_I	Input Load Current		10	μA	V_{CC} = Max. Gnd ≤ V_{IN} ≤ V_{CC}
V_{OL}	Output Low Voltage		0.4	Volts	V_{CC} = Min. I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4		Volts	V_{CC} = Min. I_{OH} = −400μA
V_{IL}	Input Low Voltage	−0.5	0.8	Volts	See Note 1
V_{IH}	Input High Voltage	2.0	V_{CC}+1	Volts	

A. C. CHARACTERISTICS (T_A = 0 C to +70 C, V_{CC} = 5.0V ± 5%, unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{ACC}	Address Access Time		450	ns	
t_{CO}	Chip Select Delay		200	ns	
t_{DF}	Chip Deselect Delay		100	ns	See Note 2
t_{OH}	Previous Data Valid After Address Change Delay	40		ns	

CAPACITANCE (T_A = 25°C, f = 1.0MHz, See Note 3)

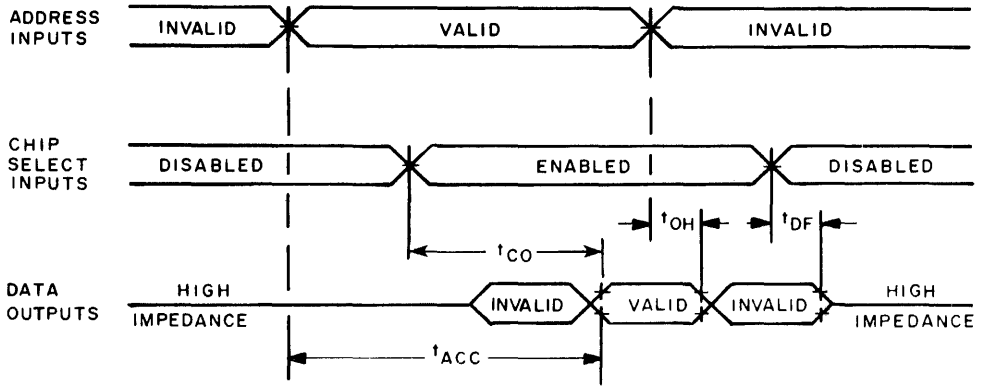
Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}	Input Capacitance		8	pF	All Pins except Pin under
C_{OUT}	Output Capacitance		10	pF	Test Tied to AC Ground

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

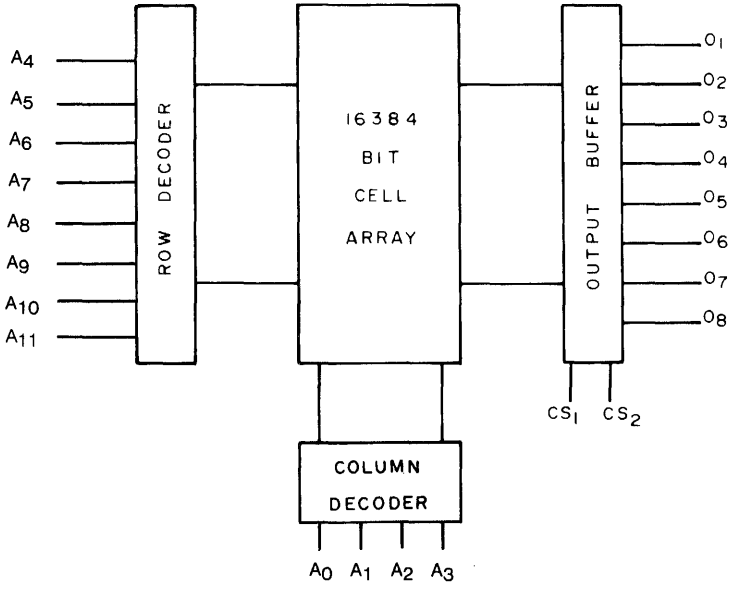
Note 2: Loading 1 TTL + 100 pF, input transition time: 20 ns
Timing measurement levels: input 1.5V, output 0.8V and 2.0V.

Note 3: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS

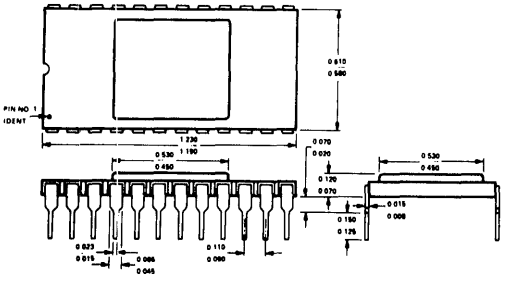


BLOCK DIAGRAM



PACKAGING DIAGRAM

CERAMIC PACKAGE



MOLDED PACKAGE