commodore semiconductor group

NMOS

MPS

6526

COMPLEX INTERFACE ADAPTER (CIA)

6526 COMPLEX INTERFACE ADAPTER (CIA)

PERIPHERALS

DESCRIPTION

The 6526 Complex Interface Adapter (CIA) is a 65XX bus compatible peripheral Interface device with extremely flexible timing and I/O capabilities.

FEATURES

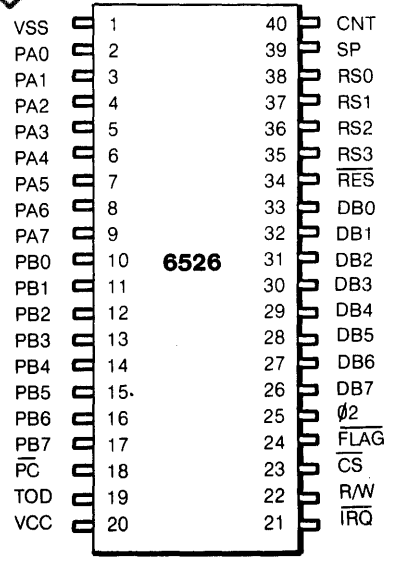
- 16 Individually programmable I/O lines
- 8 or 16-Bit handshaking on read or write
- 2 independent, linkable 16-Bit interval timers
- 24-hour (AM/PM) time of day clock with programmable alarm
- 8-Bit shift register for serial I/O
- 2TTL Load capability
- CMOS compatible I/O lines
- 1 or 2 MHz operation available

ORDERING INFORMATION

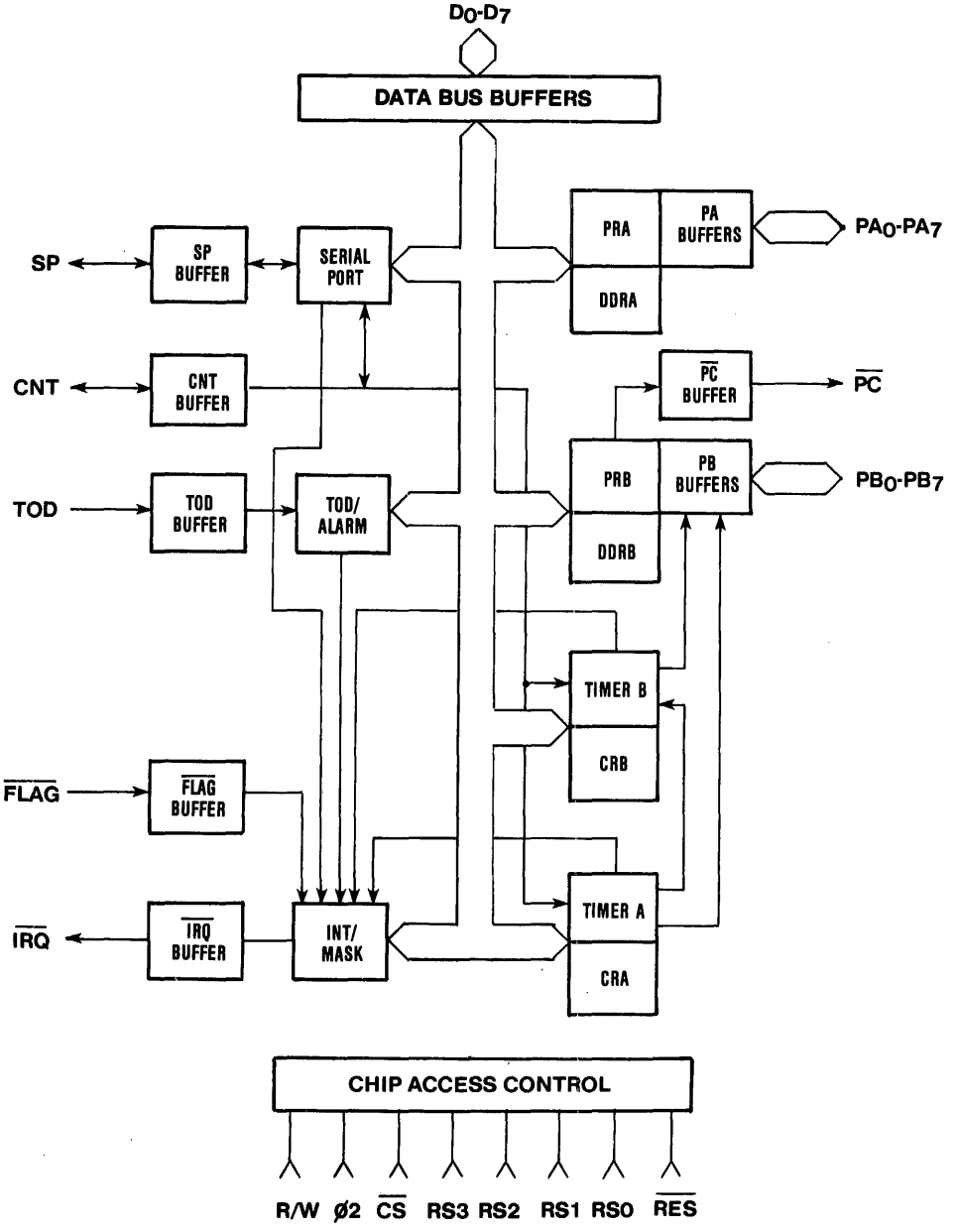
MXS 6526 ___

- FREQUENCY RANGE
  - NO SUFFIX = 1MHz
  - A = 2MHz
- PACKAGE DESIGNATOR
  - C = CERAMIC
  - P = PLASTIC

PIN CONFIGURATION



6526
BLOCK DIAGRAM



MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	−55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

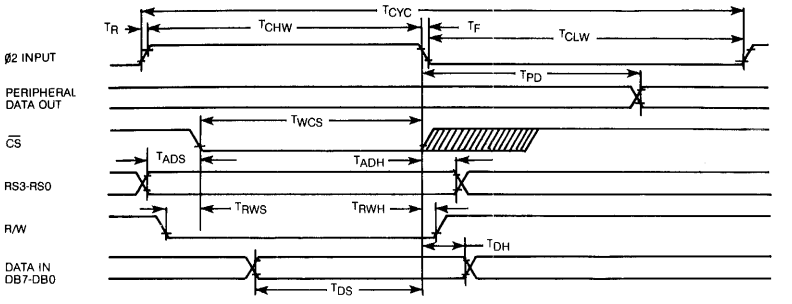
COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

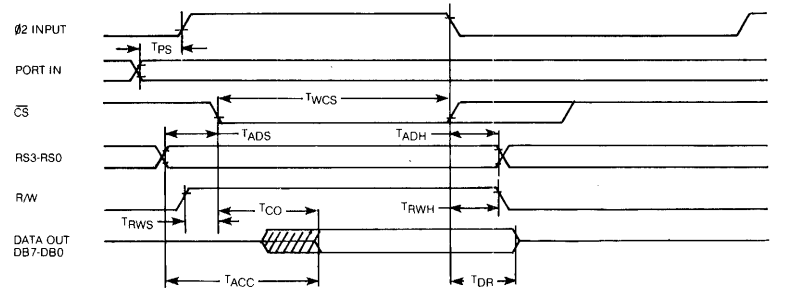
ELECTRICAL CHARACTERISTICS (V_{CC} ± 5%, VSS = 0v, T_A = 0-70°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	+ 2.4	—	V_{CC}	V
Input Low Voltage	V_{IL}	− 0.3	—	+0.8	V
Input Leakage Current; V_{IN} = V_{SS} + 5v (TOD, R/W, $\overline{FLAG}$, Ø2, $\overline{RES}$, RS0-RS3, $\overline{CS}$)	I_{IN}	—	1.0	2.5	μA
Port Input Pull-up Resistance	R_{PI}	3.1	5.0	—	KΩ
Output Leakage Current for High Impedance State (Three State); V_{IN} = 4v to 2.4v; (DB0-DB7, SP, CNT, $\overline{IRQ}$)	I_{TSI}	—	± 1.0	± 10.0	μA
Output High Voltage VCC=MIN, I_{LOAD} < −200μA (PA0-PA7, $\overline{PC}$ PB0-PB7, DB0-DB7)	V_{OH}	+ 2.4	—	V_{CC}	V
Output Low Voltage VCC = MIN, I_{LOAD} < 3.2mA	V_{OL}	—	—	+ 0.40	V
Output High Current (Sourcing); VOH > 2.4v (PA0-PA7, PB0-PB7, PC, DB0-DB7)	I_{OH}	−200	−1000	—	μA
Output Low Current (Sinking); VOL < .4 v (PA0-PA7, $\overline{PC}$, PB0-PB7, DB0-DB7)	I_{OL}	3.2	—	—	mA
Input Capacitance	C_{IN}	—	7	10	pf
Output Capacitance	C_{OUT}	—	7	10	pf
Power Supply Current	I_{CC}	—	70	100	mA

6526 WRITE TIMING DIAGRAM



6526 READ TIMING DIAGRAM



6526 INTERFACE SIGNALS

Ø2 — Clock Input

The Ø2 clock is a TTL compatible input used for internal device operation and as a timing reference for communicating with the system data bus.

CS — Chip Select Input

The CS input controls the activity of the 6526. A low level on CS while Ø2 is high causes the device to respond to signals on the R/W and address (RS) lines. A high on CS prevents these lines from controlling the 6526. The CS line is normally activated (low) at Ø2 by the appropriate address combination.

R/W — Read/Write Input

The R/W signal is normally supplied by the microprocessor and controls the direction of data transfers of the 6526. A high on R/W indicates a read (data transfer out of the 6526), while a low indicates a write (data transfer into the 6526).

RS3-RS0 — Address Inputs

The address inputs select the internal registers as described by the Register Map.

DB7-BD0 — Data Bus Inputs/Outputs

The eight data bus pins transfer information between the 6526 and the system data bus. These pins are high impedance inputs unless CS is low and R/W and Ø2 are high, to read the device. During this read, the data bus output buffers are enabled, driving the data from the selected register onto the system data bus.

IRQ — Interrupt Request Output

IRQ is an open drain output normally connected to the processor interrupt input. An external pullup resistor holds the signal high, allowing multiple IRQ outputs to be connected together. The IRQ output is normally off (high impedance) and is activated low as indicated in the functional description.

RES — Reset Input

A low on the RES pin resets all internal registers. The port pins are set as inputs and port registers to zero (although a read of the ports will return all highs because of passive pullups). The timer control registers are set to zero and the timer latches to all ones. All other registers are reset to zero.

6526 TIMING CHARACTERISTICS

Symbol	Characteristic	1MHz MIN	1MHz MAX	2MHz MIN	2MHz MAX	Unit
	ϕ_2 Clock					
T_{CYC}	Cycle Time	1,000	20,000	500	20,000	nS
T_R, T_F	Rise and Fall Time	—	25	—	25	nS
T_{CHW}	Clock Pulse Width (High)	420	10,000	200	10,000	nS
T_{CLW}	Clock Pulse Width (Low)	420	10,000	200	10,000	nS
	Write Cycle					
T_{PD}	Output Delay From ϕ_2	—	1,000	—	500	nS
T_{WCS}	$\overline{CS}$ low while ϕ_2 high	420	—	200	—	nS
T_{ADS}	Address Setup Time	0	—	0	—	nS
T_{ADH}	Address Hold Time	10	—	5	—	nS
T_{RWS}	R/W Setup Time	0	—	0	—	nS
T_{RWH}	R/W Hold Time	0	—	0	—	nS
T_{DS}	Data Bus Setup Time	150	—	75	—	nS
T_{DH}	Data Bus Hold Time	0	—	0	—	nS
	Read Cycle					
T_{PS}	Port Setup Time	300	—	150	—	nS
T_{WCS}(2)	$\overline{CS}$ low while ϕ_2 high	420	—	200	—	nS
T_{ADS}	Address Setup Time	0	—	0	—	nS
T_{ADH}	Address Hold Time	10	—	5	—	nS
T_{RWS}	R/W Setup Time	0	—	0	—	nS
T_{RWH}	R/W Hold Time	0	—	0	—	nS
T_{ACC}	Data Access from RS3-RS0	—	550	—	275	nS
T_{CO}(3)	Data Access from $\overline{CS}$	—	320	—	150	nS
T_{DR}	Data Release Time	50	—	25	—	nS

NOTES: 1 — All timings are referenced from V_{IL} max and V_{IH} min on inputs and V_{OL} max and V_{OH} min on outputs.
2 — T_{WCS} is measured from the later of ϕ2 high or $\overline{CS}$ low. $\overline{CS}$ must be low at least until the end of ϕ2 high.
3 — T_{CO} is measured from the later of ϕ2 high or $\overline{CS}$ low.
Valid data is available only after the later of T_{ACC} or T_{CO}.

REGISTER MAP

RS3	RS2	RS1	RS0	REG		
0	0	0	0	0	PRA	PERIPHERAL DATA REG A
0	0	0	1	1	PRB	PERIPHERAL DATA REG B
0	0	1	0	2	DDRA	DATA DIRECTION REG A
0	0	1	1	3	DDRB	DATA DIRECTION REG B
0	1	0	0	4	TA LO	TIMER A LOW REGISTER
0	1	0	1	5	TA HI	TIMER A HIGH REGISTER
0	1	1	0	6	TB LO	TIMER B LOW REGISTER
0	1	1	1	7	TB HI	TIMER B HIGH REGISTER
1	0	0	0	8	TOD 10THS	10THS OF SECONDS REGISTER
1	0	0	1	9	TOD SEC	SECONDS REGISTER
1	0	1	0	A	TOD MIN	MINUTES REGISTER
1	0	1	1	B	TOD HR	HOURS — AM/PM REGISTER
1	1	0	0	C	SDR	SERIAL DATA REGISTER
1	1	0	1	D	ICR	INTERRUPT CONTROL REGISTER
1	1	1	0	E	CRA	CONTROL REG A
1	1	1	1	F	CRB	CONTROL REG B

6526 FUNCTIONAL DESCRIPTION

I/O Ports (PRA, PRB, DDRA, DDRB)

Ports A and B each consist of an 8-bit Peripheral Data Register (PR) and an 8-bit Data Direction Register (DDR). If a bit in the DDR is set to a one, the corresponding bit in the PR is an output, if a DDR bit is set to a zero, the corresponding PR bit is defined as an input. On a READ, the PR reflects the information present on the actual port pins (PA0-PA7, PB0-PB7) for both input and output bits. Port A and Port B have passive pull-up devices as well as active pull-ups, providing both CMOS and TTL compatibility. Both ports have two TTL load drive capability. In addition to normal I/O operation, PB6 and PB7 also provide timer output functions.

Handshaking

Handshaking on data transfers can be accomplished using the $\overline{PC}$ output pin and the $\overline{FLAG}$ input pin. $\overline{PC}$ will go low for one cycle following a read or write of PORT B. This signal can be used to indicate "data ready" at PORT B or "data accepted" from PORT B. Handshaking on 16-bit data transfers (using both PORT A and PORT B) is possible by always reading or writing PORT A first. $\overline{FLAG}$ is a negative edge sensitive input which can be used for receiving the $\overline{PC}$ output from another 6526, or as a general purpose interrupt input. Any negative transition on $\overline{FLAG}$ will set the $\overline{FLAG}$ interrupt bit.

REG	NAME	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	PRA	PA_7	PA_6	PA_5	PA_4	PA_3	PA_2	PA_1	PA_0
1	PRB	PB_7	PB_6	PB_5	PB_4	PB_3	PB_2	PB_1	PB_0
2	DDRA	DPA_7	DPA_6	DPA_5	DPA_4	DPA_3	DPA_2	DPA_1	DPA_0
3	DDRB	DPB_7	DPB_6	DPB_5	DPB_4	DPB_3	DPB_2	DPB_1	DPB_0

Interval Timers (Timer A, Timer B)

Each interval timer consists of a 16-bit read-only Timer Counter and a 16-bit write-only Timer Latch. Data written to the timer are latched in the Timer Latch, while data read from the timer are the present contents of the Timer Counter. The timers can be used independently or linked for extended operations. The various timer modes allow generation of long time delays, variable width pulses, pulse trains and variable frequency waveforms. Utilizing the CNT input, the timers can count external pulses or measure frequency, pulse width and delay times of external signals. Each timer has an associated control register, providing independent control of the following functions:

Start/Stop
A control bit allows the timer to be started or stopped by the microprocessor at any time.

PB On/Off:
A control bit allows the timer output to appear on a PORT B output line (PB6 for TIMER A and PB7 for TIMER B). This function overrides the DDRB control bit and forces the appropriate PB line to an output.

Toggle/Pulse
A control bit selects the output applied to PORT B. On every timer underflow the output can either toggle or generate a single positive pulse of one cycle duration. The Toggle output is set high whenever the timer is started and is set low by $\overline{RES}$.

One-Short/Continuous
A control bit selects either timer mode. In one-shot mode, the timer will count down from the latched value to zero, generate an interrupt, reload the latched value, then stop. In continuous mode, the timer will count from the latched value to zero, generate an interrupt, reload the latched value and repeat the procedure continuously.

Force Load
A strobe bit allows the timer latch to be loaded into the timer counter at any time, whether the timer is running or not.

Input Mode:
Control bits allow selection of the clock used to decrement the timer. TIMER A can count Ø2 clock pulses or external pulses applied to the CNT pin. TIMER B can count Ø2 pulses, external CNT pulses, TIMER A underflow pulses or TIMER A underflow pulses while the CNT pin is held high.

The timer latch is loaded into the timer on any timer underflow, on a force load or following a write to the high byte of the prescaler while the timer is stopped. If the timer is running, a write to the high byte will load the timer latch, but not reload the counter.

READ (TIMER)

REG	NAME								
4	TA LO	TAL_7	TAL_6	TAL_5	TAL_4	TAL_3	TAL_2	TAL_1	TAL_0
5	TA HI	TAH_7	TAH_6	TAH_5	TAH_4	TAH_3	TAH_2	TAH_1	TAH_0
6	TB LO	TBL_7	TBL_6	TBL_5	TBL_4	TBL_3	TBL_2	TBL_1	TBL_0
7	TB HI	TBH_7	TBH_6	TBH_5	TBH_4	TBH_3	TBH_2	TBH_1	TBH_0

WRITE (PRESCALER)

REG	NAME								
4	TA LO	PAL_7	PAL_6	PAL_5	PAL_4	PAL_3	PAL_2	PAL_1	PAL_0
5	TA HI	PAH_7	PAH_6	PAH_5	PAH_4	PAH_3	PAH_2	PAH_1	PAH_0
6	TB LO	PBL_7	PBL_6	PBL_5	PBL_4	PBL_3	PBL_2	PBL_1	PBL_0
7	TB HI	PBH_7	PBH_6	PBH_5	PBH_4	PBH_3	PBH_2	PBH_1	PBH_0

Time of Day Clock (TOD)

The TOD clock is a special purpose timer for real-time applications. TOD consists of a 24-hour (AM/PM) clock with 1/10th second resolution. It is organized into 4 registers: 10ths of seconds, Seconds, Minutes and Hours. The AM/PM flag is in the MSB of the Hours register for easy bit testing. Each register reads out in BCD format to simplify conversion for driving displays, etc. The clock requires an external 60 Hz or 50 Hz (programmable) TTL level input on the TOD pin for accurate time-keeping. In addition to time-keeping, a programmable ALARM is provided for generating an interrupt at a desired time. The ALARM registers are located at the same addresses as the corresponding TOD registers. Access to the ALARM is governed by a Control Register bit. The ALARM is write-only; any read of a TOD address will read time regardless of the state of the ALARM access bit.

A specific sequence of events must be followed for proper setting and reading of TOD. TOD is automatically stopped whenever a write to the Hours register occurs. The clock will not start again until after a write to the 10ths of seconds register. This assures TOD will always start at the desired time. Since a carry

from one stage to the next can occur at any time with respect to a read operation, a latching function is included to keep all Time Of Day information constant during a read sequence. All four TOD registers latch on a read of Hours and remain latched until after a read of 10ths of seconds. The TOD clock continues to count when the output registers are latched. If only one register is to be read, there is no carry problem and the register can be read "on the fly," provided that any read of Hours is followed by a read of 10ths of seconds to disable the latching.

READ

REG	NAME								
8	TOD 10THS	0	0	0	0	T_8	T_4	T_2	T_1
9	TOD SEC	0	SH_4	SH_2	SH_1	SL_8	SL_4	SL_2	SL_1
A	TOD MIN	0	MH_4	MH_2	MH_1	ML_8	ML_4	ML_2	ML_1
B	TOD HR	PM	0	0	HH	HL_8	HL_4	HL_2	HL_1

WRITE
CRB_7=0 TOD
CRB_7=1 ALARM
(SAME FORMAT AS READ)

Serial Port (SDR)

The serial port is a buffered, 8-bit synchronous shift register system. A control bit selects input or output mode. In input mode, data on the SP pin is shifted into the shift register on the rising edge of the signal applied to the CNT pin. After 8 CNT pulses, the data in the shift register is dumped into the Serial Data Register and an interrupt is generated. In the output mode, TIMER A is used for the baud rate generator. Data is shifted out on the SP pin at ½ the underflow rate of TIMER A. The maximum baud rate possible is Ø2 divided by 4, but the maximum useable baud rate will be determined by line loading and the speed at which the receiver responds to input data. Transmission will start following a write to the Serial Data Register (provided TIMER A is running and in continuous mode). The clock signal derived from TIMER A appears as an output on the CNT pin. The data in the Serial Data Register will be loaded into the shift register then shift out to the SP pin when a CNT pulse occurs. Data shifted out becomes valid on the falling edge of CNT and remains valid until the next falling edge. After 8 CNT pulses, an interrupt is generated to indicate more data can be sent. If the Serial Data Register was loaded with new information prior to this interrupt, the new data will automatically be loaded into the shift register and transmission will continue. If the microprocessor stays one byte ahead of the shift register, transmission will be continuous. If no further data is to be transmitted, after the 8th CNT pulse, CNT will return high and SP will remain at the level of the last data bit transmitted. SDR data is shifted out MSB first and serial input data should also appear in this format.

The bidirectional capability of the Serial Port and CNT clock allows many 6526 devices to be connected to a common serial communication bus on which one 6526 acts as a master, sourcing data and shift clock, while all other 6526 chips act as slaves. Both CNT and SP outputs are open drain to allow such a common bus. Protocol for master/slave selection can be transmitted over the serial bus, or via dedicated handshaking lines.

REG	NAME								
C	SDR	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Interrupt Control (ICR)

There are five sources of interrupts on the 6526: underflow from TIMER A, underflow from TIMER B, TOD ALARM, Serial Port full/empty and $\overline{FLAG}$. A single register provides masking and interrupt information. The Interrupt Control Register consists of a write-only MASK register and a read-only DATA register. Any interrupt will set the corresponding bit in the DATA register. Any interrupt which is enabled by the MASK register will set the IR bit (MSB) of the DATA register and bring the $\overline{IRQ}$ pin low. In a multi-chip system, the IR bit can be polled to detect which chip has generated an interrupt request. The interrupt DATA register is cleared and the $\overline{IRQ}$ line returns high following a read of the DATA register. Since each interrupt sets an interrupt bit regardless of the MASK, and each interrupt bit can be selectively masked to prevent the generation of a processor interrupt, it is possible to intermix polled interrupts with true interrupts. However, polling the IR bit will cause the DATA register to clear, therefore, it is up to the user to preserve the information contained in the DATA register if any polled interrupts were present.

The MASK register provides convenient control of individual mask bits. When writing to the MASK register, if bit 7 (SET/$\overline{CLEAR}$) of the data written is a ZERO, any mask bit written with a one will be cleared, while those mask bits written with a zero will be unaffected. If bit 7 of the data written is a ONE, any mask bit written with a one will be set, while those mask bits written with a zero will be unaffected. In order for an interrupt flag to set IR and generate an Interrupt Request, the corresponding MASK bit must be set.

READ (INT DATA)

REG	NAME								
D	ICR	IR	0	0	FLG	SP	ALRM	TB	TA

WRITE (INT MASK)

REG	NAME								
D	ICR	S/$\overline{C}$	X	X	FLG	SP	ALRM	TB	TA

PERIPHERALS

CONTROL REGISTERS

There are two control registers in the 6526, CRA and CRB. CRA is associated with TIMER A and CRB is associated with TIMER B. The register format is as follows:

CRA:

Bit	Name	Function
0	START	1=START TIMER A, 0=STOP TIMER A. This bit is automatically reset when underflow occurs during one-shot mode.
1	PBON	1=TIMER A output appears on PB6, 0=PB6 normal operation.
2	OUTMODE	1=TOGGLE, 0=PULSE
3	RUNMODE	1=ONE-SHOT, 0=CONTINUOUS
4	LOAD	1=FORCE LOAD (this is a STROBE input, there is no data storage, bit 4 will always read back a zero and writing a zero has no effect).
5	INMODE	1=TIMER A counts positive CNT transitions, 0=TIMER A counts Ø2 pulses.
6	SPMODE	1=SERIAL PORT output (CNT sources shift clock), 0=SERIAL PORT input (external shift clock required).
7	TODIN	1=50 Hz clock required on TOD pin for accurate time, 0=60 Hz clock required on TOD pin for accurate time.

CRB:

Bit	Name	Function
		(Bits CRB0-CRB4 are identical to CRA0-CRA4 for TIMER B with the exception that bit 1 controls the output of TIMER B on PB7).
5,6	INMODE	Bits CRB5 and CRB6 select one of four input modes for TIMER B as: CRB6 CRB5 0 0 TIMER B counts Ø2 pulses. 0 1 TIMER B counts positive CNT transistions. 1 0 TIMER B counts TIMER A underflow pulses. 1 1 TIMER B counts TIMER A underflow pulses while CNT is high.
7	ALARM	1=writing to TOD registers sets ALARM, 0=writing to TOD registers sets TOD clock.

REG	NAME	TOD IN	SP MODE	IN MODE	LOAD	RUN MODE	OUT MODE	PB ON	START
E	CRA	0=60Hz	0=INPUT	0=Ø2	1=FORCE LOAD	0=CONT.	0=PULSE	0=PB6 OFF	0=STOP
		1=50Hz	1=OUTPUT	1=CNT	(STROBE)	1=O.S.	1=TOGGLE	1=PB6 ON	1=START

TA

REG	NAME	ALARM	IN MODE		LOAD	RUN MODE	OUT MODE	PB ON	START
F	CRB	0=TOD	0	0=Ø2	1=FORCE LOAD	0=CONT.	0=PULSE	0=PB7 OFF	0=STOP
			0	1=CNT					
			1	0=TA					
		1= ALARM	1	1=CNT•TA	(STROBE)	1=O.S.	1=TOGGLE	1=PB7 ON	1=START

TB

All unused register bits are unaffected by a write and are forced to zero on a read.