commodore semiconductor group

NMOS

MPS

6551

ASSYNCHRONOUS COMMUNICATION INTERFACE ADAPTER

6551 ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER

PERIPHERALS

CONCEPT:

The 6551 is an Asynchronous Communication Adapter (ACIA) intended to provide for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

FEATURES:

- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud).
- Programmable interrupt and status register to simplify software design.
- Single +5 volt power supply.
- Serial echo mode.
- False start bit detection.
- 8-bit bi-directional data bus for direct communication with the microprocessor.
- External 16x clock input for non-standard baud rates (up to 125 Kbaud).
- Programmable: word lengths; number of stop bits; and parity bit generation and detection.
- Data set and modem control signals provided.
- Parity: (odd, even, none, mark, space).
- Full-duplex or half-duplex operation.
- 5, 6, 7, 8 and 9 bit transmission.

ORDER NUMBER

MXS 6551 —

- FREQUENCY RANGE
  - NO SUFFIX = 1 MHz
  - A = 2 MHz
  - B = 3 MHz
- PACKAGE DESIGNATOR
  - C = CERAMIC
  - P = PLASTIC

6551 PIN CONFIGURATION

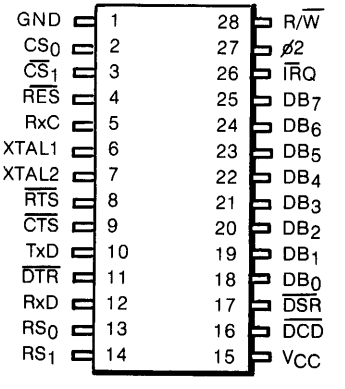
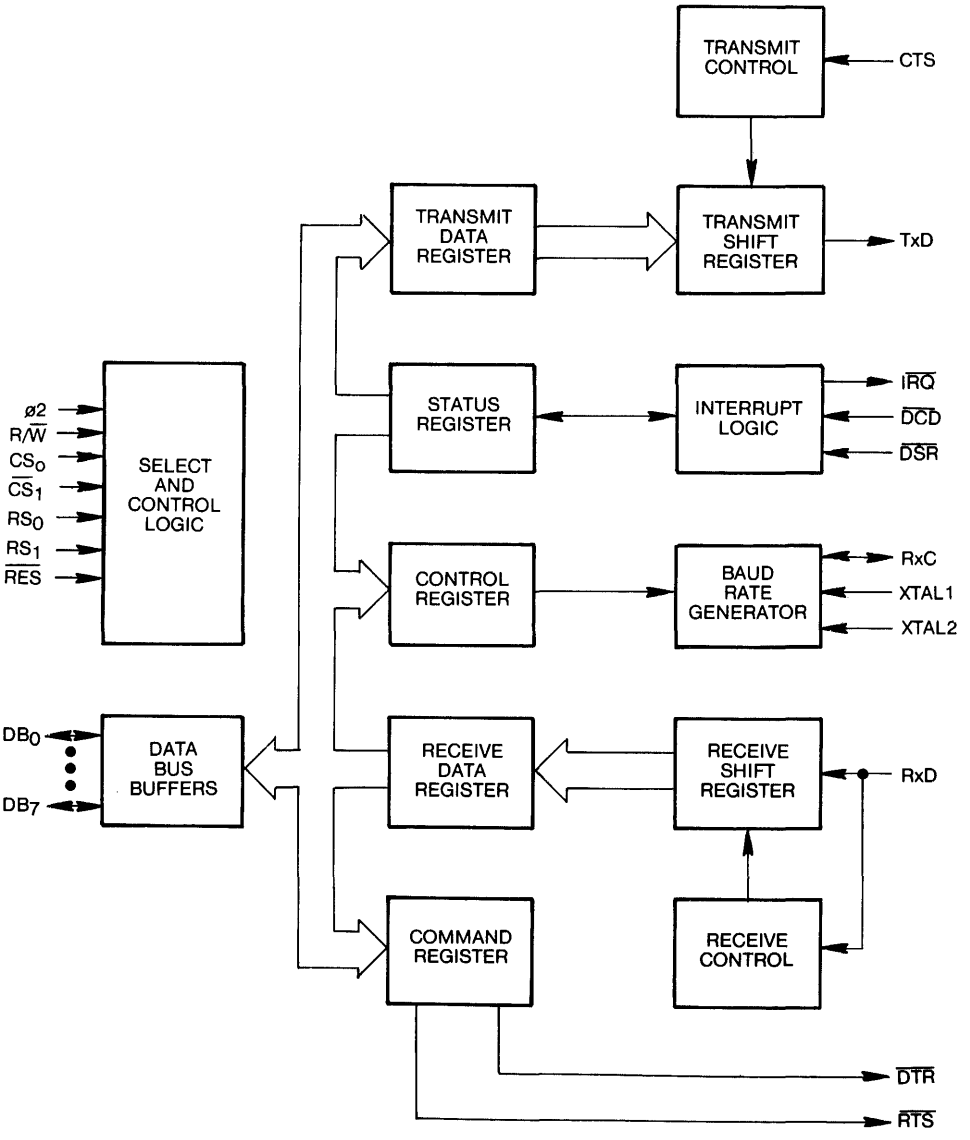


Figure 1. Block Diagram



MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	−55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

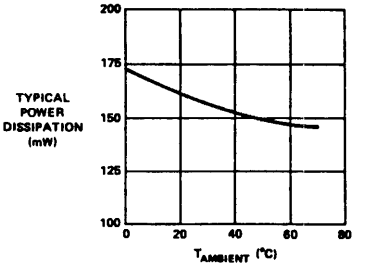
COMMENT

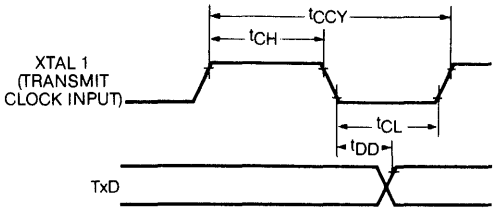
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V + 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Input Leakage Current: V_{IN}=0 to 5V. (ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS_0}$, CS_1, RS_0, RS_1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	—	±1.0	±2.5	µA
Input Leakage Current for High Impedance State (Three State)	I_{TSI}	—	±2.0	±10.0	µA
Output High Voltage: I_{LOAD}=−100µA	V_{OH}	2.4	—	—	V
Output Low Voltage: I_{LOAD} = 1.6mA (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	—	—	0.4	V
Output High Current (Sourcing): V_{OH}=2.4V	I_{OH}	−250	—	—	µA
Output Low Current (Sinking): V_{OL}=0.4V	I_{OL}	1.6	—	—	µA
Output Leakage Current (off state): V_{OUT}=5V ($\overline{IRQ}$)	I_{OFF}	—	1.0	10.0	µA
Clock Capacitance (ø2)	C_{CLK}	—	—	20	pF
Input Capacitance (except XTAL1 and XTAL2)	C_{IN}	—	—	10	pF
Output Capacitance	C_{OUT}	—	—	10	pF
Power Dissipation	P_D	—	170	300	mw

Power Dissipation vs Temperature





NOTE: TxD rate is 1/16 TxC rate.

Figure 4a. Transmit Timing with External Clock

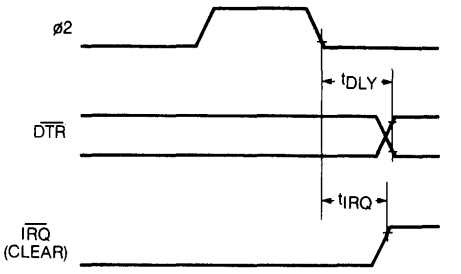
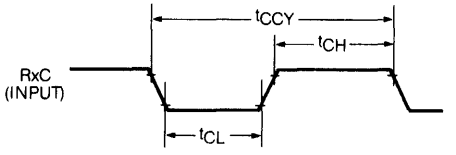


Figure 4b. Interrupt and RTS Timing



NOTE: RxD rate is 1/16 RxC rate.

Figure 4c. Receive External Clock Timing

TRANSMIT/RECEIVE CHARACTERISTICS

Characteristic	Symbol	6551 Min	6551 Max	6551A Min	6551A Max	Unit
Transmit/Receive Clock Rate	t_{CCY}	400*	—	400*	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	175	—	ns
Transmit/Receive Clock Low Time	t_{CL}	175	—	175	—	ns
XTAL1 to TxD Propagation Delay	t_{DD}	—	500	—	500	ns
$\overline{RTS}$ Propagation Delay	t_{RTS}	—	500	—	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	500	—	500	ns

(t_r, t_f = 10 to 30 nsec)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

INTERFACE SIGNAL DESCRIPTION

$\overline{RES}$ (Reset)
During system initialization a low on the $\overline{RES}$ input will cause internal registers to be cleared.

ø2 (Input Clock)
The input clock is the system ø2 clock and is used to trigger all data transfers between the system microprocessor and the 6551.

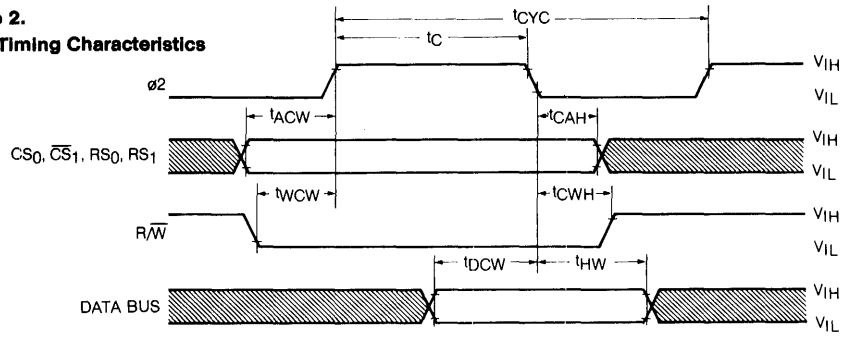
R/$\overline{W}$ (Read/Write)
The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the 6551. A low on the R/$\overline{W}$ pin allows a write to the 6551.

$\overline{IRQ}$ (Interrupt Request)
The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0 — DB_7(Data Bus)
The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the 6551. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

CS_0, $\overline{CS_1}$ (Chip Selects)
The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The 6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

Figure 2.
Write Timing Characteristics



(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	6551 Min	6551 Max	6551A Min	6551A Max	Unit
Cycle Time	t_{CYC}	1.0	40	0.5	40	µs
ø2 Pulse Width	t_C	470	—	235	—	ns
Address Set-Up Time	t_{ACW}	180	—	90	—	ns
Address Hold Time	t_{CAH}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	180	—	90	—	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	300	—	150	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	ns

(t_r and t_f = 10 to 30 ns)

Clock Generation

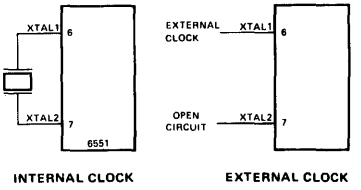
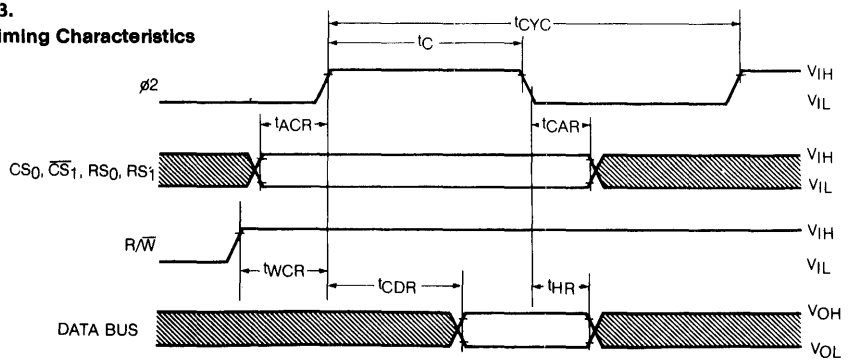


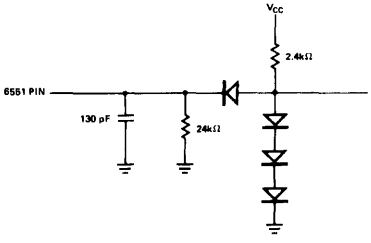
Figure 3.
Read Timing Characteristics



(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	6551 Min	6551 Max	6551A Min	6551A Max	Unit
Cycle Time	t_{CYC}	1.0	40	0.5	40	µs
Pulse Width (ø2)	t_C	470	—	235	—	ns
Address Set-Up Time	t_{ACR}	180	—	90	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCR}	180	—	90	—	ns
Read Access Time	t_{CDR}	—	395	—	200	ns
Read Hold Time	t_{HR}	10	—	10	—	ns

(t_r and t_f = 10 to 30 ns)



Test Load for Data Bus (DB_0-DB_7)
$\overline{T}$ x D, $\overline{DTR}$, RTS Outputs

RS_0, RS_1 (Register Selects)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various 6551 internal registers. The following table indicates the internal register select coding:

RS_1	RS_0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the 6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$) and these differences are described in the individual register definitions.

ACIA/MODEM INTERFACE SIGNAL DESCRIPTION

XTAL1, XTAL2 (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float. XTAL1 is the input pin for the transmit clock.

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ outpin pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready)

This ouput pin is used to indicate the status of the 6551 to the modem. A low on $\overline{DTR}$ indicates the 6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate to the 6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready." $\overline{DSR}$ is a high-impedance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{DSR}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 6 will reflect the new level. The state of DSR does not affect either Transmitter or Receiver operation.

$\overline{DCD}$ (Data Carrier Detect)

The $\overline{DCD}$ input pin is used to indicate to the 6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that is is not. $\overline{DCD}$, like $\overline{DSR}$, is a high-impedance input and must not be a no-connect.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{DCD}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 5 will reflect the new level. The state of $\overline{DCD}$ does not affect Transmitter operation, but must be low for the Receiver to operate.

INTERNAL ORGANIZATION

The Transmitter/Receiver sections of the 6551 are depicted by the block diagram in Figure 5.

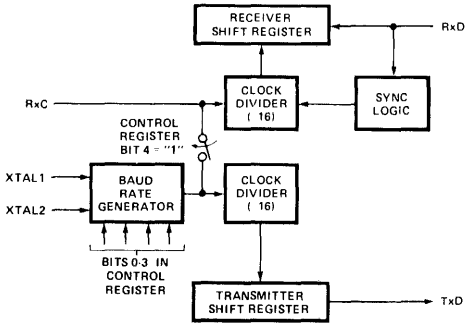


Figure 5. Transmitter/Receiver Clock Circuits

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the 6551.

CONTROL REGISTER

The Control Register is used to select the desired mode for the 6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 6.

CONTROL REGISTER

7	6	5	4	3	2	1	0

STOP BITS

0 = 1 Stop Bit
1 = 2 Stop Bits
1 Stop Bit if Word Length = 8 Bits and Parity*
1½ Stop Bits if Word Length = 5 Bits and No Parity.

WORD LENGTH

BIT 6	BIT 5	DATA WORD LENGTH
0	0	8
0	1	7
1	0	6
1	1	5

RECEIVER CLOCK SOURCE

0 = External Receiver Clock
1 = Baud Rate Generator

BAUD RATE GENERATOR

0	0	0	0	16x EXTERNAL CLOCK
0	0	0	1	50 BAUD
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

*This allows for 9-bit transmission (8 data bits plus parity).

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	–	–	–	–	–

Figure 6. Control Register Format

COMMAND REGISTER

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 7.

COMMAND REGISTER

7	6	5	4	3	2	1	0

PARITY CHECK CONTROLS

BIT 7	BIT 6	BIT 5	OPERATION
–	–	0	Parity Disabled - No Parity Bit Generated - No Parity Bit Received
0	0	1	Odd Parity Receiver and Transmitter
0	1	1	Even Parity Receiver and Transmitter
1	0	1	Mark Parity Bit Transmitted, Parity Check Disabled
1	1	1	Space Parity Bit Transmitted, Parity Check Disabled

DATA TERMINAL READY

0 = Disable Receiver and All Interrupts ($\overline{DTR}$ high)
1 = Enable Receiver and All Interrupts ($\overline{DTR}$ low)

RECEIVER INTERRUPT ENABLE

0 = $\overline{IRQ}$ Interrupt Enabled from Bit 3 of Status Register
1 = $\overline{IRQ}$ Interrupt Disabled

TRANSMITTER CONTROLS

BIT 3	BIT 2	TRANSMIT INTERRUPT	$\overline{RTS}$ LEVEL	TRANSMITTER
0	0	Disabled	High	Off
0	1	Enabled	Low	On
1	0	Disabled	Low	On
1	1	Disabled	Low	Transmit BRK

NORMAL/ECHO MODE FOR RECEIVER

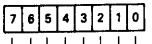
0 = Normal
1 = Echo (Bits 2 and 3 must be "0")

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	0	0	0	0	0

Figure 7. Command Register Format

STATUS REGISTER

The Status Register is used to indicate to the processor the status of various 6551 functions and is outlined in Figure 8.



STATUS	SET BY	CLEARED BY
Parity Error*	0 = No Error 1 = Error	Self Clearing**
Framing Error*	0 = No Error 1 = Error	Self Clearing**
Overrun*	0 = No Error 1 = Error	Self Clearing**
Receive Data Register Full	0 = Not Full 1 = Full	Read Receive Data Register
Transmit Data Register Empty	0 = Not Empty 1 = Empty	Write Transmit Data Register
$\overline{DCD}$	0 = $\overline{DCD}$ Low 1 = $\overline{DCD}$ High	Not Resettable Reflects $\overline{DCD}$ State
$\overline{DSR}$	0 = $\overline{DSR}$ Low 1 = $\overline{DSR}$ High	Not Resettable Reflects $\overline{DSR}$ State
IRQ	0 = No Interrupt 1 = Interrupt	Read Status Register

*NO INTERRUPT GENERATED FOR THESE CONDITIONS.
**CLEARED AUTOMATICALLY AFTER A READ OF RDR AND THE NEXT ERROR FREE RECEIPT OF DATA.

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	–	–	1	0	0	0	0
PROGRAM RESET	–	–	–		–	0	–	

Figure 8. Status Register Format

TRANSMIT AND RECEIVE DATA REGISTERS

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 9 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

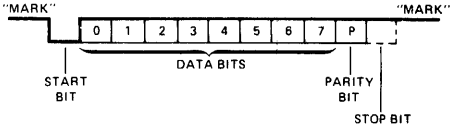


Figure 9 Serial Data Stream Example