

65C00 MICROPROCESSORS

THE 65C00 MICROPROCESSOR FAMILY CONCEPT —

The 65C00 Series Microprocessors represent the first totally software compatible microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors in the 65C00 group are software compatible within the group and are bus compatible with the M6800 product offering.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for the multi processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz maximum operating frequencies.

FEATURES OF THE 6500 FAMILY

- Single +5 volt supply
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type or speed memory
- 8 BIT Bi-directional Data Bus
- Addressable memory range of up to 65K bytes
- "Ready" input (for single cycle execution)
- Direct memory access capability
- Bus compatible with M6800
- Choice of external or on-board clocks
- 1 MHz operation
- On-the-chip clock options
 - *External single clock input
 - *RC time base input
 - *Crystal time base input
- Pipeline architecture

MEMBERS OF THE 65C00 MICROPROCESSOR (CPU) FAMILY

Microprocessors with On-Chip Clock Oscillator

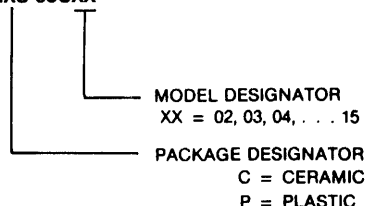
Model	Addressable Memory
MPS65C02	65K Bytes
MPS65C03	4K Bytes
MPS65C04	8K Bytes
MPS65C05	4K Bytes
MPS65C06	4K Bytes
MPS65C07	8K Bytes

Microprocessors with External Two Phase Clock Inputs

MPS65C12	65K Bytes
MPS65C13	4K Bytes
MPS65C14	8K Bytes
MPS65C15	4K Bytes

ORDER NUMBER:

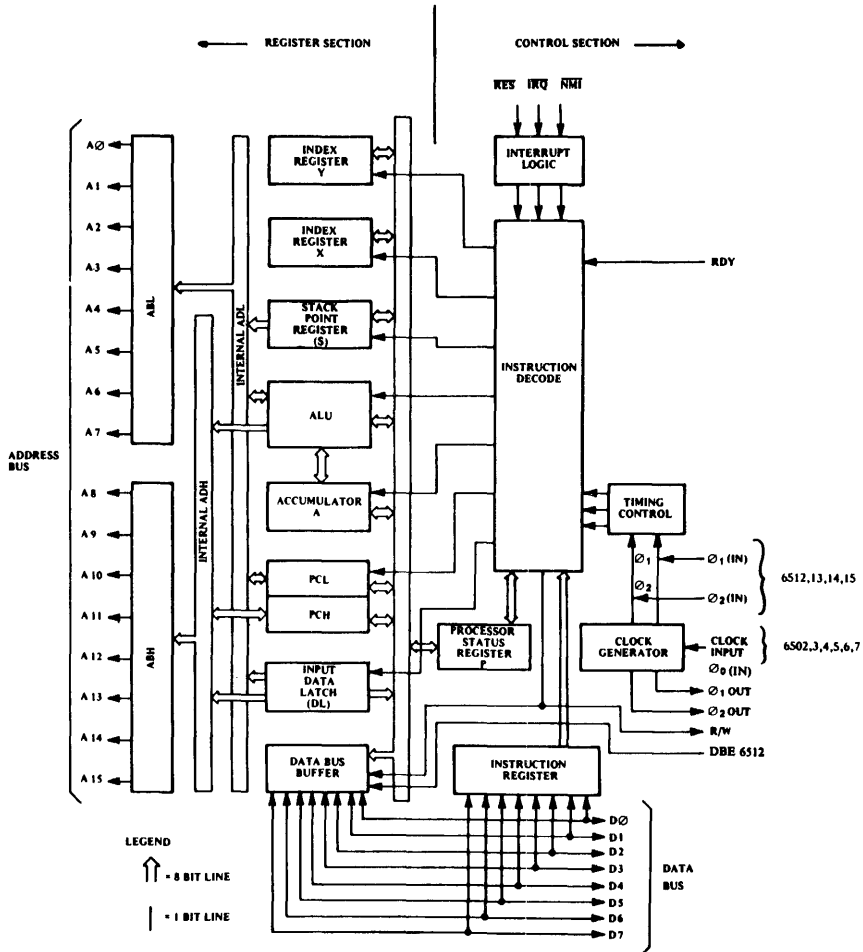
MXS 65CXX



COMMENTS ON THE DATA SHEET

The data sheet is constructed to review first the basic "Common Characteristics"—those features which are common to the general family of microprocessors. Subsequent to a review of the family characteristics will be sections devoted to each member of the group with specific features of each.

COMMON CHARACTERISTICS



Note 1. Clock Generator is not included on 65C12,13,14,15
 Note 2. Addressing Capability and control options vary with each of the 65C00 Products.

65C00 Internal Architecture

COMMON CHARACTERISTICS
MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	V _{CC}	-0.3 to +7.0	Vdc
INPUT VOLTAGE	V _{IN}	-0.3 to +7.0	Vdc
OPERATING TEMPERATURE	T _A	0 to +70	°C
STORAGE TEMPERATURE	T _{STG}	-55 to +150	°C

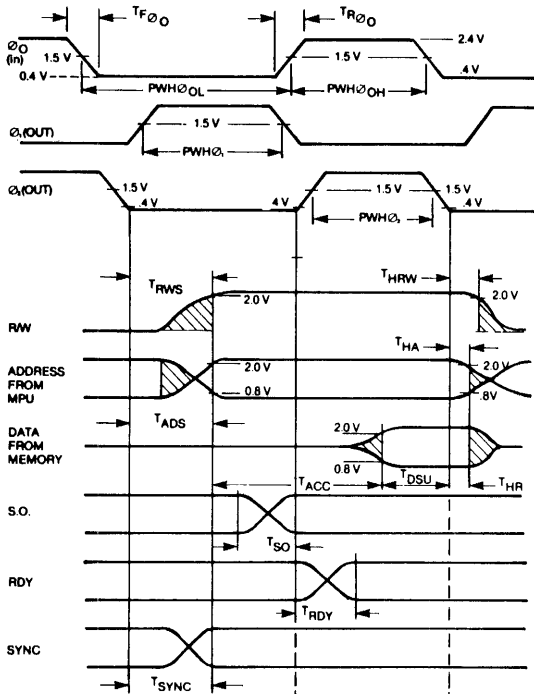
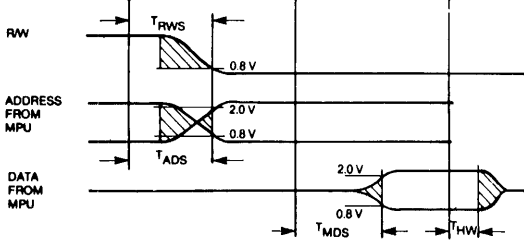
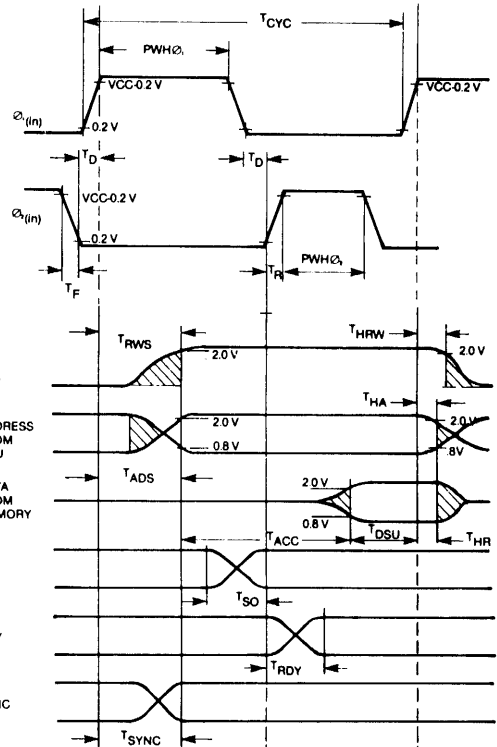
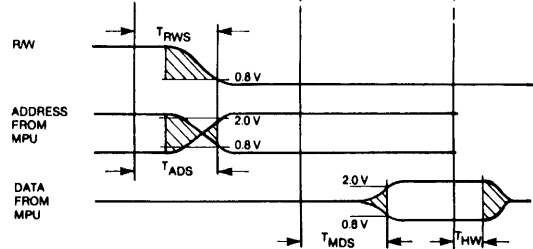
This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0° to +70°C)

∅₁, ∅₂ (in) applies to 65C12, 13, 14, 15; ∅₀ (in) applies to 65C02, 03, 04, 05, 06 and 07

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage Logic, ∅ ₀ (in) ∅ ₁ , ∅ ₂ (in)	V _{IH}	V _{SS} + 2.4 V _{CC} - 0.2	— —	V _{CC} V _{CC} + 1.0V	Vdc Vdc
Input High Voltage RES, NMI, RDY, IRQ, Data, S.O.		V _{SS} + 2.0	—	—	Vdc
Input Low Voltage Logic, ∅ ₀ (in) ∅ ₁ , ∅ ₂ (in)	V _{IL}	V _{SS} - 0.3 V _{SS} - 0.3	— —	V _{SS} + 0.4 V _{SS} + 0.2	Vdc Vdc
Input Low Voltage RES, NMI, RDY, IRQ, Data, S.O.		—	—	V _{SS} + 0.8	Vdc
Input Leakage Current (V _{IN} = 0 to 5.25V, V _{CC} = 5.25V) Logic (Excl. RDY, S.O.) ∅ ₁ , ∅ ₂ (in) ∅ ₀ (in)	I _{IN}	— — —	— — —	2.5 100 10.0	μA μA μA
Three State (Off State) Input Current (V _{IN} = 0.4 to 2.4V, V _{CC} = 5.25V) Data Lines	I _{TSI}	—	—	10	μA
Output High Voltage (I _{OH} = -100μAdc, V _{CC} = 4.75V) SYNC, Data, AO-A15, RW	V _{OH}	V _{SS} + 2.4	—	—	Vdc
Out Low Voltage (I _{OL} = 1.6mAdc, V _{CC} = 4.75V) SYNC, Data, AO-A15, RW	V _{OL}	—	—	V _{SS} + 0.4	Vdc
Supply Current	I _{CC}	—	—	20	mA
Capacitance (V _{IN} = 0, T _A = 25°C, f = 1MHz) Logic Data AO-A15, RW, SYNC ∅ ₀ (in) ∅ ₁ ∅ ₂	C C _{IN} C _{OUT} C _{∅₀} (in) C _{∅₁} C _{∅₂}	— — — — — —	— — — — 30 50	10 15 12 15 50 80	pF

Note: IRQ and NMI require 3K pull-up resistors.

COMMON CHARACTERISTICS
Clock Timing — 65C02, 03, 04, 05, 06, 07

Timing for Reading Data from Memory or Peripherals

Timing for Writing Data to Memory or Peripherals
Clock Timing — 65C13, 14, 15

Timing for Reading Data from Memory or Peripherals

Timing for Writing Data to Memory or Peripherals

COMMON CHARACTERISTICS
1 MHz TIMING

 Electrical Characteristics: ($V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$, $T_A = 0^\circ-70^\circ C$)

CLOCK TIMING — 65C02, 03, 04, 05

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.
Cycle Time	TCYC	1000	—	—
ϕ_0 (IN) Pulse Width (measured at 1.5v)	PWH ϕ_0	460	—	520
ϕ_0 (IN) Rise, Fall Time	TR ϕ_0 , TF ϕ_0	—	—	10
Delay Time between Clocks (measured at 1.5v)	T _D	5	—	—
ϕ_1 (OUT) Pulse Width (measured at 1.5v)	PWH ϕ_1	PWH ϕ_{OL-20}	—	PWH ϕ_{OL}
ϕ_2 (OUT) Pulse Width (measured at 1.5v)	PWH ϕ_2	PWH ϕ_{OH-40}	—	PWH ϕ_{OH-10}
ϕ_1 (OUT), ϕ_2 (OUT) Rise, Fall Time (measured .8v to 2.0v) (Load ½ 30pf ½ 1 TTL)	T _R , T _F	—	—	25

CLOCK TIMING: 65C12, 13, 14, 15

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.
Cycle Time	TCYC	1000	—	—
Clock Pulse Width ϕ_1 (Measured at $V_{CC} - 0.2v$) ϕ_2	PWH ϕ_1 PWH ϕ_2	430 470	—	—
Fall Time, Rise Time (Measured from 0.2v to $V_{CC} - 0.2v$)	T _F , T _R	—	—	25
Delay Time between Clocks (Measured at 0.2v)	T _D	0	—	—

READ/ WRITE TIMING (LOAD = ITTL)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.
Read/ Write Setup Time from 65C00	TRWS	—	100	300
Address Setup Time from 65C00	T _{ADS}	—	100	300
Memory Read Access Time	T _{ACC}	—	—	575
Data Stability Time Period	T _{DSU}	100	—	—
Data Hold Time — Read	T _{HR}	10	—	—
Data Hold Time — Write	T _{HW}	30	60	—
Data Setup Time from 65C00	T _{MDS}	—	150	200
S.O. Setup Time	T _{S.O.}	100	—	—
SYNC Setup Time from 6500	T _{SYNC}	—	—	350
Address Hold Time	T _{HA}	30	60	—
R/W Hold Time	T _{HRW}	30	60	—
RDY Setup Time	T _{RDY}	100	—	—

COMMON CHARACTERISTICS
65C00 SIGNAL DESCRIPTION
Clocks (ϕ_1 , ϕ_2)

The 65C1X requires a two phase non-overlapping clock that runs at the Vcc voltage level.

The 65C0X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

Address Bus (A_7 - A_{15})

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pf.

Data Bus (D_0 - D_7)

Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130pf.

Data Bus Enable (DBE)

This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (ϕ_2) clock, thus allowing data output from microprocessor only during ϕ_2 . During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

Ready (RDY)

This input signal allows the user to single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one (ϕ_1) and up to 100ns after phase two (ϕ_2) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two (ϕ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If Ready is low during a write cycle, it is ignored until the following read operation.

Interrupt Request ($\overline{\text{IRQ}}$)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K Ω external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{\text{NMI}}$)

A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. NMI is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{\text{IRQ}}$ will be performed, regardless of the interrupt mask flag status. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

NMI also requires an external 3K Ω resistor to Vcc for proper wire-OR operations.

Inputs $\overline{\text{IRQ}}$ and NMI are hardware interrupt lines that are sampled during ϕ_2 (phase 2) and will begin the appropriate interrupt routine on the ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of ϕ_1 .

SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After Vcc reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the RW and (SYNC) signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

COMMON CHARACTERISTICS
ADDRESSING MODES

ACCUMULATOR ADDRESSING—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING—In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING—The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X," or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING—In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

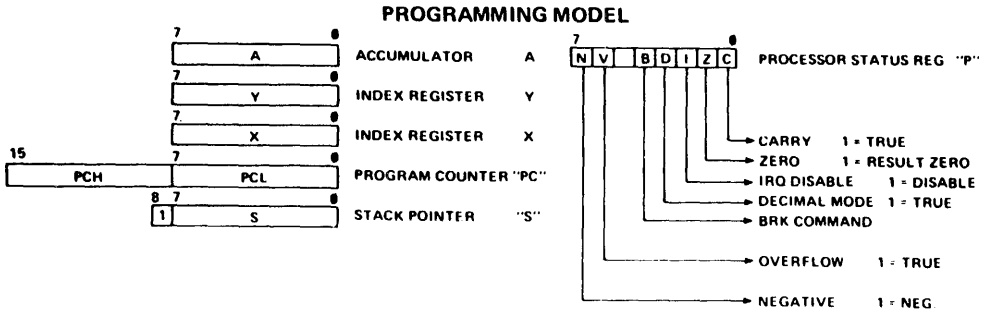
INDIRECT INDEXED ADDRESSING—In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET—ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
BCC	Branch on Carry Clear	LSR	Shift One Bit Right (Memory or Accumulator)
BCS	Branch on Carry Set	NOP	No Operation
BEQ	Branch on Result Zero	ORA	"OR" Memory with Accumulator
BIT	Test Bits in Memory with Accumulator	PHA	Push Accumulator on Stack
BMI	Branch on Result Minus	PHP	Push Processor Status on Stack
BNE	Branch on Result not Zero	PLA	Pop Accumulator from Stack
BPL	Branch on Result Plus	PLP	Pop Processor Status from Stack
BRK	Force Break	ROL	Rotate One Bit Left (Memory or Accumulator)
BVC	Branch on Overflow Clear	ROR	Rotate One Bit Right (Memory or Accumulator)
BVS	Branch on Overflow Set	RTI	Return from Interrupt
CLC	Clear Carry Flag	RTS	Return from Subroutine
CLD	Clear Decimal Mode	SBC	Subtract Memory from Accumulator with Borrow
CLI	Clear Interrupt Disable Bit	SEC	Set Carry Flag
CLV	Clear Overflow Flag	SED	Set Decimal Mode
CMP	Compare Memory and Accumulator	SEI	Set Interrupt Disable Status
CPX	Compare Memory and Index X	STA	Store Accumulator in Memory
CPY	Compare Memory and Index Y	STX	Store Index X in Memory
DEC	Decrement Memory by One	STY	Store Index Y in Memory
DEX	Decrement Index X by One	TAX	Transfer Accumulator to Index X
DEY	Decrement Index Y by One	TAY	Transfer Accumulator to Index Y
EOR	"Exclusive-or" Memory with Accumulator	TSX	Transfer Stack Pointer to Index X
INC	Increment Memory by One	TXA	Transfer Index X to Accumulator
INX	Increment Index X by One	TXS	Transfer Index X to Stack Register
INY	Increment Index Y by One	TYA	Transfer Index Y to Accumulator
JMP	Jump to New Location		
JSR	Jump to New Location Saving Return Address		

COMMON CHARACTERISTICS



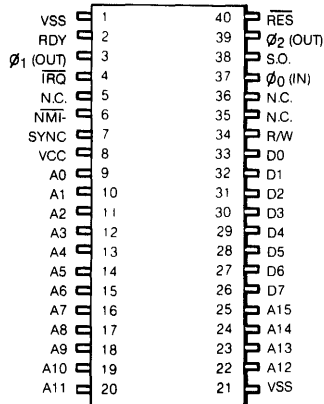
INSTRUCTION SET – OP CODES, Execution Time, Memory Requirements

INSTRUCTION	OPERATION	ADDRESS		ZERO FLAG		CARRY	OVERFLOW	MODE 1	MODE 2	PAGE 1	PAGE 2	MODE 1	MODE 2	RELATIVE	MODE 1	PAGE 1	MODE 2	CONDITION CODES	
		OP N	OP N	OP N	OP N														OP N
ADC	A ← M ← C ← A	(4)11	60	2	2	BD	4	3	65	3	2								
AND	A ← M ← A	(1)1	78	2	2	BD	4	3	26	1	2								
ASL	C ← [D] ← C		06	6	3	06	5	2	BA	2	1								
BCC	BRANCH ON C=0	(2)													56	2	2		
BCS	BRANCH ON C=1	(2)													56	2	2		
BEO	BRANCH ON Z=1	(2)													58	2	2		
BIT	A ← M					7C	4	3	24	3	2								
BMI	BRANCH ON N=1	(2)													06	2	2		
BNE	BRANCH ON Z=0	(2)													06	2	2		
BPL	BRANCH ON N=0	(2)													18	2	2		
BRK	(See Fig. 1)																		
BVC	BRANCH ON V=0	(2)													56	2	2		
BVS	BRANCH ON V=1	(2)													78	2	2		
CLC	C ← 0																		
CLE	C ← 1																		
CLI	B ← 1																		
CLV	B ← V																		
CMP	A ← M	(1)1	69	2	2	CD	4	3	05	3	2								
CPX	X ← M	(6)2	7	EC	4	3	E4	3	2										
CPY	Y ← M	(6)2	7	CC	4	3	C4	3	2										
DEC	M ← M - 1					CE	6	3	C6	5	2								
DER	X ← X - 1																		
DEY	Y ← Y - 1																		
EOR	A ← M ← A	(1)1	69	2	2	AD	4	3	45	3	2								
INC	M ← M + 1					EE	6	3	E6	5	2								
INX	X ← X + 1																		
INY	Y ← Y + 1																		
JMP	JUMP TO NEW LOC					AC	3	3											
JSR	(See Fig. 2) JUMP SUB					76	6	3											
LDA	M ← A	(1)1	69	2	2	AD	4	3	A5	3	2								

INSTRUCTION	OPERATION	ADDRESS		ZERO FLAG		CARRY	OVERFLOW	MODE 1	MODE 2	PAGE 1	PAGE 2	MODE 1	MODE 2	RELATIVE	MODE 1	PAGE 1	MODE 2	CONDITION CODES		
		OP N	OP N	OP N	OP N														OP N	OP N
LDR	M ← R	(1)1	69	2	2	AE	4	3	A6	3	2									
LDD	M ← Y	(1)1	69	2	2	AC	4	3	A4	3	2									
LSR	B ← [D] ← B					AE	6	3	A6	5	2									
NOP	NO OPERATION																			
ORA	A ← M ← A	(6)2	7	BD	4	3	BD	3	2											
PHA	A ← M																			
PHP	P ← M																			
PLA	M ← A																			
PLP	S ← S - 1																			
ROL	[D] ← [D] ← C					7E	6	3	7E	5	2									
ROR	[D] ← [D] ← C					7E	6	3	7E	5	2									
RTI	(See Fig. 1) RETURN																			
RTS	(See Fig. 2) RETURN SUB																			
SBC	A ← M ← A	(1)1	69	2	2	ED	4	3	E5	3	2									
SEC	C ← 1																			
SED	C ← 0																			
SEI	I ← 1																			
STA	A ← M					BD	4	3	BD	3	2									
STX	X ← M					BE	4	3	BE	3	2									
STY	Y ← M					BC	4	3	BC	3	2									
TAX	A ← X																			
TAY	A ← Y																			
TSX	S ← X																			
TEA	X ← A																			
TXS	X ← S																			
TYA	Y ← A																			

Note: MOS Technology cannot assume liability for the use of undefined OP Codes

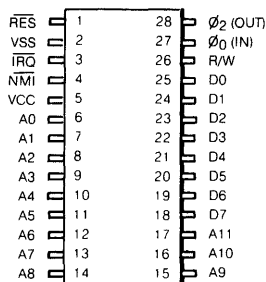
MICRO-PROCESSORS



65C02 — 40 Pin Package

Features of 65C02

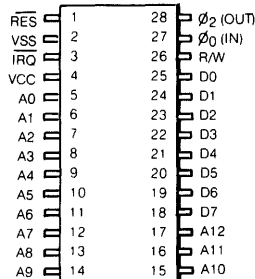
- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{\text{IRQ}}$ Interrupt
- On-the-chip Clock
 - TTL Level Single Phase Input
 - RC Time Base Input
 - Crystal Time Base Input
- SYNC Signal
(can be used for single instruction execution)
- RDY Signal
(can be used to halt or single cycle execution)
- Two Phase Output Clock for Timing of Support Chips
- NMI Interrupt



65C03 — 28 Pin Package

Features of 65C03

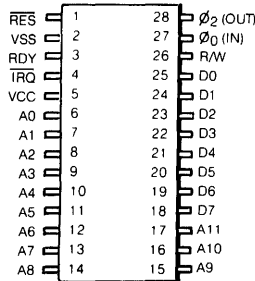
- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- $\overline{\text{IRQ}}$ Interrupt
- NMI Interrupt
- 8 Bit Bidirectional Data Bus



65C04 — 28 Pin Package

Features of 65C04

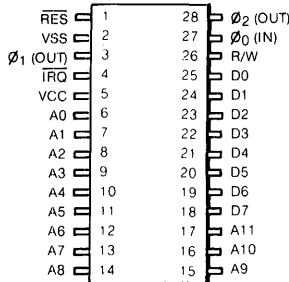
- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- $\overline{\text{IRQ}}$ Interrupt
- 8 Bit Bidirectional Data Bus



65C05 — 28 Pin Package

Features of 65C05

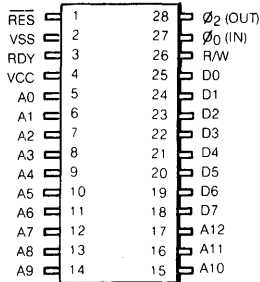
- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- $\overline{\text{IRQ}}$ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus



65C06 — 28 Pin Package

Features of 65C06

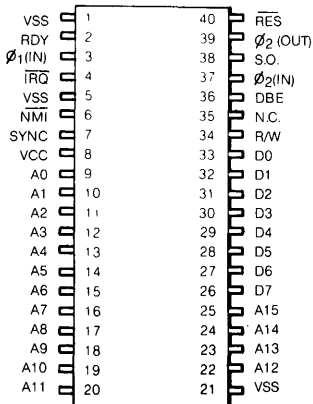
- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- $\overline{\text{IRQ}}$ Interrupt
- Two phase output clock for timing of support chips
- 8 Bit Bidirectional Data Bus



65C07 — 28 Pin Package

Features of 65C07

- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- RDY Signal
- 8 Bit Bidirectional Data Bus



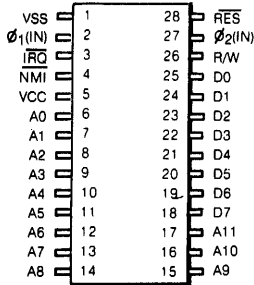
65C12 — 40 Pin Package

Features of 65C12

- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{\text{IRQ}}$ Interrupt
- NMI Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus
- SYNC Signal
- Two phase clock input
- Data Bus Enable

MICRO-PROCESSORS

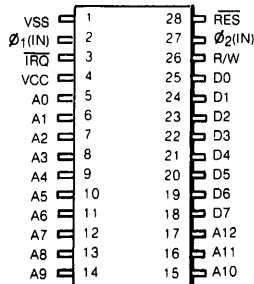
MICRO-PROCESSORS



65C13 — 28 Pin Package

Features of 65C13

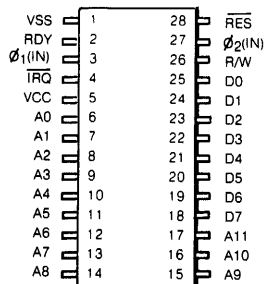
- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- \overline{IRQ} Interrupt
- NMI Interrupt
- 8 Bit Bidirectional Data Bus



65C14 — 28 Pin Package

Features of 65C14

- 8K Addressable Bytes of Memory (A0-A12)
- Two phase clock input
- \overline{IRQ} Interrupt
- 8 Bit Bidirectional Data Bus



65C15 — 28 Pin Package

Features of 65C15

- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- \overline{IRQ} Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus

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