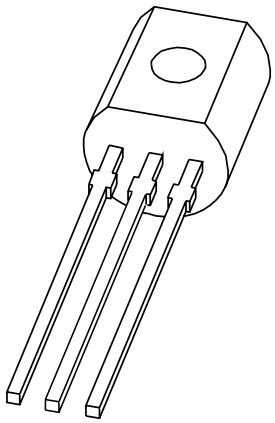
DATA SHEET



MPSA92
PNP high-voltage transistor

Product data sheet
Supersedes data of 2001 Dec 07

2004 Aug 20

PNP high-voltage transistor MPSA92

FEATURES

- Low current (max. 100 mA)
- High voltage (max. 300 V).

APPLICATIONS

- General purpose switching and amplification.

DESCRIPTION

PNP high-voltage transistor in a TO-92; SOT54 plastic package. NPN complement: MPSA42.

PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter

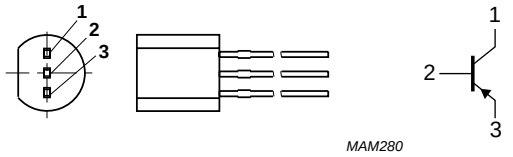


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	−300	V
V_{CEO}	collector-emitter voltage	open base	–	−300	V
V_{EBO}	emitter-base voltage	open collector	–	−5	V
I_C	collector current (DC)		–	−100	mA
I_{CM}	peak collector current		–	−200	mA
I_{BM}	peak base current		–	−100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	625	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		−65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	200	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

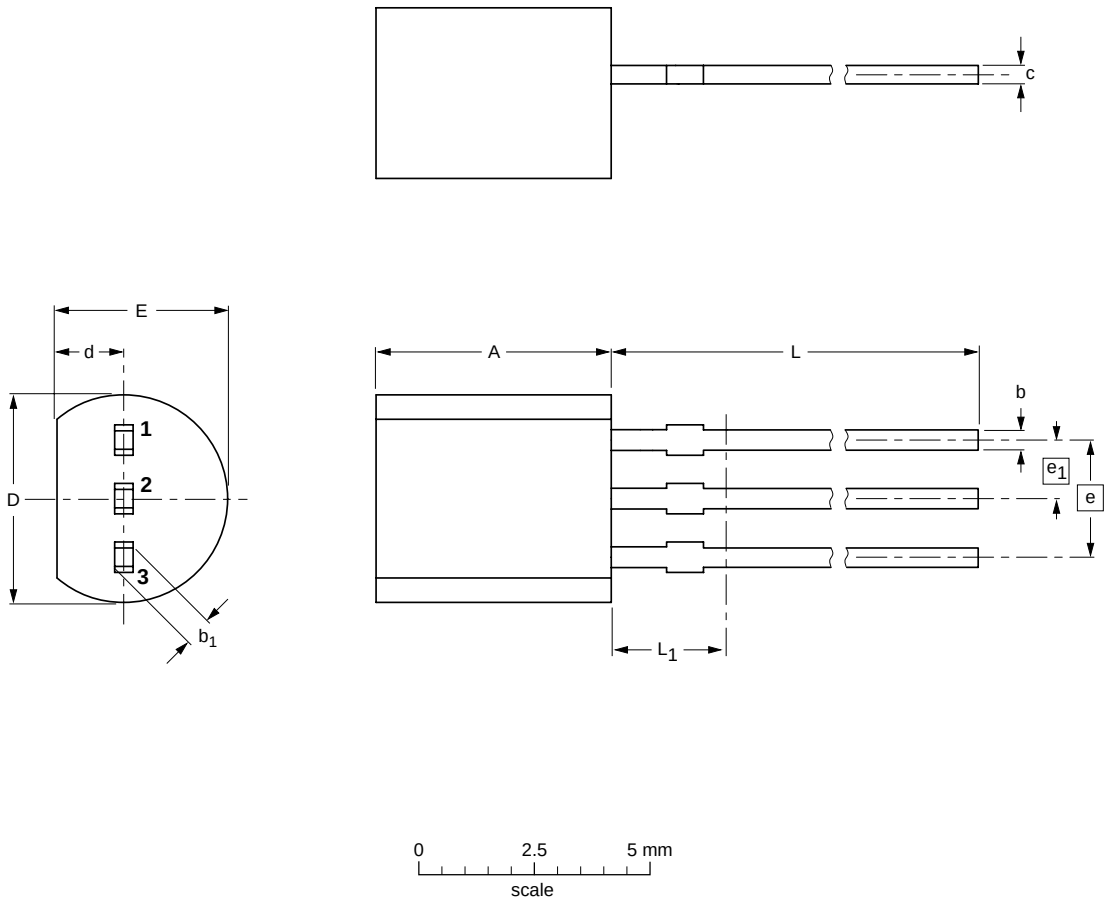
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = −200 V	−	−250	nA
I_{EBO}	emitter cut-off current	I_C = 0; V_{BE} = −3 V	−	−100	nA
h_{FE}	DC current gain	V_{CE} = −10 V; note 1			
		I_C = −1 mA	25	−	
		I_C = −10 mA	40	−	
		I_C = −30 mA	25	−	
V_{CEsat}	collector-emitter saturation voltage	I_C = −20 mA; I_B = −2 mA; note 1	−	−500	mV
V_{BEsat}	base-emitter saturation voltage	I_C = −20 mA; I_B = −2 mA; note 1	−	−900	mV
C_c	collector capacitance	$I_E = i_e$ = 0; V_{CB} = −20 V; f = 1 MHz	−	6	pF
f_T	transition frequency	I_C = −10 mA; V_{CE} = −20 V; f = 100 MHz	50	−	MHz

Note

1. Pulse test: $t_p \leq 300\ \mu s$; $\delta \leq 0.02$.

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~04-06-28~~ 04-11-16

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
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Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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