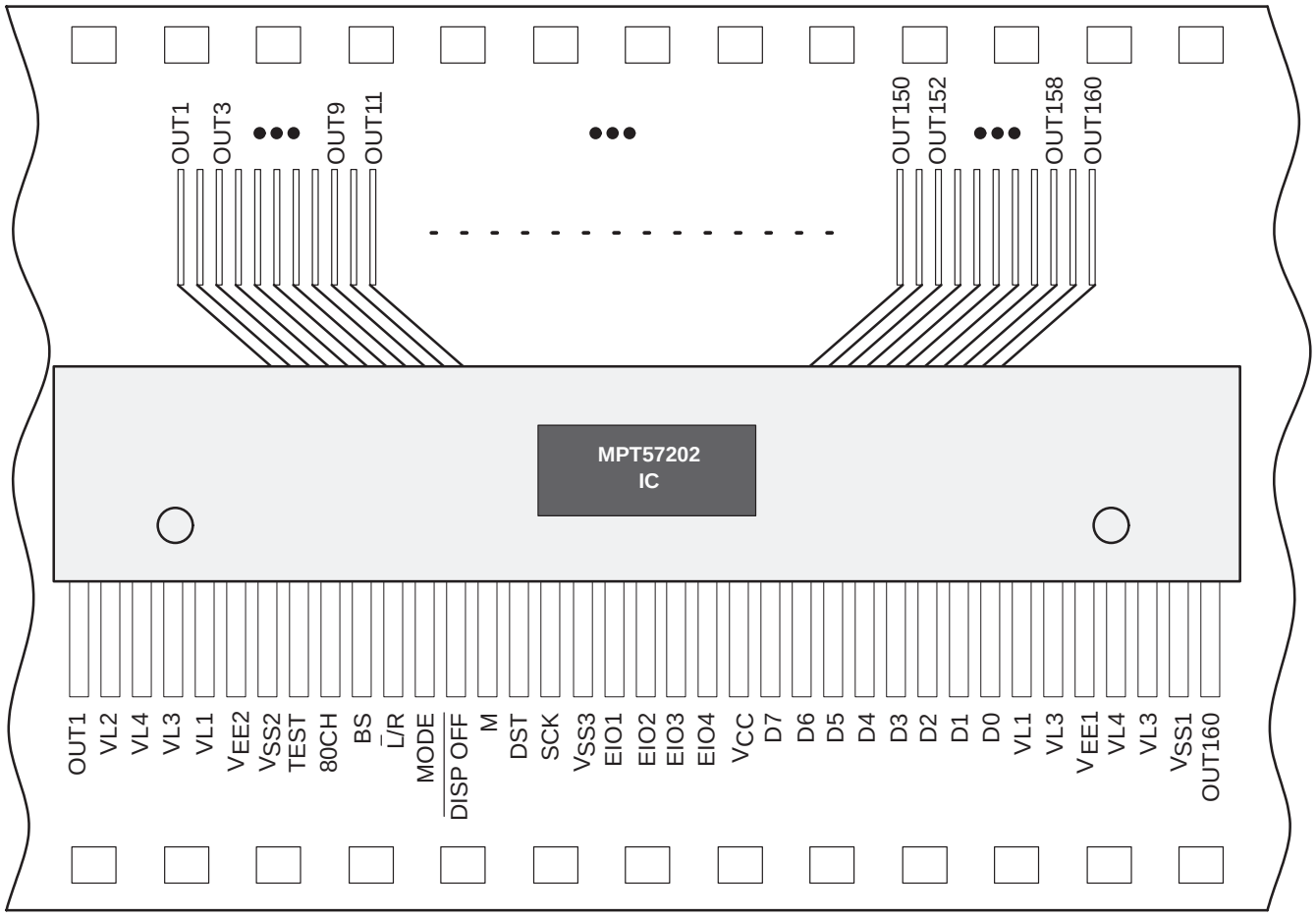
- **Duty Cycle for LCD Driver is Over 1/400**
- **Recommended V_{EE} Voltage Range for LCD Driver: 20 V to 42 V (45 V Max)**
- **160 Channel Outputs**
- **Power Supply Voltage . . . 5 V ± 10%**
- **High-Voltage CMOS SI Gate Technology**
- **TAB (Tape Automated Bonding) Packaging**

description

The MPT57202 is a CMOS integrated circuit designed to drive an LCD (liquid crystal display) for a dot matrix STN (super twisted nematic). The outputs can be configured as one set of 160 output channels or as two sets of 80 output channels. The duty cycle is over 1/400, and the output bias voltage range (V_{EE}) is from 20 V to 42 V (45 V maximum).

The outputs can be configured as one set of 160 output channels or as 2 sets of 80 output channels. This high-voltage CMOS SI gate device is available in a custom TAB (tape automated bonding) package.

The MPT57202 is characterized for operation over the full military temperature range of –55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

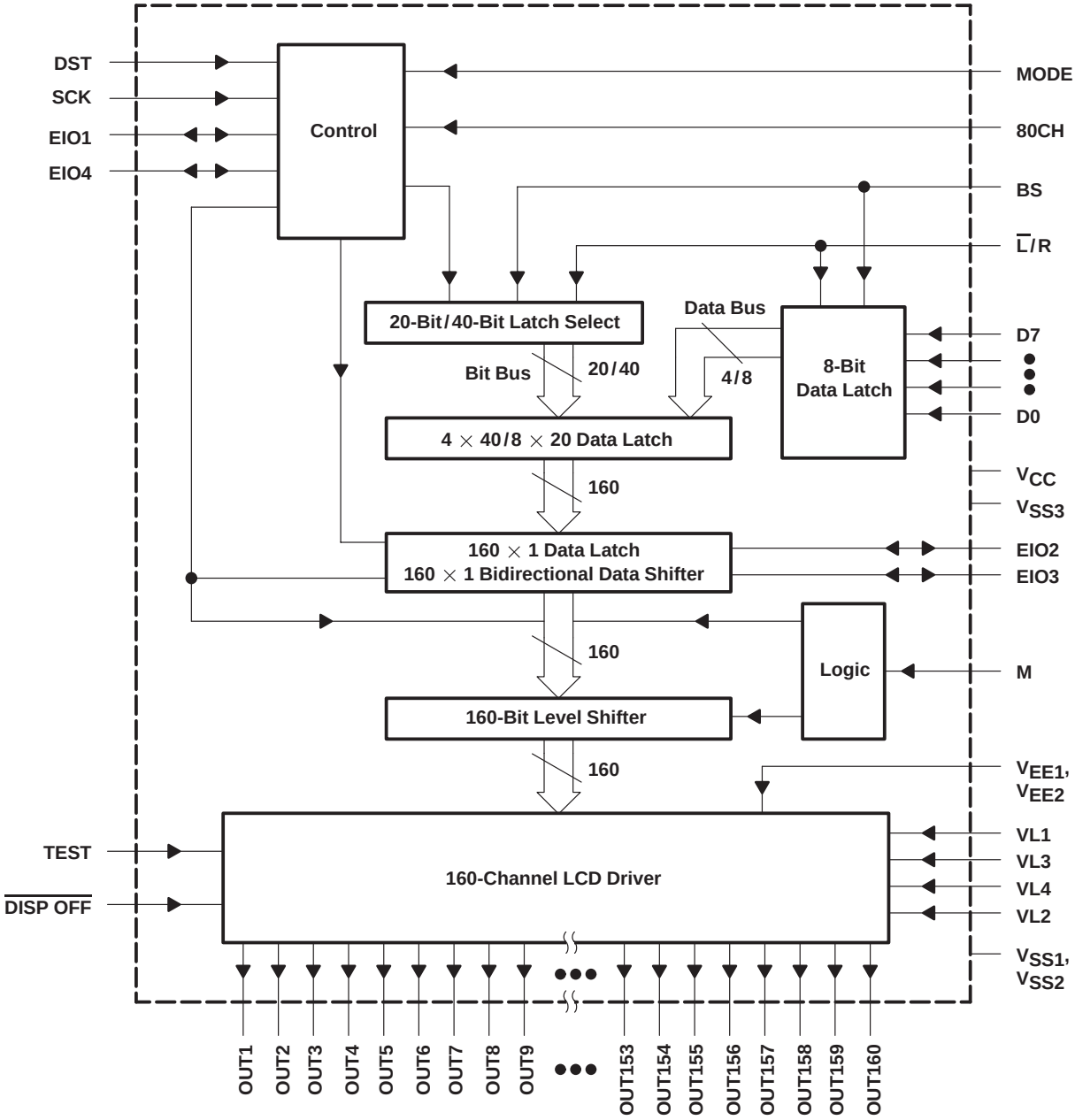
function table

SIGNAL	COMMON (ROW) MODE	
BS	Not Used (tie low)	
D7-D0	Not Used (tie low)	
$\overline{\text{DISP OFF}}$†	TEST VL2 (display off): L	
DST	Data shift on falling edge	
80 CH	L = 160-channel	H=80-channel x 2 (parallel)
EIO1	Serial I/O	1 CH Serial I/O
EIO2	See Note 1	80 CH Serial I/O
EIO3	See Note 1	81 CH Serial I/O
EIO4	Serial I/O	160 CH Serial I/O
$\overline{\text{L}}$/R	L/R = L (left shift) EIO1 ← <R1> ← <R2> ← <R3>...← <R160> ← EIO4	
	L/R = H (right shift) EIO1 → <R1> → <R2> → <R3>...→ <R160> → EIO4	
M	M, data combination	Selects level
	0,1 1,0 0,0 1,1	VL1 VL3 VL4 VL2
MODE	L	
SCK	Not used (tie low)	
TEST	Test pin = L or open	

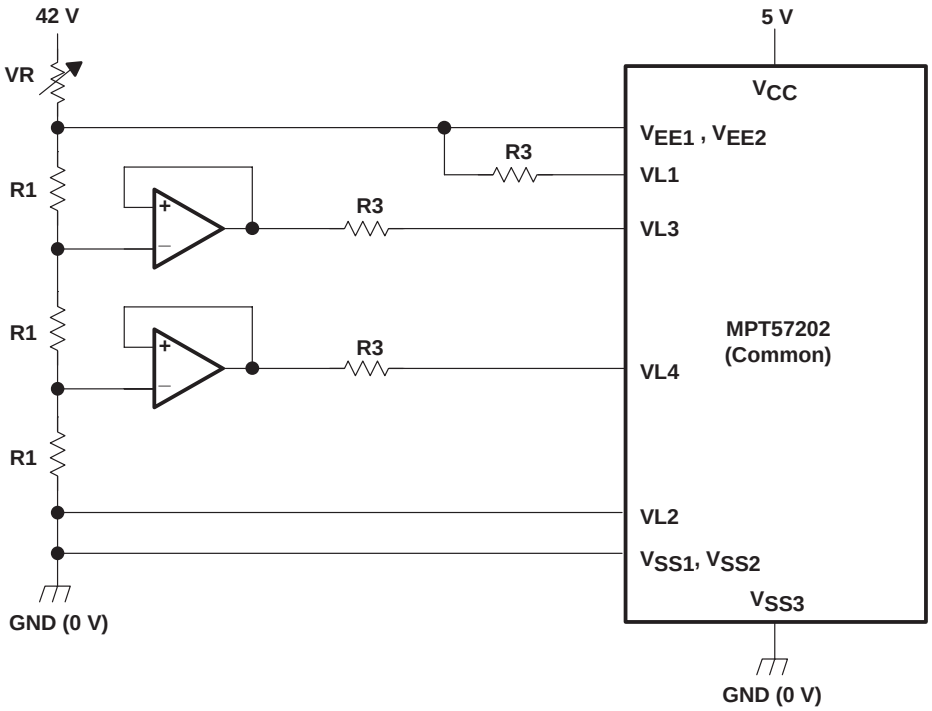
† This terminal should be low at power up for logic resetting.

NOTE 1: This terminal is not used in this configuration. Although the pin produces a low output level, it should be left open.

functional block diagram

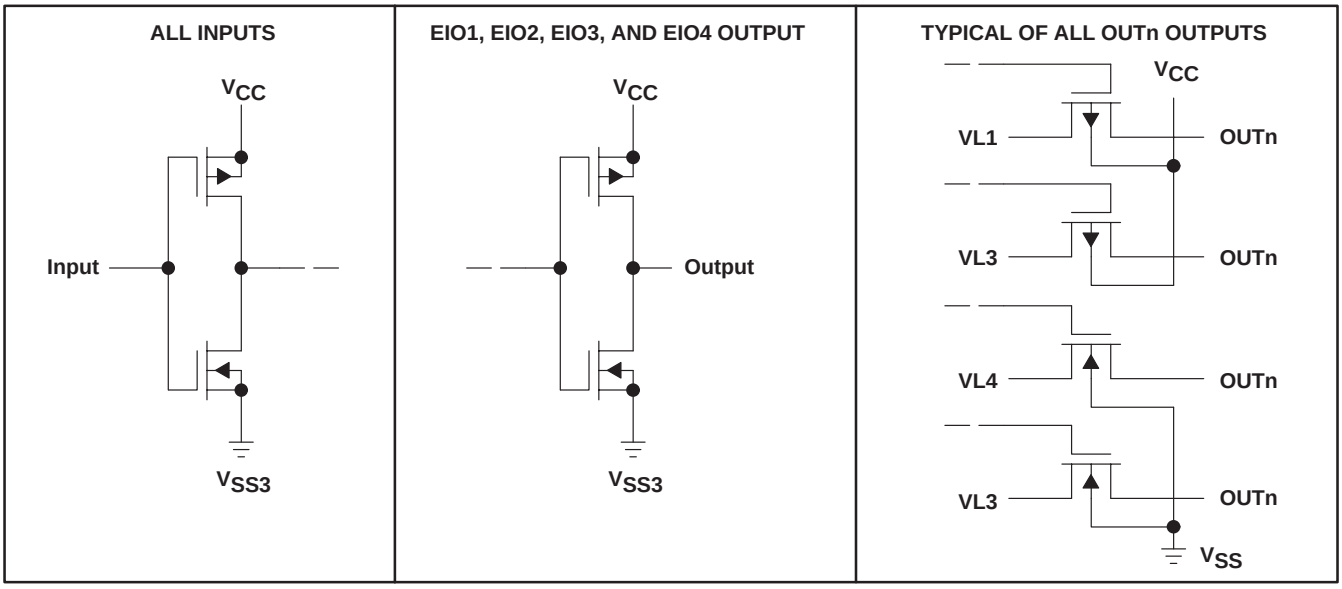


power supply circuit



NOTE A. Separation between high voltage GND (V_{SS1}, V_{SS2}) line and logic GND (V_{SS3}) line is recommended to avoid noise problems.

schematics of inputs and outputs



Terminal Functions

common (row) driver mode

TERMINAL NAME	I/O	DESCRIPTION
80CH	I	80CH is the 160-channel/80-channel mode select L = 160-channel data shift mode; H = 80-channel-×-2 data shift mode
BS	I	Not used (tie low)
D7–D0	I	Not used (tie low)
$\overline{\text{DISP OFF}}$	I	Display off. A low level on $\overline{\text{DISP OFF}}$ disables normal operation, turning the display off (0V) and enabling the test mode. $\overline{\text{DISP OFF}}$ must be tied high for normal operation.
DST	I	Data strobe. DST is the data strobed input.
EIO1	I/O	Serial I/O 1. When $\overline{\text{L}}$/R is high, EIO1 is an active-high serial input. When $\overline{\text{L}}$/R is low (left-shift mode), EIO1 is an active-high serial output.
EIO2	I/O	Serial I/O 2: When the device is configured in 160-channel data shift mode (80CH = L), EIO2 is not used and should be left open. When the device is configured in 80-channel-×-2 data shift mode (80CH = H) and $\overline{\text{L}}$/R is low; this EIO2 is an active-high serial input for the first 80-channel output section. $\overline{\text{L}}$/R is high; EIO2 is an active-high serial output for the first 80-channel output section.
EIO3	I/O	Serial I/O 3: When MPT57202 is configured in 160-channel data shift mode (80 CH = L), EIO3 is not used and should be left open. When the device is configured in 80-channel-×-2 data shift mode (80CH = H) and $\overline{\text{L}}$/R is low; EIO3 is an active-high serial output for the first 80-channel output section. $\overline{\text{L}}$/R is high; EIO3 is an active-high serial input for the first 80-channel output section.
EIO4	I/O	Serial I/O 4: When $\overline{\text{L}}$/R = H: EIO4 is an active-high serial output When $\overline{\text{L}}$/R = L: EIO4 is an active-high serial input
$\overline{\text{L}}$/R	I	Select left or right shift When the MPT57202 is in 160-channel data shift mode (80CH = L) and $\overline{\text{L}}$/R = H, data is right shifted into EIO1 and out from EIO4 EIO1 → <R1> → <R2> → <R3>...→ <R160> → EIO4 When the MPT57202 is in 160-channel data shift mode (80CH = L) and $\overline{\text{L}}$/R = L, data is left shifted into EIO4 and out from EIO1 EIO1 ← <R1> ← <R2> ← <R3>...← <R160> ← EIO4 When the MPT57202 is in 80-channel-×-2 data shift mode with two parallel 80-channel output sections (80CH = H) and $\overline{\text{L}}$/R = H, data is right shifted into EIO1 and EIO3 and out from EIO2 and EIO4 EIO1 → <R1> → <R2> → <R3>...→ <R80> → EIO2 EIO3 → <R81> → <R82> → <R83>...→ <R160> → EIO4 When the MPT57202 is in 80-channel-×-2 data shift mode with two parallel 80-channel output sections (80CH = H) and $\overline{\text{L}}$/R = L, data is left shifted into EIO2 and EIO4 and out from EIO1 and EIO3 EIO1 ← <R1> ← <R2> ← <R3>...← <R80> ← EIO2 EIO3 ← <R81> ← <R82> ← <R83>...← <R160> ← EIO4 In all cases, R<1> → OUT1, e.g., R<1> → OUT1, R<76> → OUT76, etc. See Table 1 for the cascade configuration.
M	I	Frame signal input
MODE	I	Common/segment mode select. MODE should be tied low.
OUT1–OUT160	O	Common (row) driver output channels (see Table 2)
SCK	I	Not used (tie low)

Terminal Functions (continued)

TERMINAL NAME	I/O	DESCRIPTION
TEST	I	TEST is used for factory testing only. For normal operation tie TEST low or leave it open. TEST has an internal pulldown resistor.
V_{CC}		5-V supply terminal
V_{EE1}		Output buffer bias
V_{EE2}		Output logic bias
VL1		VL1 is the on-level of the LCD driver output
VL2		VL2 is the off-level of the LCD driver output
VL3		VL3 is the on-level of the LCD driver output
VL4		VL4 is the off-level of the LCD driver output
V_{SS1}		Ground terminal with respect to V_{EE1}
V_{SS2}		Ground terminal with respect to V_{EE2}
V_{SS3}		Ground terminal with respect to V_{CC}

Table 1. Cascade Configurations - Common-Driver Mode (MODE = L)

INPUTS		I/O				NUMBER OF CHANNELS/ SHIFT DIRECTION
80 CH	$\overline{L}$/R	EIO1	EIO2	EIO3	EIO4	
L	H	Input	-	-	Output	160/right
L	L	Output	-	-	Input	160/left
H	H	Input	Output	Input	Output	80 x 2/right
H	L	Output	Input	Output	Input	80 x 2/left

absolute maximum ratings over free-air temperature range†

Supply voltage range, V_{CC} (see Note 2) . . . . . –0.3 V to 7 V
Supply voltage (V_{SS1}, V_{SS2}, V_{SS3}) . . . . . 0 V
Input voltage range, V_I (DST, SCK, M, MODE, 80CH, L/R, BS, EIO1-EIO4, D0-D7, DISP OFF, TEST) . . . . . –0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O (EIO1, EIO2, EIO3, EIO4) . . . . . –0.3 V to V_{CC} + 0.3 V
Output bias voltage range for LCD (V_{EE1}, V_{EE2}) . . . . . –0.3 V to 45 V
Supply voltage range for LCD (VL1, VL2, VL3, VL4) (see Note 3) . . . . . –0.3 V to V_{EE} + 0.3 V
Input current, I_I . . . . . ± 10 mA
Output current, I_O: EIO1 to EIO4 . . . . . 10 mA
OUT1 to OUT160 . . . . . 5 mA
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. Voltage values are with respect to V_{SS1}, V_{SS2}, and V_{SS3}.
3. The following conditions must be met:
V_{EE1} and $V_{EE2} \geq VL1 \geq VL3 \geq VEE - 7\ V$, and $7\ V \geq VL4 \geq VL2 \geq V_{SS1}, V_{SS2}, V_{SS3}$
V_{EE1} and $V_{EE2} > VL1 > VL3 > V_{EE} - \Delta V$, and $\Delta V > VL4 > VL2 > V_{SS1}, V_{SS2}, V_{SS3}$
(See Figure 1 for a graphic representation of ΔV).

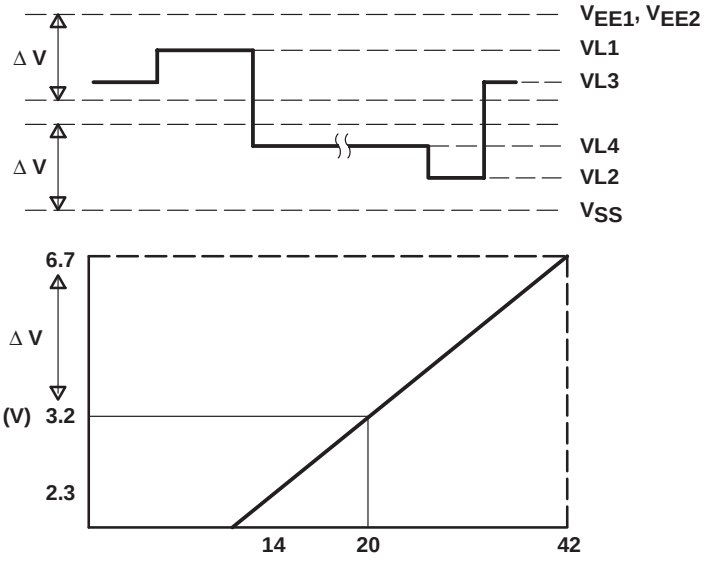


Figure 1. VLn Voltage Range

recommended operating conditions (see Figure 2)

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	See Notes 4 and 5		4.5	5	5.5	V
Supply voltage, V_{SS}				0		V
Supply voltage for LCD drive	See Notes 4 and 5	V_{EE1}, V_{EE2}, VL1, VL3, VL4, VL2	20		42	V
High-level input voltage, V_{IH}		80CH, BS, D7–D0, $\overline{\text{DISP OFF}}$, DST, EIO1-EIO4, L/R, M, MODE, SCK, TEST	0.8 V_{CC}		V_{CC}	V
Low-level input voltage, V_{IL}		80CH, BS, D7–D0, $\overline{\text{DISP OFF}}$, DST, EIO1-EIO4, L/R, M, MODE, SCK, TEST	V_{SS}		0.2 V_{CC}	V
Clock frequency, f_{CLK}		DST			1	MHz
Operating free-air temperature, T_A			–55		125	°C

NOTES: 4. VLn voltage range should be under the following conditions:
V_{EE1} and $V_{EE2} \geq$ VL1 $\geq$ VL3 $\geq V_{EE}$ - 7 V, and 7 V $\geq$ VL4 $\geq$ VL2 $\geq V_{SS1}$, V_{SS2} V_{SS3}
V_{EE1} and V_{EE2} > VL1 > VL3 > V_{EE} - Δ V, and Δ V > VL4 > VL2 > V_{SS1}, V_{SS2} V_{SS3}
5. Power-up and power-down sequences are as follows:
Power-up sequence: V_{CC} → Input → V_{EE1}, V_{EE2}, V_{EE3}
Power-down sequence: V_{EE1}, V_{EE2}, V_{EE3} → Input → V_{CC}

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	EIO1-EIO4	V_{CC} = 5 V ± 10%, I_{OH} = -0.4 MA	V_{CC}- 0.4		V_{CC}	V
V_{OL}	Low-level output voltage	EIO1-EIO4	V_{CC} = 5 V ± 10%, I_{OL} = -0.4 MA	V_{SS}		0.4	V
I_{IH}	High-level input current	80CH, BS, D7–D0, $\overline{\text{DISP OFF}}$, DST, EIO1-EIO4, L/R, M, MODE, SCK	V_{IH} = V_{CC}			5	μA
		TEST				500	μA
I_{IL}	Low-level input current	80CH, BS, D7–D0, $\overline{\text{DISP OFF}}$, DST, EIO1-EIO4, L/R, M, MODE, SCK	V_{IL} = V_{SS}			-5	μA
		TEST				-5	μA
Z_O	Output impedance	OUT1 to OUT160	V_{EE} = 14 V, VLn = ΔV, I_O = 150 μA,			3	kΩ
ΔZ_O	Output impedance variance	OUT1 to OUT160	See Note 6		±10%	±30%	
I_I	Input current	VL1, VL2, VL3, VL4	V_I = V_{EE}, V_{SS}			±100	μA
I_{CC}	Supply current	V_{CC}	1/480 duty operation, See Note 7			1	mA
I_{EE}	Supply current	V_{EE1}, V_{EE2}				0.5	mA
I_{CC}	Supply current	V_{CC}	1/480 duty operation			5	mA
I_{EE}	Supply current	V_{EE1}, V_{EE2}				2	mA
$I_{I(standby)}$	Standby current	V_{CC}	See Note 8			500	μA

NOTES: 6. ΔZ_O = (1-Xn/Xaverage) x 100
Xn = impedance or OUTn, Xaverage = impedance of average OUTn
7. f_{DST} = 36 kHz, V_{IH} = V_{CC}, V_{IL} = V_{SS}, and no output load.
8. Voltage level at EIO1 input = V_{CC}

timing requirements over full range of recommended operating conditions (unless otherwise noted)

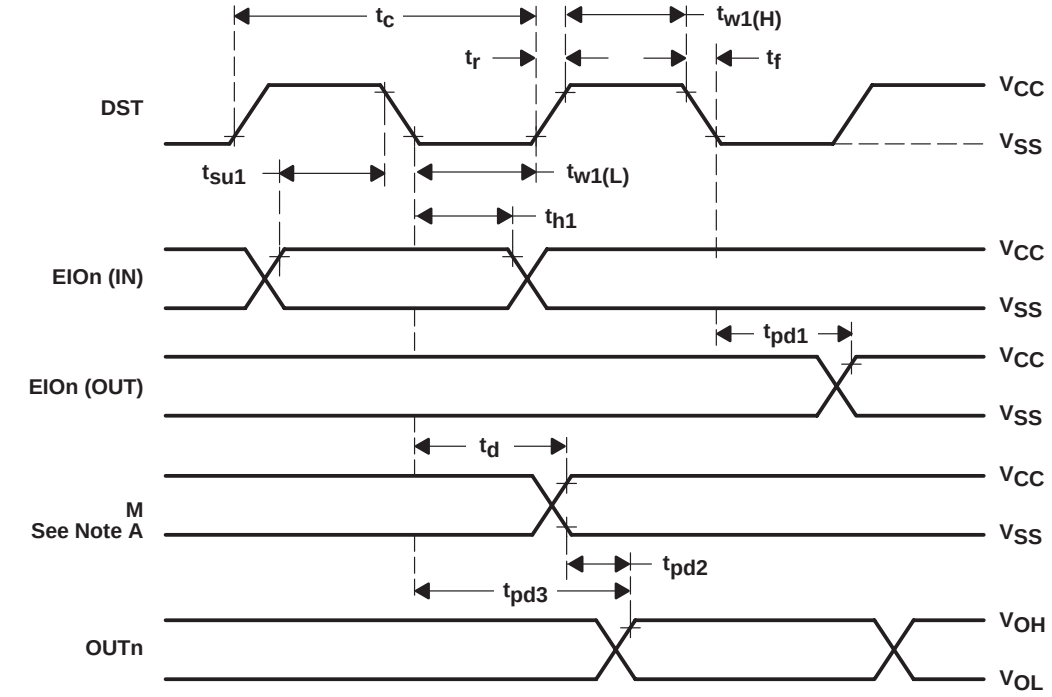
	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_c	Cycle time	DST		1		µs
$t_{w1(L)}$	Pulse duration, low pulse width	DST	See Figure 2	970		ns
$t_{w1(H)}$	Pulse duration, high pulse width			30		ns
t_{su1}	Setup time, EIOn valid to DST↓		See Figure 2	100		ns
t_{h1}	Hold time, EIOn valid to DST↓			30		ns
t_d	Frame delay tolerance time		See Note 10		±300	ns

NOTE 9: This parameter is not production tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
$t_{pd}1$	Propagation delay time, DST↓ to EIO1 valid	C_L = 30 pF,	See Figure 2		110	ns
$t_{pd}2$	Propagation delay time, M valid to OUTn valid	C_L = 45 pF,	See Figure 2		1.5	µs
$t_{pd}3$	Propagation delay time, DST↓ to OUTn valid				0.7	µs

PARAMETER MEASUREMENT INFORMATION



NOTES: A. t_r and $t_f \leq 30$ns for input pulses
B. $V_{IH} = 0.8\ V_{CC}$, $V_{IL} = 0.2\ V_{CC}$

Figure 2. Clock Timing Waveforms for Common-Driver Mode

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