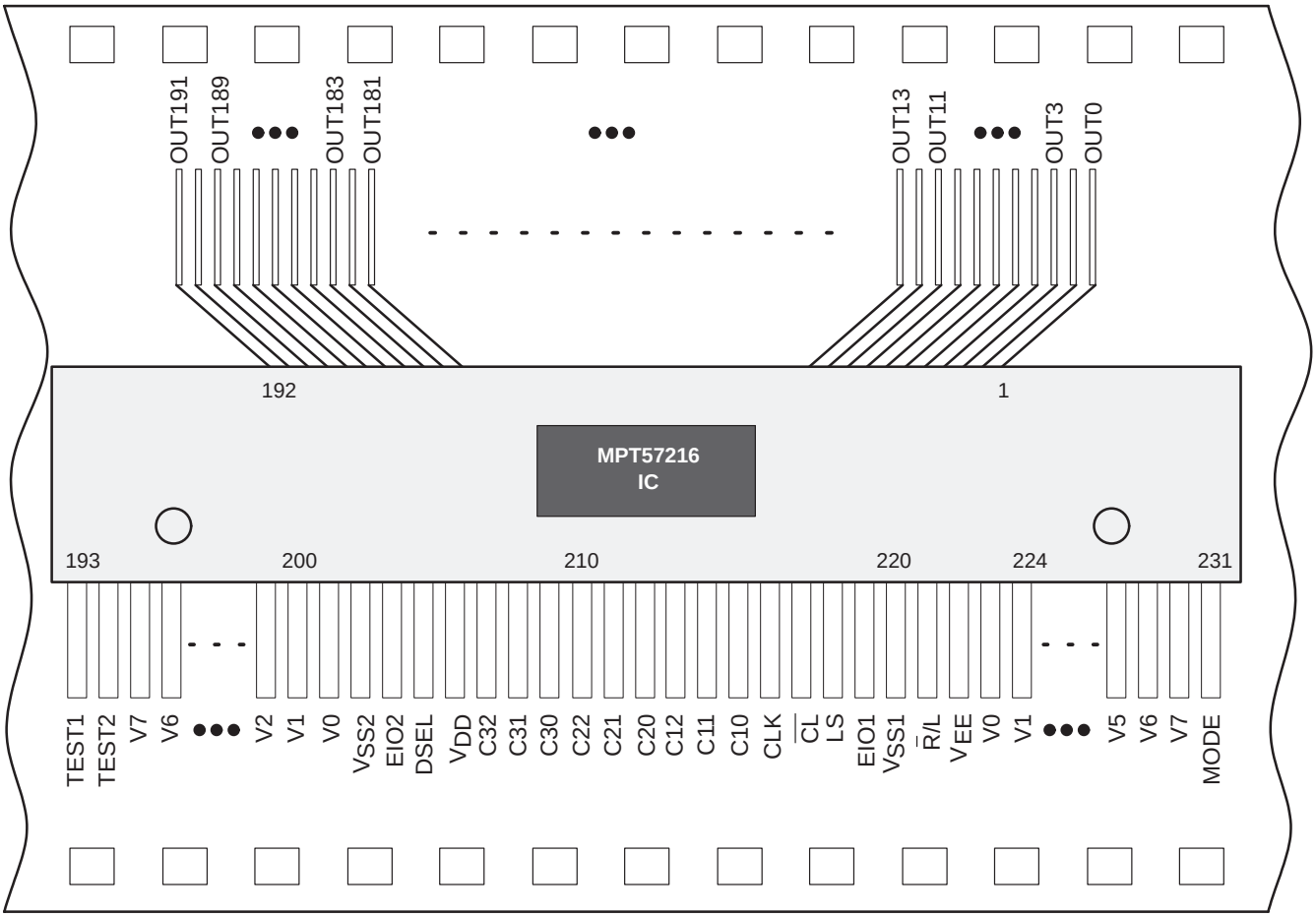
- **Column (Source) Driver**
- **V_{EE} of 14 V to 18 V for LCD Driving**
- **192 Channel Outputs**
- **Data Bus With 3 x 3 (RGB) Bits**
- **512 Colors (8 Gray Scale)**
- **15-MHz Data Transfer Clock**
- **Clock-Control Circuit Conserves Power Consumption**
- **Power Supply Voltage of 5 V ±10%**
- **High-Voltage CMOS SI Gate Technology**
- **231-Pin TAB (Tape Automated Bonding)**
- **Functional Equivalent of MPT57206**

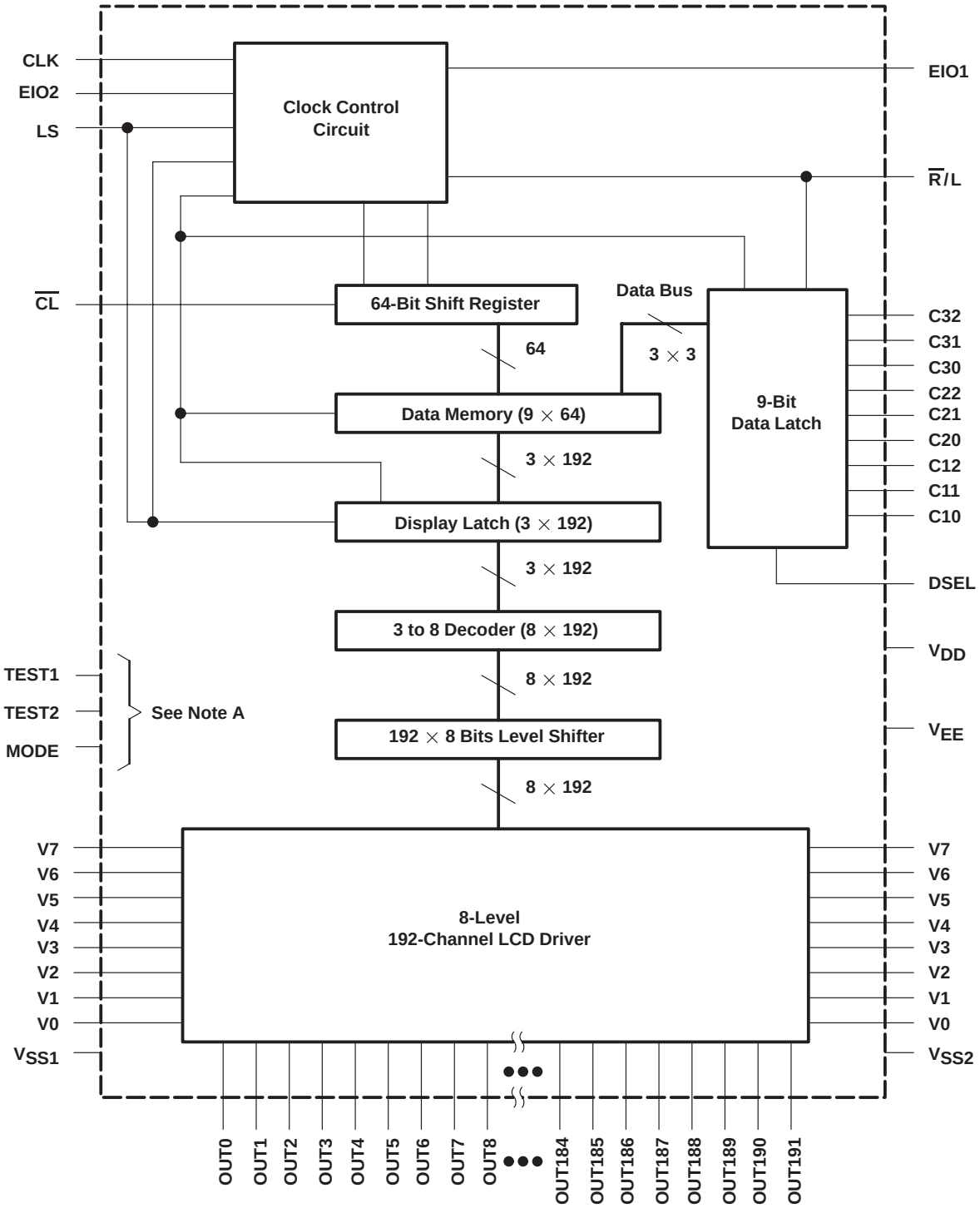


NOTE A: Pin numbering is for reference only to the function table. The pin numbering in this figure does not correspond to the numbering on the custom tape.

description

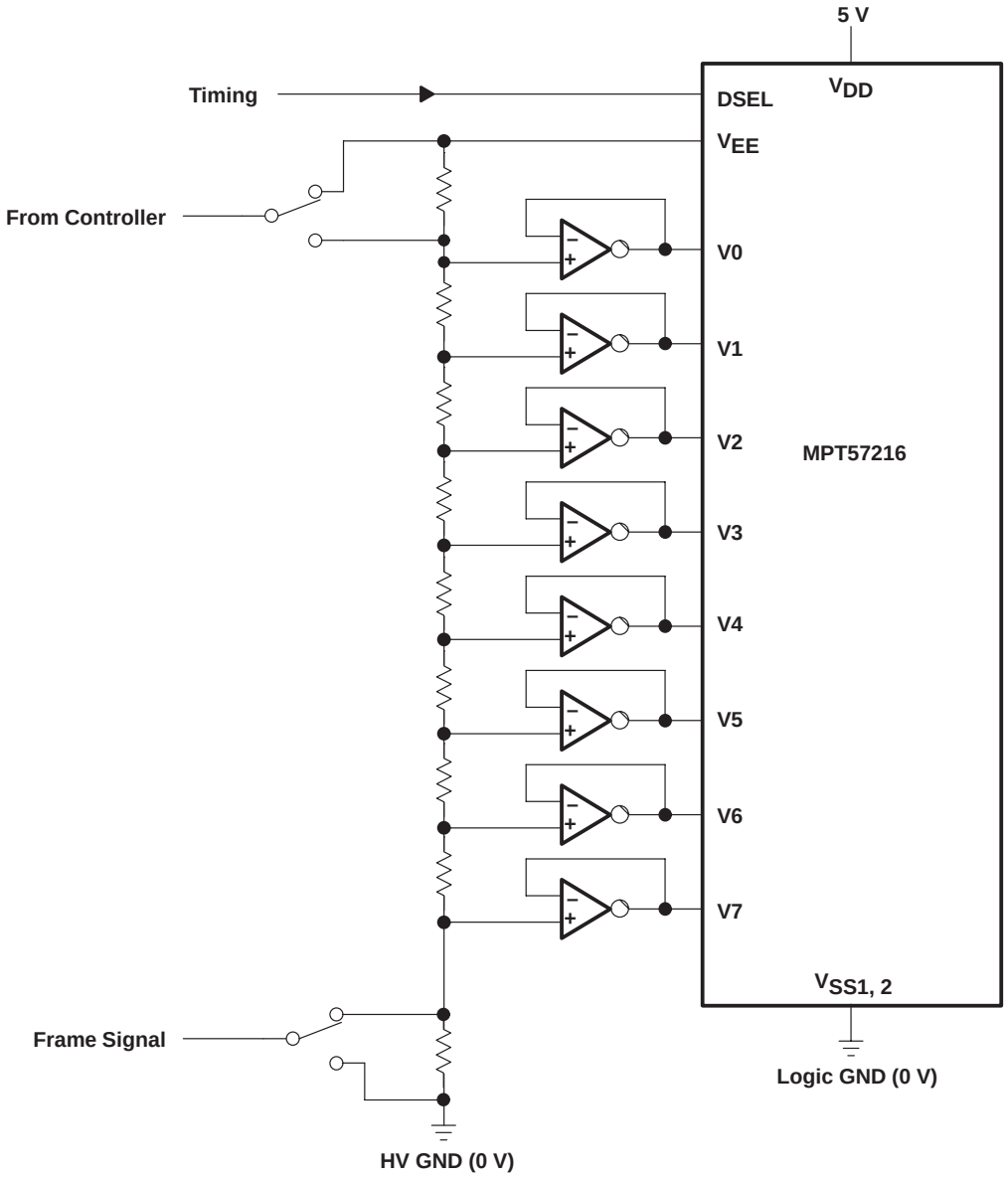
The MPT57216 is a 192-channel color thin-film transistor (TFT) LCD driver based on an active matrix LCD (AMLCD). It has 3 bits for each RGB input. These 3 bits are decoded internally to select one of eight bias-voltage levels, V0 to V7 for output, in order to support 512 colors (R = 2^3 = 8; G = 2^3 = 8; B = 2^3 = 8; RGB = 2^9 = 512).

functional block diagram



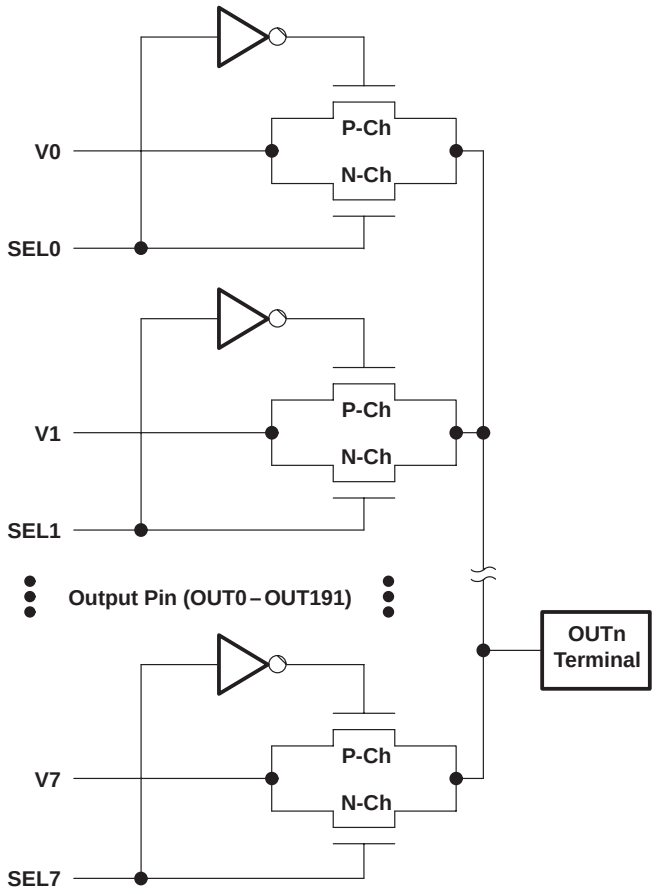
NOTE A: These terminals are for factory testing only and should be left open.

power supply circuit



NOTE A: Separation between high voltage GND line and logic GND line is recommended to avoid noise problems.

decoding for OUT0 – OUT191



NOTE A. The C32 – C10 inputs are decoded internally to derive SEL0 – SEL7 from the output of a 3-to-8 decoder. Only one of the decoder outputs, SEL0 – SEL7, puts ≈V_{EE} on the P-CH and ≈V_{SS} on the N-CH of its corresponding transmission gate. This allows only one of eight bias voltages, V0 – V7, to pass onto OUTn.

Terminal Functions

<table>
<tr><th>NAME</th><th>TERMINAL</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>C32
C31
C30
C22
C21
C20
C12
C11
C10</td><td>207
208
209
210
211
212
213
214
215</td><td>I</td><td>RGB color data input. These nine inputs of 3-bit input data at each of 3 RGB ports selects up to 8-levels of grey scale on the LCD outputs. For Cmn: m = port number and n = weight selected.
<table>
<tr><th colspan="3">INPUT</th><th colspan="2">OUTPUT</th></tr>
<tr><th>C32
C22
C12</th><th>C31
C21
C11</th><th>C30
C20
C10</th><th>DSEL = L
(Noninverted)</th><th>DESEL = H
(Inverted)</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>V7</td><td>V0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>V6</td><td>V1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>V5</td><td>V2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>V4</td><td>V3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>V3</td><td>V4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>V2</td><td>V5</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>V1</td><td>V6</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>V0</td><td>V7</td></tr>
</table></td></tr>
<tr><td>$\overline{CL}$</td><td>217</td><td>I</td><td>Clear input. This active-low clear input resets the clock control circuit, shift register, data memory, and display latch. $\overline{CL}$ also sets output to the V0 level. $\overline{CL}$ must be asserted high for normal operation.</td></tr>
<tr><td>CLK</td><td>216</td><td>I</td><td>Clock input. CLK is the rising edge systems clock for the 64-bit shift register. Also, 9 bits of data are stored in the data memory by the falling edge of CLK. The clock control circuit stops the internal system clock to save power consumption after 64 clocks.</td></tr>
<tr><td>DSEL</td><td>205</td><td>I</td><td>Data select input. This input inverts the data on C10 to C32 input.
<table>
<tr><th>INPUT DATA</th><th colspan="2">DATA MEMORY</th></tr>
<tr><th>C10 to C32</th><th>DSEL = L</th><th>DSEL = H</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>EIO1
EIO2</td><td>219
204</td><td>I/O</td><td>Enable I/O. EIO1 and EIO2 are data enable input/output for cascade interface.
<table>
<tr><th>$\overline{R}$/L</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>H (Left Shift)</td><td>Cascade Input</td><td>Cascade Output (OUT0 – OUT191)</td></tr>
<tr><td>L (Right Shift)</td><td>Cascade Output</td><td>Cascade Input (OUT191 – OUT0)</td></tr>
</table></td></tr>
<tr><td>LS</td><td>218</td><td>I</td><td>Latch Strobe Input. When LS is high, 9 x 64 bits of data memory is latched into the display latch (3 x 192) and passed through a 3-to-8 decoder. The decoder selects one of eight bias voltage V0 – V7 to be passed on to OUTn using a transmission gate. LS also clears the shift register and clock control circuit.</td></tr>
<tr><td>MODE</td><td>231</td><td>I</td><td>Mode input. MODE is used for factory testing only and should be left open. The internal pullup resistors connected to V_{DD} force the inputs into a high state.</td></tr>
<tr><td>OUT0 –
OUT191</td><td>1 – 192</td><td>O</td><td>192-channel output for RGB color LCD display. C1x, C2x, and C3x select bias voltages, V0 – V7, on OUT(3n), OUT(3n+1), and OUT(3n+2), where n = 0 – 63, respectively.</td></tr>
</table>

Terminal Functions (continued)

<table>
<tr><th>NAME</th><th>TERMINAL</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>$\overline{R}$/L</td><td>221</td><td>I</td><td>Select right/left shift. $\overline{R}$/L selects which direction the EIOn enable pulse advances through the 64-bit shift register. It also selects which direction the 3-bit × 3 RGB data from the data latch is loaded into three different but adjacent channels of data memory. This data is loaded as the channels are enabled three at a time by the enable pulse from the shift register. It advances from one output to the next when shifting through the shift register with each clock pulse.
<table>
<tr><th>$\overline{R}$/L</th><th>H</th><th>L</th></tr>
<tr><td>Shift Direction</td><td>Left</td><td>Right</td></tr>
<tr><td>EIO1</td><td>Input</td><td>Output</td></tr>
<tr><td>EIO2</td><td>Output</td><td>Input</td></tr>
<tr><td>CLK</td><td>1, 2, 3, ... 64</td><td>1, 2, 3, ... 64</td></tr>
<tr><td>C32 – C30</td><td>2, 5, 8, ... 191</td><td>191, 188, 185, ... 2</td></tr>
<tr><td>C22 – C20</td><td>1, 4, 7, ... 190</td><td>190, 187, 184, ... 1</td></tr>
<tr><td>C12 – C10</td><td>0, 3, 6, ... 189</td><td>189, 186, 183, ... 0</td></tr>
</table></td></tr>
<tr><td>TEST1
TEST2</td><td>193
194</td><td>I</td><td>Test input. TEST1 and TEST2 are used for factory testing only and should be left open. The internal pullup resistors connected to V_{DD} force the inputs into a high state.</td></tr>
<tr><td>V0 – V7
V0 – V7</td><td>202 – 195
223 – 230</td><td>I</td><td>Eight-level input bias voltage for output buffer. After the three bits for each RGB color are decoded, the device outputs one voltage level from the eight possible bias voltages (V0 – V7). There is no priority on the V0 to V7 terminals. A pair of V0 to V7 bias voltage terminals are provided. Each pair of terminals is required to be connected together externally.</td></tr>
<tr><td>V_{DD}</td><td>206</td><td></td><td>5-V supply input for logic circuits</td></tr>
<tr><td>V_{EE}</td><td>222</td><td></td><td>Supply input for level shifter and output transmission gate.</td></tr>
<tr><td>V_{SS1}
V_{SS2}</td><td>220
203</td><td></td><td>Ground terminals</td></tr>
</table>

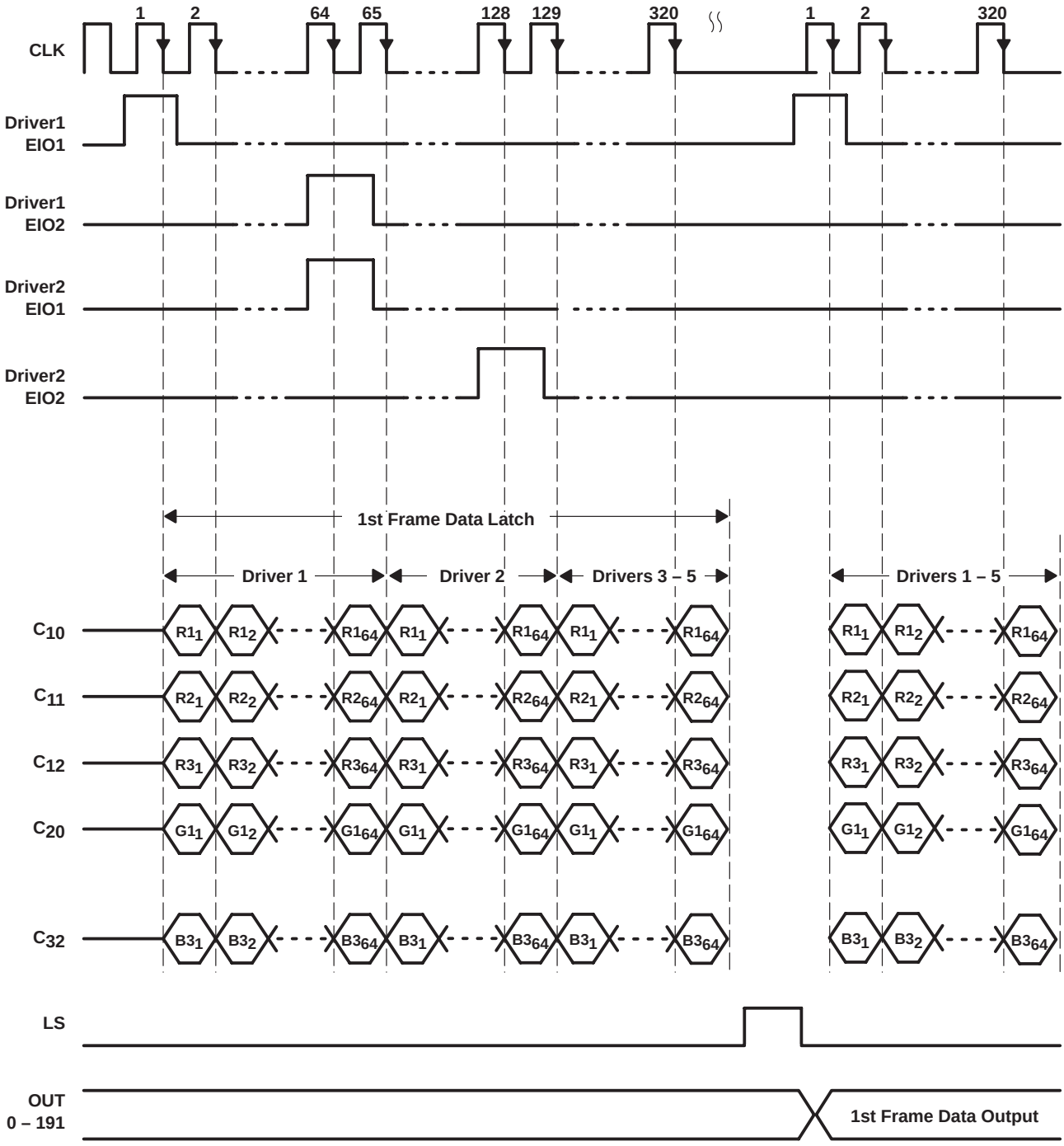


Figure 1. Timing Diagram ($\overline{R}$/L = H)

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.3 V to 7 V
Supply voltage range for LCD, V_{EE} . –0.3 V to 22 V
Input voltage range, V_I (CLK, LS, R/L, $\overline{CL}$, C32 to C10, DSEL, EIO1, EIO2) . . . . . –0.3 V to V_{DD} + 0.3 V
Output voltage range, V_O (E101, E102) . . . . . –0.3 V to V_{DD} + 0.3 V
Output bias voltage range for LCD, Vx . . . . . –0.6 V to V_{DD} + 0.6 V
Input current, I_I . . . . . ± 10 mA
Output current, I_O: E101, E102 . . . . . 10 mA
OUT0 to OUT191 . . . . . 5 mA
Power dissipation, P_D . . . . . 0.3 W
Operating free-air temperature range, T_A . . . . . –55 to 125°C
Storage temperature range, T_{stg} . . . . . 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to V_{SS1} and V_{SS2}

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	See Note 2	4.5	5	5.5	V
Supply voltage, V_{EE}	See Note 2	14		18	V
Output bias voltage for LCD driver	V0, V1, V2, V3, V4, V5, V6, V7 See Note 2	0		V_{EE}	V
High-level input voltage, V_{IH}	CLK, LS, DSEL, R/L, $\overline{CL}$, EIO1, EIO2, C32 to C10	0.8 V_{DD}		V_{DD}	V
Low-level input voltage, V_{IL}	CLK, LS, DSEL, R/L, $\overline{CL}$, EIO1, EIO2, C32 to C10	V_{SS}		0.2 V_{DD}	V
Clock frequency at CLK, $f_{(CLK)}$	CLK			15	MHZ
Clock frequency at LS, $f_{(LS)}$	LS			100	kHz
Operating free-air temperature, T_A		–55		125	°C

NOTE 2: Turn-on and -off sequence of power must be as follows:
Turn-on sequence: V_{DD} → Logic Input → V_{EE} → V7 to V0
Turn-off sequence: V7 to V0 → V_{EE} → Input → V_{DD}

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	E101, E102	I_{OH} = –0.3 mA		V_{DD}–0.4		V
V_{OL}	Low-level output voltage	E101, E102	I_{OH} = 0.3 mA			0.4	V
I_{IH}	High-level input current	CLK, DSEL, LS, R/L, CL, EIO1, EIO2, C32 to C10	$V_{IH} = V_{DD}$			10	μA
I_{IL}	Low-level input current	CLK, DSEL, LS, R/L, CL, EIO1, EIO2, C32 to C10	$V_{IL} = V_{SS}$			10	μA
I_{lkg}	Input leakage current	V7 to V0	$V_{SS} < Vx < V_{EE}$		–100	100	μA
ΔV_{IO}	Voltage difference between Vx to OUTn (voltage variance)	Vx - OUTn	$I_{I/O}$ = ± 10 μA,	$V_{SS} < Vx < V_{EE}$		50	mV
$R_{o(on)}$	Output resistance	OUT0 – OUT191	I_O = ± 100 μA			5	kΩ
I_{DD}	Supply current	V_{DD}	$f_{(CLK)}$ = 15 MHZ, $f_{(LS)}$ = 30 KHZ, V_{EE} = 18V	$f_{(EIOxin)}$ = 30 KHZ, V_{DD} = 5.5 V,		4	mA
I_{EE}	Supply current	V_{EE}	$f_{(CLK)}$ = 15 MHZ, $f_{(LS)}$ = 30 KHZ, V_{EE} = 17V	$f_{(EIOxin)}$ = 30 KHZ, V_{DD} = 5 V,		1	mA
$I_{I(standby)}$	Standby current	V_{DD}	V_{DD} = 5 V, See Note 3	V_{EE} = 17 V		300	μA
		V_{EE}	V_{DD} = 5 V, See Note 3	V_{EE} = 17 V		100	μA

NOTE 3: Test conditions of standby current are added at $\overline{R}/L = V_{DD}$, and EIO1 = V_{SS}.

timing requirements, V_{DD} = 5 V, T_A = –55°C to 125°C

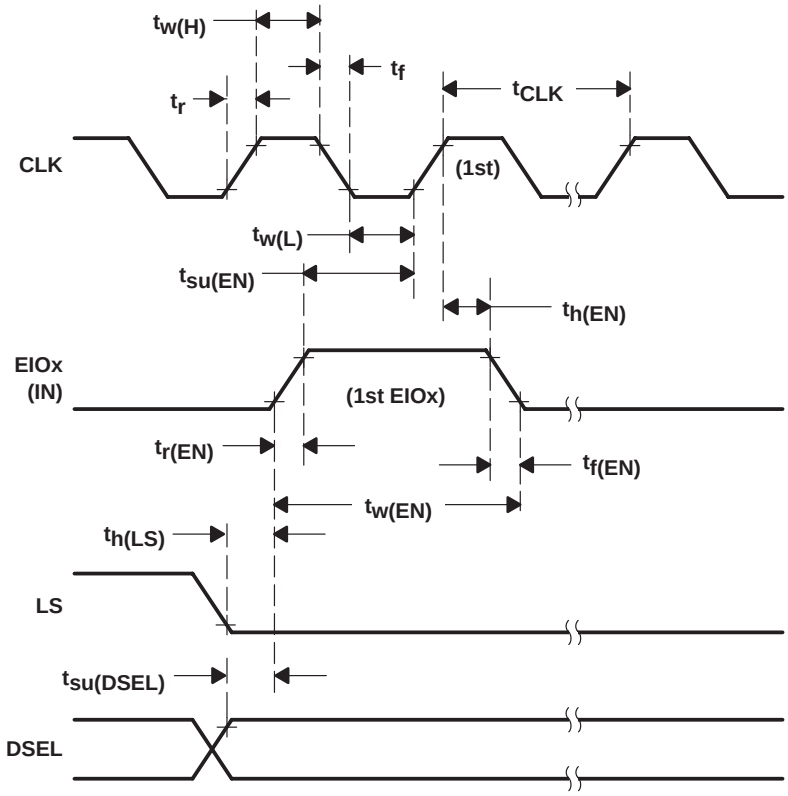
PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
t_{CLK}	Clock cycle time	CLK	See Figures 2 and 4	66		ns
$t_{W(L)}$	Low-level pulse width		See Figure 2	23		ns
$t_{w(H)}$	High-level pulse width		See Figure 2	18		ns
t_{su}	Data setup time	Cxx ─ CLK	See Figure 4	10		ns
t_h	Data hold time	CLK ─ Cxx	See Figure 4	15		ns
$t_{w(EN)}$	Enable high-level pulse width	EIO1, EIO2	See Figure 2	$1/f_{CLK}$		ns
$t_{su(EN)}$	Enable setup time	EIOx ─ CLK	See Figure 2	20	30 or $1/f_{CLK}$	ns
$t_{h(EN)}$	Enable hold time	CLK ─ EIOx	See Figure 2	10	$t_{CLK} \times 62$	ns
$t_{w(LS)}$	Latch strobe high-level pulse width	LS	See Figure 3	40		ns
$t_{su(LS)}$	LS setup time		See Figure 3	66		ns
$t_{h(LS)}$	LS hold time		See Figure 2	40		ns
$t_{su(DSEL)}$	DSEL setup time	EIOx ─ DSEL	See Figure 2	66		ns

switching characteristics, V_{DD} = 5 V, T_A = –55°C to 125°C over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$t_{p(EN)}$	Enable propagation delay time	CLK – EIOx	C_L = 35 pF, See Note 4 and Figure 4		40	ns
$t_{p(OUT)}$	Output propagation delay time	LS – OUTn	C_L = 200 pF, See Note 4 and Figure 3		3.0	µs

NOTE 4: C_L includes probe and jig capacitance.

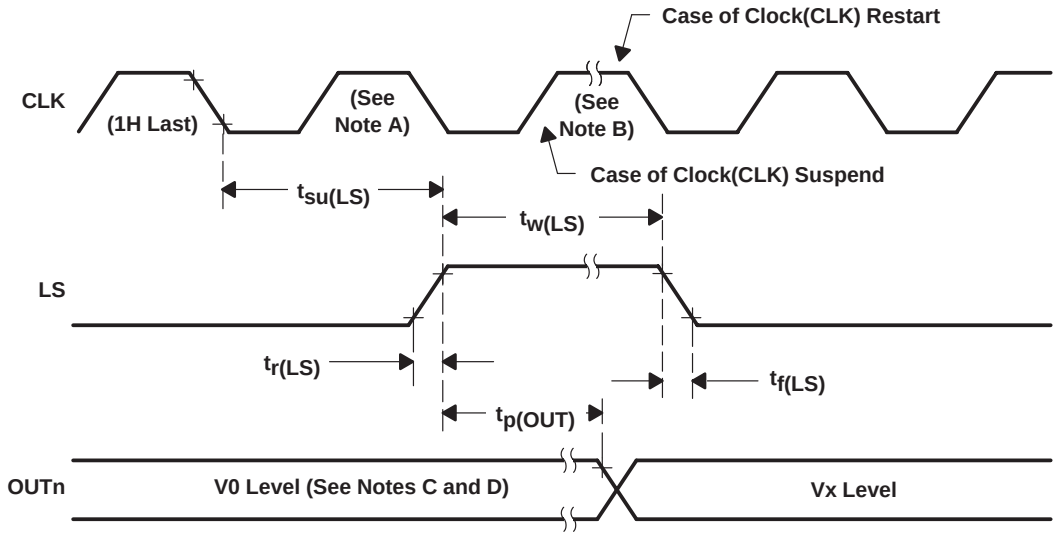
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulse generators have the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 15 ns, t_f ≤ 15 ns, z_o = 50 Ω.
B. V_{IH} and V_{IL} for all waveforms are at 0.8 V_{DD} and 0.2 V_{DD} respectively.
C. All timing parameters and measurements are referenced at the 0.5 V_{DD} point of each waveform.

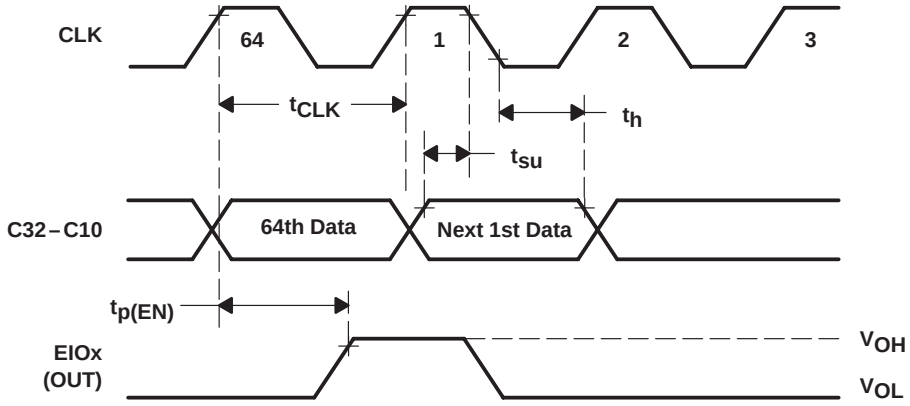
Figure 2. EIOx (IN), LS, and DSEL Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Case of data input change: if data has changed after the last clock of 1H, then it is recommended to add a dummy clock of one pulse after the last 1H pulse of the clock.
B. Case of suspending clock (CLK) after data transfer (1H) completion: it is recommended that the data input not be changed while the clock is suspended.
C. All timing parameters and measurements are referenced at the 0.5 V_{DD} point of each waveform except $t_{p(OUT)}$ on the OUTn waveform. The reference point on the OUTn waveform is V0 + 0.1 Vx for positive-going transitions and V0 – 0.1 Vx for negative-going transitions.
D. OUTn waveform transitions are from V0 level to Vx level. Maximum V0 and Vx levels are 8.0 V due to tester limitations.
E. Input pulse generators have the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 15 ns, t_f ≤ 15 ns, z_o = 50 Ω.
F. V_{IH} and V_{IL} for all waveforms are at 0.8 V_{DD} and 0.2 V_{DD} respectively.

Figure 3. LS and OUTn Timing Waveforms



NOTES: A. Input pulse generators have the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 15 ns, t_f ≤ 15 ns, z_o = 50 Ω.
B. V_{IH} and V_{IL} for all waveforms are at 0.8 V_{DD} and 0.2 V_{DD} respectively.
C. All timing parameters and measurements are referenced at the 0.5 V_{DD} point of each waveform.

Figure 4. Cxx and EIOx (OUT) Timing Waveforms

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