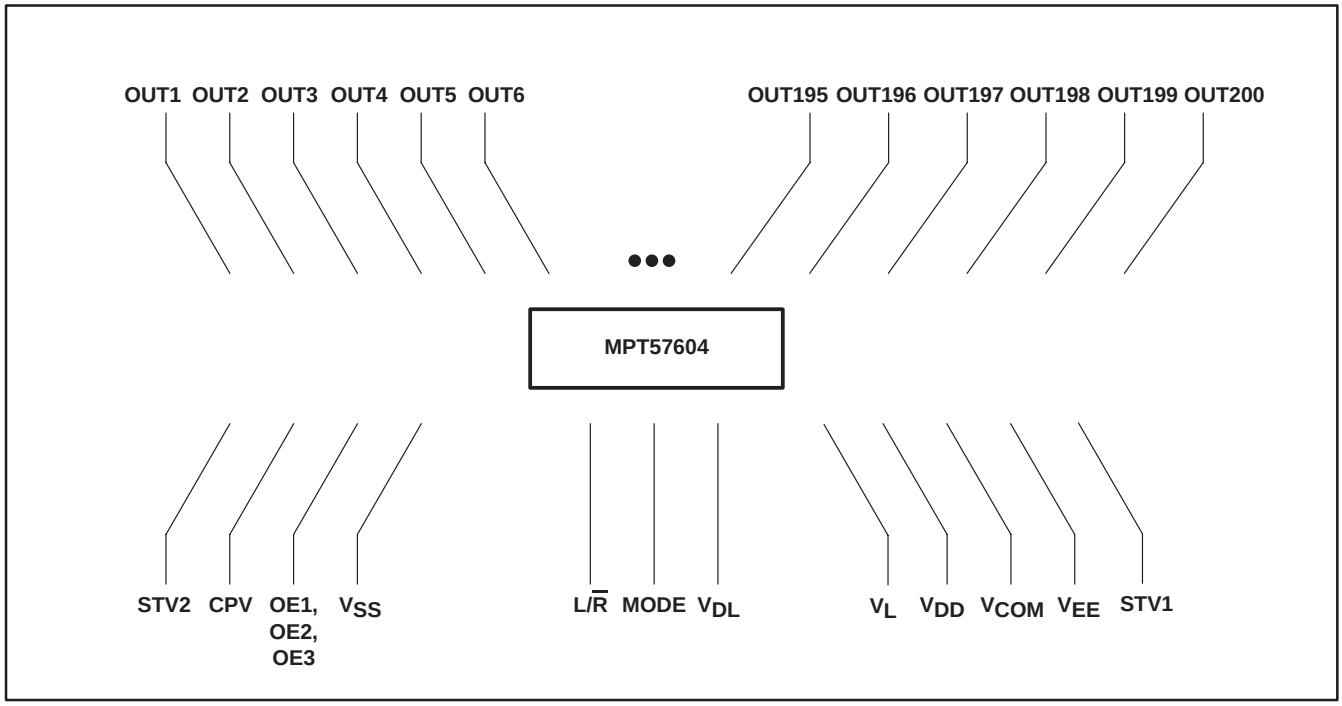
- **Gate Driver LSI for Active-Matrix LCD**
- **Liquid-Crystal Control Outputs: 200 (Switchable to 192 Outputs)**
- **Enables High-Voltage Operation: Liquid-Crystal Control Signal V_L + 35 V (max)**
- **Liquid-Crystal Control Signal's Negative-Voltage Output is Enabled by a Level-Shift Circuit**
- **On-Chip Bidirectional Shift Registers**
- **TCP (Tape Carrier Package)**
- **CMOS-LSI Structure**

description

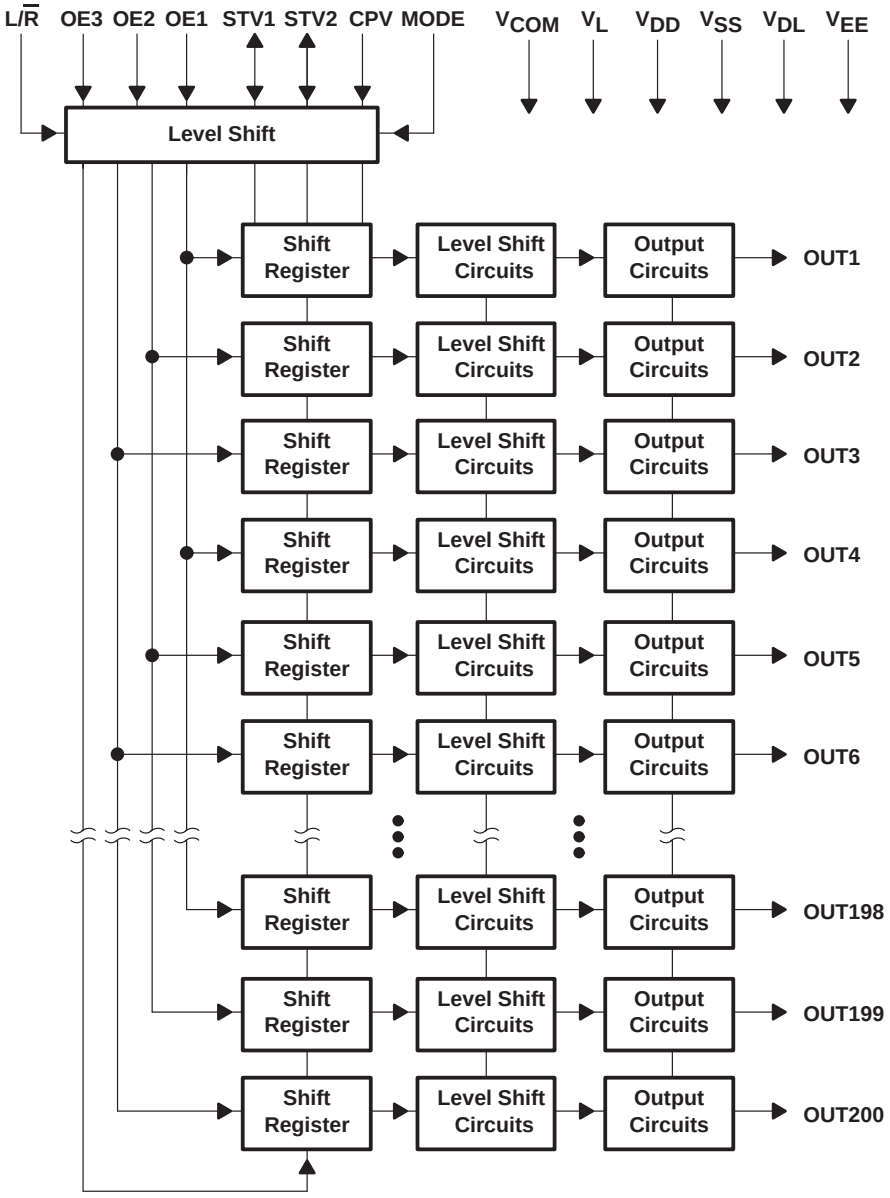
The MPT57604 is a gate driver LSI that drives an active-matrix LCD panel and that implements a multi-pin configuration, low power consumption, and high voltage. Furthermore, the level-shift circuit enables positive and negative power supplies. Also, it has a liquid-crystal control output switching mode (192 outputs/200 outputs), so it is compatible with various SVGA/XGA panels.



NOTE A: This figure shows the copper foil side and does not describe the TAB outline or show the NC pins.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CPV		I	Vertical shift clock input The shift register's shift clock. Data are shifted in sync with the rising edge of this pin.
OE1 OE2 OE3		I	Output enable pins The liquid-crystal control output is held low by setting pins OE1, 2, and 3 High. However, the shift registers are not cleared. OE is async with CPV. Enable control target pin: 200-output mode OE1: OUT1, OUT4, OUT7...OUT196, OUT199 OE2: OUT2, OUT5, OUT8...OUT197, OUT200 OE3: OUT3, OUT6, OUT9...OUT198 192-output mode OE1: OUT1, OUT4, OUT7...OUT190 OE2: OUT2, OUT5, OUT8...OUT191 OE3: OUT3, OUT6, OUT9...OUT192 These combinations are generally as above, regardless of the L/$\overline{R}$ polarity.
L/$\overline{R}$		I	Shift direction switching pin This pin is used to switch the data's shift direction. L/$\overline{R}$ = L: Mode = V_{EE} STV1 ← OUT1 ← OUT2...OUT199 ← OUT200 ← STV2 Mode = V_{DL} STV1 ← OUT1 ← OUT2...OUT191 ← OUT192 ← STV2 L/$\overline{R}$ = H: Mode = V_{EE} STV1 → OUT1 → OUT2...OUT199 → OUT200 → STV2 Mode = V_{DL} STV1 → OUT1 → OUT2...OUT191 → OUT192 → STV2
Mode		I	Mode switching input pin Sets either the 200-output mode or the 192-output mode. Connects to V_{EE} in the 200-output mode. Connects to V_{DL} in the 192-output mode. For details regarding the output pins, refer to pins OUT1-OUT200. Furthermore, the mode pin is connected on the TCP.
STV1 STV2		I/O	Shift data I/O pins These pins are used to input/output data to/from a shift register. During input, data are captured in sync with the leading edge of CPV. During output, data are output in sync with its trailing edge. L/$\overline{R}$ = L: STV1 is the next-stage data output pin, and STV2 is the shift data input pin. L/$\overline{R}$ = H: STV1 is the shift data input pin, and STV2 is the next-stage data output pin.

Terminal Functions (continued)

<table>
<tr><th colspan="2">TERMINAL
NAME NO.</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td colspan="2">OUT1
thru
OUT200</td><td>O</td><td>Liquid-crystal control output pin
A shift register’s data are output after level conversion.
The Mode pin is used to select 192 outputs or 200 outputs.
In the 192-channel mode, the shift registers operate, except for the data corresponding to OUT97-104.

<table>
<tr><th colspan="2">192-Ch Mode</th><th colspan="2">200-Ch Mode</th></tr>
<tr><td colspan="2">MODE = ”V_{DL}”</td><td colspan="2">MODE = ”V_{EE}”</td></tr>
<tr><td>OUT1</td><td>(OE1)</td><td>OUT1</td><td>(OE1)</td></tr>
<tr><td>OUT2</td><td>(OE2)</td><td>OUT2</td><td>(OE2)</td></tr>
<tr><td>OUT3</td><td>(OE3)</td><td>OUT3</td><td>(OE3)</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>OUT94</td><td>(OE1)</td><td>OUT94</td><td>(OE1)</td></tr>
<tr><td>OUT95</td><td>(OE2)</td><td>OUT95</td><td>(OE2)</td></tr>
<tr><td>OUT96</td><td>(OE3)</td><td>OUT96</td><td>(OE3)</td></tr>
<tr><td></td><td>N/A</td><td>OUT97</td><td>(OE1)</td></tr>
<tr><td></td><td>N/A</td><td>OUT98</td><td>(OE2)</td></tr>
<tr><td></td><td>N/A</td><td>OUT99</td><td>(OE3)</td></tr>
<tr><td></td><td>N/A</td><td>OUT100</td><td>(OE1)</td></tr>
<tr><td></td><td>N/A</td><td>OUT101</td><td>(OE2)</td></tr>
<tr><td></td><td>N/A</td><td>OUT102</td><td>(OE3)</td></tr>
<tr><td></td><td>N/A</td><td>OUT103</td><td>(OE1)</td></tr>
<tr><td></td><td>N/A</td><td>OUT104</td><td>(OE2)</td></tr>
<tr><td>OUT105</td><td>(OE1)</td><td>OUT105</td><td>(OE3)</td></tr>
<tr><td>OUT106</td><td>(OE2)</td><td>OUT106</td><td>(OE1)</td></tr>
<tr><td>OUT107</td><td>(OE3)</td><td>OUT107</td><td>(OE2)</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>OUT197</td><td>(OE3)</td><td>OUT197</td><td>(OE2)</td></tr>
<tr><td>OUT198</td><td>(OE1)</td><td>OUT198</td><td>(OE3)</td></tr>
<tr><td>OUT199</td><td>(OE2)</td><td>OUT199</td><td>(OE1)</td></tr>
<tr><td>OUT200</td><td>(OE3)</td><td>OUT200</td><td>(OE2)</td></tr>
</table>

N/A: Output pins do not exist and are therefore unusable.
(OEn) indicates the relationship among OE1, OE2, and OE3.</td></tr>
<tr><td colspan="2">V_{COM}</td><td></td><td>Power supply for high-withstand-voltage logic</td></tr>
<tr><td colspan="2">V_{DD}</td><td></td><td>Power supply for logic input</td></tr>
<tr><td colspan="2">V_{SS}</td><td></td><td>GND for logic input</td></tr>
<tr><td colspan="2">V_{DL}</td><td></td><td>Power supply for internal logic</td></tr>
<tr><td colspan="2">V_{EE}</td><td></td><td>GND</td></tr>
<tr><td colspan="2">V_L</td><td></td><td>Negative power supply for liquid-crystal control</td></tr>
</table>

detailed description

Liquid-Crystal Control Output Voltage

The MPT57604 enables negative-voltage output for the liquid-crystal control output.

$V_{COM} – V_L$ = 35 V max $V_L – V_{EE}$ = 0-6 V. $V_{COM} – V_{SS}$ = 10-20 V.

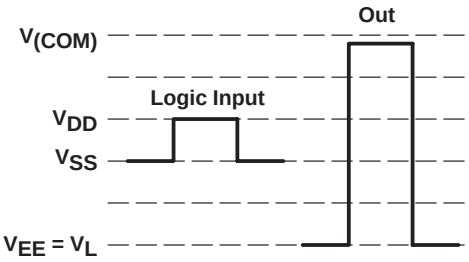


Figure 1. Liquid-Crystal Control Output Voltage

For the input signals (CPV, OE1-3, L/$\overline{R}$, STV1 and STV2), input the amplitude of V_{DD} from V_{SS}.

The next-stage data output pins (STV1, STV2) output the next level:
H level = V_{DD}
L level = V_{SS}

Details of Operation

The liquid-crystal control outputs (OUT1-200) output either a selective signal (H) or a non-selective signal (L), depending on the input signals (STV1 and STV2, CPV, OE1, OE2, OE3).

A right data shift (OUT1 $\rightarrow$ OUT200) or a left data shift (OUT200 $\rightarrow$ OUT1) can be selected by means of the shift direction switching pin (L/$\overline{R}$).

When the L/$\overline{R}$ pin is H, the vertical shift data (STV1) are captured at the leading edge of the shift clock (CPV), after which they are output to the liquid-crystal control output OUT1. Furthermore, the OUT1 output data are shifted to OUT2 at the leading edge of the next CPV, and the data newly fetched from STV1 are output to OUT1. In this manner, they are shifted successively in sync with the leading edge of CPV, and the OUT200 data are output to STV2 in sync with the trailing edge of CPV.

When the L/$\overline{R}$ pin is L, the vertical shift data (STV2) are captured at the leading edge of the shift clock (CPV), after which they are output to the liquid-crystal control output OUT200. Furthermore, the OUT200 output data are shifted to OUT199 at the leading edge of the next CPV, and the data newly fetched from STV2 are output to OUT200. In this manner, they are shifted successively in sync with the leading edge of CPV, and the OUT1 data are output to STV1 in sync with the trailing edge of CPV.

Also, while OE1, OE2, and OE3 are H, the corresponding liquid-crystal control outputs (OE1: OUT1, 4, 7,...; OE2: OUT2, 5, 8,...; OE3: OUT 3, 6, 9,...) all become non-selective signals (L). In order to hold the internal data, however, the previous state is restored by again setting to L.

detailed description (continued)

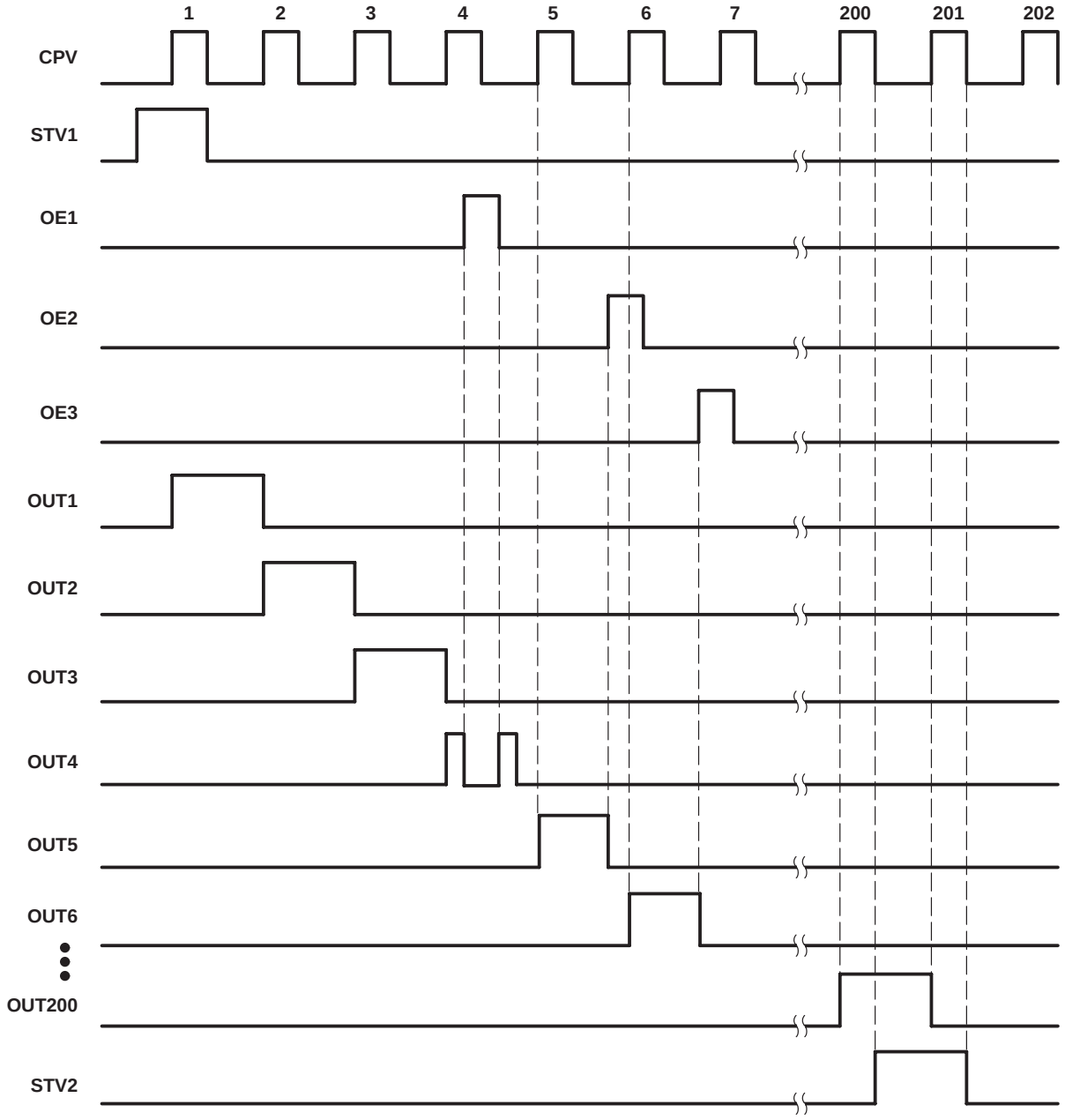


Figure 2. Recommended Operation Timing (L/$\overline{R}$ = H)

absolute maximum ratings (referenced to V_{SS} = 0 V)†

Supply voltage‡§, V_{DD} . . . . . –0.3 to 7 V
V_{EE} . . . . . –20 to 0.3 V
V_{DL} . . . . . V_{EE} – 0.3 to V_{EE} + 7 V
V_L . . . . . V_{EE} – 0.3 to V_{EE} + 7 V
$V_{COM} – V_{EE}$ . . . . . –0.3 to 40 V
$V_{DL} – V_{EE}$ . . . . . 7 V
Input voltage, V_{IN} . . . . . –0.3 to V_{DD} + 0.3 V
Storage temperature, T_{STR} . . . . . –55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Unless otherwise indicated, all voltages are with reference to V_{SS}.
§ Power up in the following order: $V_{DD} \rightarrow V_{EE} \rightarrow V_{DL} \rightarrow$ input signal $\rightarrow V_{COM}$. Power down by reversing the sequence.

recommended operating conditions (referenced to V_{SS} = 0 V)

	MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}	3.0	3.3	3.6	V
Supply voltage, V_{COM}	10		25	V
Supply voltage, V_{EE}	–15		–5	V
Supply voltage, V_{DL}	V_{EE} + 4.5		V_{EE} + 5.5	V
Supply voltage, $V_L – V_{EE}$	0		6	V
Supply voltage, $V_{COM} – V_{EE}$	17		35	V
Low-level input voltage, V_{IL}	V_{SS}		0.1 × V_{DD}	V
High-level input voltage, V_{IH}	0.9 × V_{DD}		V_{DD}	V
Clock frequency, f_{CPV}			100	kHz
Operating free-air temperature, T_A	–55		125	°C

electrical characteristics over full range of recommended operating conditions, V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage (STV1, STV2)	I_{OL} = 40 µA	V_{SS}		V_{SS} + 0.4	V
V_{OH}	High-level output voltage (STV1, STV2)	I_{OH} = –40 µA	V_{DD} – 0.4		V_{DD}	V
R_{OL}	Low-level output resistance (OUT1 - OUT200)	$V_{OUT} = V_L$ + 0.2 V			1000	Ω
R_{OH}	High-level output resistance (OUT1 - OUT200)	$V_{OUT} = V_{COM}$ – 0.2 V			1000	Ω
I_I	Input current	All input terminals	–5		5	µA
I_{DD}	Continuous current dissipation	See Notes 1 and 2			500	µA
I_{DL}	Continuous current dissipation				100	
I_{COM}	Continuous current dissipation				100	

NOTES: 1. Current consumption by a 1/600-duty liquid-crystal display.
2. Condition: The outputs are no load. The inputs are $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, f_{CPV} = 50 kHz, f_{STV} = 83.4 Hz, and OE1-3 = V_{IL}.

timing requirements over full range of recommended operating conditions, V_{SS} = 0 V (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
f_{CP}	Operating frequency		100	KHz
t_{CPVH}, t_{CPVL}	CPV clock pulse width	4		µs
t_{WCL}	Clear enable time	1		µs
t_{su}	Data setup time	700		ns
t_h	Data hold time	700		ns

switching characteristics over full range of recommended operating conditions, V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	Propagation delay time, CPV to outputs	C_L = 300 pF		1000	ns
t_{pd2}	Propagation delay time, CPV to STV2	C_L = 30 pF		800	ns
t_{pd3}	Propagation delay time, output enables to outputs	C_L = 300 pF		1000	ns

NOTE: The ac timing is 50% of the I/O amplitude, for each signal.

timing diagram of ac characteristics (when L/$\overline{R}$ = H)

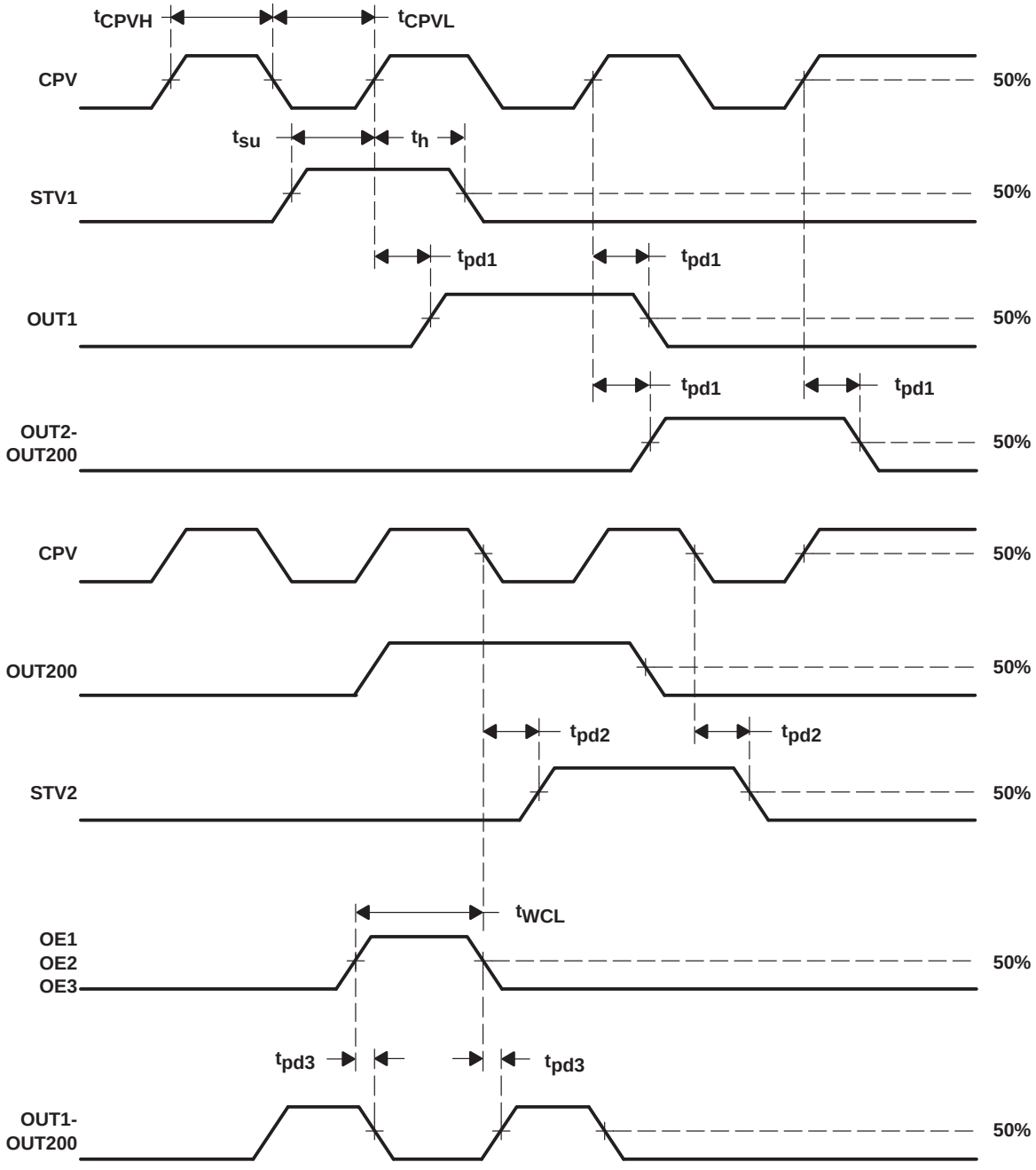


Figure 3. Timing Waveform

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.