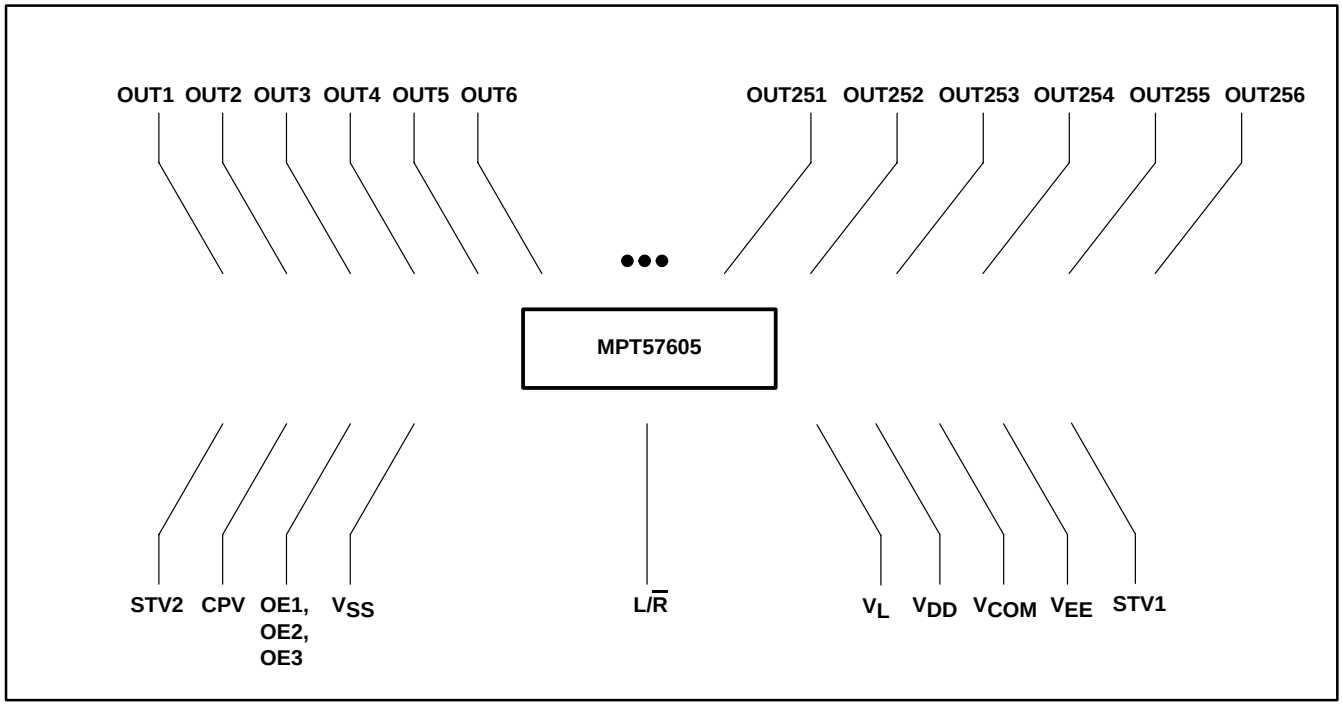
- **Gate Driver LSI for Active-Matrix LCD**
- **Liquid-Crystal Control Outputs: 256**
- **Enables High-Voltage Operation: Liquid-Crystal Control Signal V_L + 35 V (max)**
- **Liquid-Crystal Control Signal's Negative-Voltage Output Is Enabled by a Level-Shift Circuit**
- **On-Chip Bidirectional Shift Registers**
- **TCP (Tape Carrier Package)**
- **CMOS-LSI Structure**

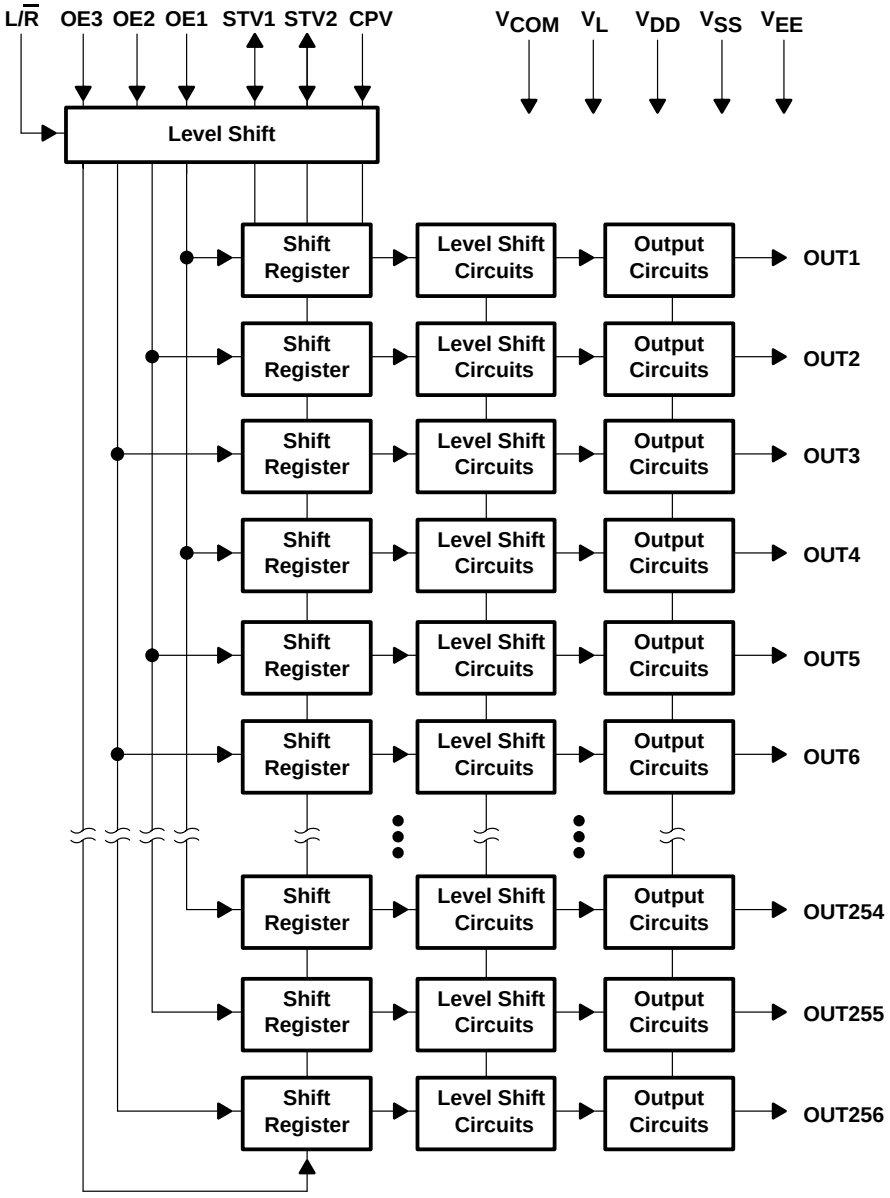
description

The MPT57605 is a gate driver LSI that drives an active-matrix LCD panel and implements a multi-pin configuration, low power consumption, and high voltage. Furthermore, the level-shift circuit enables positive and negative power supplies. Also, it is compatible with various SVGA/XGA panels.



NOTE A: This figure shows the copper foil side and does not describe the TAB outline or show the NC pins.

block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
CPV	I	Vertical shift clock input The shift register's shift clock. Data are shifted in sync with the rising edge of this pin.
OE1 OE2 OE3	I	Output enable pins The liquid-crystal control output is held low by setting pins OE1, 2, and 3 High. However, the shift registers are not cleared. OE is async with CPV. Enable control target pin: OE1: OUT1, OUT4, OUT7...OUT253, OUT256 OE2: OUT2, OUT5, OUT8...OUT254 OE3: OUT3, OUT6, OUT9...OUT255 These combinations are generally as above, regardless of the L/$\overline{R}$ polarity.
L/$\overline{R}$	I	Shift direction switching pin This pin is used to switch the data's shift direction. L/$\overline{R}$ = L: STV1 ← OUT1 ← OUT2...OUT255 ← OUT256 ← STV2 L/$\overline{R}$ = H: STV1 → OUT1 → OUT2...OUT255 → OUT256 → STV2
STV1 STV2	I/O	Shift data I/O pins These pins are used to input/output data to/from a shift register. During input, data are captured in sync with the leading edge of CPV. During output, data are output in sync with its trailing edge. L/$\overline{R}$ = L: STV1 is the next-stage data output pin, and STV2 is the shift data input pin. L/$\overline{R}$ = H: STV1 is the shift data input pin, and STV2 is the next-stage data output pin.
OUT1 thru OUT256	O	Output terminals
V_{COM}		Power supply for high-withstand-voltage logic
V_{DD}		Power supply for logic input
V_{SS}		GND for logic input
V_{EE}		GND
V_L		Negative power supply for liquid-crystal control

detailed description

liquid-crystal control output voltage

The MPT57605 enables negative-voltage output for the liquid-crystal control output.

$V_{COM} – V_L$ = 35 V max $V_L – V_{EE}$ = 0-6 V. $V_{COM} – V_{SS}$ = 10-25 V.

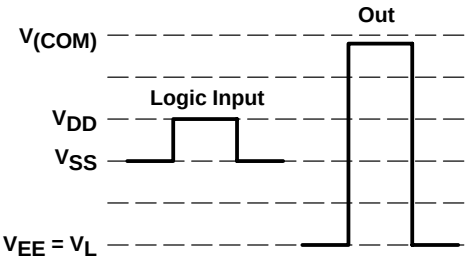


Figure 1. Liquid-Crystal Control Output Voltage

For the input signals (CPV, OE1-3, L/$\overline{R}$, STV1 and STV2), input the amplitude of V_{DD} from V_{SS}.

The next-stage data output pins (STV1, STV2) output the next level:
H level = V_{DD}
L level = V_{SS}

details of operation

The liquid-crystal control outputs (OUT1-256) output either a selective signal (H) or a nonselective signal (L), depending on the input signals (STV1 and STV2, CPV, OE1, OE2, OE3).

A right data shift (OUT1 → OUT256) or a left data shift (OUT256 → OUT1) can be selected by means of the shift direction switching pin (L/$\overline{R}$).

When the L/$\overline{R}$ pin is H, the vertical shift data (STV1) are captured at the leading edge of the shift clock (CPV), after which they are output to the liquid-crystal control output OUT1. Furthermore, the OUT1 output data are shifted to OUT2 at the leading edge of the next CPV, and the data newly fetched from STV1 are output to OUT1. In this manner, they are shifted successively in sync with the leading edge of CPV, and the OUT256 data are output to STV2 in sync with the trailing edge of CPV.

When the L/$\overline{R}$ pin is L, the vertical shift data (STV2) are captured at the leading edge of the shift clock (CPV), after which they are output to the liquid-crystal control output OUT256. Furthermore, the OUT256 output data are shifted to OUT255 at the leading edge of the next CPV, and the data newly fetched from STV2 are output to OUT256. In this manner, they are shifted successively in sync with the leading edge of CPV, and the OUT1 data are output to STV1 in sync with the trailing edge of CPV.

Also, while OE1, OE2, and OE3 are H, the corresponding liquid-crystal control outputs (OE1: OUT1, 4, 7,...; OE2: OUT2, 5, 8,...; OE3: OUT 3, 6, 9,...) all become nonselective signals (L). In order to hold the internal data, however, the previous state is restored by again setting to L.

detailed description (continued)

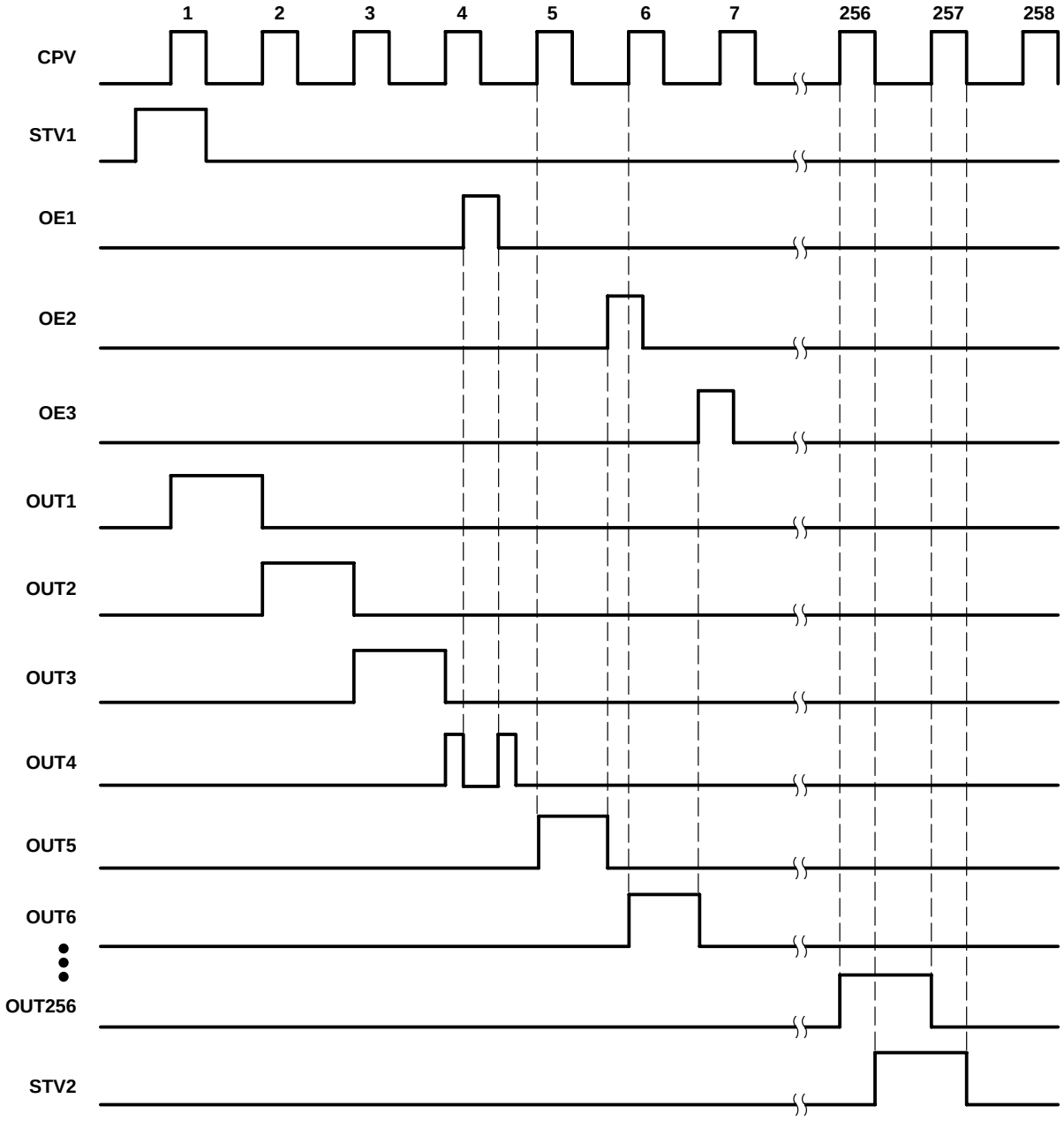


Figure 2. Recommended Operation Timing (L/$\overline{R}$ = H)

absolute maximum ratings (referenced to V_{SS} = 0 V)†

Supply voltage‡§, V_{DD} . . . . . –0.3 to 7 V
V_{EE} . . . . . –20 to 0.3 V
V_L . . . . . V_{EE} – 0.3 to V_{EE} + 7 V
$V_{COM} – V_{EE}$ . . . . . –0.3 to 40 V
Input voltage, V_{IN} . . . . . –0.3 to V_{DD} + 0.3 V
Storage temperature, T_{STR} . . . . . –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Unless otherwise indicated, all voltages are with reference to V_{SS}.
§ Power up in the following order: $V_{DD} \rightarrow V_{EE} \rightarrow$ input signal $\rightarrow V_{COM}$. Power down by reversing the sequence.

recommended operating conditions (referenced to V_{SS} = 0 V)

	MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}	3.0	3.3	3.6	V
Supply voltage, V_{COM}	10		25	V
Supply voltage, V_{EE}	–15		–5	V
Supply voltage, $V_L – V_{EE}$	0		6	V
Supply voltage, $V_{COM} – V_{EE}$	17		35	V
Low-level input voltage, V_{IL}	V_{SS}		$0.1 \times V_{DD}$	V
High-level input voltage, V_{IH}	$0.9 \times V_{DD}$		V_{DD}	V
Clock frequency, f_{CPV}			100	kHz
Operating free-air temperature, T_A	–55		125	°C

electrical characteristics over full range of recommended operating conditions, V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage (STV1, STV2)	I_{OL} = 40 μA	V_{SS}		V_{SS} + 0.4	V
V_{OH}	High-level output voltage (STV1, STV2)	I_{OH} = –40 μA	V_{DD} – 0.4		V_{DD}	V
R_{OL}	Low-level output resistance (OUT1–OUT256)	$V_{OUT} = V_L$ + 0.2 V			1000	Ω
R_{OH}	High-level output resistance (OUT1–OUT256)	$V_{OUT} = V_{COM}$ – 0.2 V			1000	Ω
I_I	Input current	All input terminals	–5		5	μA
I_{DD}	Continuous current dissipation	See Notes 1 and 2			500	μA
I_{COM}	Continuous current dissipation				100	

NOTES: 1. Current consumption by a 1/768-duty liquid-crystal display.
2. Condition: The outputs are no load. The inputs are $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, f_{CPV} = 50 kHz, f_{STV} = 104.2 Hz, and OE1-3 = V_{IL}.

timing requirements over full range of recommended operating conditions, V_{SS} = 0 V (unless otherwise noted)

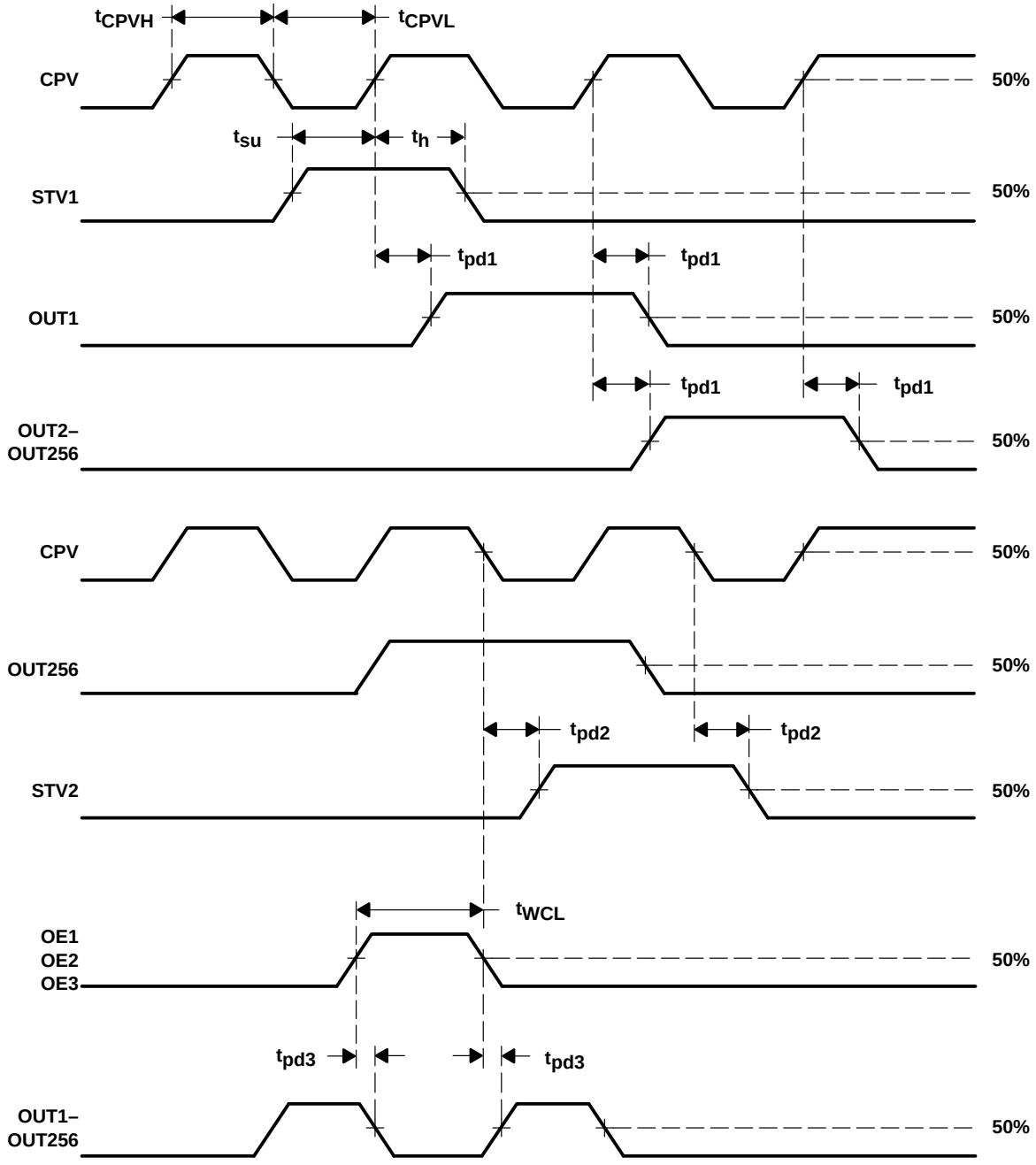
PARAMETER		MIN	MAX	UNIT
f_{CP}	Operating frequency		100	KHz
t_{CPVH}, t_{CPVL}	CPV clock pulse width	4		µs
t_{WCL}	Clear enable time	1		µs
t_{su}	Data setup time	700		ns
t_h	Data hold time	700		ns

switching characteristics over full range of recommended operating conditions, V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	Propagation delay time, CPV to outputs	C_L = 300 pF		1500	ns
t_{pd2}	Propagation delay time, CPV to STV1, STV2	C_L = 30 pF		800	ns
t_{pd3}	Propagation delay time, output enables to outputs	C_L = 300 pF		800	ns

NOTE: The ac timing is 50% of the I/O amplitude, for each signal.

timing diagram of ac characteristics (when L/$\overline{R}$ = H)



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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265