STANDARD MICROSYSTEMS CORPORATION

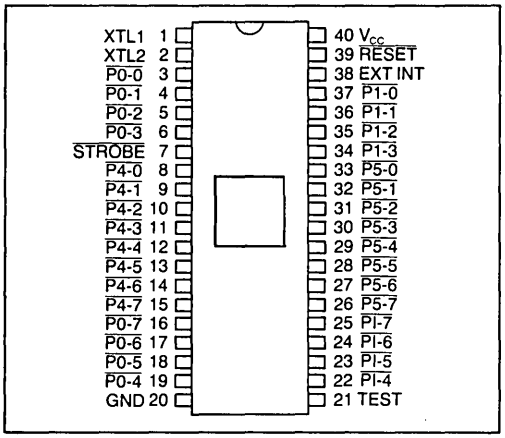
MPU 3870
μPC FAMILY

Single Chip 8-Bit Microcomputer

FEATURES

- ☐ 2K bytes of mask programmable ROM memory
- ☐ 64 bytes of scratch pad RAM
- ☐ 32 bits (4 ports) TTL compatible I/O
- ☐ Programmable binary timer
  - interval timer mode
  - pulse width measurement mode
  - event counter mode
- ☐ External Interrupt Input
- ☐ Crystal, LC, RC, or external time base options
- ☐ Low Power (275 mW typical)

PIN CONFIGURATION



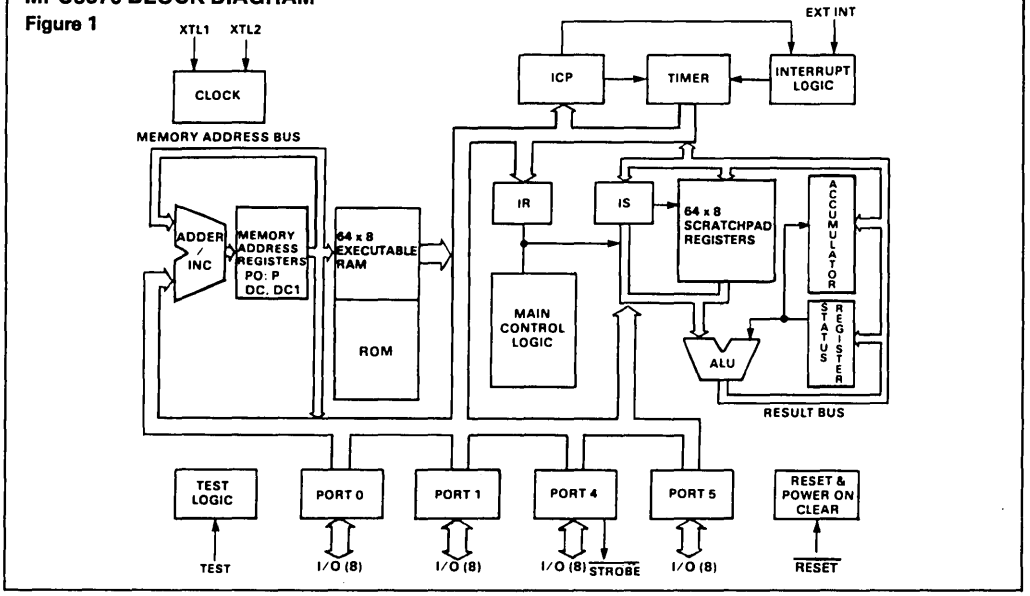
GENERAL DESCRIPTION

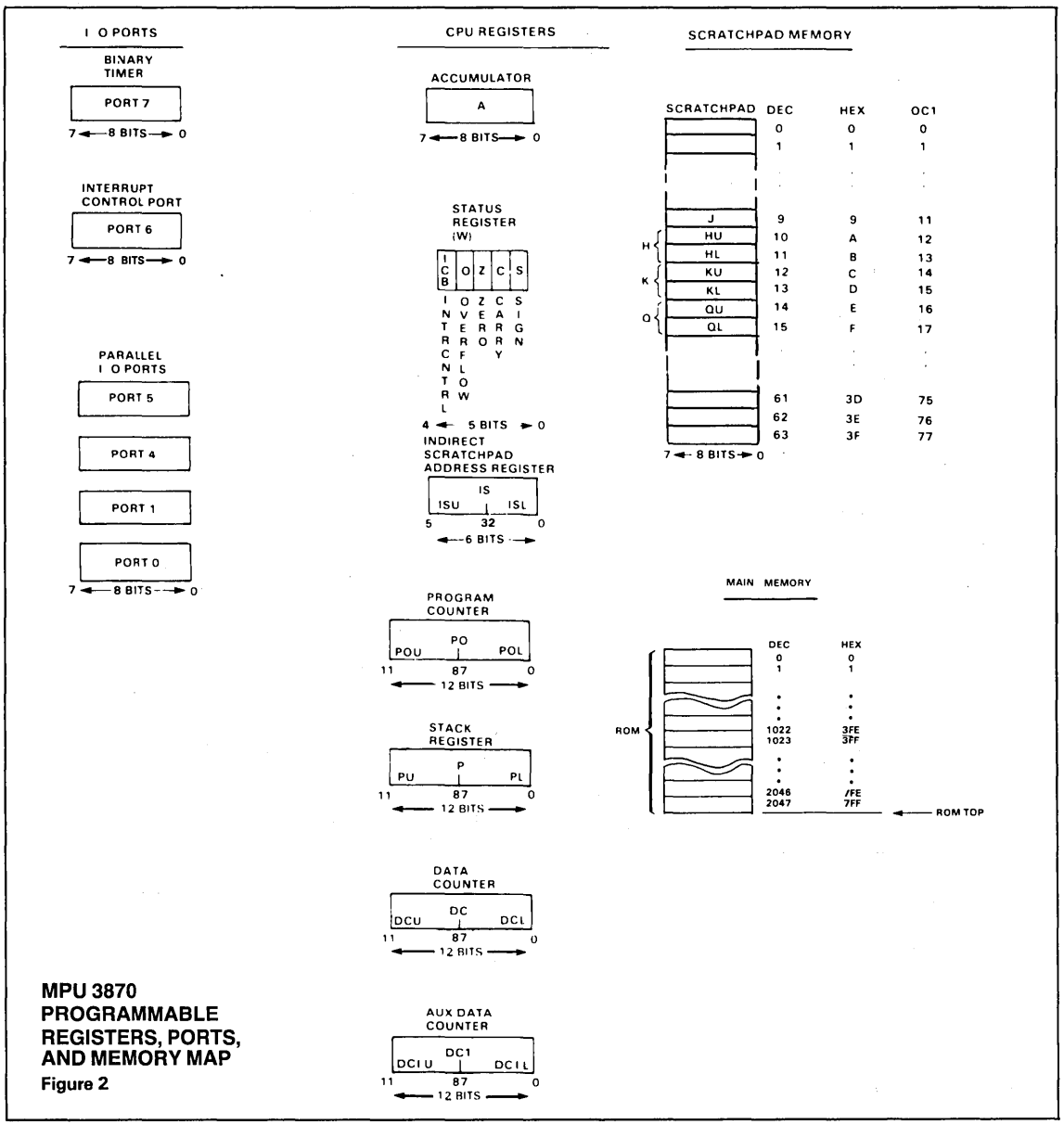
The MPU3870 is a complete 8-bit microcomputer on a single MOS integrated circuit. The MPU3870 can execute a set of more than 70 instructions. The MPU3870 features 2K bytes of ROM, 64 bytes of scratch pad RAM, a programmable binary timer, and 32 bits of I/O.

The programmable binary timer operates by itself in the interval timer mode or in conjunction with the external interrupt input in the pulse width measurement and the event counter modes of operation. Two sources of vectored, prioritized interrupt are provided with the binary timer and the external interrupt input. The user has the option of specifying one of four clock sources: crystal, LC, RC or external clock.

MPU3870 BLOCK DIAGRAM

Figure 1





MPU 3870 PROGRAMMABLE REGISTERS, PORTS, AND MEMORY MAP

Figure 2

MPU3870 MAIN MEMORY

There are four address registers used to access main memory. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC), and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions or immediate operands. The Stack Register is used to save the contents of the Program Counter during an interrupt or subroutine call. Thus, the Stack Register contains the return address at which processing is to resume upon completion of the subroutine or interrupt routine. The Data Counter is used to address data tables. The register is auto-incrementing. Of the two data counters, only Data Counter (DC), can access the ROM. However, the XDC instruction allows the Data Counter and Auxiliary Data Counter to be exchanged.

I/O PORTS

The MPU3870 provides four, 8 bit bidirectional Input/Output ports. These are ports 0, 1, 4, 5. In addition, the Interrupt Control Port is addressed as Port 6 and the binary timer is addressed as Port 7. The programming of Ports 6 and 7 and the bidirectional I/O pin are covered in the 3870 Technical Manual. The schematic of an I/O pin and available output drive options are shown in Figure 4.

An output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the MPU3870 has just completed an output of new data to Port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. STROBE may also be used as an input strobe to Port 4 after completing the input operation.

MPU3870 CLOCKS

The time base network used with the MPU3870 may be one of the four different types listed below.

Crystal
LC
RC
External Clock

The type of network which is to be used with the MPU3870 is to be specified at the time when mask ROM MPU3870 devices are ordered. The time base specifications for each of the four modes are covered in the 3870 Technical Manual.

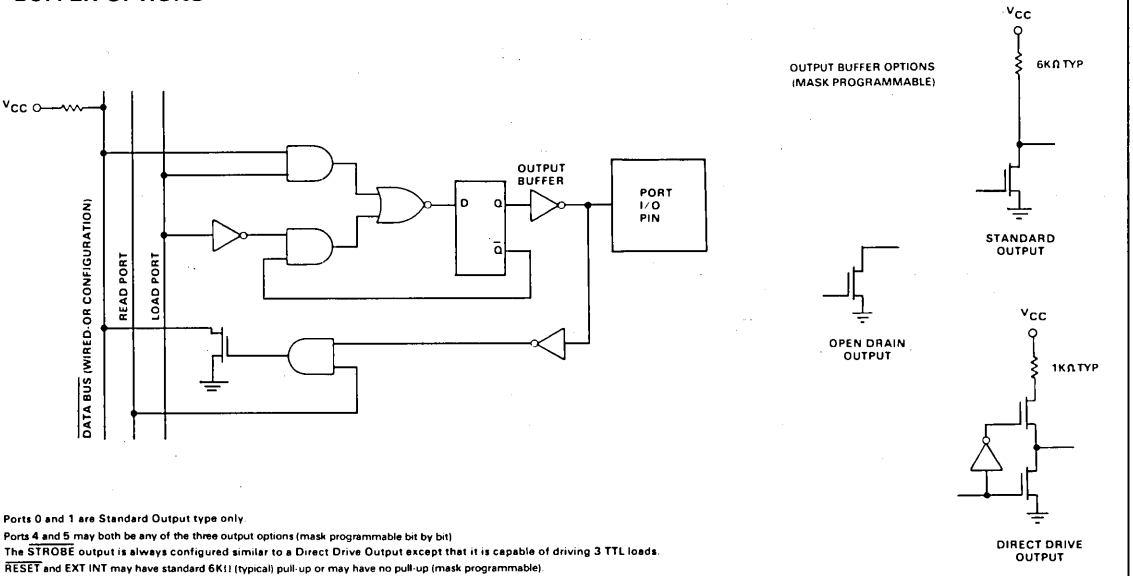
MPU3870 ARCHITECTURE

The basic functional elements of the MPU3870 are shown in Figure 1. A programming model is shown in Figure 2. The user is referred to the 3870 Technical Manual for a thorough discussion of the architecture, instruction set, and other features.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	DESCRIPTION	FUNCTION
3-6, 19-16 37-34, 22-25 8-15 33-26	$\overline{P0\text{-}0}$–$\overline{P0\text{-}7}$ $\overline{P1\text{-}0}$–$\overline{P1\text{-}7}$ $\overline{P4\text{-}0}$–$\overline{P4\text{-}7}$ $\overline{P5\text{-}0}$–$\overline{P5\text{-}7}$	I/O Port 0 I/O Port 1 I/O Port 4 I/O Port 5	$\overline{P0\text{-}0}$ through $\overline{P0\text{-}7}$, $\overline{P1\text{-}0}$ through $\overline{P1\text{-}7}$, $\overline{P4\text{-}0}$ through $\overline{P4\text{-}7}$, and $\overline{P5\text{-}0}$ through $\overline{P5\text{-}7}$ are 32 lines which can be individually used as either TTL compatible inputs or as latched outputs.
7	$\overline{\text{STROBE}}$	Ready Strobe	$\overline{\text{STROBE}}$ is a ready strobe associated with I/O Port 4. This output pin, which is normally high, provides a single low pulse after valid data is present on the $\overline{P4\text{-}0}$ through $\overline{P4\text{-}7}$ pins during an output instruction.
38	EXT INT	External Interrupt	EXT INT is the external interrupt input. Its active state is software programmable. This input is also used in conjunction with the timer for pulse width measurement and event counting.
39	$\overline{\text{RESET}}$	External Reset	$\overline{\text{RESET}}$ may be used to externally reset the MK3870. When pulled low the MK3870 will reset. When then allowed to go high the MK3870 will begin program execution at program location H '000'.
1, 2	XTL 1, XTL 2	Time Base	XTL 1 and XTL 2 are the time base inputs to which a crystal, LC network, RC network, or an external single-phase clock may be connected. The time base network must be specified when ordering a mask ROM MK3870. The MK38P70 will operate with any of the four configurations.
21	TEST	Test Line	TEST is an input, used only in testing the MK3870. For normal circuit functionality this pin may be left unconnected, but it is recommended that TEST be grounded.
40	V_{CC}	Power Supply	+5 volt supply pin
20	GND	Ground	Ground

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS



Ports 0 and 1 are Standard Output type only.
Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)
The $\overline{\text{STROBE}}$ output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.
$\overline{\text{RESET}}$ and EXT INT may have standard 6KΩ (typical) pull-up or may have no pull-up (mask programmable).

SECTION IX

OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temperature T_A
—00	+5V ± 10%*	0°C-70°C
—05	+5V ± 5%	0°C-70°C
—10	+5V ± 10%*	−40°C-+85°C
—15	+5V ± 5%*	−40°C-+85°C

See Ordering Information for explanation of part numbers.

ABSOLUTE MAXIMUM RATINGS*

	−00, −05	−10, −15
Temperature Under Bias	−20°C to +85°C	−50°C to +100°C
Storage Temperature	−65°C to +150°C	−65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	−1.0V to +7V	−1.0V to +7V
Voltage on TEST with Respect to Ground	−1.0V to +9V	−1.0V to +9V
Voltage on Open Drain Pins With Respect to Ground	−1.0V to +13.5V	−1.0V to +13.5V
Power Dissipation	1.5W	1.5W
Power Dissipation by any one I/O pin	60mW	60mW
Power Dissipation by all I/O pins	600mW	600mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARCTERISTICS T_A, V_{CC} within specified operating range. I/O power dissipation ≤100mW (Note 2)

SIGNAL	SYM	PARAMETER	−00, −05 MIN	−00, −05 MAX	−10, −15 MIN	−10, −15 MAX	UNIT	NOTES
XTL1 XTL2	t_O	Timer Base Period, all clock modes	250	500	250	500	ns	4MHz-2MHz
	$t_{ex(H)}$	External clock pulse width high	90	400	100	390	ns	
	$t_{ex(L)}$	External clock pulse width low	100	400	110	390	ns	
Φ	t_Φ	Internal Φ clock	$2t_O$		$2t_O$			
WRITE	t_W	Internal WRITE Clock period	4tΦ 6tΦ		4tΦ 6tΦ			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	100	0	1200	ns	50pF plus one TTL load
	$t_{sI/O}$	Input setup time to intrenal WRITE clock	1000		1200		ns	
$\overline{STROBE}$	$t_{I/O-s}$	Output valid to $\overline{STROBE}$ delay	3tΦ −1000	3tΦ +250	3tΦ −1200	3tΦ +300	ns	I/O load = 50pF + 1 TTL load
	t_{sL}	$\overline{STROBE}$ low time	8tΦ −250	12tΦ +250	8tΦ −300	12tΦ +300	ns	$\overline{STROBE}$ load = 50pF + 3TTL loads
$\overline{RESET}$	t_{RH}	$\overline{RESET}$ hold time, low	6tΦ +750		6tΦ +1000		ns	
	t_{RPOC}	$\overline{RESET}$ hold time, low for power clear	power supply rise time −0.1		power supply rise time +15		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	6tΦ +750		6tΦ +1000		ns	To trigger interrupt
			2tΦ		2tΦ		ns	To trigger timer

DC CHARACTERISTICS T_A, V_{CC} within specified operating range I/O power dissipation≤100mW (Note 2)

SYM	PARAMETER	−00, −05 MIN	−00, −05 MAX	−10, −15 MIN	−10, −15 MAX	UNIT	CONDITIONS
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	−.3	.6	−.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	$V_{IHEX} = V0_{CC}$
I_{ILEX}	External Clock input low current		−100		−130	μA	$V_{ILEX} = V_{SS}$
$V_{IHI/O}$	Input high level, I/O pins	2.0	5.8	2.0	5.8	V	Standard pull-up
		2.0	13.2	2.0	13.2	V	Open drain (1)
V_{IHR}	Input high level, $\overline{RESET}$	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IL}	Input low level	−.3	.8	−.3	.7	V	(1)
I_{IL}	Input low current, all pins with standard pull-up resistor		−1.6		−1.9	mA	$V_{IN} = 0.4V$
I_L	Input leakage current, open drain pins, and inputs with no pull-up resistor		+10 −5		+18 −8	μA μA	$V_{IN} = 13.2V$ $V_{IN} = 0.0V$
I_{OH}	Output high current pins with standard pull-up resistor	−100 −30		−89 −25		μA μA	$V_{OH} = 2.4V$ $V_{OH} = 3.9V$
I_{OHDD}	Output high current, direct drive pins	−100 −1.5 	 −8.5	−80 −1.3 	 −11	μA mA mA	$V_{OH} = 2.4V$ $V_{OH} = 1.5V$ $V_{OH} = 0.7V$
I_{OHS}	$\overline{STROBE}$ Output High current	−300		−270		μA	$V_{OL} = 2.4V$
I_{OL}	Output low current	1.8		1.65		mA	$V_{OL} = 0.4V$
I_{OLS}	$\overline{STROBE}$ Output Low current	5.0		4.5		mA	$V_{OL} = o.4V$
I_{CC}	Average Power Supply Current		85		110	mA	MK3870/20 Outputs Open

TIMER AC CHARACTERISTICS

Definitions:
Error = Indicated time value − actual time value
tpsc = tΦ × Prescale Value

Interval Timer Mode:

Single interval error, free running (Note 3) ..... ±6tΦ
Cumulative interval error, free running (Note 3) 0
Error between two Timer reads (Note 2) ..... ±(tpsc+tΦ)
Start Timer to stop Timer error (Notes 1, 4) ..... +tΦ to − (tpsc+tΦ)
Start Timer to read Timer error (Notes 1, 2) ..... −5tΦ to − (tpsc+7tΦ)
Start Timer to interrupt request error (Notes 1, 3) ..... −2tΦ to −8tΦ
Load Timer to stop Timer error (Note 1) ..... +tΦ to − (tpsc+2tΦ)
Load Timer to read Timer error (Notes 1, 2) ..... −5tΦ ± to − (tpsc + 8tΦ)
Load Timer to interrupt request error (Notes 1, 3) ..... −2tΦ to −9tΦ

Pulse Width Measurement Mode:

Measurement accuracy (Note 4) ..... +tΦ to − (tpsc+2tΦ)
Minimum pulse width of EXT INT pin 2tΦ

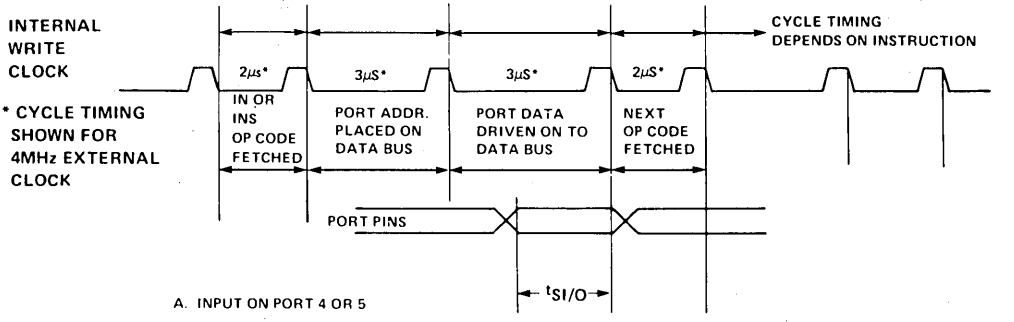
Event Counter Mode:

Minimum active time of EXT INT pin 2tΦ
Minimum inactive time of EXT INT pin 2tΦ

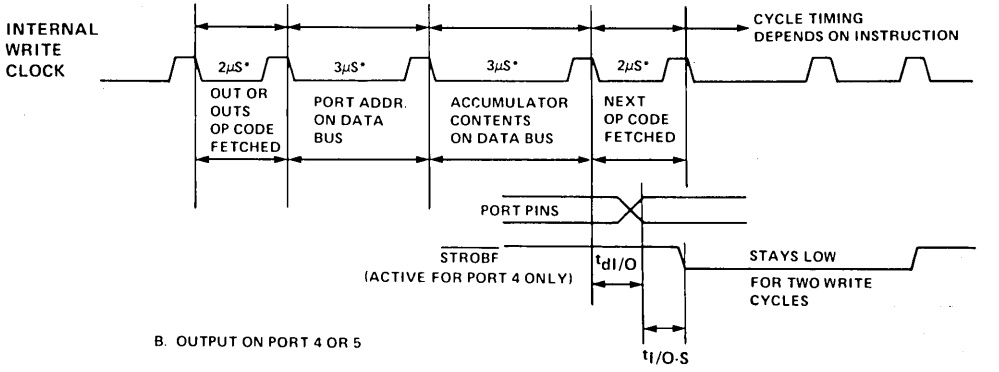
Notes:

1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

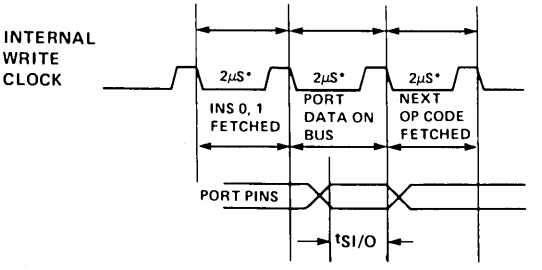
INPUT/OUTPUT AC TIMING



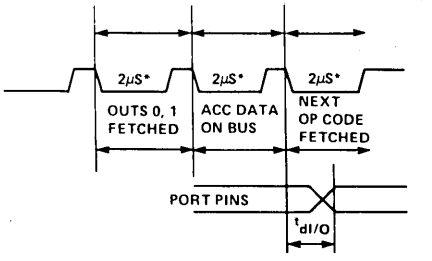
A. INPUT ON PORT 4 OR 5



B. OUTPUT ON PORT 4 OR 5

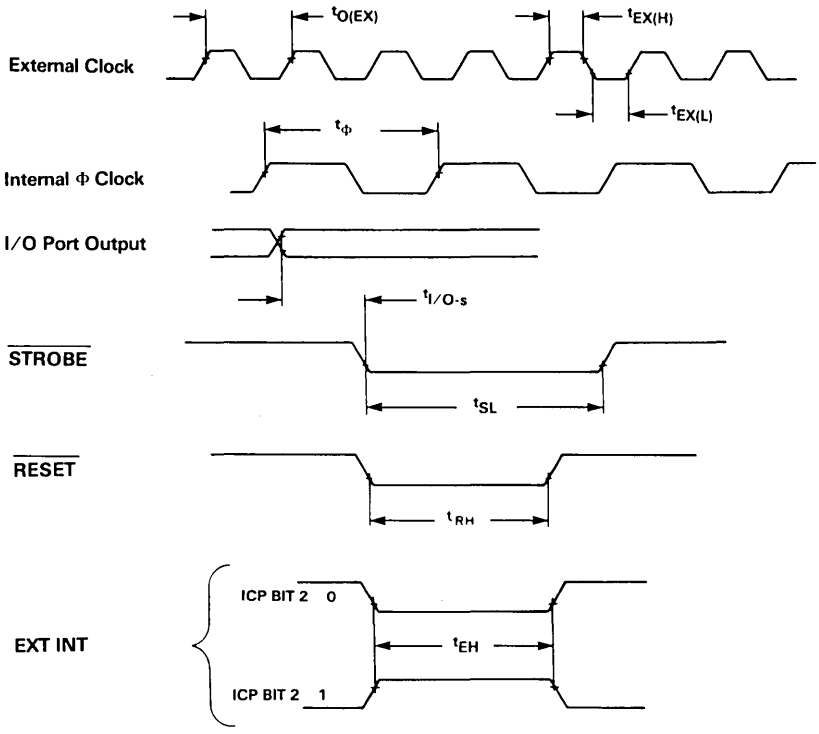


C. INPUT ON PORT 0 OR 1



D. OUTPUT ON PORT 0, 1

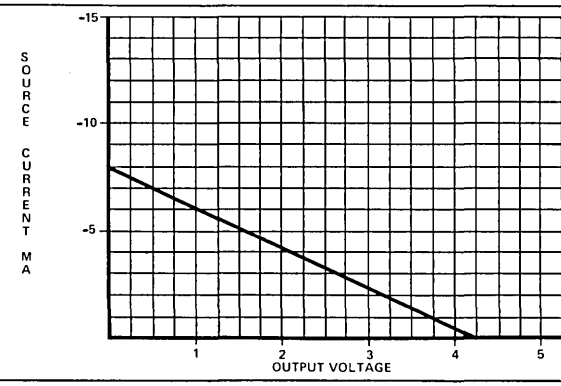
AC TIMING DIAGRAM



Note: All measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} max., or V_{OH} min.

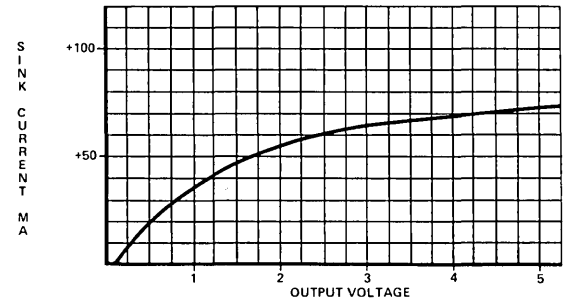
STROBE SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5V, T_A = 25°C)

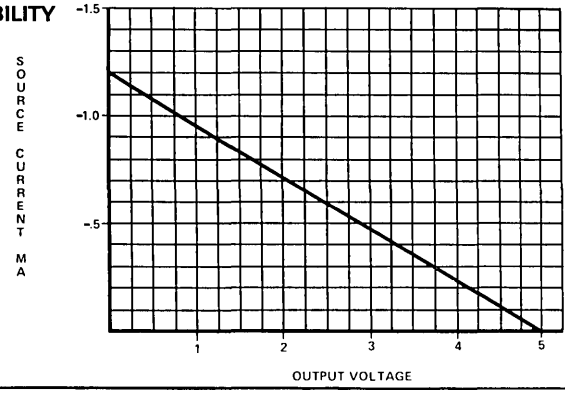


STROBE SINK CAPABILITY

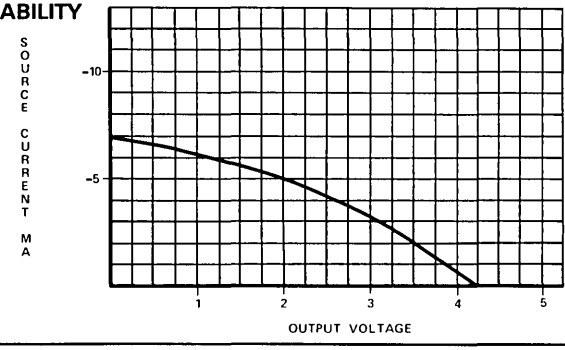
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)



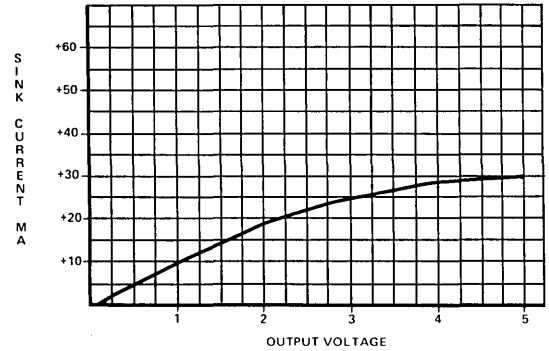
STANDARD I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)



DIRECT DRIVE I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)



I/O PORT SINK CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION