

MPxx5004, 0 to 3.92 kPa, Differential and Gauge, Integrated Pressure Sensor

Freescale's MPxx5004 series piezoresistive transducer is a state-of-the-art monolithic silicon pressure sensor designed for a wide range of applications, but particularly those employing a microcontroller or microprocessor with A/D inputs. This sensor combines a highly sensitive implanted strain gauge with advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure.

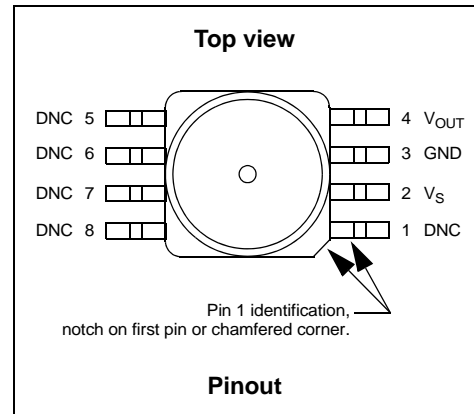
Features

- 1.5% maximum error for 0 to 100 mm H₂O over +10 °C to +60 °C with autozero
- 2.5% maximum error for 100 to 400 mm H₂O over +10 °C to +60 °C with autozero
- 6.25% maximum error for 0 to 400 mm H₂O over 10 °C to +60 °C without autozero
- Temperature compensated over 10 °C to 60 °C
- Available in gauge surface mount (SMT) or through-hole (DIP) configurations
- Durable thermoplastic (PPS) package

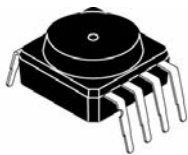
Applications

- Washing machine water level
- Ideally suited for microprocessor or microcontroller-based systems
- Appliance liquid level and pressure measurement
- Respiratory equipment

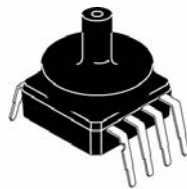
**MPXV5004
MPVZ5004**



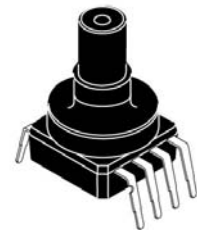
Small outline packages, through-hole



MPVZ5004G7U
Case 98ASB17758C



MPXV5004GC7U
Case 98ASB17759C

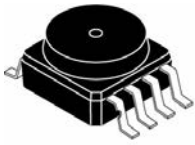


MPVZ5004GW7U
Case 98ASA10611D

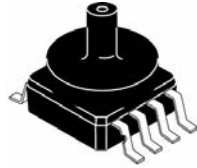
Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

© 2006-2009, 2015 Freescale Semiconductor, Inc. All rights reserved.

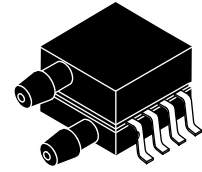
Small outline packages, surface mount



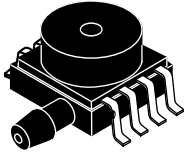
MPVZ5004G6U/6T1
Case 98ASB17756C



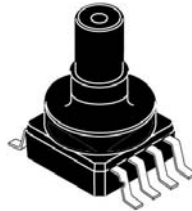
MPXV5004GC6T1/6U, MPVZ5004GC6U
Case 98ASB17757C



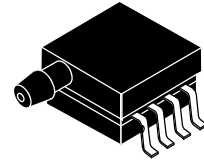
MPXV5004DP
Case 98ASA99255D



MPXV5004GVP
Case 98ASA99302D



MPVZ5004GW6U
Case 98ASA10686D



MPXV5004GP/GPT1
Case 98ASA99303D

Ordering Information									
Part number	Shipping	Package	# of Ports			Pressure type			Device marking
			None	Single	Dual	Gauge	Differential	Absolute	
Small outline package (MPXV5004 series)									
MPXV5004DP	Tray	98ASA99255D			•		•		MPXV5004DP
MPXV5004GC6T1	Reel	98ASB17757C		•		•			MPXV5004G
MPXV5004GC6U	Rail	98ASB17757C		•		•			MPXV5004G
MPXV5004GC7U	Rail	98ASB17759C		•		•			MPXV5004G
MPXV5004GP	Tray	98ASA99303D		•		•			MPXV5004GP
MPXV5004GPT1	Reel	98ASA99303D		•		•			MPXV5004GP
MPXV5004GVP	Tray	98ASA99302D		•		•			MPXV5004GVP
Small outline package (Media resistant gel) (MPVZ5004 series)									
MPVZ5004G6T1	Reel	98ASB17756C	•			•			MPVZ5004G
MPVZ5004G6U	Rail	98ASB17756C	•			•			MPVZ5004G
MPVZ5004G7U	Rail	98ASB17758C	•			•			MPVZ5004G
MPVZ5004GC6U	Rail	98ASB17757C		•		•			MPVZ5004G
MPVZ5004GW6U	Rail	98ASA10686D		•		•			MZ5004GW
MPVZ5004GW7U	Rail	98ASA10611D		•		•			MZ5004GW



Contents

1	General Description	4
1.1	Block diagram	4
1.2	Pinout	4
2	Mechanical and Electrical Specifications	5
2.1	Maximum ratings	5
2.2	Operating characteristics	5
3	On-chip Temperature Compensation and Calibration	6
4	Package Information	8
4.1	Pressure (P1)/Vacuum (P2) side identification	8
4.2	Minimum recommended footprint for surface mounted applications	8
4.3	Package Dimensions	9
5	Revision History	25

Related Documentation

The MPXV5004G device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to the Freescale homepage at:
<http://www.freescale.com/>
2. In the Keyword search box at the top of the page, enter the device number MPXV5004G.
3. In the Refine Your Result pane on the left, click on the Documentation link.

MPxx5004

1 General Description

1.1 Block diagram

Figure 1 shows a block diagram of the internal circuitry integrated on a pressure sensor chip.

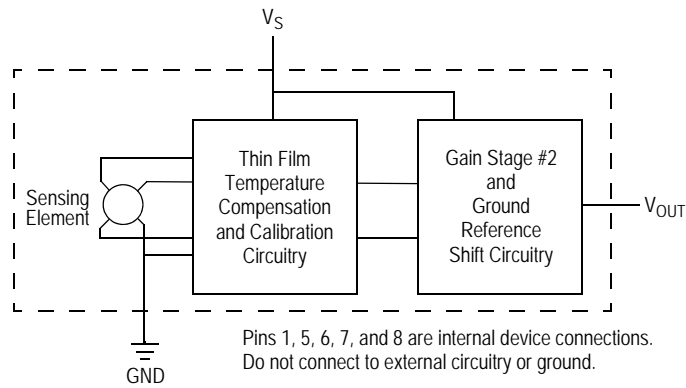


Figure 1. Integrated pressure sensor schematic

1.2 Pinout

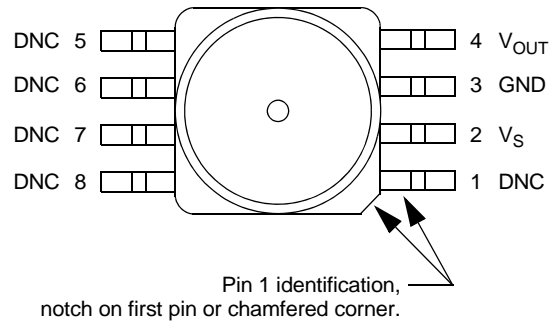


Figure 2. Device pinout (top view)

Table 1. Pin functions

Pin	Name	Function
1	DNC	Do not connect to external circuitry or ground. Pin 1 is notated by the notch in the lead or chamfered corner.
2	V_S	Voltage supply
3	GND	Ground
4	V_{OUT}	Output voltage
5	DNC	Do not connect to external circuitry or ground.
6	DNC	Do not connect to external circuitry or ground.
7	DNC	Do not connect to external circuitry or ground.
8	DNC	Do not connect to external circuitry or ground.

2 Mechanical and Electrical Specifications

2.1 Maximum ratings

Table 2. Maximum ratings⁽¹⁾

Rating	Symbol	Value	Unit
Maximum pressure (P1 > P2)	P _{MAX}	16	kPa
Storage temperature	T _{STG}	-30 to +100	°C
Operating temperature	T _A	0 to +85	°C

1. Exposure beyond the specified limits may cause permanent damage or degradation to the device.

2.2 Operating characteristics

Table 3. Operating characteristics (V_S = 5.0 V_{DC}, T_A = 25 °C unless otherwise noted, P1 > P2)

Characteristic	Symbol	Min	Typ	Max	Units
Pressure range	P _{OP}	0	—	3.92 400	kPa mm H ₂ O
Supply voltage ⁽¹⁾	V _S	4.75	5.0	5.25	V _{DC}
Supply current	I _S	—	—	10	mAdc
Span @ 306 mm H ₂ O (3 kPa) ⁽²⁾ Full-scale span @ 400 mm H ₂ O (3.92 kPa) ⁽²⁾	V _{FSS}	— —	3.0 3.92	— —	V
Offset ⁽³⁾	V _{OFF}	0.75	1.0	1.25	V
Sensitivity	V/P	—	1.0	—	V/kPa
Accuracy ^{(4) (5)}					
0 to 100 mm H ₂ O (10 °C to 60 °C)	—	—	—	±1.5	%V _{FSS} with autozero
100 to 400 mm H ₂ O (10 °C to 60 °C)	—	—	—	±2.5	%V _{FSS} with autozero
0 to 400 mm H ₂ O (10 °C to 60 °C)	—	—	—	±6.25	%V _{FSS} without autozero

- Device is ratiometric within this specified excitation range.
- Span is defined as the algebraic difference between the output voltage at specified pressure and the output voltage at the minimum rated pressure.
- Offset (V_{off}) is defined as the output voltage at the minimum rated pressure.
- Accuracy (error budget) consists of the following:
 - Linearity: Output deviation from a straight line relationship with pressure, using endpoint method, over the specified pressure range.
 - Temperature hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to and from the minimum or maximum operating temperature points, with zero differential pressure applied.
 - Pressure hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from the minimum or maximum rated pressure, at 25 °C.
 - TcSpan: Output deviation over the temperature range of 10 °C to 60 °C, relative to 25 °C.
 - TcOffset: Output deviation with minimum rated pressure applied, over the temperature range of 10 °C to 60 °C, relative to 25 °C.
 - Variation from nominal: The variation from nominal values, for offset or full-scale span, as a percent of V_{FSS}, at 25 °C.
- Autozero at factory installation: Due to the sensitivity of the MPxx5004G, external mechanical stresses and mounting position can affect the zero pressure output reading. Autozeroing is defined as storing the zero pressure output reading and subtracting this from the device's output during normal operations. Reference AN1636 for specific information. The specified accuracy assumes a maximum temperature change of ±5 °C between autozero and measurement.

3 On-chip Temperature Compensation and Calibration

The performance over temperature is achieved by integrating the shear-stress strain gauge, temperature compensation, calibration and signal conditioning circuitry onto a single monolithic chip.

Figure 3 illustrates the gauge configuration in the basic chip carrier (case 98ASB17756C). A fluorosilicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm.

The MPxx5004 series sensor operating characteristics are based on use of dry air as pressure media. Media, other than dry air, may have adverse effects on sensor performance and long-term reliability. Internal reliability and qualification test for dry air, and other media, are available from the factory. Contact the factory for information regarding media tolerance in your application.

Figure 4 shows the recommended decoupling circuit for interfacing the output of the MPxx5004 to the A/D input of the microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

Typical, minimum and maximum output curves are shown for operation over a temperature range of 10 °C to 60 °C using the decoupling circuit shown in Figure 4. The output will saturate outside of the specified pressure range.

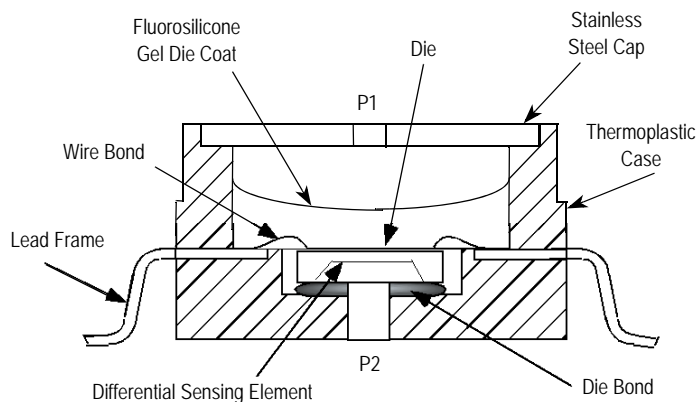


Figure 3. Cross-sectional diagram (not to scale)

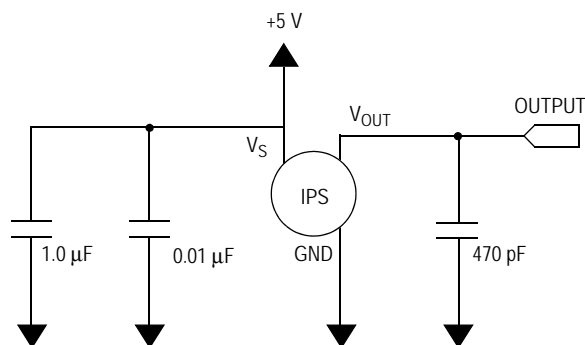


Figure 4. Recommended power supply decoupling and output filtering
(For additional output filtering, please refer to AN1646.)

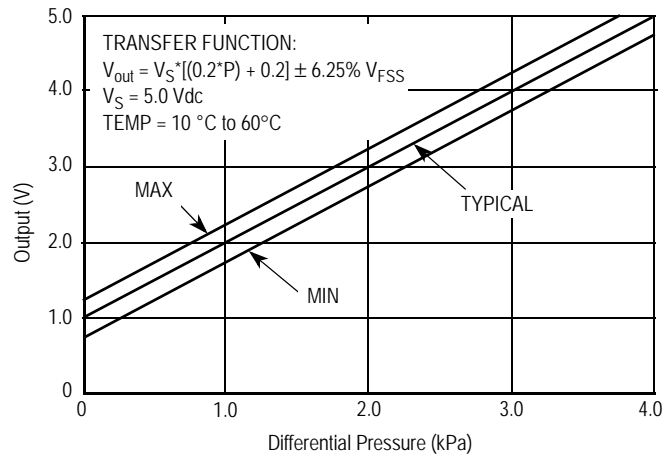


Figure 5. Output vs. pressure differential at $\pm 6.25\% V_{FSS}$ (without autozero, Table 3, note 5)

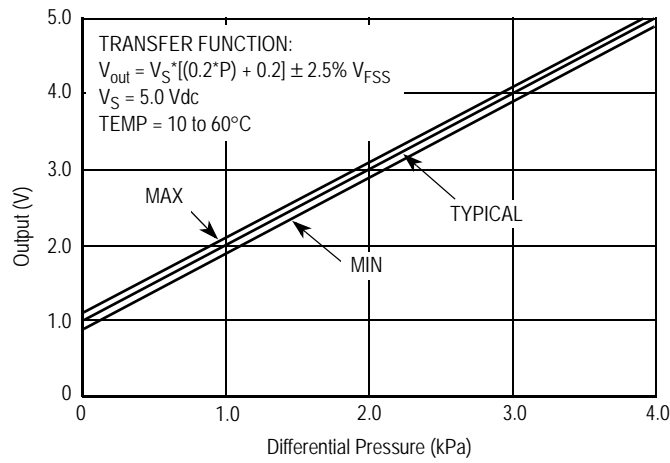


Figure 6. Output vs. pressure differential at $\pm 2.5\% V_{FSS}$ (with autozero, Table 3, note 5)

4 Package Information

4.1 Pressure (P1)/Vacuum (P2) side identification

Freescale Semiconductor designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The pressure (P1) side is the side containing silicone gel which isolates the die from the environment.

The Freescale Semiconductor pressure sensor is designed to operate with positive differential pressure applied, $P1 > P2$.

The pressure (P1) side may be identified by using the table below.

Table 4. Pressure (P1)/Vacuum (P2) side identification table

Part number	Case number	Pressure (P1) side identifier
MPXV5004DP	98ASA99255D	Side with part marking
MPXV5004GC6U/6T1, MPVZ5004GC6U	98ASB17757C	Side with port attached
MPXV5004GC7U	98ASB17759C	Side with port attached
MPXV5004GP/GPT1	98ASA99303D	Side with port attached
MPXV5004GVP	98ASA99302D	Stainless steel cap
MPVZ5004G6U/6T1	98ASB17756C	Stainless steel cap
MPVZ5004G7U	98ASB17758C	Stainless steel cap
MPVZ5004GW6U	98ASA10686D	Vertical port attached
MPVZ5004GW7U	98ASA10611D	Vertical port attached

4.2 Minimum recommended footprint for surface mounted applications

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct footprint, the packages will self align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

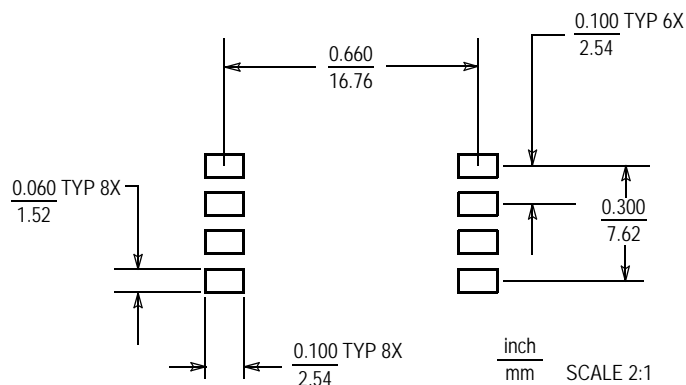
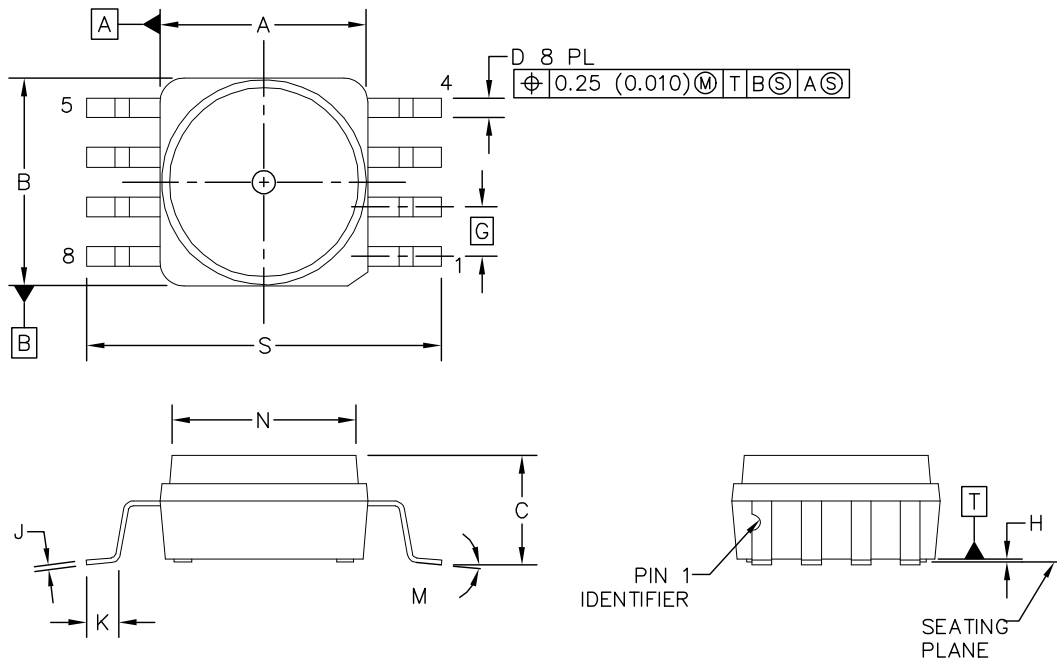


Figure 7. SOP footprint (case 98ASB17756C)

4.3 Package Dimensions

This drawing is located at http://cache.freescale.com/files/shared/doc/package_info/98ASB17756C.pdf.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.54	10.79	0.415	0.425
B	10.54	10.79	0.415	0.425
C	5.38	5.84	0.212	0.230
D	0.96	1.07	0.038	0.042
G	2.54 BSC		0.100 BSC	
H	0.05	0.25	0.002	0.010
J	0.23	0.28	0.009	0.011
K	1.55	1.80	0.061	0.071
M	0°	7°	0°	7°
N	10.29	10.54	0.405	0.415
S	18.01	18.41	0.709	0.725

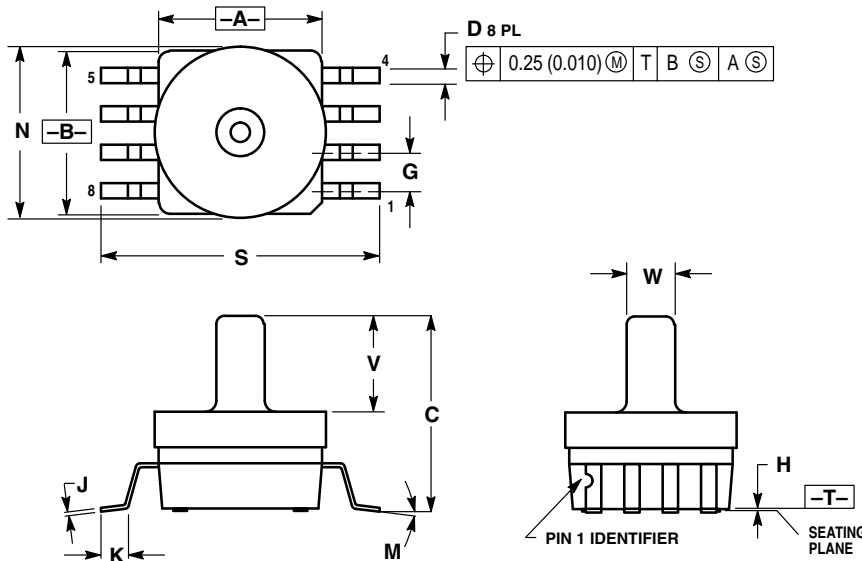
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 8 LD SENSOR SOP	DOCUMENT NO: 98ASB17756C STANDARD: NON-JEDEC	REV: A 10 JAN 2013

Case 98ASB17756C, small outline package, surface mount

This drawing is located at http://cache.freescale.com/files/shared/doc/package_info/98ASB17757C.pdf.

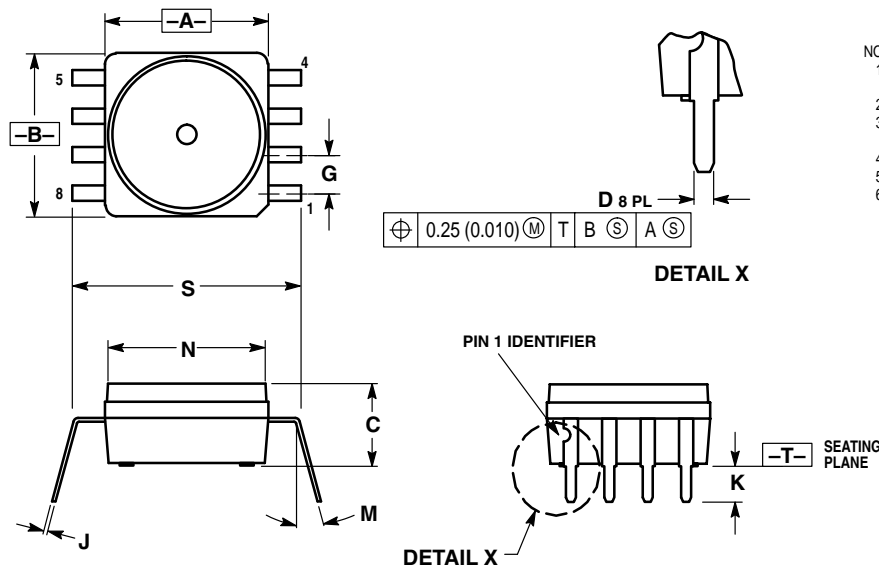


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
 5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.500	0.520	12.70	13.21
D	0.038	0.042	0.96	1.07
G	0.100 BSC		2.54 BSC	
H	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0°	7°	0°	7°
N	0.444	0.448	11.28	11.38
S	0.709	0.725	18.01	18.41
V	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

Case 98ASB17757C, small outline package, through-hole

This drawing is located at http://cache.freescale.com/files/shared/doc/package_info/98ASB17758C.pdf.

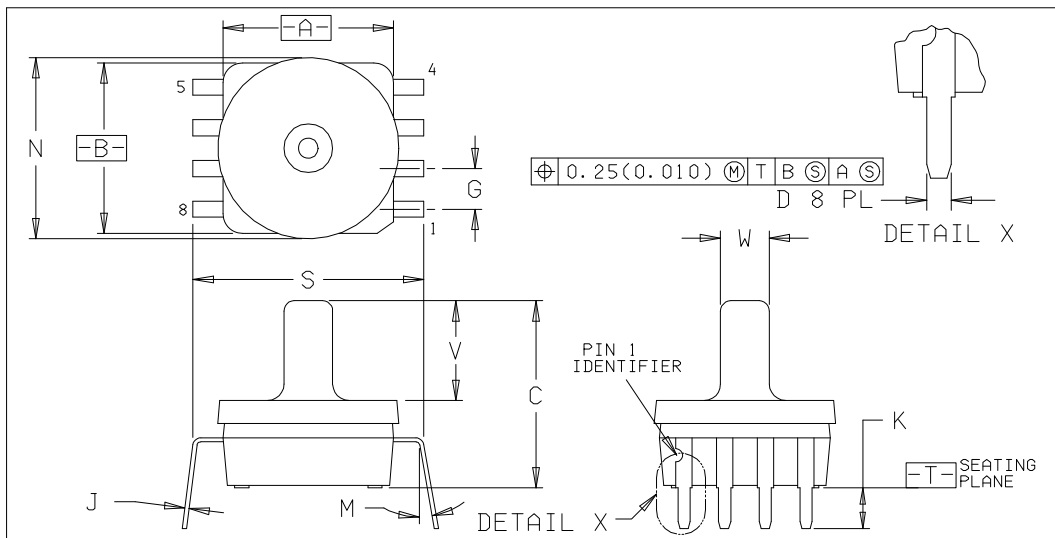


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
 5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
 6. DIMENSION S TO CENTER OF LEAD WHEN FORMED PARALLEL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.210	0.220	5.33	5.59
D	0.026	0.034	0.66	0.864
G	0.100 BSC		2.54 BSC	
J	0.009	0.011	0.23	0.28
K	0.100	0.120	2.54	3.05
M	0°	15°	0°	15°
N	0.405	0.415	10.29	10.54
S	0.540	0.560	13.72	14.22

Case 98ASB17758C, small outline package, through-hole

FREESCALE	MECHANICAL OUTLINES DICTIONARY	98ASB17759C	
		PAGE	482C
DO NOT SCALE THIS DWG	ALL APPROVAL SIGNATURES ON FILE IN DOCUMENT CENTRAL	ISSUE	D SHEET 1 OF 2



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.54	10.79	0.415	0.425
B	10.54	10.79	0.415	0.425
C	12.70	13.21	0.500	0.520
D	0.66	0.864	0.026	0.034
G	2.54 BSC		0.100 BSC	
J	0.23	0.28	0.009	0.011
K	2.54	3.05	0.100	0.120
M	0°	15°	0°	15°
N	11.28	11.38	0.444	0.448
S	13.72	14.22	0.540	0.560
V	6.22	6.48	0.245	0.255
W	2.92	3.17	0.115	0.125

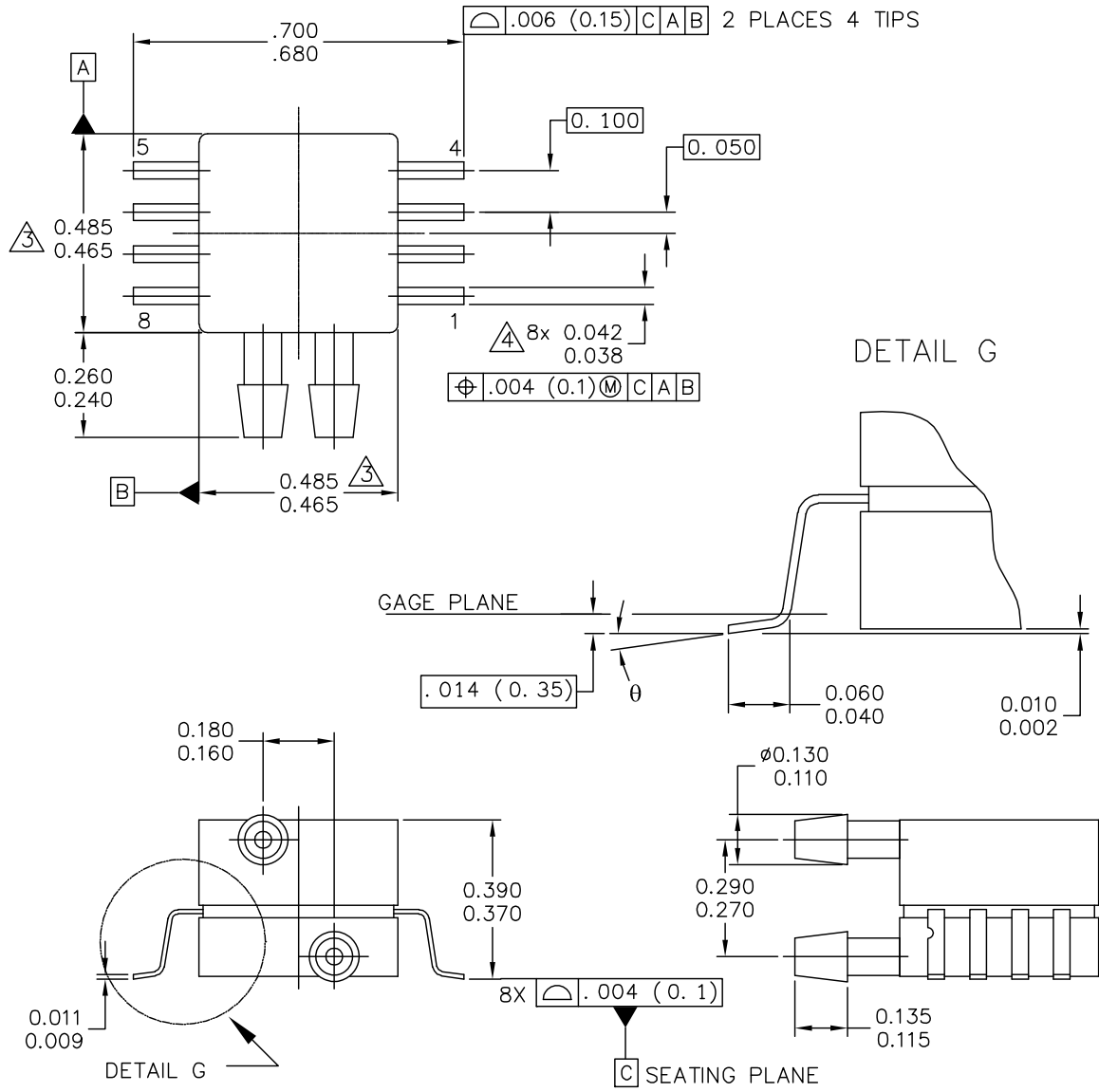
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION 'A' AND 'B' DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15(0.006).
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION 'S' TO CENTER OF LEAD WHEN FORMED PARALLEL.
7. 482C-01 AND -02 OBSOLETE. NEW STANDARD 482C-03.

CASE NO.	482C-03
STATUS	MOTOROLA STANDARD
NEW STD	
USED ON	

ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM WWCN.
PRINTED VERSIONS ARE UNCONTROLLED, EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.

Case 98ASB17759C, small outline package, through-hole



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 8 LD SNSR, DUAL PORT	DOCUMENT NO: 98ASA99255D	REV: A
	CASE NUMBER: 1351-01	27 JUL 2005
	STANDARD: NON-JEDEC	

Case 98ASA99255D, small outline package, surface mount



NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE.

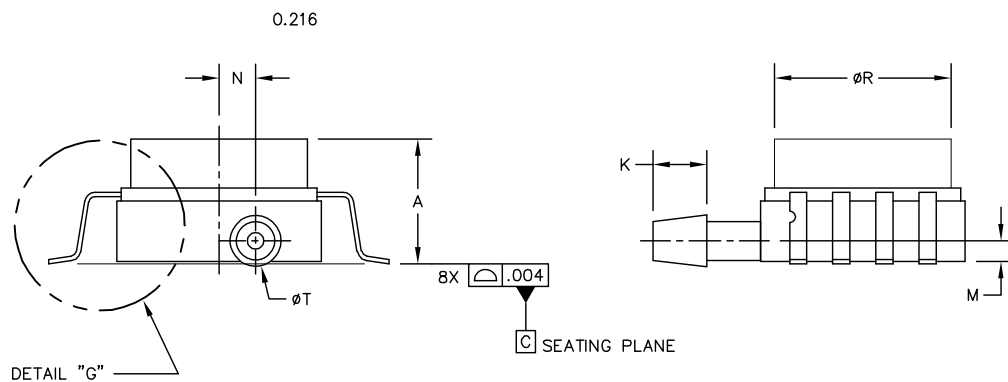
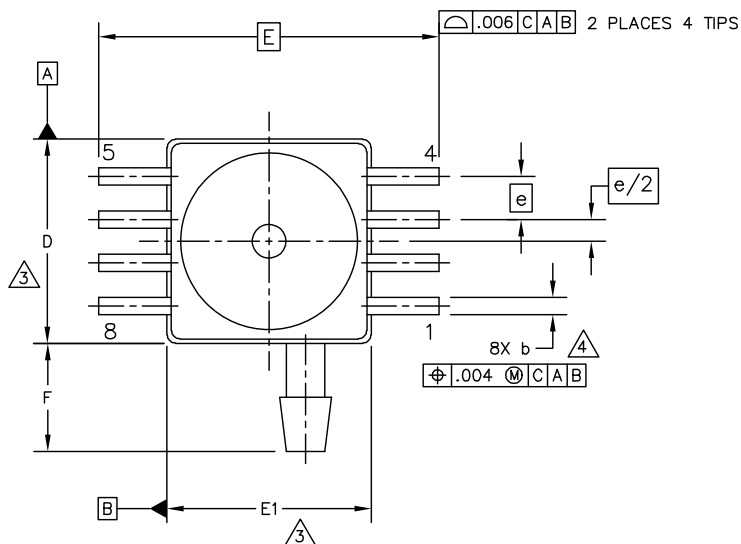
4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL BE .008 MAXIMUM.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 8 LD SNSR, DUAL PORT	DOCUMENT NO: 98ASA99255D	REV: A	
	CASE NUMBER: 1351-01	27 JUL 2005	
	STANDARD: NON-JEDEC		

PAGE 2 OF 2

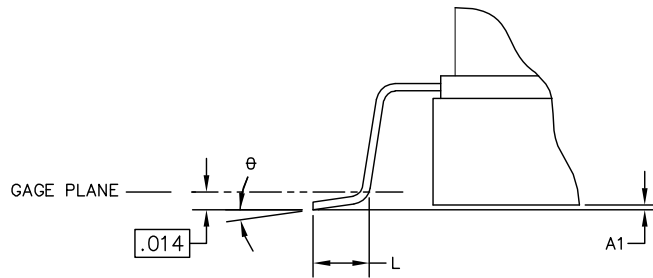
Case 98ASA99255D, small outline package, surface mount

MPxx5004



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 8 LD SOP, GVP	DOCUMENT NO: 98ASA99302D	REV: C	
	CASE NUMBER: 1368-01	18 DEC 2008	
	STANDARD: NON-JEDEC		

Case 98ASA99302D, small outline package, surface mount



DETAIL "G"

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 8 LD SOP, GVP	DOCUMENT NO: 98ASA99302D	REV: C	
	CASE NUMBER: 1368-01	18 DEC 2008	
	STANDARD: NON-JEDEC		

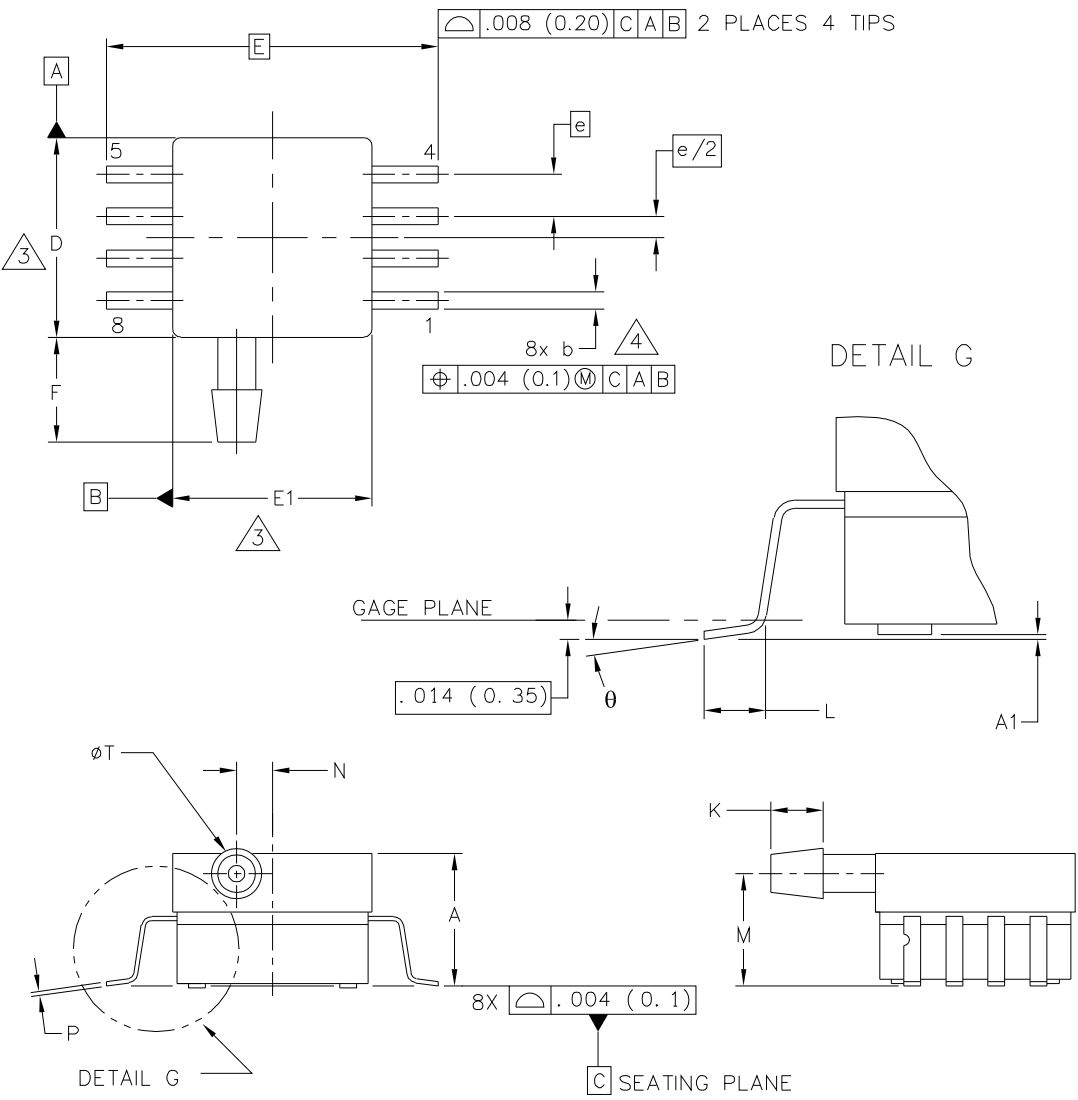


NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. THIS DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE.
4. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 MAXIMUM.

DIM	INCHES		MILLIMETERS		DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.280	.300	7.11	7.62	R	.405	.415	10.28	10.54
A1	.002	.010	0.05	0.25	Ø	0*	7*	0*	7*
b	.038	.042	0.96	1.07	-	---	---	---	---
D	.465	.485	11.81	12.32	-	---	---	---	---
E	.690 BSC		17.52 BSC		-	---	---	---	---
E1	.465	.485	11.81	12.32	-	---	---	---	---
e	.100 BSC		2.54 BSC		-	---	---	---	---
F	.240	.260	6.10	6.60	-	---	---	---	---
K	.115	.135	2.92	3.43	-	---	---	---	---
L	.040	.060	1.02	1.52	-	---	---	---	---
M	.035	.055	0.89	1.39	-	---	---	---	---
N	.075	.095	1.90	2.41	-	---	---	---	---
P	.009	.011	0.23	0.28	-	---	---	---	---
T	.110	.130	2.79	3.30	-	---	---	---	---
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: 8 LD SOP, GVP					DOCUMENT NO: 98ASA99302D			REV: C	
					CASE NUMBER: 1368-01			18 DEC 2008	
					STANDARD: NON-JEDEC				

Case 98ASA99302D, small outline package, surface mount



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 8 LD SOP, SIDE PORT	DOCUMENT NO: 98ASA99303D	REV: D	
	CASE NUMBER: 1369-01	13 DEC 2010	
	STANDARD: NON-JEDEC		

Case 98ASA99303D, small outline package



NOTES:

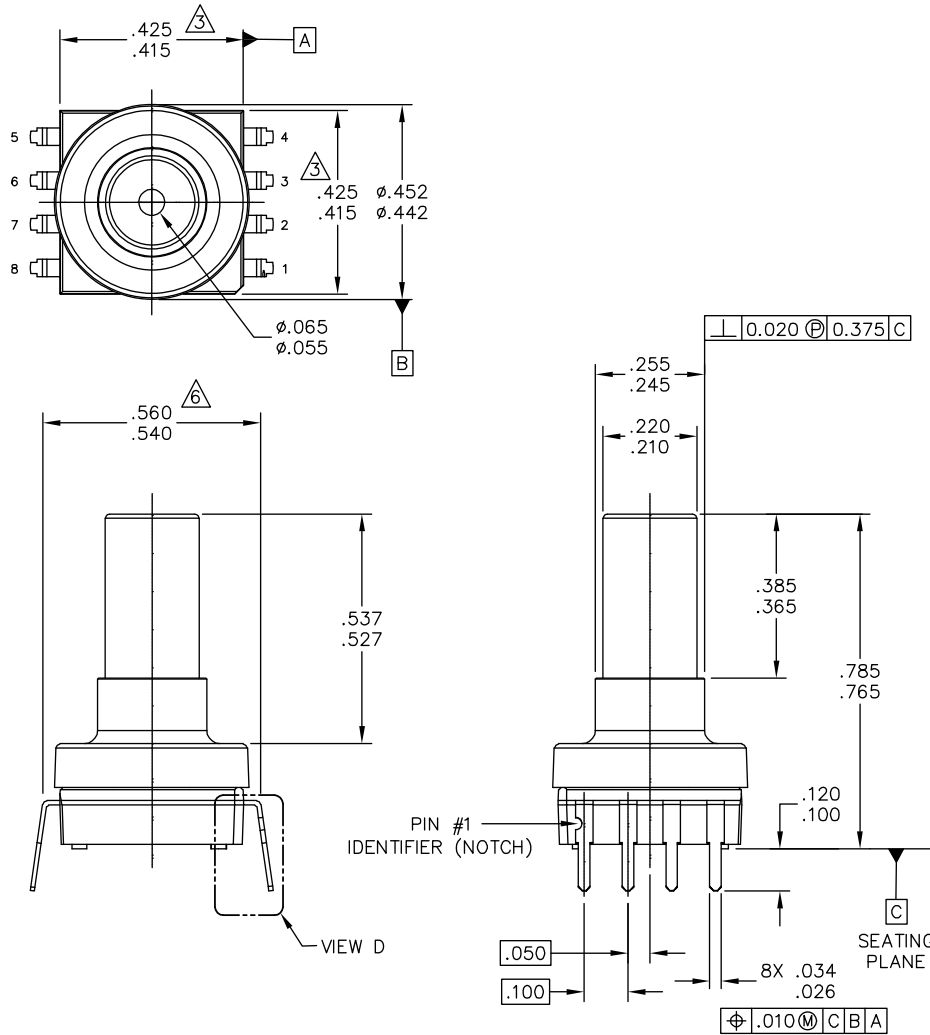
1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 (0.152) PER SIDE.

DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 (0.203) MAXIMUM.

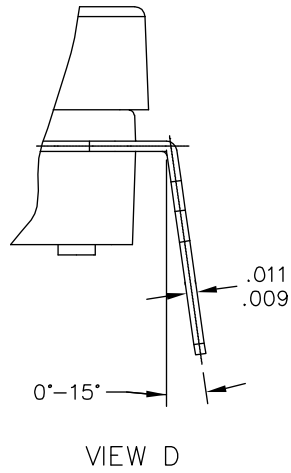
DIM	INCHES		MILLIMETERS		DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.300	.330	7.62	8.38	θ	0°	7°	0°	7°
A1	.002	.010	0.05	0.25	-	---	---	---	---
b	.038	.042	0.96	1.07	-	---	---	---	---
D	.465	.485	11.81	12.32	-	---	---	---	---
E	.717 BSC		18.21 BSC		-	---	---	---	---
E1	.465	.485	11.81	12.32	-	---	---	---	---
e	.100 BSC		2.54 BSC		-	---	---	---	---
F	.245	.255	6.22	6.47	-	---	---	---	---
K	.120	.130	3.05	3.30	-	---	---	---	---
L	.061	.071	1.55	1.80	-	---	---	---	---
M	.270	.290	6.86	7.36	-	---	---	---	---
N	.080	.090	2.03	2.28	-	---	---	---	---
P	.009	.011	0.23	0.28	-	---	---	---	---
T	.115	.125	2.92	3.17	-	---	---	---	---
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: 8 LD SOP, SIDE PORT					DOCUMENT NO: 98ASA99303D			REV: D	
					CASE NUMBER: 1369-01			13 DEC 2010	
					STANDARD: NON-JEDEC				

Case 98ASA99303D, small outline package



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10611D	REV: D	
	CASE NUMBER: 1560-03	25 FEB 2009	
	STANDARD: NON-JEDEC		

Case 98ASA10611D, small outline package



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10611D	REV: D	
	CASE NUMBER: 1560-03	25 FEB 2009	
	STANDARD: NON-JEDEC		

PAGE 2 OF 3

Case 98ASA10611D, small outline package



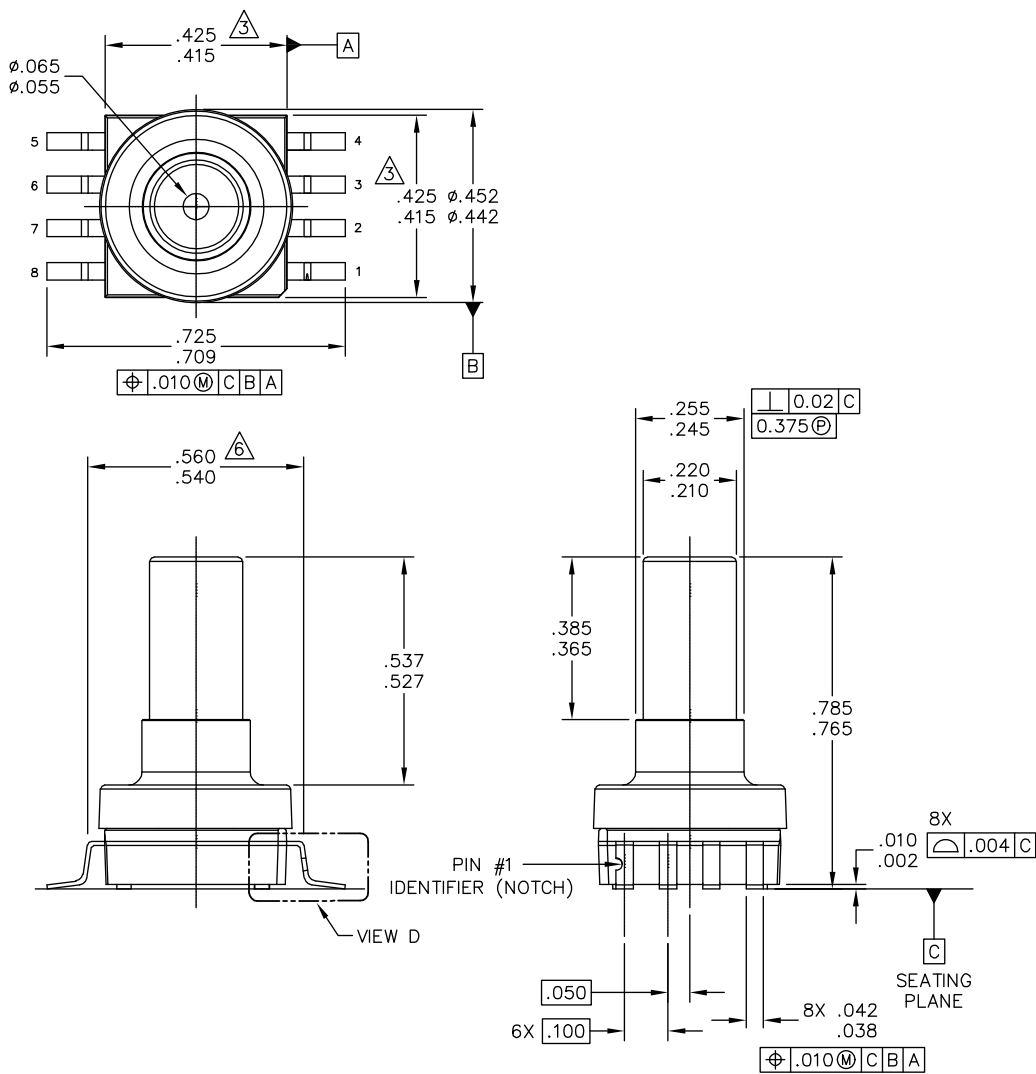
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION IS .006.
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10611D	REV: D	
	CASE NUMBER: 1560-03	25 FEB 2009	
	STANDARD: NON-JEDEC		

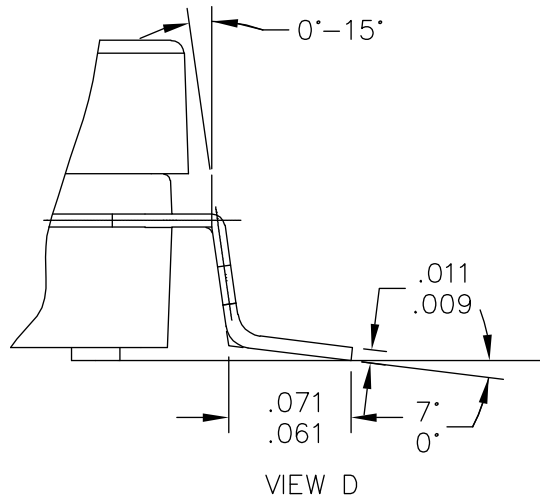
PAGE 3 OF 3

Case 98ASA10611D, small outline package



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10686D	REV: B	
	CASE NUMBER: 1735-02	19 FEB 2009	
	STANDARD: NON-JEDEC		

Case 98ASA10686D, small outline package



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10686D	REV: B	
	CASE NUMBER: 1735-02	19 FEB 2009	
	STANDARD: NON-JEDEC		

PAGE 2 OF 3

Case 98ASA10686D, small outline package



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION IS .006.
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10686D	REV: B	
	CASE NUMBER: 1735-02	19 FEB 2009	
	STANDARD: NON-JEDEC		

PAGE 3 OF 3

Case 98ASA10686D, small outline package

5 Revision History

Table 5. Revision history

Revision number	Revision date	Description
12.1	05/2015	<ul style="list-style-type: none">• Updated format.• Table 3: Updated Full-scale span Typ value, was 4.0 to 3.92. Updated Linearity definition in note 4.• Updated package drawings with current versions.



How to Reach Us:

Home Page:

freescale.com

Web Support:

freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/salestermsandconditions.

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners.

© 2006-2009, 2015 Freescale Semiconductor, Inc.