MPY012H

Multiplier

12 x 12 Bit, 115ns

The MPY012H is a high-speed 12 x 12 bit parallel multiplier which operates at a 115ns cycle time (8.7MHz multiplication rate). The multiplicand and the multiplier may be independently specified as two's complement or unsigned magnitude, yielding a full-precision 24-bit product.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The MPY012H is built with TRW's 2-micron bipolar process.

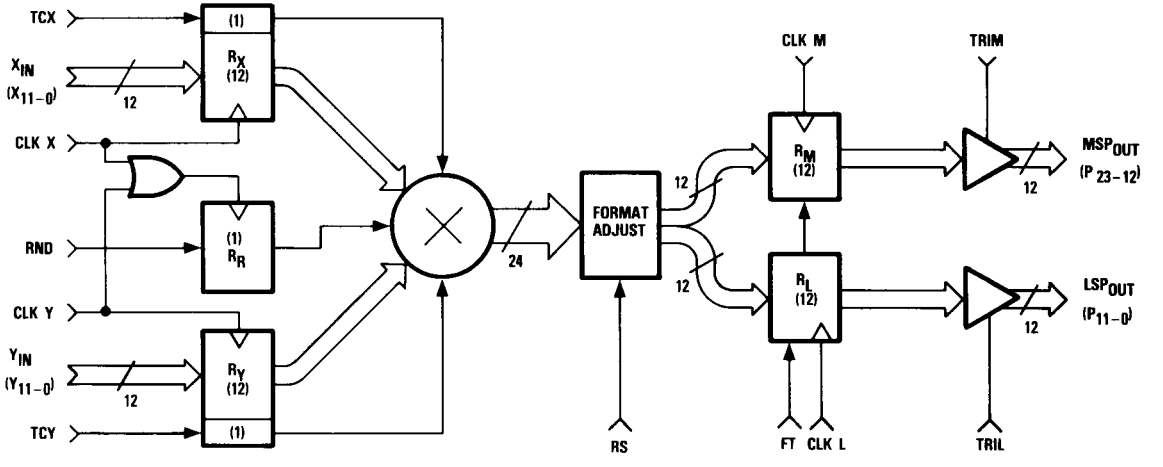
Features

- 115ns Multiply Time (Worst Case)
- 12 x 12 Bit Parallel Multiplication With 24-Bit Product Output
- Three-State Outputs
- Fully TTL Compatible
- Two's Complement, Unsigned Magnitude, And Mixed Mode Multiplication
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In A 64 Pin Ceramic DIP

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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ADS-012-H Rev. D 11/90
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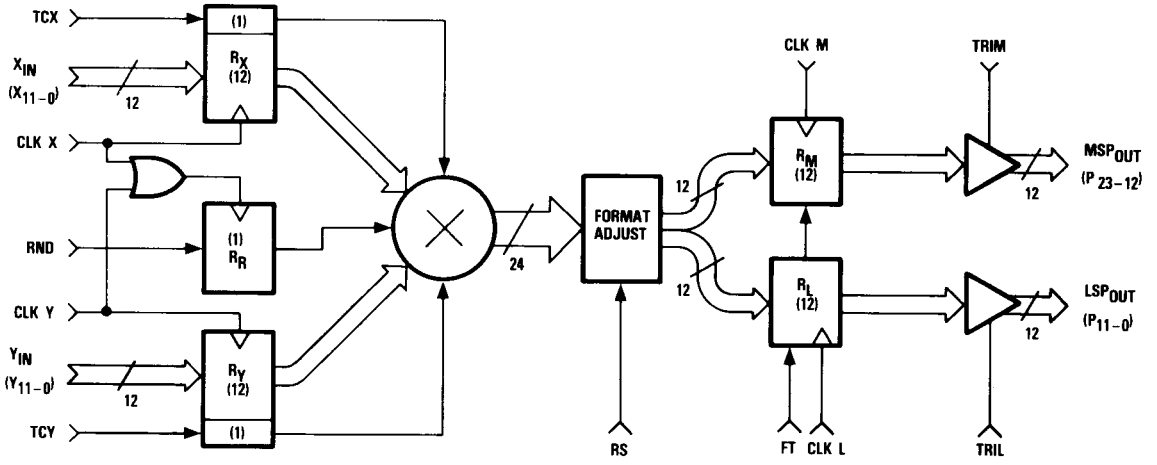
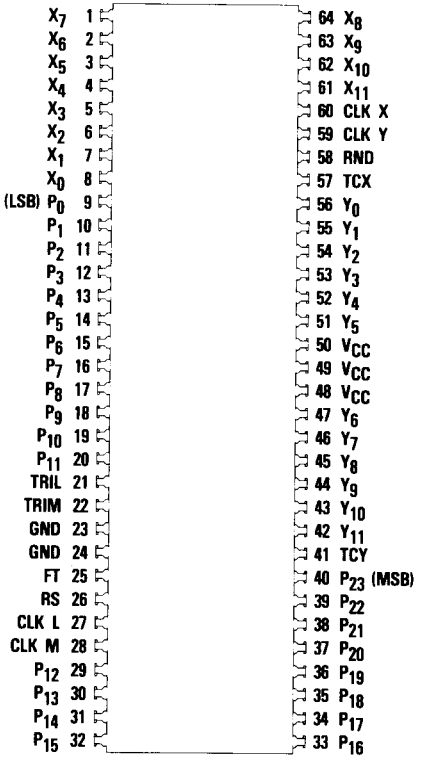
Functional Block Digram



Pin Assignments



64 Lead DIP – J1 Package

Functional Description

General Information

The MPY012H has three functional sections: input registers, an asynchronous multiplier array, and output registers. The input registers store the two 12-bit numbers which are to be multiplied and the instruction which controls the output rounding. This rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders, designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 12-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the MPY012H to be used on a bus, or allow the least and most significant outputs to be multiplexed over the same 12-bit output lines.

Power

The MPY012H operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J1 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 48, 49, 50
GND	Ground	0.0V	Pins 23, 24

Control

The MPY012H has seven control lines:

FT — A control line which makes the output register transparent if it is HIGH.

TRIM, TRIL — Three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when the appropriate control is LOW.

RS — RS is an output format control. A HIGH level on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, and two's complement integer operations.

RND — When RND is HIGH, a one is added to the MSB of the LSP. Note that this bit depends on the state of the RS control. If RS is LOW when RND is HIGH, a one will be added to the 2^{-12} bit (P_{10}). If RS is HIGH when RND is HIGH, a one will be added to the 2^{-11} bit (P_{11}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction; in some systems this may introduce a systematic bias.

TCX, TCY — Control how the device interprets data on the X and Y inputs. A HIGH on TCX or TCY forces the MPY012H to consider the appropriate input as a two's complement number, while a LOW forces the MPY012H to consider the appropriate input as a magnitude only number.

FT, RS, TRIM and TRIL are not registered. The TCX input is registered, and clocked in at the rising edge of the X clock signal, CLK X. The TCY input is also registered, and clocked in at the rising edge of the Y clock signal, CLK Y. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading the RND control signal can be avoided by the use of normally LOW clocks.

Control (Cont.)

Name	Function	Value	J1 Package
RND	Round Control Bit	TTL	Pin 58
TCX	X Input, Two's Complement	TTL	Pin 57
TCY	Y Input, Two's Complement	TTL	Pin 41
FT	Output Register Feedthrough	TTL	Pin 25
RS	Output Right Shift	TTL	Pin 26
TRIM	MSP Three-State Control	TTL	Pin 22
TRIL	LSP Three-State Control	TTL	Pin 21

Data Inputs

The MPY012H has two 12-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{11} and Y_{11}, carry the sign information for the two's complement notation. The remaining bits are denoted X_0 through X_{10} and Y_0 through Y_{10} (with X_0 and Y_0 the Least Significant Bits). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6.

Name	Function	Value	J1 Package
X_{11}	X Data MSB	TTL	Pin 61
X_{10}		TTL	Pin 62
X_9		TTL	Pin 63
X_8		TTL	Pin 64
X_7		TTL	Pin 1
X_6		TTL	Pin 2
X_5		TTL	Pin 3
X_4		TTL	Pin 4
X_3		TTL	Pin 5
X_2		TTL	Pin 6
X_1		TTL	Pin 7
X_0	X Data LSB	TTL	Pin 8
Y_{11}	Y Data MSB	TTL	Pin 42
Y_{10}		TTL	Pin 43
Y_9		TTL	Pin 44
Y_8		TTL	Pin 45
Y_7		TTL	Pin 46
Y_6		TTL	Pin 47
Y_5		TTL	Pin 51
Y_4		TTL	Pin 52
Y_3		TTL	Pin 53
Y_2		TTL	Pin 54
Y_1		TTL	Pin 55
Y_0	Y Data LSB	TTL	Pin 56

Data Outputs

The MPY012H has a 24-bit two's complement or unsigned magnitude output which is the product of the two input data values. This output is divided into two 12-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP). The Most Significant Bit (MSB) of both the MSP and the LSP is the sign bit if fractional two's complement notation is used (TCX=TCY=1, RS=0). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6. For the MSP and LSP to be read, the respective TRIM and TRIL controls must be LOW. RS is an output format control. A logical "1" on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, or integer two's complement operation.

Name	Function	Value	J1 Package
P_{23}	Product MSB	TTL	Pin 40
P_{22}		TTL	Pin 39
P_{21}		TTL	Pin 38
P_{20}		TTL	Pin 37
P_{19}		TTL	Pin 36
P_{18}		TTL	Pin 35
P_{17}		TTL	Pin 34
P_{16}		TTL	Pin 33
P_{15}		TTL	Pin 32
P_{14}		TTL	Pin 31
P_{13}		TTL	Pin 30
P_{12}		TTL	Pin 29
P_{11}		TTL	Pin 20
P_{10}		TTL	Pin 19
P_9		TTL	Pin 18
P_8		TTL	Pin 17
P_7		TTL	Pin 16
P_6		TTL	Pin 15
P_5		TTL	Pin 14
P_4		TTL	Pin 13
P_3		TTL	Pin 12
P_2		TTL	Pin 11
P_1		TTL	Pin 10
P_0	Product LSB	TTL	Pin 9

Clocks

The MPY012H has four clock lines, one for each of the input registers and one for each product register. Data and two's complement instructions present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading this control signal can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package
CLK X	Clock Input Data X	TTL	Pin 60
CLK Y	Clock Input Data Y	TTL	Pin 59
CLK L	Clock LSP Register	TTL	Pin 27
CLK M	Clock MSP Register	TTL	Pin 28

Figure 1. Fractional Two's Complement Notation

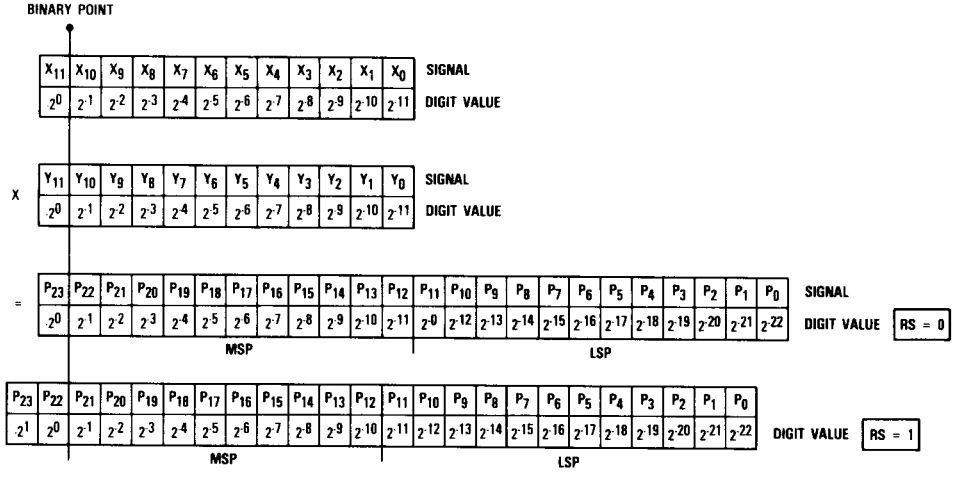


Figure 2. Fractional Unsigned Magnitude Notation

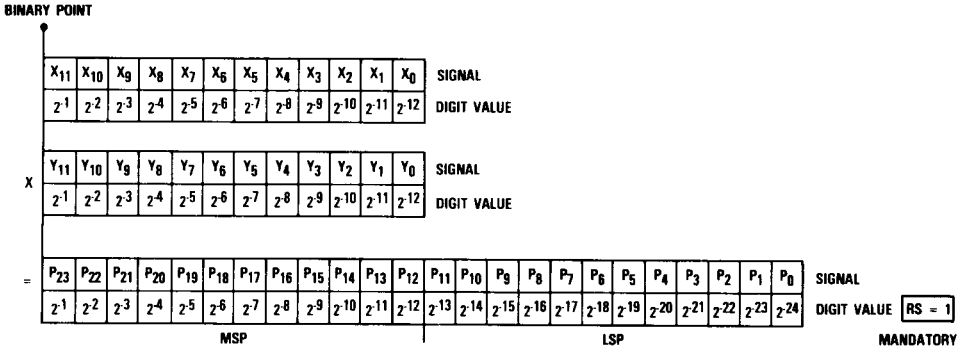


Figure 3. Fractional Mixed Mode Notation

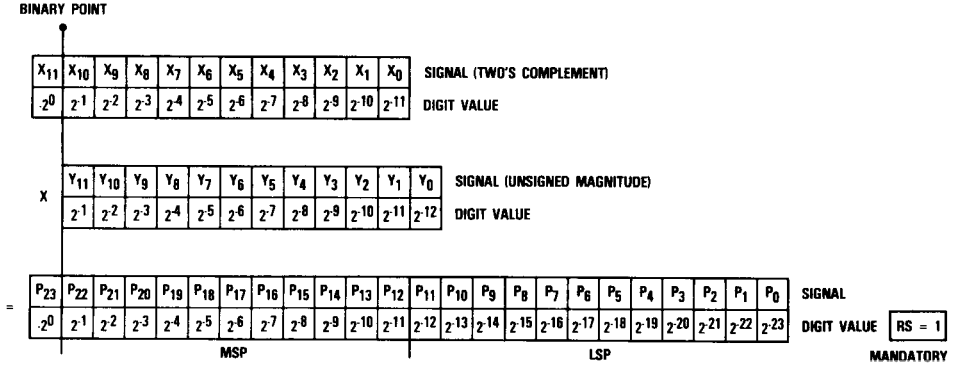


Figure 4. Integer Two's Complement Notation

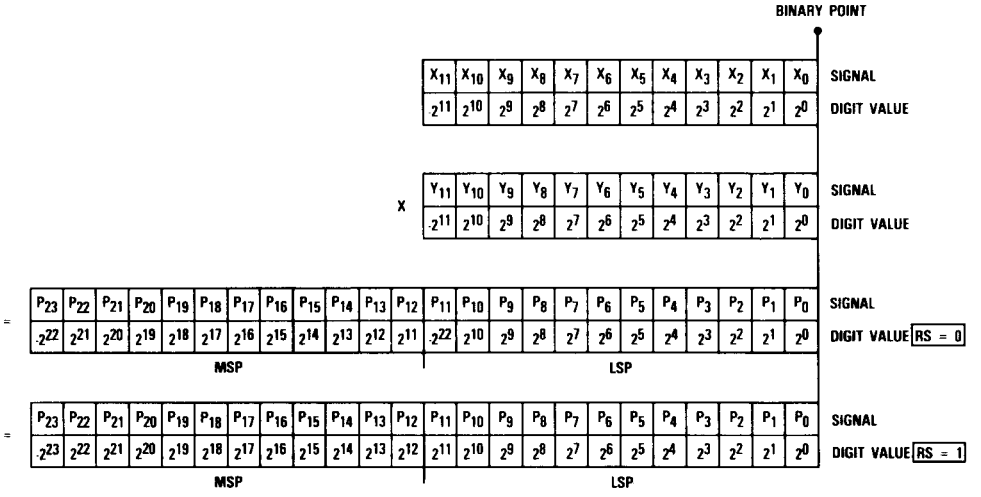


Figure 5. Integer Unsigned Magnitude Notation

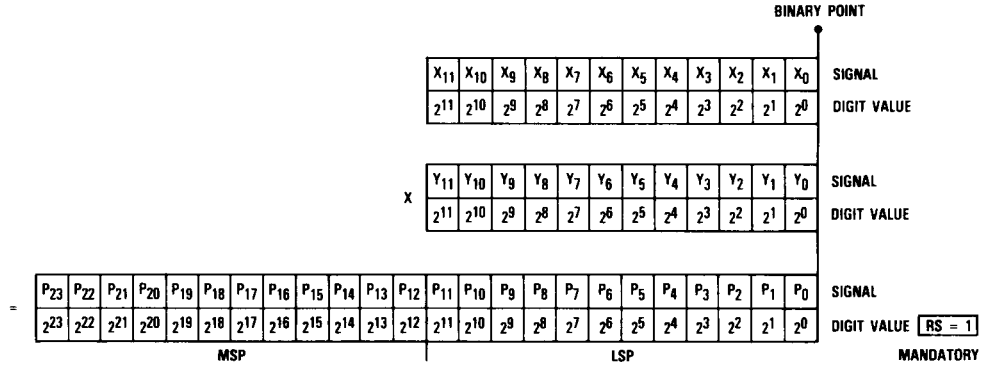


Figure 6. Integer Mixed Mode Notation

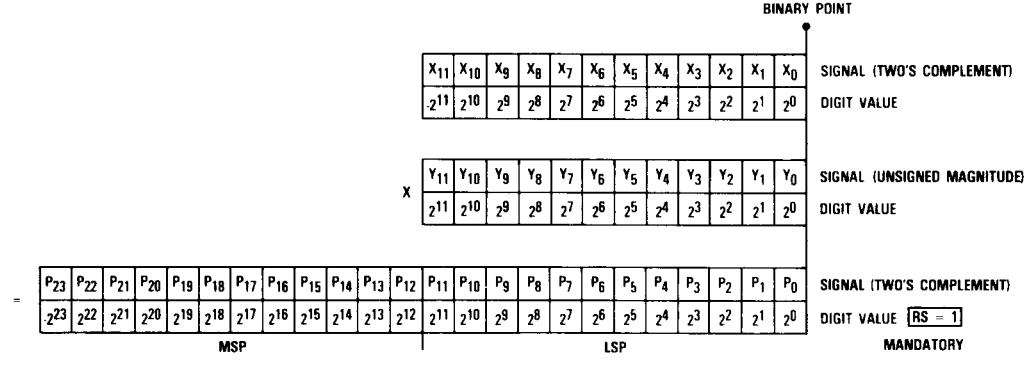


Figure 7. Timing Diagram

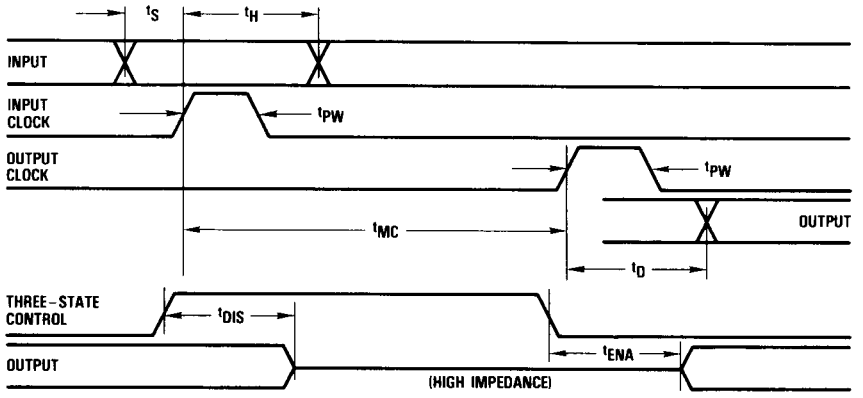


Figure 8. Timing Diagram, Unclocked Mode

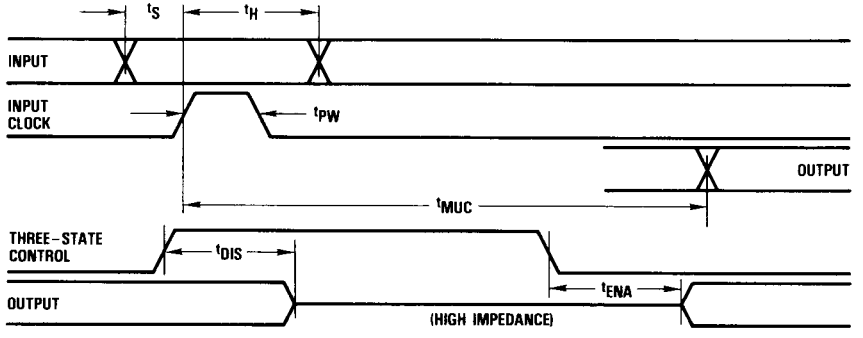
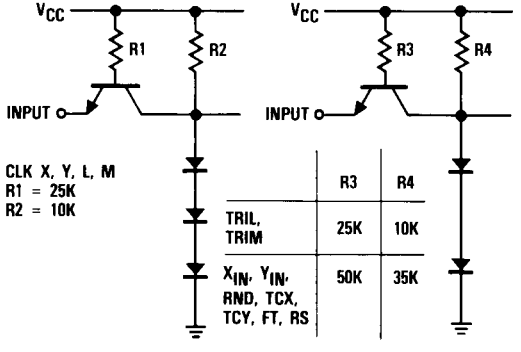


Figure 9. Equivalent Input Circuit



	R3	R4
TRIL, TRIM	25K	10K
X_{IN}, Y_{IN}, RND, TCX, TCY, FT, RS	50K	35K

Figure 10. Equivalent Output Circuit

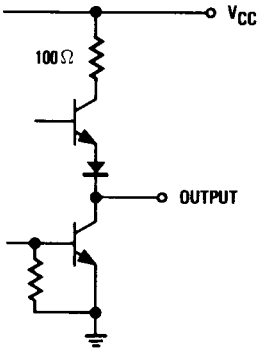


Figure 11. Test Load

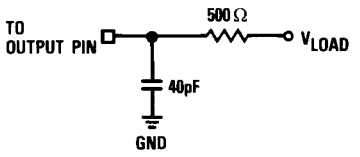
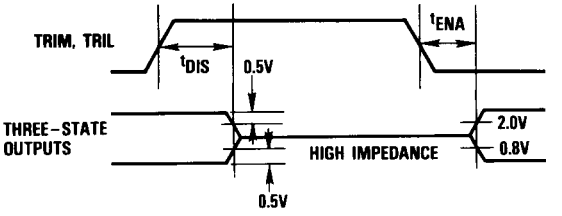


Figure 12. Three-State Delay Test Load



Application Notes

Mixed Mode Multiplication

There are several applications in which mixed mode multiplication may be advantageous. For example, inputs to a digital signal processor are often generated as unsigned magnitude numbers (e.g., data from an analog-to-digital converter). These numbers are effectively all positive values. In contrast, filter coefficients must often be negative. As a result, either the unsigned magnitude data must be converted to two's complement notation (which requires an additional bit), or the multiplier must be capable of mixed mode operation. The MPY012H provides this capability by independently specifying the mode of the multiplicand (X) and the multiplier (Y) on the TCX and TCY pins. No additional circuitry is required and the resulting product is in two's complement notation.

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the selected register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the MPY012H does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design.

Because common design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 6.

Register Shift (RS) Control

In two's complement notation, the acceptable range of values for a given word size is not the same for positive and negative numbers. The largest negative number is one LSB larger than the largest positive number. This is true for either fractional or integer notation. A problem can arise when the largest representable negative number is multiplied by itself. This should give a positive number of the same magnitude. However, the largest representable positive number is one LSB less than this value. As a result, this product cannot be correctly represented without using one additional output bit.

The MPY012H has a Register Shift (RS) control that permits shifting of the result to provide a correct answer for every two's complement multiplication. When RS is active, the value of all bits in the MSP is doubled (i.e., shifted left one position), which provides the capability to represent the largest possible product. The MSB of the Least Significant Product is changed from a duplicate of the sign bit to the necessary bit to fill in the output word. The effects of this control are illustrated in Figures 1 and 4. Note that for unsigned magnitude operation, the RS control must be HIGH.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage		−0.5 to +7.0V
Input		
	Applied voltage	−0.5 to +5.5V [2]
	Forced current	−6.0 to +6.0mA
Output		
	Applied voltage	−0.5 to +5.5V [2]
	Forced current	−1.0 to +6.0mA [3,4]
	Short-circuit duration (single output in high state to ground)	1 sec
Temperature		
	Operating, case	−55 to +125°C
	junction	175°C
	Lead, soldering (10 seconds)	300°C
	Storage	−65 to 150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	25			30			ns
t_S	Input Register Setup Time	25			30			ns
t_H	Input Register Hold Time	0			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			-400			-400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{CC}	Supply Current	V_{CC} = MAX, Static[1]		700		750	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		X_{IN}, Y_{IN}, RND, FT		-0.4		-0.4	mA
		TCX, TCY, RS		-0.8		-0.8	mA
		CLK L, M, X, and Y; TRIM, TRIL		-1.0		-1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		X_{IN}, Y_{IN}, RND, FT		75		100	μA
		TCX, TCY, RS		75		100	μA
		CLK L, M, X, and Y; TRIM, TRIL		75		100	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V		-40		-40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, one pin to ground, one second duration max, output HIGH		-50		-50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:
1. All inputs and outputs LOW.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MC}	Multiply Time, Clocked	V_{CC} = Min		115		140	ns
t_{MUC}	Multiply Time, Unclocked	V_{CC} = Min		155		185	ns
t_D	Output Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = Min, Test Load: V_{LOAD} = 1.8V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.6V (t_{DIS0}) [2] V_{LOAD} = 0.0V (t_{DIS1}) [2]		40		45	ns

Notes: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 12.

2. t_{DIS1} denotes the transition from logical 1 to three-state.
t_{DIS0} denotes the transition from logical 0 to three-state.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
MPY012HJ1C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Ceramic DIP	012HJ1C
MPY012HJ1A	EXT – T_C = –55°C to 125°C	High Reliability	64 Pin Ceramic DIP	012HJ1A