MQ051K1VPX LDMOS TRANSISTOR

Document Number: MQ051K1VPX
Preliminary Datasheet V1.0

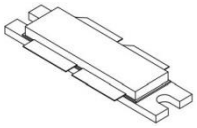
1100W, 50V High Power RF LDMOS FETs

Description

The MQ051K1VPX is a 1100-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 0.5 GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

MQ051K1VPX



- Typical Performance (On Innogration narrow band fixture with device soldered):

  V_{DD} = 52 Volts, I_{DQ} = 100 mA, Pulse CW, Pulse Width=100 us, Duty cycle=10% .

Frequency	G_P (dB)	P_{SAT} (W)	η_D@P_{SAT} (%)
325 MHz	20.5	1122	70.6

- Typical Performance (On Innogration narrow band fixture with device soldered): V_{DD} = 52 Volts, I_{DQ} = 100 mA, CW .

Frequency	Gp (dB)	P_{SAT} (W)	η_D@P_{SAT} (%)
325 MHz	20.1	1023	70.3

- Capable of Handling >10:1 VSWR, @ 52Vdc, 325 MHz,1100 Watts Pulse CW Output Power Designed for Enhanced Ruggedness.

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+52	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case,Case Temperature 80°C, 1200W Pulse CW, 50 Vdc, I_{DQ} = 100 mA	$R_{\theta JC}$	0.16	°C/W

Table 3. ESD Protection Characteristics

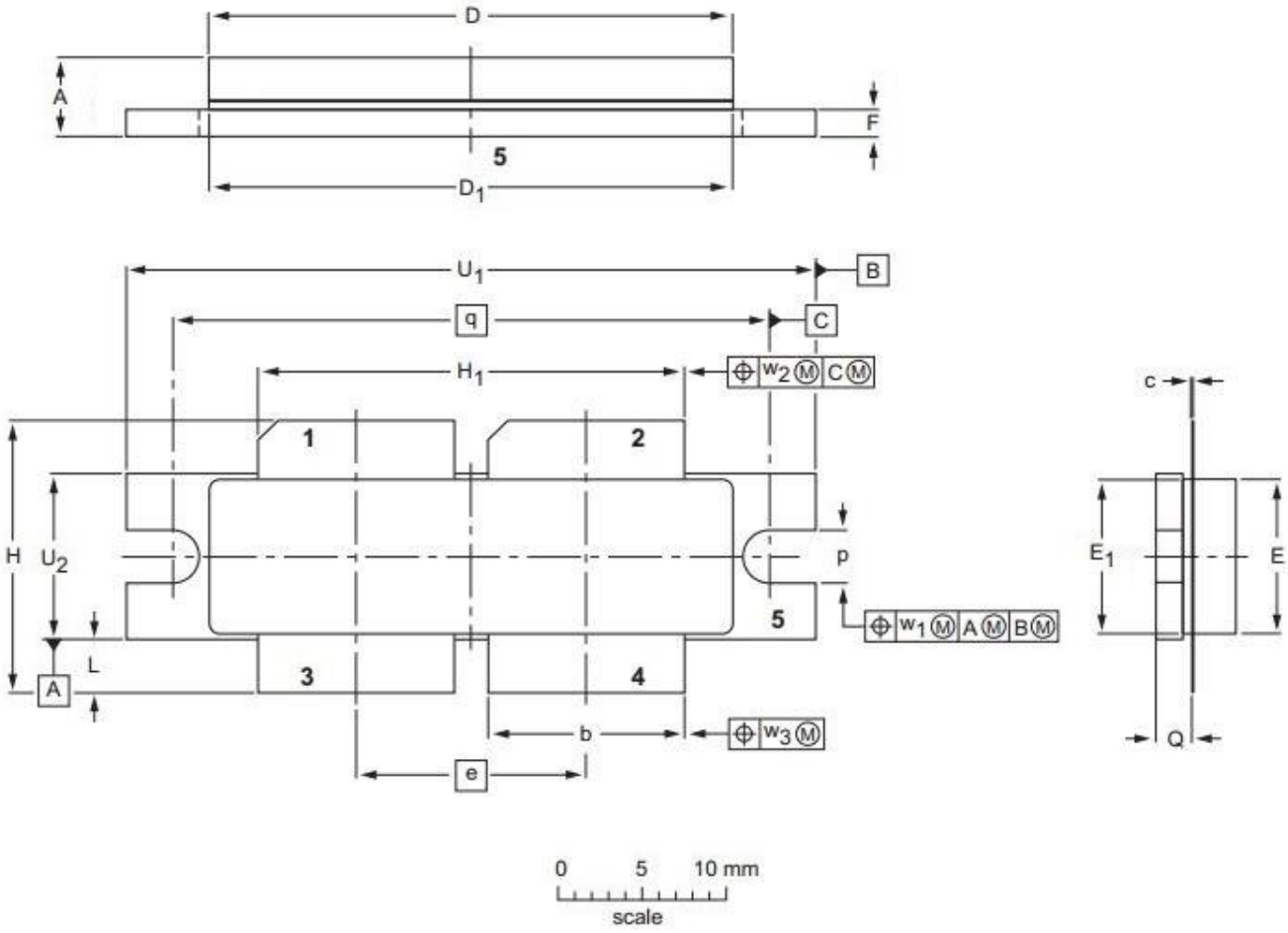
Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	110	——	——	V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS}(th)$	——	1.6	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	2.1	2.6	3.1	V
Functional Tests (In Innogration Demo-1030MHz, 50 ohm system) : V_{DD} = 52 Vdc, I_{DQ} = 100 mA, f = 325 MHz, Pulse CW Signal Measurements. (Pulse Width=100 μs, Duty cycle=10%)					
Power Gain @ P_{SAT}	Gp	——	20.5	——	dB
Saturated Output Power	P_{SAT}	——	1122	——	W
Drain Efficiency @ P_{SAT}	η_D	——	70.6	——	%
Input Return Loss	IRL	——	-7	——	dB

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/04/20	**Rev 1.0**	**Preliminary Datasheet**

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