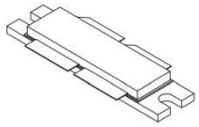
MQ1270VP LDMOS TRANSISTOR

Document Number: MQ1270VP
Preliminary Datasheet V1.0

700W, 50V High Power RF LDMOS FETs

MQ1270VP



Description

The MQ1270VP is a 700-watt, high performance, internally matched LDMOS FET, designed for avionics applications with frequencies 960 to 1215MHz.

It is featured for high power and high ruggedness.

It is recommended to use this device under pulse condition only

- Typical **long pulse** Performance (on innogration wide band test fixture with device soldered):

  Pulse width:100uS, duty cycle: 10%, Vds = 50 V, Idq = 100 mA, TA = 25 °C

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	Eff(%)
960	46.5	59	800	3.76	12.5	43
990	46.5	59.7	933	3.96	13.2	48
1010	46.5	60.2	1047	4.37	13.7	48
1040	46.5	58.9	776	3.81	12.4	41
1070	46.5	59.6	912	4.48	13.1	41
1100	46.5	58.8	750	4.37	12.3	35
1130	46.5	59.1	812	4.35	12.6	38
1160	46.5	59.4	870	4.44	12.9	40
1190	46.5	59	800	4	12.5	41
1215	46.5	59.4	870	4.2	12.9	42

- Typical **short pulse** Performance (on innogration wide band test fixture with device soldered):

  Pulse width:24uS, duty cycle: 2%, Vds = 50 V, Idq = 100 mA, TA = 25 °C

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	Eff(%)
960	46.5	59.3	868	0.85	12.8	46
990	46.5	60	1000	0.92	13.5	48
1010	46.5	60.4	1106	1	13.9	49
1040	46.5	59.1	829	0.89	12.6	41
1070	46.5	59.9	986	1.01	13.4	43
1100	46.5	58.9	792	1	12.4	35
1130	46.5	59.4	883	1	12.9	39
1160	46.5	59.8	957	1.03	13.3	41
1190	46.5	59.3	858	0.95	12.8	40
1215	46.5	59.7	946	0.96	13.2	43

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Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case,Case Temperature 80°C, 870W Pout, Pulse width: 100us, duty cycle: 10%, Vds=50 V, I_{DQ} = 100 mA	$R_{\theta JC}$	0.02	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	115			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS}(th)$		1.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.14		V
Functional Tests (In Innogration test fixture, 50 ohm system) : V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f = 1215 MHz, Pulse CW Signal Measurements. (Pulse Width=100 μs, Duty cycle=10%), Pin=46.5dBm					
Power Gain @ Pout	Gp		12.9		dB
Output Power	Pout	58.5	59.4		dBm

Drain Efficiency@Pout	η_D		42.0		%
Input Return Loss	IRL		-7		dB

Reference Circuit of Test Fixture Assembly Diagram

(Layout file upon request)

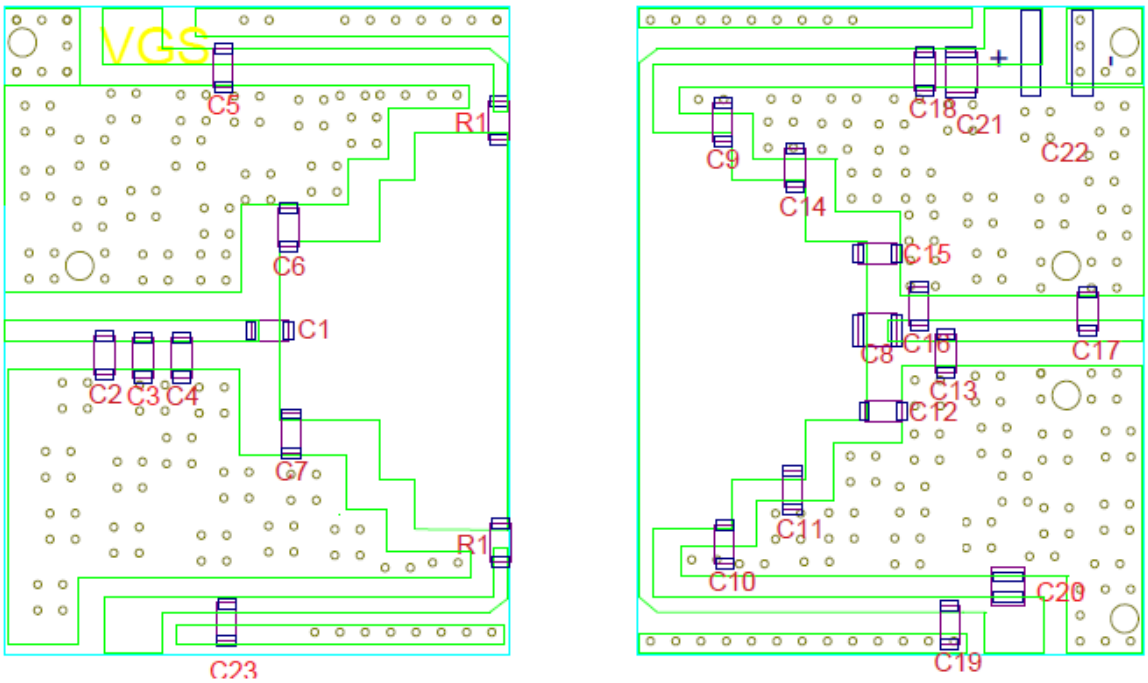


Figure 1. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

(Layout file upon request)

Part	description	Model
C1	100PF	ATC800B
C2,C17	2PF	ATC800B
C3,C16	1PF	ATC800B
C4	0.8PF	ATC800B
C5,C8,C18,C19,C23	47PF	ATC800B
C6,C9,C10	9.1PF	ATC800B
C7	3.9PF	ATC800B
C11,C15,	6.8PF	ATC800B
C12	1.5PF	ATC800B
C13	2.4PF	ATC800B
C14	5.1PF	ATC800B
C20,C21	10UF	100V/10UF
C22	1000UF	63V/1000UF
R1,R2	10Ω	0603
Q1	MQ1270VPS	182606S-01
PCB	4350B	30Mil

TYPICAL CHARACTERISTICS

Pulse width:100uS, duty cycle: 10%, Vds = 50 V, Idq = 100 mA, TA = 25 °C at fixed Pin=46.5dBm

Figure 2: Power gain and Pout as a Function of frequency

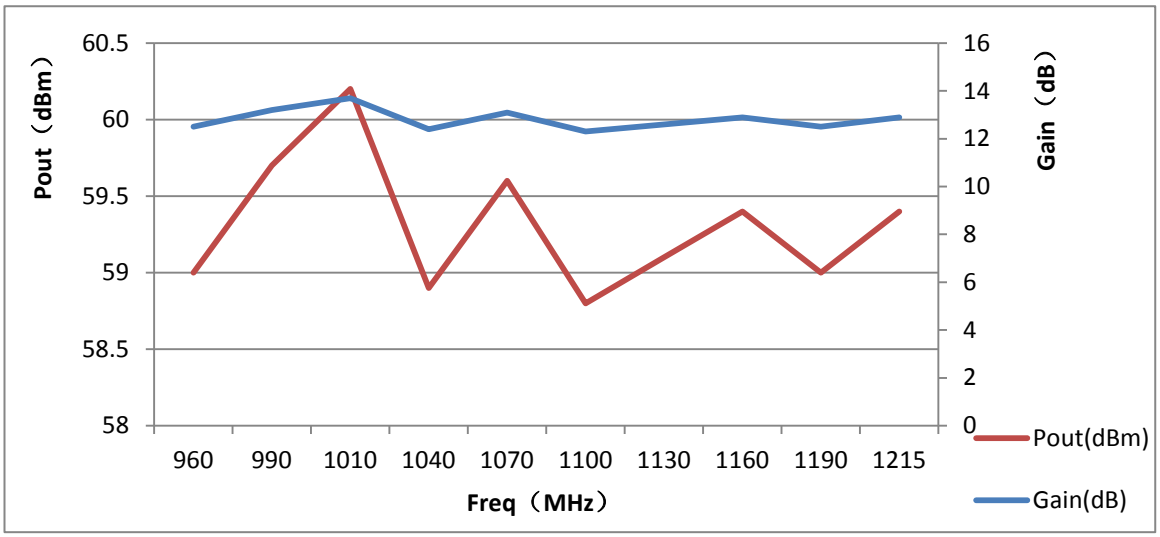
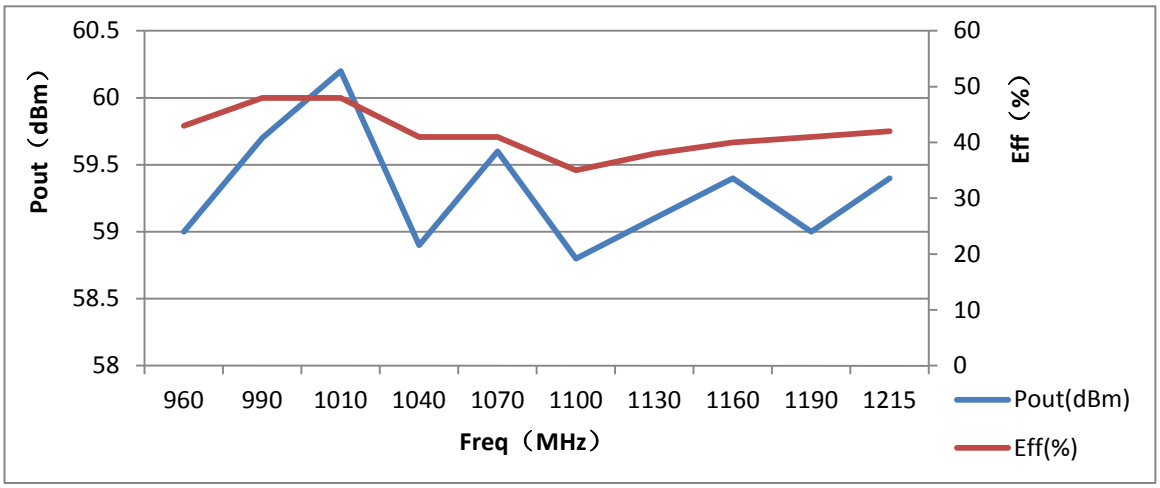
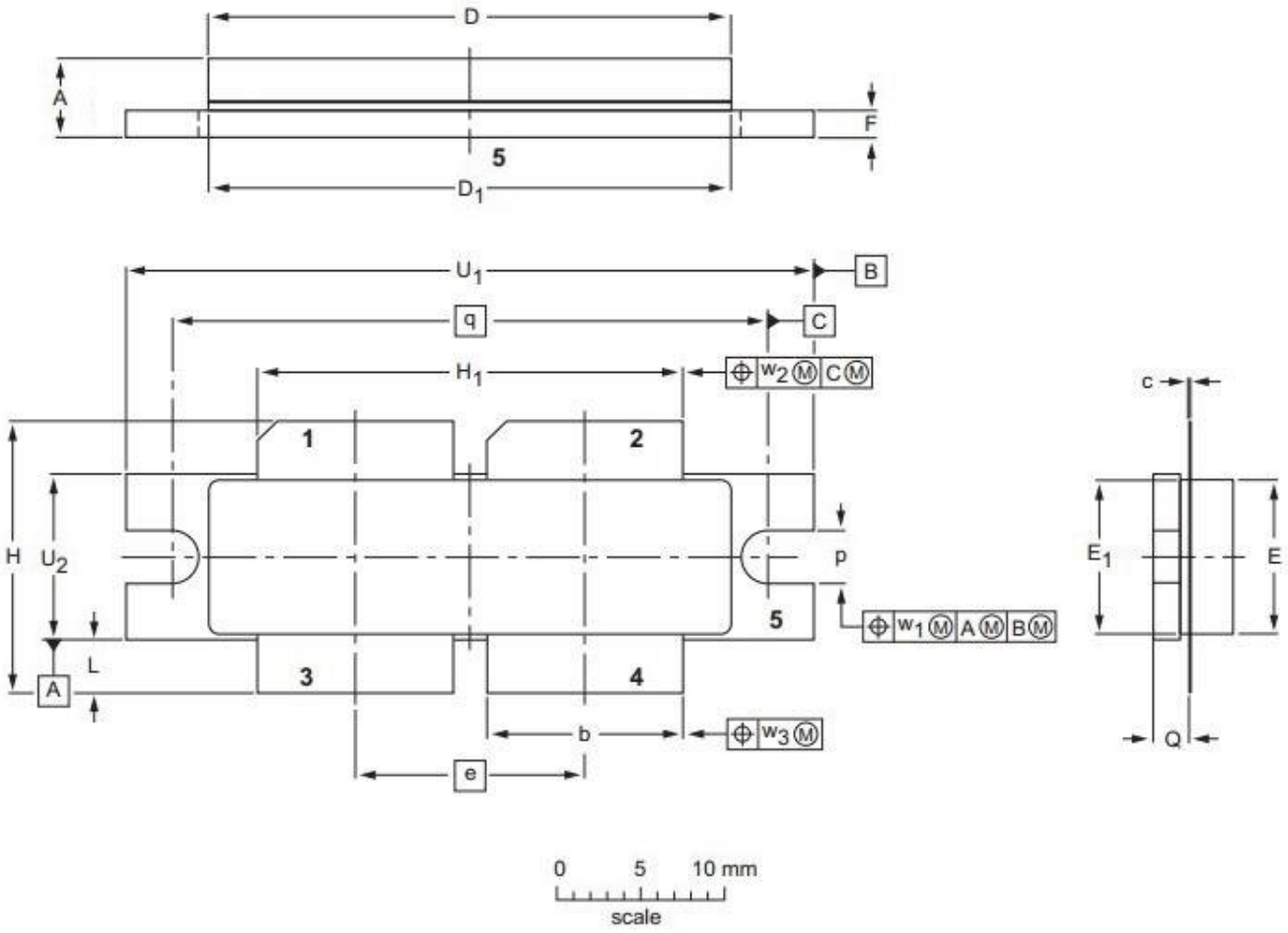


Figure 3:Effiicen and Pout as a Function of frequency



Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
Mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
Inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2018/8/3	Rev 1.0	Preliminary Datasheet Creation

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