MR2002C LDMOS TRANSISTOR

Document Number: MR2002C
Preliminary Datasheet V1.1

20W, 28V High Power RF LDMOS FETs

Description

The MR2002C is a 20-watt, unmatched LDMOS FETs, designed for Wide-band and Mobile radio applications with frequencies under 2000 MHz. It can be used in Class AB/B and Class C for all typical modulation formats.

It can also operate at lower voltage down to 12V with decreased power capability.

- Typical Performance (On Innogration fixture with device soldered):

  V_{DD} = 28 Volts, I_{DQ} = 100 mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	η_D@P_{-1} (%)
1000 MHz	22	20	65

MR2002C

Notice:

It is recommended to operate this device only below 24V like 14V,12V etc, if operation band is below 500MHz.

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	1.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics (per half section)

Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	65	69		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 9 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 μA)	$V_{GS(th)}$	——	2.23	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =14 V, f = 1 MHz)	C_{ISS}		10.1		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =14 V, f = 1 MHz)	C_{OSS}		3.9		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =14 V, f = 1 MHz)	C_{RSS}		0.29		pF
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		10.3		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		3.1		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		0.26		pF

Functional Tests (On Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 100 mA, f = 1000 MHz, CW Signal Measurements.

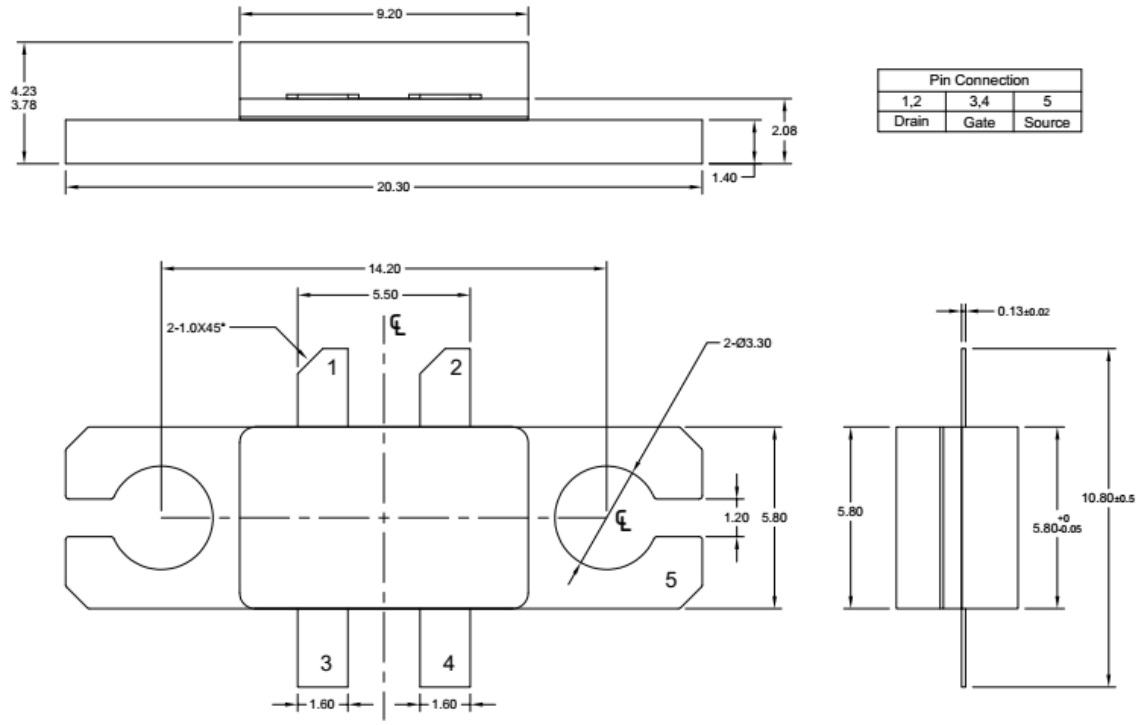
Power Gain	Gp		22		dB
Drain Efficiency@P1dB	η_D		65		%
1 dB Compression Point	P_{-1dB}		20		W
Input Return Loss	IRL		-10		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 100 mA, f = 1000 MHz

VSWR 10:1 at 20W pulse CW Output Power	No Device Degradation

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-G4E					2018/01/19

Figure 1. Package Outline PKG-G4E

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/6/14	Rev 1.0	Preliminary Datasheet
2018/8/2	Rev 1.1	Add notice of below 500MHz operation

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