MR26V51252R

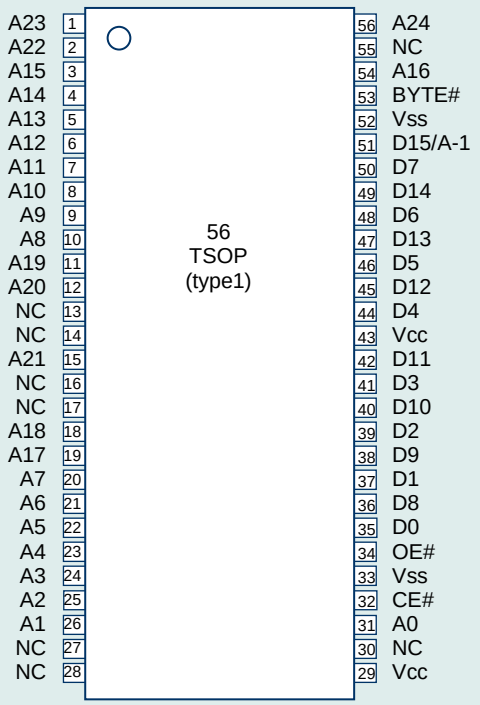
32M–Word × 16–Bit or 64M–Word × 8–Bit Page Mode P2ROM

FEATURES

32Mx16 or 64Mx8-bit
electrically switchable configuration

· Page size of 8-word x 16-Bit or 16-word x 8-Bit
· 3.0 V to 3.6 V power supply
·Random Access time 105 ns MAX
·Page Access time 25 ns MAX
· Operating current 50 mA MAX
· Standby current 4 mA MAX
· Input/Output TTL compatible
· Three-state output

PIN CONFIGURATION (TOP VIEW)



PACKAGES

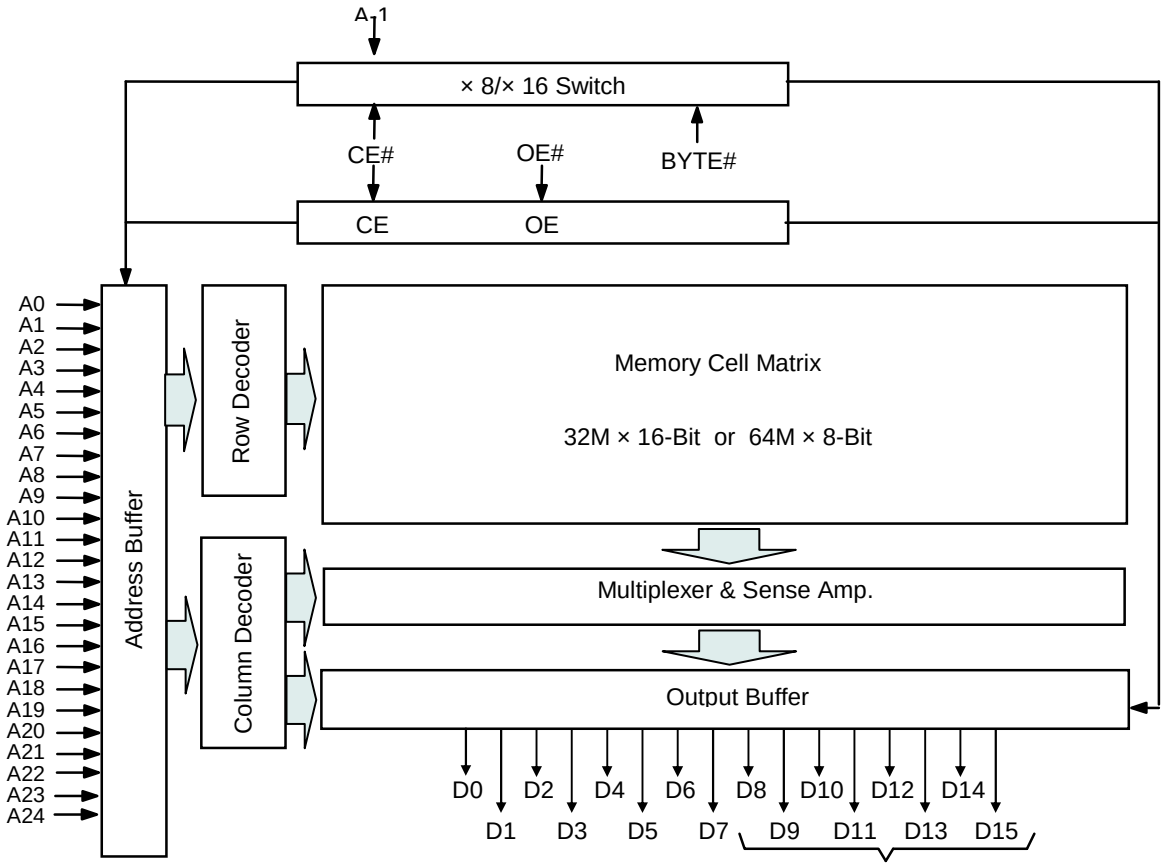
· MR26V51252R-xxxTA
56-pin plastic TSOP (P-TSOP(1)56-1420-0.50-K-MC)

P2ROM ADVANCED TECHNOLOGY

P2ROM stands for Production Programmed ROM. This exclusive LAPIS Semiconductor technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

· **Short lead time**, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
· **No mask charge**, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
· **No additional programming charge**, unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
· **Custom Marking** is available at no additional charge.

BLOCK DIAGRAM



In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

PIN DESCRIPTIONS

Pin name	Functions
D15 / A–1	Data output / Address input
A0 to A24	Address inputs
D0 to D14	Data outputs
CE#	Chip enable input
OE#	Output enable input
BYTE#	Word / Byte select input
V_{CC}	Power supply voltage
V_{SS}	Ground
NC	No connect

FUNCTION TABLE

Mode	CE#	OE#	BYTE#	V_{CC}	D0 to D7	D8 to D15	A-1
Read (16-Bit)	L	L	H	3.3 V	D_{OUT}		*
Read (8-Bit)	L	L	L		D_{OUT}	Hi–Z	L/H
Output disable	L	H	H		Hi–Z		*
			L				
Standby	H	*	H		Hi–Z		*
			L				

*: Don't Care (H or L)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	Ta	—	0 to 70	°C
Storage temperature	T_{STG}		–55 to 125	°C
Input voltage	V_I	relative to V_{SS}	–0.5 to V_{CC}+0.5	V
Output voltage	V_O		–0.5 to V_{CC}+0.5	V
Power supply voltage	V_{CC}		–0.5 to 5	V
Output short circuit current	I_{OS}	—	10	mA
Power dissipation per package	P_D	Ta=25°C	1.0	W

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{CC} power supply voltage	V_{CC}	V_{CC} = 3.0 to 3.6 V	3.0	—	3.6	V
Input "H" level	V_{IH}		2.2	—	V_{CC}+0.5*	V
Input "L" level	V_{IL}		–0.5**	—	0.6	V

Voltage is relative to V_{SS}.

* : V_{CC}+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

PIN CAPACITANCE

(V_{CC} = 3.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C_{IN1}	V_I = 0 V	—	—	10	pF
BYTE#	C_{IN2}		—	—	200	
Output	C_{OUT1}	V_O = 0 V	—	—	20	
D15/A-1	C_{OUT2}		—	—	20	

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	V_I = 0 to V_{CC}		—	—	10	μA
Output leakage current	I_{LO}	V_O = 0 to V_{CC}		—	—	10	μA
V_{CC} power supply current (Standby)	I_{CCSC}	CE# = Add.=V_{CC}		—	—	4	mA
	I_{CCST}	CE# = Add.=V_{IH}		—	—	4	mA
V_{CC} power supply current (Read)	I_{CCA1}	CE# = V_{IL} OE# = V_{IH}	tc = 200 ns	—	—	50	mA
Input "H" level	V_{IH}	—		2.2	—	V_{CC}+0.5*	V
Input "L" level	V_{IL}	—		–0.5**	—	0.6	V
Output "H" level	V_{OH}	I_{OH} = –2 mA		2.4	—	—	V
Output "L" level	V_{OL}	I_{OL} = 2 mA		—	—	0.4	V

Voltage is relative to V_{SS}.

* : V_{CC}+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

AC Characteristics

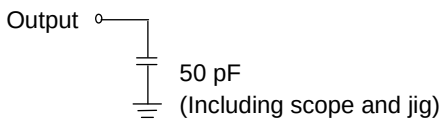
(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	t_C	—	105	—	ns
Address access time	t_{ACC}	—	—	105	ns
Page cycle time	t_{PC}	—	25	—	ns
Page access time	t_{PAC}	CE# = OE# = V_{IL}	—	25	ns
CE# access time	t_{CE}	OE# = V_{IL}	—	105	ns
OE# access time	t_{OE}	CE# = V_{IL}	—	25	ns
Output disable time	t_{CHZ}	OE# = V_{IL}	0	20	ns
	t_{OHZ}	CE# = V_{IL}	0	20	ns
Output hold time	t_{OH}	CE# = OE# = V_{IL}	0	—	ns

Measurement conditions

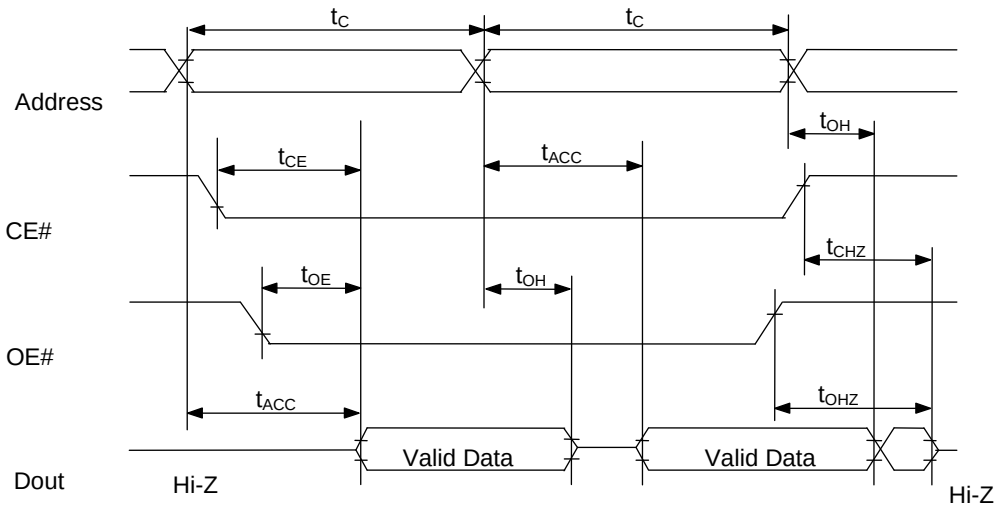
Input signal level ····· 0 V/3 V
Input timing reference level ····· 1/2V_{CC}
Output load ····· 50 pF
Output timing reference level ····· 1/2V_{CC}

Output load

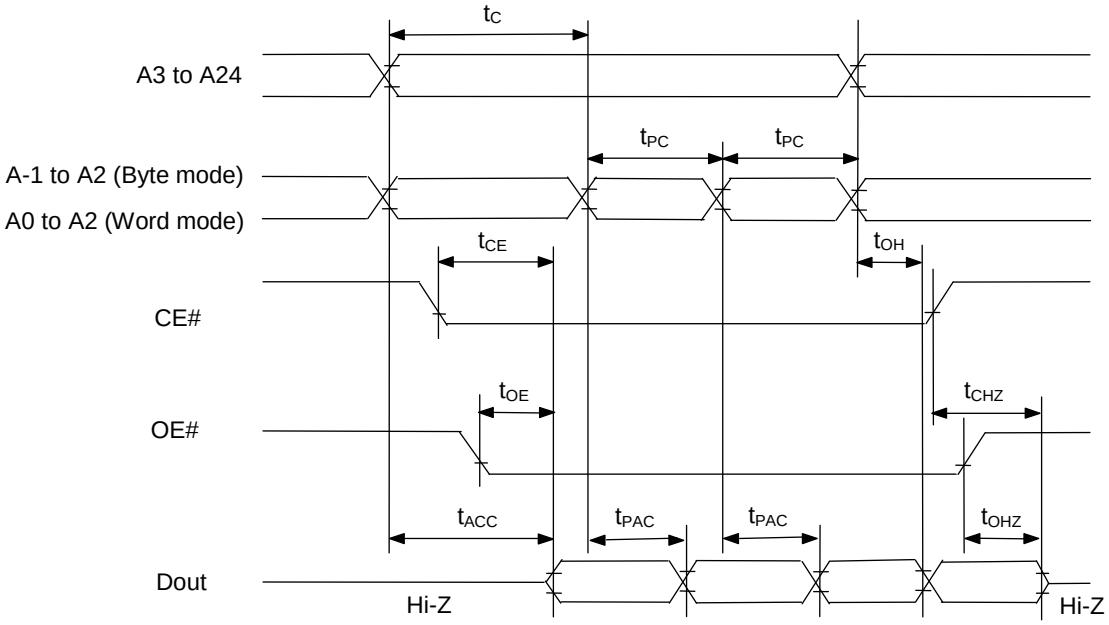


TIMING CHART (READ CYCLE)

Random Access Mode Read Cycle



Page Access Mode Read Cycle

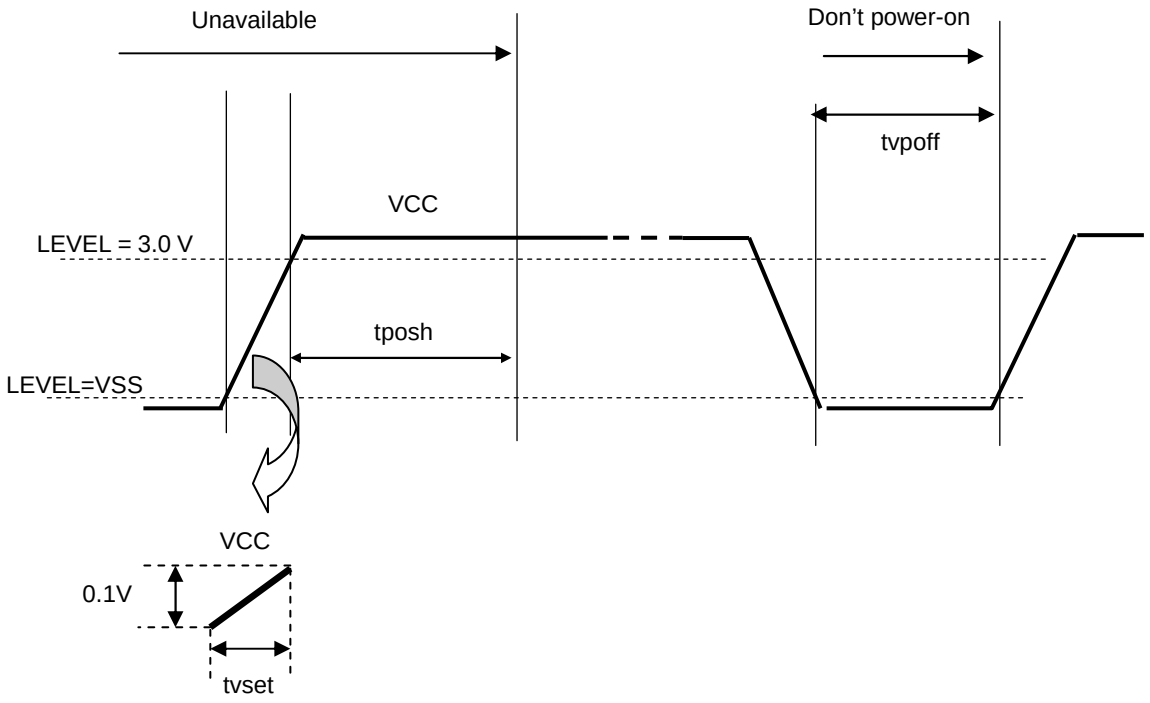


POWER ON CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
VCC set up time	tvset	—	5	270	us
Power on sequence hold time	tposh	—	1	—	ms
Power off hold time	tvpoff	—	1	—	ms

TIMING CHART (POWER ON)

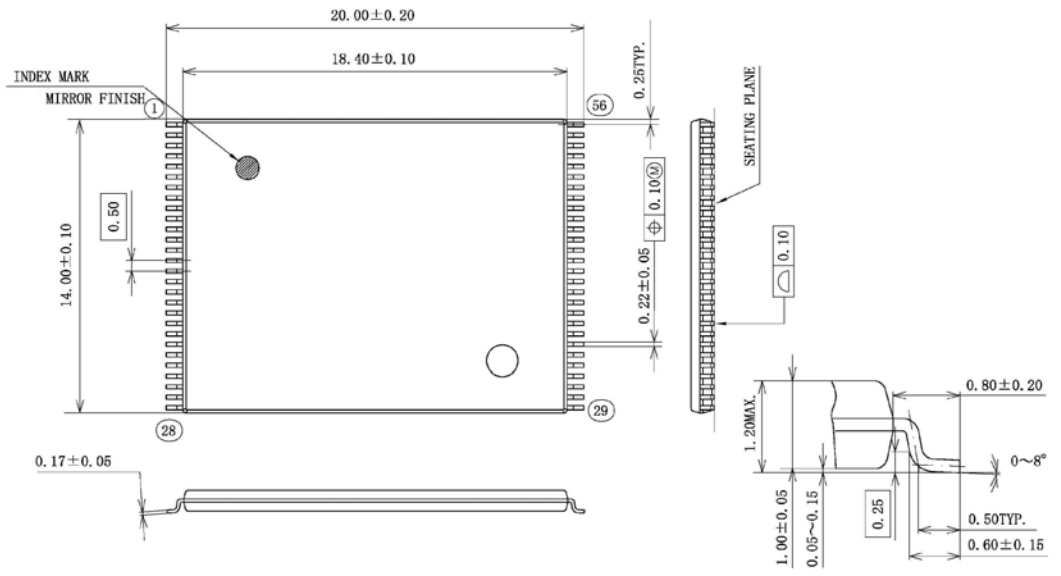


Note: A start-up delay of 1ms is required after power-on.
If you power-off VCC ,you must wait 1ms to power-on.
CE# must be HIGH while VCC power on sequence.

PACKAGE DIMENSIONS

(Unit: mm)

P-TSOP(1)56-1420-0.50-K-MC



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.67 TYP.
Rev. No./Last Revised	1/Aug. 9, 2007

LAPIS Semiconductor Co.,Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR26V51252R-01-01	June 24, 2008	–	–	Final edition 1
FEDR26V51252R-01-02	Aug 29, 2008	1 7	1 7	Correct PACKAGE code Replaced package diagram
FEDR26V51252R-002-02	Oct. 1, 2008	–	–	Changed company logo and name to OKI SEMICONDUCTOR

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