LAPIS
SEMICONDUCTOR

MR27T1602L

1M–Word × 16–Bit or 2M–Word × 8–Bit P2ROM

FEATURES

· 1,048,576-word × 16-bit / 2,097,152-word × 8-bit electrically switchable configuration
· +2.7 V to 3.6 V power supply
· Access time   70 ns MAX
· Operating current   16 mA MAX (5MHz)
· Standby current   10 μA MAX
· Input/Output TTL compatible
· Three-state output

Packages
· MR27T1602L-xxxMA
        44-pin plastic SOP (SOP44-P-600-1.27-K)
· MR27T1602L-xxxTN
        48-pin plastic TSOP (TSOP I 48-P-1220-0.50-1K)
· MR27T1602L-xxxLA
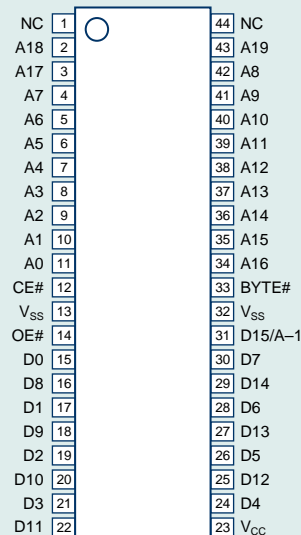   48-ball BGA (BGA48-6.0x8.0-0.8)

P2ROM ADVANCED TECHNOLOGY

P2ROM stands for Production Programmed ROM. This exclusive LAPIS Semiconductor technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing.
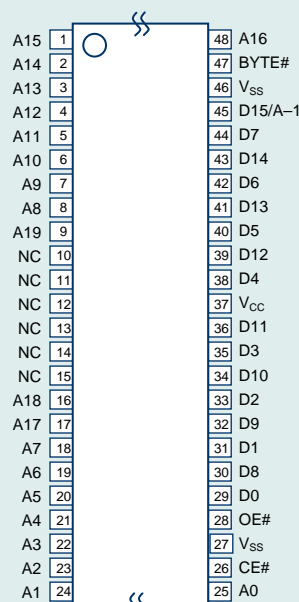
Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

· **Short lead time**, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
· **No mask charge**, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
· **No additional programming charge,** unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
· **Custom Marking is** available at no additional charge.
· **Pin Compatible with Mask ROM** and some FLASH product
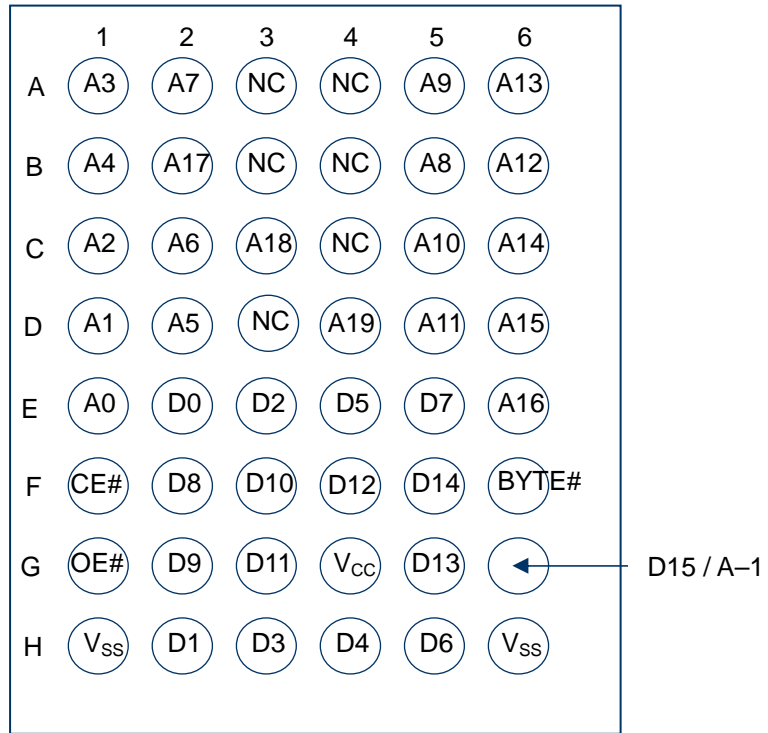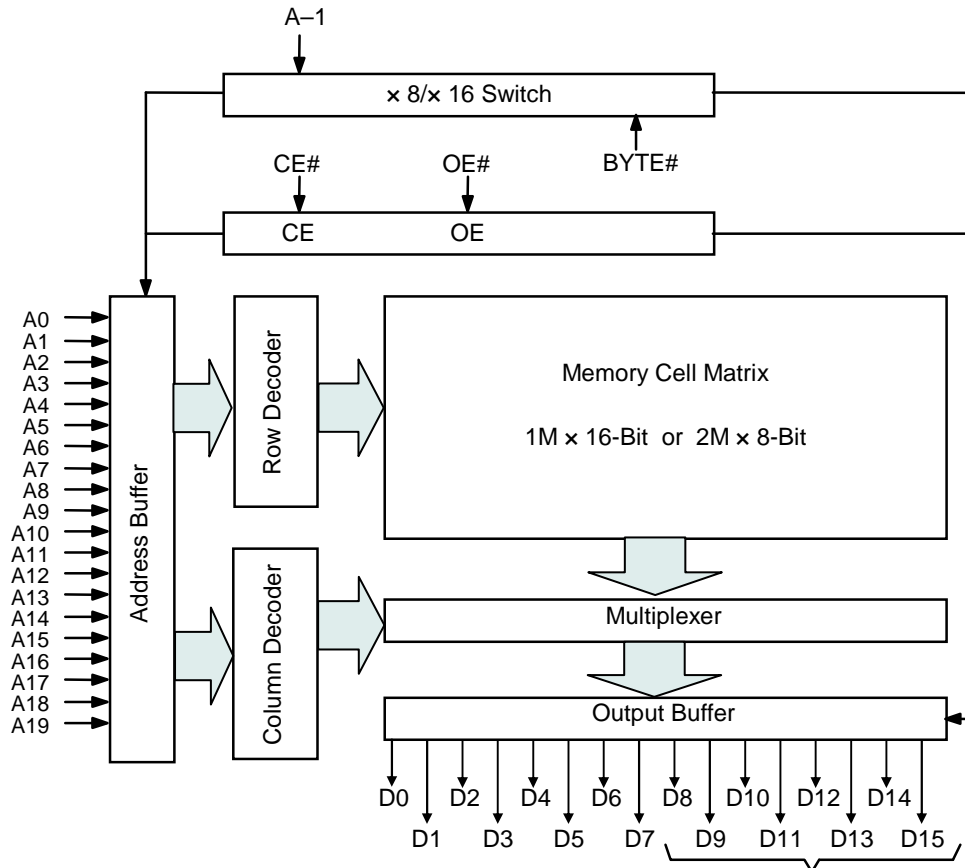
PIN CONFIGURATION (TOP VIEW)

	44SOP	
NC	1	44 NC
A18	2	43 A19
A17	3	42 A8
A7	4	41 A9
A6	5	40 A10
A5	6	39 A11
A4	7	38 A12
A3	8	37 A13
A2	9	36 A14
A1	10	35 A15
A0	11	34 A16
CE#	12	33 BYTE#
V_{SS}	13	32 V_{SS}
OE#	14	31 D15/A−1
D0	15	30 D7
D8	16	29 D14
D1	17	28 D6
D9	18	27 D13
D2	19	26 D5
D10	20	25 D12
D3	21	24 D4
D11	22	23 V_{CC}

44SOP

	48TSOP(Type-I)	
A15	1	48 A16
A14	2	47 BYTE#
A13	3	46 V_{SS}
A12	4	45 D15/A−1
A11	5	44 D7
A10	6	43 D14
A9	7	42 D6
A8	8	41 D13
A19	9	40 D5
NC	10	39 D12
NC	11	38 D4
NC	12	37 V_{CC}
NC	13	36 D11
NC	14	35 D3
NC	15	34 D10
A18	16	33 D2
A17	17	32 D9
A7	18	31 D1
A6	19	30 D8
A5	20	29 D0
A4	21	28 OE#
A3	22	27 V_{SS}
A2	23	26 CE#
A1	24	25 A0

48TSOP(Type-I)

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PIN CONFIGURATION (TOP VIEW): BGA PACKAGES

TOP View - Ball Side Down

	1	2	3	4	5	6
A	A3	A7	NC	NC	A9	A13
B	A4	A17	NC	NC	A8	A12
C	A2	A6	A18	NC	A10	A14
D	A1	A5	NC	A19	A11	A15
E	A0	D0	D2	D5	D7	A16
F	CE#	D8	D10	D12	D14	BYTE#
G	OE#	D9	D11	V_{CC}	D13	← D15 / A−1
H	V_{SS}	D1	D3	D4	D6	V_{SS}

48-ball BGA

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BLOCK DIAGRAM

In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

PIN DESCRIPTIONS

Pin name	Functions
D15 / A–1	Data output / Address input
A0 to A19	Address inputs
D0 to D14	Data outputs
CE#	Chip enable input
OE#	Output enable input
BYTE#	Word / Byte select input
V_{CC}	Power supply voltage
V_{SS}	Ground
NC	No connect

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FUNCTION TABLE

Mode	CE#	OE#	BYTE#	V_{CC}	D0 to D7	D8 to D14	D15/A–1
Read (16-Bit)	L	L	H		D_{OUT}		
Read (8-Bit)	L	L	L		D_{OUT}	Hi–Z	L/H
Output disable	L	H	H	3.0 V	Hi–Z		
			L				*
Standby	H	*	H		Hi–Z		
			L				*

*: Don't Care (H or L)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	Ta	—	0 to 70	°C
Storage temperature	Tstg		−55 to 125	°C
Input voltage	V_I		−0.5 to V_{CC}+0.5	V
Output voltage	V_O	relative to V_{SS}	−0.5 to V_{CC}+0.5	V
Power supply voltage	V_{CC}		−0.5 to 5	V
Power dissipation per package	P_D	Ta = 25°C	1.0	W
Output short circuit current	I_{OS}	—	10	mA

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{CC} power supply voltage	V_{CC}		2.7	—	3.6	V
Input "H" level	V_{IH}	V_{CC} = 2.7 to 3.6 V	2.2	—	V_{CC}+0.5*	V
Input "L" level	V_{IL}		−0.5**	—	0.6	V

Voltage is relative to VSS.
* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.
** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

PIN CAPACITANCE

(V_{CC} = 3.0 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C_{IN1}	V_I = 0 V	—	—	8	
BYTE#	C_{IN2}		—	—	120	pF
Output	C_{OUT}	V_O = 0 V	—	—	10	

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ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = 2.7 V to 3.6 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	V_I = 0 to V_{CC}	—	—	10	μA
Output leakage current	I_{LO}	V_O = 0 to V_{CC}	—	—	10	μA
V_{CC} power supply current (Standby)	I_{CCSC}	CE# = V_{CC}	—	—	10	μA
	I_{CCST}	CE# = V_{IH}	—	—	1	mA
V_{CC} power supply current (Read)	I_{CCA}	CE# = V_{IL}, OE# = V_{IH} f=5MHz	—	—	16	mA
Input "H" level	V_{IH}	—	2.2	—	V_{CC}+0.5∗	V
Input "L" level	V_{IL}	—	−0.5∗∗	—	0.6	V
Output "H" level	V_{OH}	I_{OH} = −1 mA	2.4	—	—	V
Output "L" level	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V

Voltage is relative to V_{SS}.

∗ : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

∗∗ : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

AC Characteristics

(V_{CC} = 2.7 V to 3.6 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	t_C	—	70	—	ns
Address access time	t_{ACC}	CE# = OE# = V_{IL}	—	70	ns
CE# access time	t_{CE}	OE# = V_{IL}	—	70	ns
OE# access time	t_{OE}	CE# = V_{IL}	—	25	ns
Output disable time	t_{CHZ}	OE# = V_{IL}	0	30	ns
	t_{OHZ}	CE# = V_{IL}	0	25	ns
Output hold time	t_{OH}	CE# = OE# = V_{IL}	0	—	ns

Measurement conditions

    Input signal level----------------------------------- 0 V / Vcc
    Input timing reference level --------------------- 1/2 Vcc
    Output load-- 50 pF
    Output timing reference level-------------------- 1/2 Vcc

Output load

        Output ○——

                 50 pF

                 (Including scope and jig)

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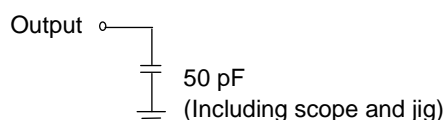
TIMING CHART (READ CYCLE)

16-Bit Read Mode (BYTE# = V_{IH})

8-Bit Read Mode (BYTE# = V_{IL})

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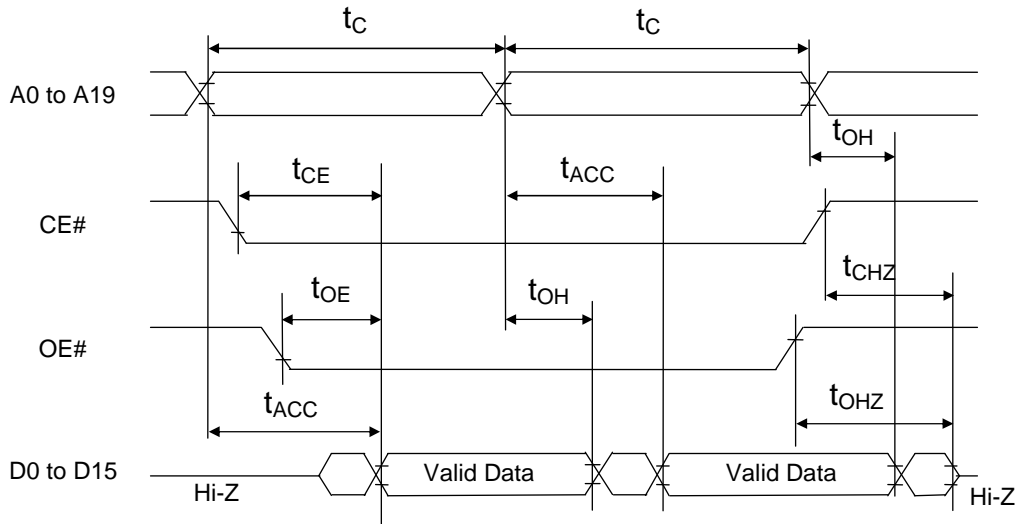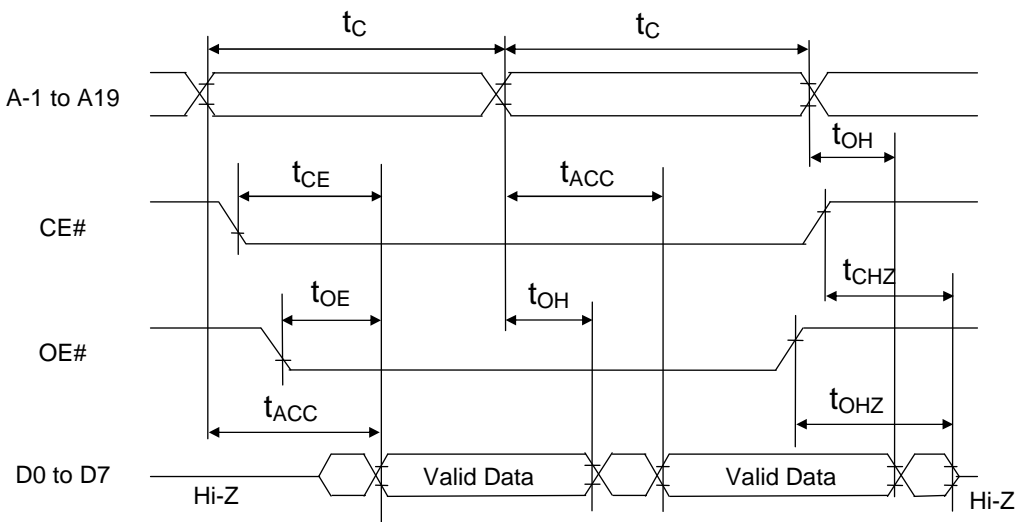
PACKAGE DIMENSIONS

(Unit: mm)

SOP44-P-600-1.27-K

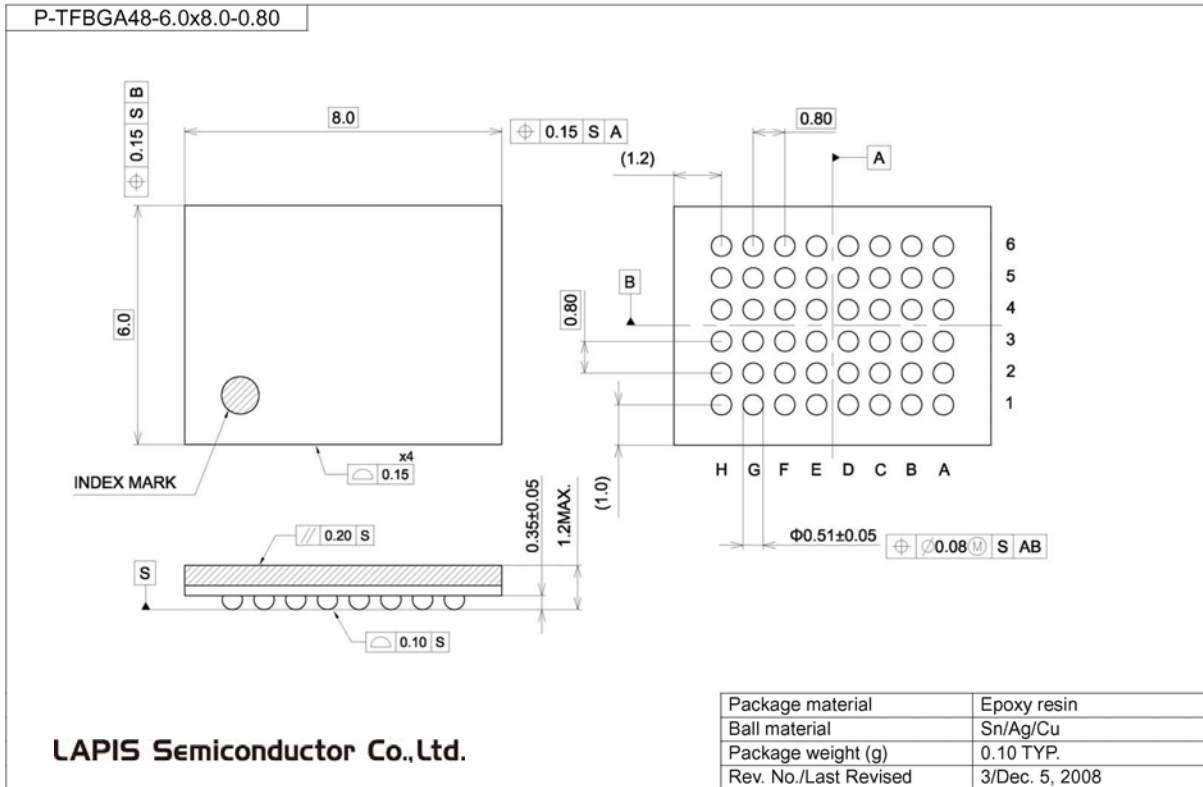| Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	2.10 TYP.
Rev. No./Last Revised	2/Oct. 10, 2008

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Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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(Unit: mm)

TSOP I 48-P-1220-0.50-1K

Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	1/Aug. 10, 2007

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Notes for Mounting the Surface Mount Type Package

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perature and times).

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(Unit: mm)

P-TFBGA48-6.0x8.0-0.80

Package material	Epoxy resin
Ball material	Sn/Ag/Cu
Package weight (g)	0.10 TYP.
Rev. No./Last Revised	3/Dec. 5, 2008

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Notes for Mounting the Surface Mount Type Package

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REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR27T1602L-02-01	Dec. 08, 2004	–	–	Final edition 1
FEDR27T1602L-002-02	Oct. 30, 2008	1, 5	1, 5	Change tC, tACC, tCE to 70ns Change tOE to 25ns Change tCHZ, tOHZ to 20ns
		5	5	Changed Input signal level from "0V/3V" to "0V/Vcc"
		–	–	Changed company logo and name to OKI SEMICONDUCTOR
FEDR27T1602L-002-03	Jan.6, 2009	1	1,2,7,9	Add MR27T1602L-xxxMA(44SOP package)/ MR27T1602L-xxxLA (BGA package)

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