

MR27T25603L

16M-Word x 16-Bit or 32M-Word x 8-Bit P2ROM

FEATURES

- \cdot 16,777,216-word \times 16-bit/33,554,432-word \times 8-bit electrically switchable configuration
- \cdot Access time
- 2.7 V to 3.6 V power supply......120 ns MAX
- 3.0 V to 3.6 V power supply......100 ns MAX
- \cdot Operating current35 mA MAX(5MHz)
- Input/Output TTL compatible
- \cdot Three-state output

PACKAGES

• MR27T25603L-xxxTM 50-pin plastic TSOP (TSOP(2)50-P-400-0.80-K)

P2ROM ADVANCED TECHNOLOGY

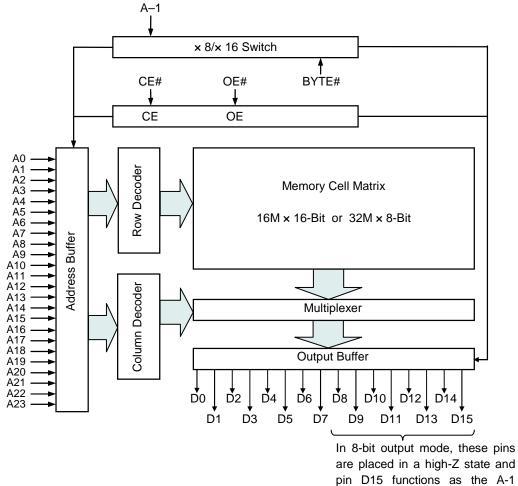
P2ROM stands for Production Programmed ROM. This exclusive LAPIS Semiconductor technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing.

Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

- Short lead time, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
- No mask charge, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
- No additional programming charge, unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
- · Custom Marking is available at no additional charge.

A11 1 A10 2 A9 3 A8 4 A7 5 A6 6 A5 7 A4 8 A3 9 A2 10 A1 11 A23 12 GND 13 BYTE# 14 A0 15 D0 16 D8 17 D1 18 D9 19 Vcc 20 D1 22 D10 22 D10 22 GND 12 A1 124 GND 125	50TSOP (Type2)	50) (TOP VIEW) 50) CE# 49 A12 49 A12 49 A13 47 A14 46 A15 45 Vcc 44 A16 43 A17 42 A18 41 A19 40 A20 39 A21 38 GND 37 A22 38 NC 35 OE# 34 D15/A-1 33 D7 32 D14 31 D6 30 D13 29 D5 28 D12 27 D4 28 Vcc
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BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin name	Functions			
D15 / A–1	Data output / Address input			
A0 to A23	Address inputs			
D0 to D14	Data outputs			
CE#	Chip enable input			
OE#	Output enable input			
BYTE#	Word / Byte select input			
V _{CC}	Power supply voltage			
V _{SS}	Ground			

address pin.

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MR27T25603L / P2ROM

FUNCTION TABLE

Mode	CE#	OE#	BYTE#	V _{CC}	D0 to D7	D8 to D14	D15/A–1
Read (16-Bit)	L	L	Н			Dout	
Read (8-Bit)	L	L	L	2.7 V	Dout	Hi–Z	L/H
Output disable		Н	Н			Hi–Z	_
Output disable	L	п	L	to 3.6 V			*
Standby	н *		Н	3.0 V			
Standby	Н	*	L			Hi–Z	

*: Don't Care (H or L)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	Та		0 to 70	°C
Storage temperature	Tstg	_	-55 to 125	°C
Input voltage	VI		-0.5 to V _{CC} +0.5	V
Output voltage	Vo	Relative to V _{SS}	-0.5 to V _{CC} +0.5	V
Power supply voltage	Vcc		-0.5 to 5	V
Power dissipation per package	PD	Ta = 25°C	1.0	W
Output short circuit current	I _{OS}	_	10	mA

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C)

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Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
V _{CC} power supply voltage	Vcc		2.7	—	3.6	V
Input "H" level	V _{IH}	$V_{CC} = 2.7$ to 3.6 V	2.2	_	V _{CC} +0.5*	V
Input "L" level	VIL		-0.5**	_	0.6	V

Voltage is relative to V_{SS} .

* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

PIN CAPACITANCE

				$(V_{CC} = 3)$	$0 V$, $1a = 25^{\circ}$	C, T = T MHZ)
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input	C _{IN1}	$V_1 = 0 V$	_	_	10	
BYTE#	C _{IN2}	$v_1 = 0 v$	—	—	200	pF
Output	COUT	$V_0 = 0 V$	_	_	10	

(V_{CC} = 3.0 V, Ta = 25°C, f = 1 MHz)

ELECTRICAL CHARACTERISTICS

DC Characteristics

				$(V_{CC} = 2.7)$	to 3.6 V, Ta	= 0 to 70°C)
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input leakage current	ILI	$V_I = 0$ to V_{CC}	—	—	5	μA
Output leakage current	ILO	$V_0 = 0$ to V_{CC}	_	_	5	μA
V _{CC} power supply current	Iccsc	$CE\# = V_{CC}$	_	_	10	μA
(Standby)	I _{CCST}	$CE\# = V_{IH}$	_	_	1	mA
V _{CC} power supply current (Read)	I _{CCA}	$CE\# = V_{IL}, OE\# = V_{IH}$ $f=5MHz$			35	mA
Input "H" level	VIH	—	2.2	—	V _{CC} +0.5*	V
Input "L" level	VIL	—	-0.5**	—	0.6	V
Output "H" level	V _{OH}	$I_{OH} = -1 \text{ mA}$	2.4	_	_	V
Output "L" level	V _{OL}	$I_{OL} = 2 \text{ mA}$	_	_	0.4	V

Voltage is relative to VSS.

* : Vcc+1.5 V(Max.) when pulse width of overshoot is less than 10 ns.

** : -1.5 V(Min.) when pulse width of undershoot is less than 10 ns.

AC Characteristics

$(V_{CC} = 2.7 \text{ to } 3.6 \text{ V}, \text{ Ta} = 0 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	tc	—	120	—	ns
Address access time	t _{ACC}	$CE\# = OE\# = V_{IL}$	—	120	ns
CE# access time	t _{CE}	$OE\# = V_{IL}$	—	120	ns
OE# access time	t _{OE}	$CE\# = V_{IL}$	—	30	ns
Output disable time	t _{CHZ}	$OE\# = V_{IL}$	0	20	ns
	t _{OHZ}	$CE\# = V_{IL}$	0	20	ns
Output hold time	t _{OH}	$CE\# = OE\# = V_{IL}$	0	—	ns

$(V_{CC} = 3.0 \text{ to } 3.6 \text{ V}, \text{ Ta} = 0 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	t _C		100		ns
Address access time	t _{ACC}	$CE\# = OE\# = V_{IL}$	_	100	ns
CE# access time	t _{CE}	$OE\# = V_{IL}$	—	100	ns
OE# access time	t _{OE}	$CE\# = V_{IL}$	—	30	ns
Output disable time	t _{CHZ}	$OE\# = V_{IL}$	0	20	ns
	t _{OHZ}	$CE\# = V_{IL}$	0	20	ns
Output hold time	t _{OH}	$CE\# = OE\# = V_{IL}$	0		ns

Measurement conditions

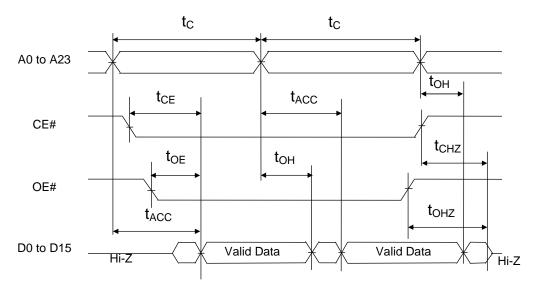
Input signal level 0 V / Vcc
Input timing reference level 1/2Vcc
Output load 50 pF
Output timing reference level 1/2Vcc

Output load

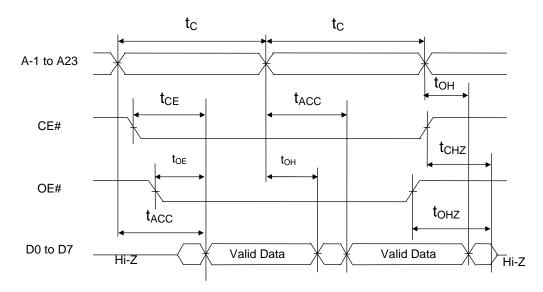
Output \sim _____ 50 pF ____ (Including scope and jig)

TIMING CHART (READ CYCLE)

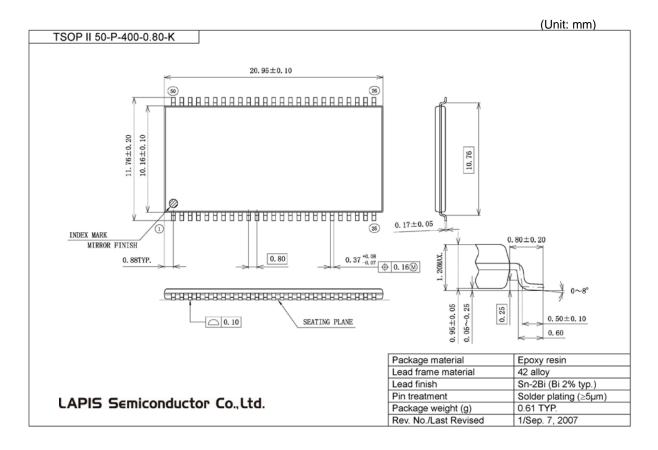
16-Bit Read Mode (BYTE# = V_{IH})



8-Bit Read Mode (BYTE# = VIL)



PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document		PageDatePreviousCurrentEditionEdition		
No.	Date			Description
FEDR27T25603L-02-01	Apr. 1, 2004	-	-	Final edition 1
FEDR27T25603L-02-02	Jun. 8, 2004	3	3	Change C _{IN1} to 10pF
FEDR27T25603L-02-03	Jul. 9, 2004	3 1, 4	3 1, 5	Add P_D condition and I_{OS} = 10mA Add access time 100ns spec.
FEDR27T25603L-02-04	Dec. 8, 2004	1, 8	1	Delete MR27T25603L-xxxMB
FEDR27T25603L-002-05	Oct 1 2008	5	5	Changed Input signal level from "0V/3V" to "0V/Vcc".
FEDR2/123603L-002-05	Oct. 1, 2008	_	-	Changed company logo and name to OKI SEMICONDUCTOR

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