

OKI Semiconductor

FEDR27T6402L-02-01

Issue Date: May. 9, 2005

MR27T6402L

4M-Word × 16-Bit or 8M-Word × 8-Bit P2ROM

FEATURES

- 4,194,304-word × 16-bit / 8,388,608-word × 8-bit electrically switchable configuration
- Access time
 - 2.7 V to 3.6 V power supply 90 ns MAX
 - 3.0 V to 3.6 V power supply 80 ns MAX
- Operating current 20 mA MAX (5MHz)
- Standby current 10 µA MAX
- Input/Output TTL compatible
- Three-state output

PACKAGES

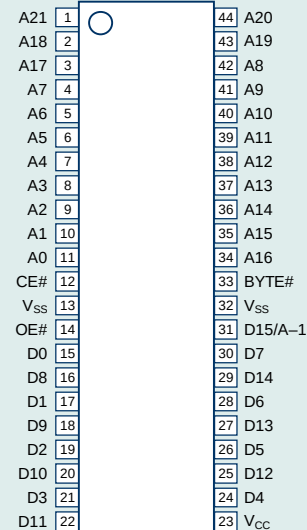
- MR27T6402L-xxxMA
44-pin plastic SOP (SOP44-P-600-1.27-K)
- MR27T6402L-xxxTN
48-pin plastic TSOP (TSOP I 48-P-1220-0.50-1K)

P2ROM ADVANCED TECHNOLOGY

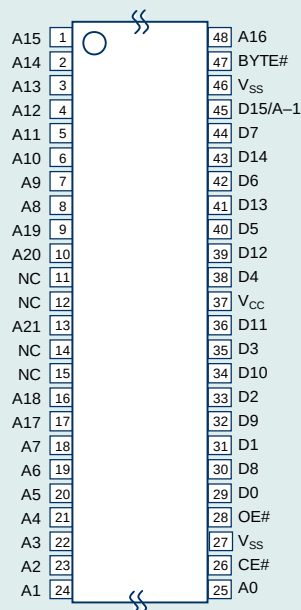
P2ROM stands for Production Programmed ROM. This exclusive Oki technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

- **Short lead time**, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
- **No mask charge**, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
- **No additional programming charge**, unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
- **Custom Marking is** available at no additional charge.
- **Pin Compatible with Mask ROM** and some FLASH products.

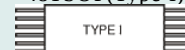
PIN CONFIGURATION (TOP VIEW)



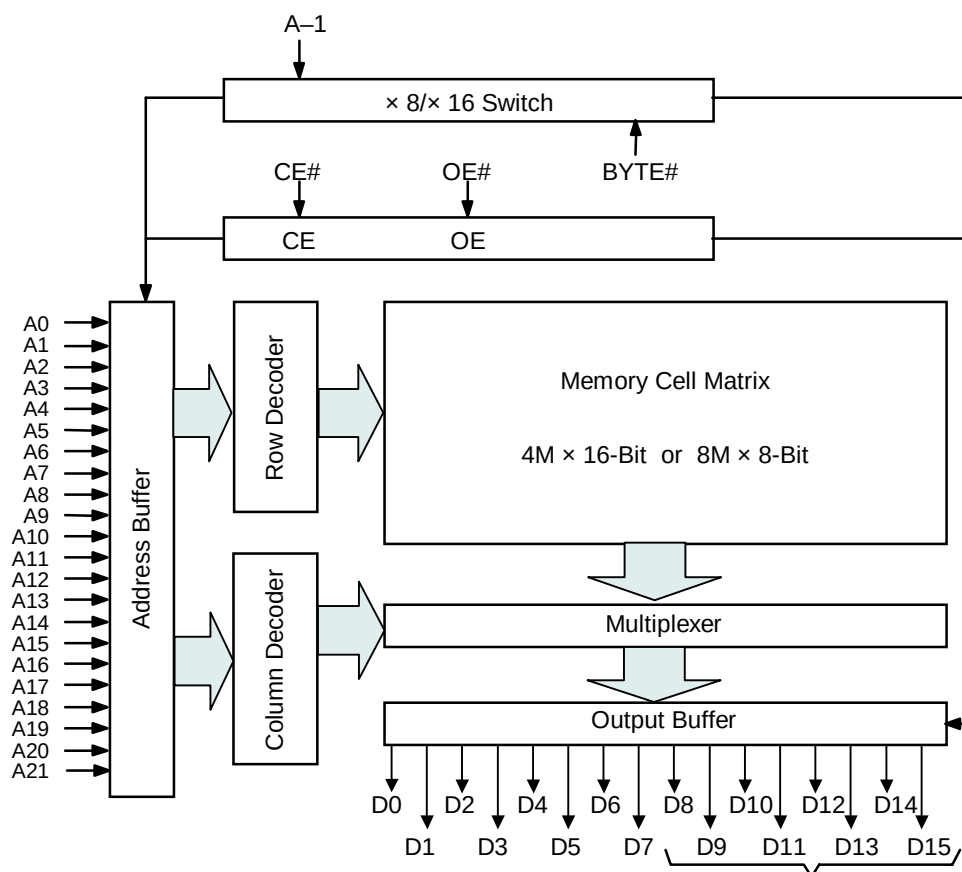
44SOP



48TSOP(Type-I)



BLOCK DIAGRAM



In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

PIN DESCRIPTIONS

Pin name	Functions
D15 / A-1	Data output / Address input
A0 to A21	Address inputs
D0 to D14	Data outputs
CE#	Chip enable input
OE#	Output enable input
BYTE#	Word / Byte select input
V _{CC}	Power supply voltage
V _{SS}	Ground
NC	No connect

FUNCTION TABLE

Mode	CE#	OE#	BYTE#	V _{CC}	D0 to D7	D8 to D14	D15/A–1
Read (16-Bit)	L	L	H	2.7 V to 3.6 V	D _{OUT}		
Read (8-Bit)	L	L	L		D _{OUT}	Hi–Z	L/H
Output disable	L	H	H		Hi–Z		*
			L				
Standby	H	*	H		Hi–Z		*
			L				

*: Don't Care (H or L)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T _a	—	0 to 70	°C
Storage temperature	T _{stg}		-55 to 125	°C
Input voltage	V _I	relative to V _{SS}	-0.5 to V _{CC} +0.5	V
Output voltage	V _O		-0.5 to V _{CC} +0.5	V
Power supply voltage	V _{CC}		-0.5 to 5	V
Power dissipation per package	P _D	T _a = 25°C	1.0	W
Output short circuit current	I _{OS}	—	10	mA

RECOMMENDED OPERATING CONDITIONS

(T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V _{CC} power supply voltage	V _{CC}	V _{CC} = 2.7 to 3.6 V	2.7	—	3.6	V
Input "H" level	V _{IH}		2.2	—	V _{CC} +0.5*	V
Input "L" level	V _{IL}		-0.5**	—	0.6	V

Voltage is relative to V_{SS}.* : V_{CC}+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

PIN CAPACITANCE

(V_{CC} = 3.0 V, T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C _{IN1}	V _I = 0 V	—	—	12	pF
BYTE#	C _{IN2}		—	—	200	
Output	C _{OUT}	V _O = 0 V	—	—	12	

ELECTRICAL CHARACTERISTICS

DC Characteristics

($V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $T_a = 0 \text{ to } 70^\circ\text{C}$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	$V_I = 0 \text{ to } V_{CC}$	—	—	10	μA
Output leakage current	I_{LO}	$V_O = 0 \text{ to } V_{CC}$	—	—	10	μA
V_{CC} power supply current (Standby)	I_{CCSC}	$CE\# = V_{CC}$	—	—	10	μA
	I_{CCST}	$CE\# = V_{IH}$	—	—	1	mA
V_{CC} power supply current (Read)	I_{CCA}	$CE\# = V_{IL}$, $OE\# = V_{IH}$ $f=5\text{MHz}$	—	—	20	mA
Input "H" level	V_{IH}	—	2.2	—	$V_{CC}+0.5^*$	V
Input "L" level	V_{IL}	—	-0.5**	—	0.6	V
Output "H" level	V_{OH}	$I_{OH} = -1 \text{ mA}$	2.4	—	—	V
Output "L" level	V_{OL}	$I_{OL} = 2 \text{ mA}$	—	—	0.4	V

Voltage is relative to V_{SS} .

* : $V_{CC}+1.5\text{V}(\text{Max.})$ when pulse width of overshoot is less than 10ns.

** : $-1.5\text{V}(\text{Min.})$ when pulse width of undershoot is less than 10ns.

AC Characteristics

(V_{CC} = 2.7 V to 3.6 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	t _C	—	90	—	ns
Address access time	t _{ACC}	CE# = OE# = V _{IL}	—	90	ns
CE# access time	t _{CE}	OE# = V _{IL}	—	90	ns
OE# access time	t _{OE}	CE# = V _{IL}	—	30	ns
Output disable time	t _{CHZ}	OE# = V _{IL}	0	30	ns
	t _{OHZ}	CE# = V _{IL}	0	25	ns
Output hold time	t _{OH}	CE# = OE# = V _{IL}	0	—	ns

(V_{CC} = 3.0 V to 3.6 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	t _C	—	80	—	ns
Address access time	t _{ACC}	CE# = OE# = V _{IL}	—	80	ns
CE# access time	t _{CE}	OE# = V _{IL}	—	80	ns
OE# access time	t _{OE}	CE# = V _{IL}	—	30	ns
Output disable time	t _{CHZ}	OE# = V _{IL}	0	20	ns
	t _{OHZ}	CE# = V _{IL}	0	20	ns
Output hold time	t _{OH}	CE# = OE# = V _{IL}	0	—	ns

Measurement conditions

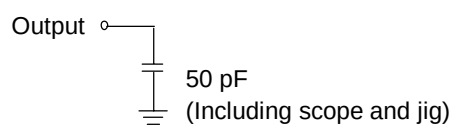
Input signal level ----- 0 V/3 V

Input timing reference level ----- 1/2V_{CC}

Output load ----- 50 pF

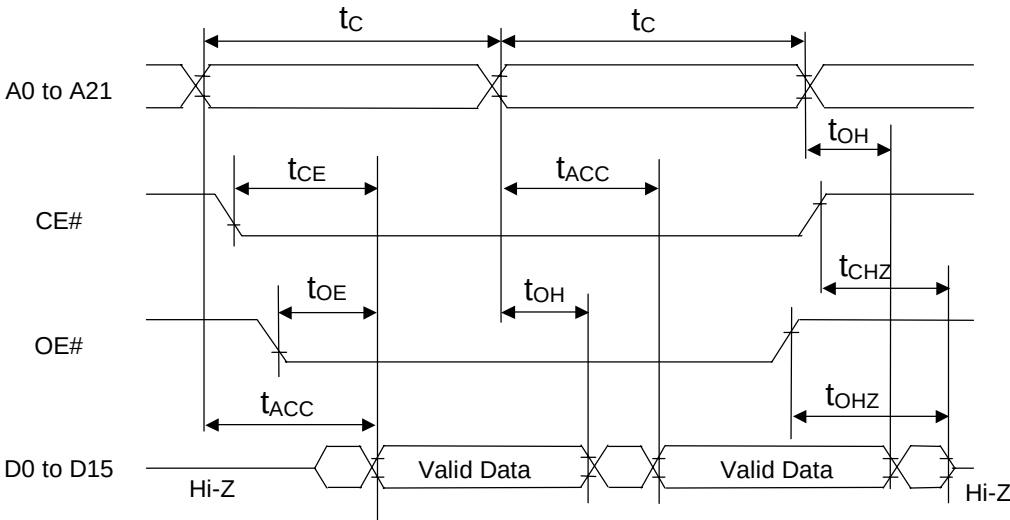
Output timing reference level ----- 1/2V_{CC}

Output load

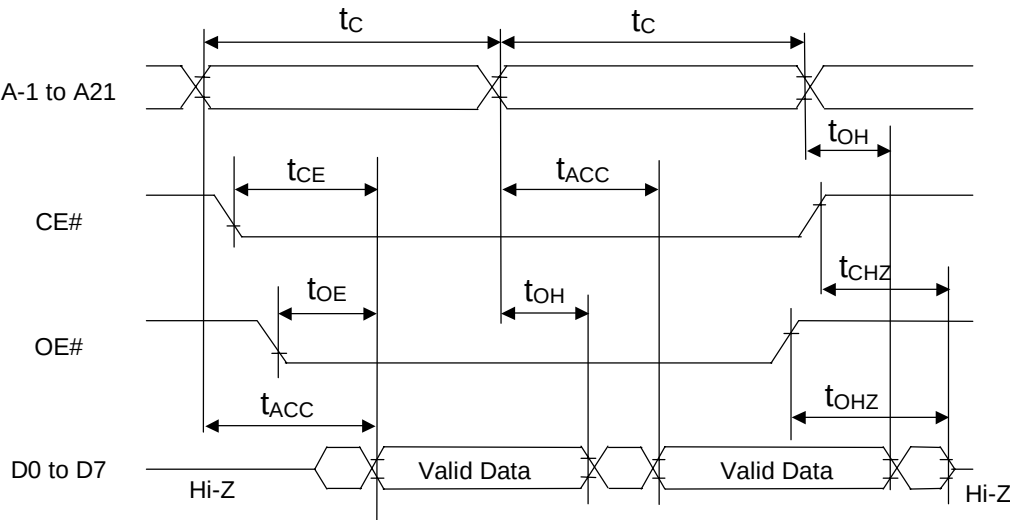


TIMING CHART (READ CYCLE)

16-BIT READ MODE (BYTE# = V_{IH})

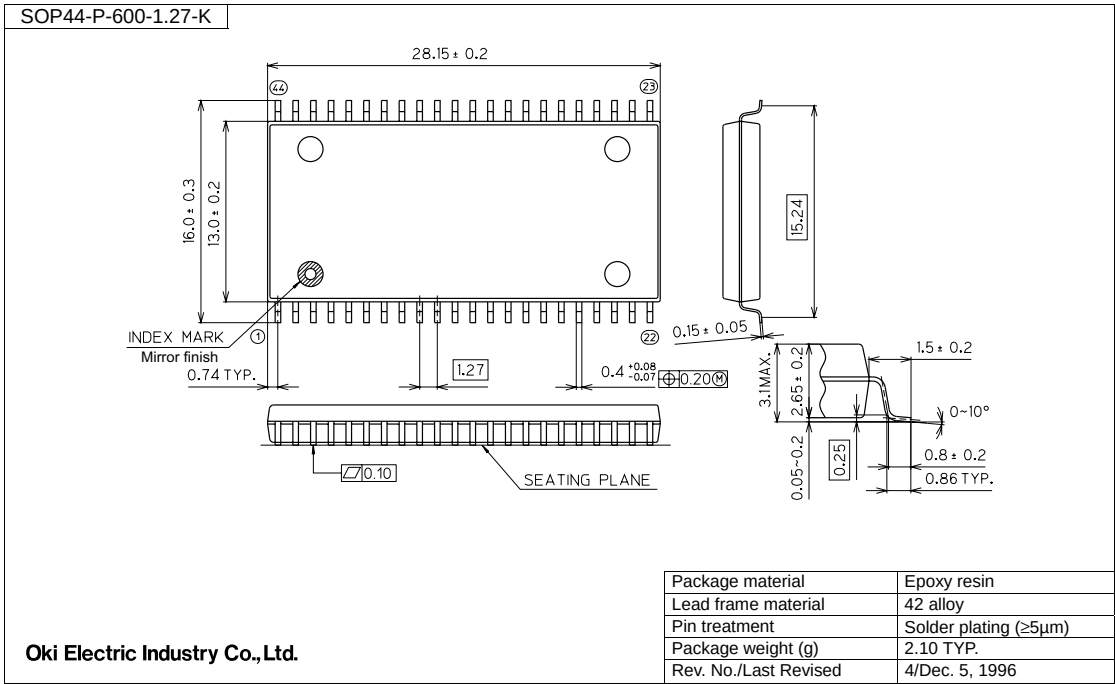


8-BIT READ MODE (BYTE# = V_{IL})



PACKAGE DIMENSIONS

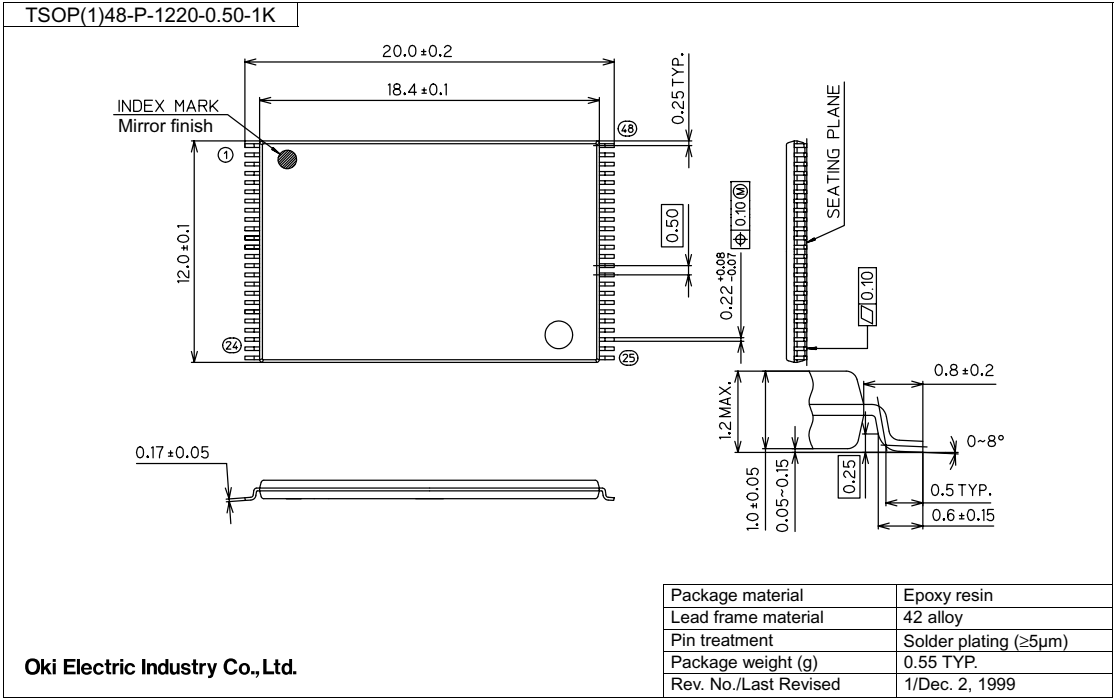
(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)



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REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR27T6402L-02-01	May. 9, 2005	–	–	Final edition 1

NOTICE

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