

# OKI Semiconductor

**FEDR27V12850J-02-03**

Issue Date: Jul. 9, 2004

## MR27V12850J

**8M-Word × 16-Bit or 16M-Word × 8-Bit Page mode P2ROM**

### FEATURES

- 8,388,608-word × 16-bit/16,777,216-word × 8-bit electrically switchable configuration
- Page size of 8-word x 16-Bit or 16-word x 8-Bit
- 3.0 V to 3.6 V power supply
- Access time 100 ns MAX
- Page Access time 25 ns MAX
- Operating current 50 mA MAX(5MHz)
- Standby current 10 μA MAX
- Input/Output TTL compatible
- Three-state output

### PACKAGES

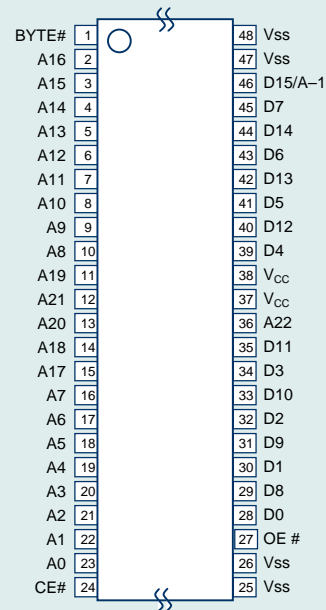
- MR27V12850J-xxxTN  
48-pin plastic TSOP (TSOP I 48-P-1220-0.50-1K)

### P2ROM ADVANCED TECHNOLOGY

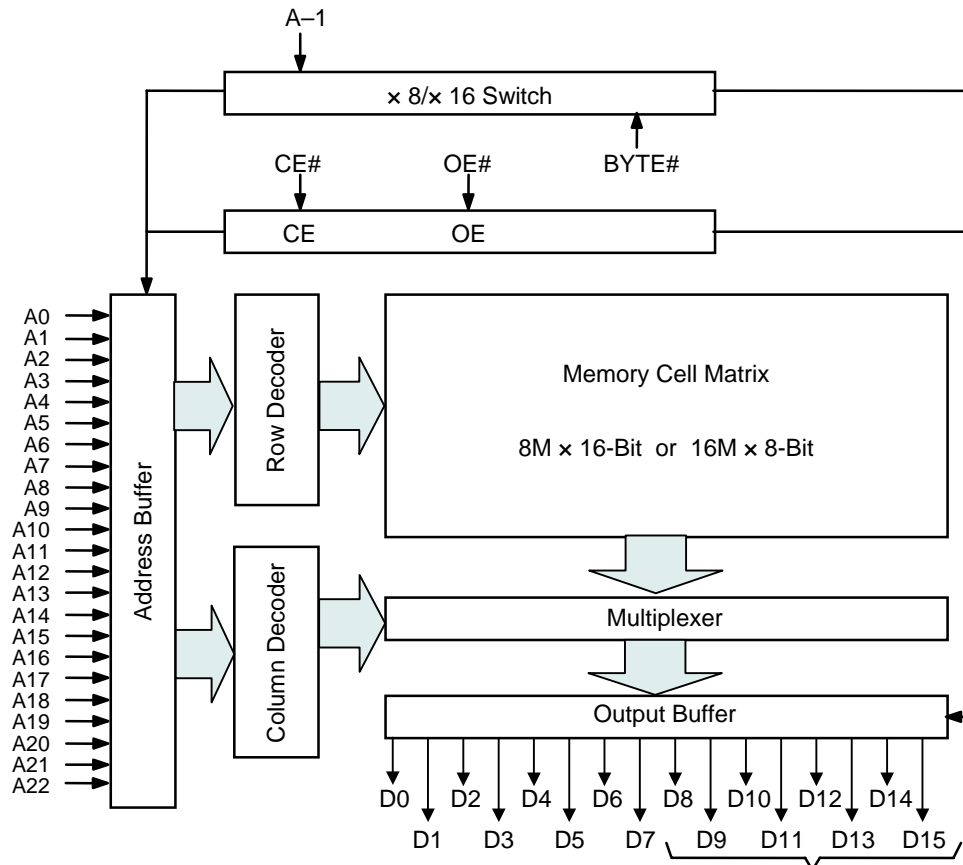
P2ROM stands for Production Programmed ROM. This exclusive Oki technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

- **Short lead time**, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
- **No mask charge**, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
- **No additional programming charge**, unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
- **Custom Marking is** available at no additional charge.
- **Pin Compatible with Mask ROM**

### PIN CONFIGURATION (TOP VIEW)

**48TSOP(Type-I)**

## BLOCK DIAGRAM



In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

## PIN DESCRIPTIONS

Pin name	Functions
D15 / A-1	Data output / Address input
A0 to A22	Address inputs
D0 to D14	Data outputs
CE#	Chip enable input
OE#	Output enable input
BYTE#	Word / Byte select input
V <sub>CC</sub>	Power supply voltage
V <sub>SS</sub>	Ground

## FUNCTION TABLE

Mode	CE#	OE#	BYTE#	V <sub>CC</sub>	D0 to D7	D8 to D14	D15/A-1
Read (16-Bit)	L	L	H	3.0 V to 3.6 V	D <sub>OUT</sub>		
Read (8-Bit)	L	L	L		D <sub>OUT</sub>	Hi-Z	L/H
Output disable	L	H	H		Hi-Z		
			L		*		
Standby	H	*	H		Hi-Z		
			L		*		

\*: Don't Care (H or L)

## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T <sub>a</sub>	—	0 to 70	°C
Storage temperature	T <sub>stg</sub>		-55 to 125	°C
Input voltage	V <sub>I</sub>	relative to V <sub>SS</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Output voltage	V <sub>O</sub>		-0.5 to V <sub>CC</sub> +0.5	V
Power supply voltage	V <sub>CC</sub>		-0.5 to 5	V
Power dissipation per package	P <sub>D</sub>	T <sub>a</sub> = 25°C	1.0	W
Output short circuit current	I <sub>OS</sub>	—	10	mA

## RECOMMENDED OPERATING CONDITIONS

(T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V <sub>CC</sub> power supply voltage	V <sub>CC</sub>	V <sub>CC</sub> = 3.0 to 3.6 V	3.0	—	3.6	V
Input "H" level	V <sub>IH</sub>		2.2	—	V <sub>CC</sub> +0.5*	V
Input "L" level	V <sub>IL</sub>		-0.5**	—	0.6	V

Voltage is relative to V<sub>SS</sub>.

\* : V<sub>CC</sub>+1.5V(Max.) when pulse width of overshoot is less than 10ns.

\*\* : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

## PIN CAPACITANCE

(V<sub>CC</sub> = 3.0 V, T<sub>a</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C <sub>IN1</sub>	V <sub>I</sub> = 0 V	—	—	8	pF
BYTE#	C <sub>IN2</sub>		—	—	200	
Output	C <sub>OUT</sub>	V <sub>O</sub> = 0 V	—	—	10	

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

(V<sub>CC</sub> = 3.0 to 3.6 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I <sub>LI</sub>	V <sub>I</sub> = 0 to V <sub>CC</sub>	—	—	5	μA
Output leakage current	I <sub>LO</sub>	V <sub>O</sub> = 0 to V <sub>CC</sub>	—	—	5	μA
V <sub>CC</sub> power supply current (Standby)	I <sub>CCSC</sub>	CE# = V <sub>CC</sub>	—	—	10	μA
	I <sub>CCST</sub>	CE# = V <sub>IH</sub>	—	—	1	mA
V <sub>CC</sub> power supply current (Read)	I <sub>CCA</sub>	CE# = V <sub>IL</sub> , OE# = V <sub>IH</sub> f=5MHz	—	—	50	mA
Input "H" level	V <sub>IH</sub>	—	2.2	—	V <sub>CC</sub> +0.5*	V
Input "L" level	V <sub>IL</sub>	—	-0.5**	—	0.6	V
Output "H" level	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	2.4	—	—	V
Output "L" level	V <sub>OL</sub>	I <sub>OL</sub> = 2 mA	—	—	0.4	V

Voltage is relative to V<sub>SS</sub>.\* : V<sub>CC</sub>+1.5V(Max.) when pulse width of overshoot is less than 10ns.

\*\* : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

### AC Characteristics

(V<sub>CC</sub> = 3.0 to 3.6 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	t <sub>C</sub>	—	100	—	ns
Address access time	t <sub>ACC</sub>	CE# = OE# = V <sub>IL</sub>	—	100	ns
Page cycle time	t <sub>PC</sub>	—	25	—	ns
Page access time	t <sub>PAC</sub>	—	—	25	ns
CE# access time	t <sub>CE</sub>	OE# = V <sub>IL</sub>	—	100	ns
OE# access time	t <sub>OE</sub>	CE# = V <sub>IL</sub>	—	30	ns
Output disable time	t <sub>CHZ</sub>	OE# = V <sub>IL</sub>	0	20	ns
	t <sub>OHZ</sub>	CE# = V <sub>IL</sub>	0	20	ns
Output hold time	t <sub>OH</sub>	CE# = OE# = V <sub>IL</sub>	0	—	ns

#### Measurement conditions

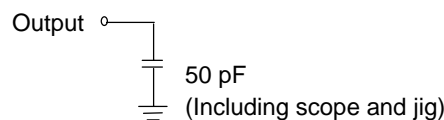
Input signal level ----- 0 V/3 V

Input timing reference level----- 1/2V<sub>CC</sub>

Output load ----- 50 pF

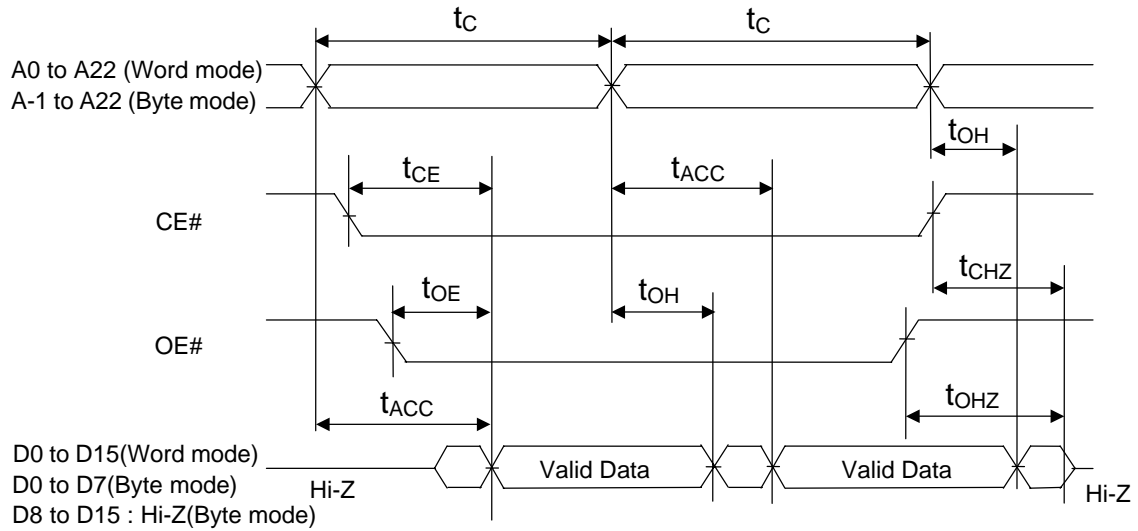
Output timing reference level ----- 1/2V<sub>CC</sub>

#### Output load

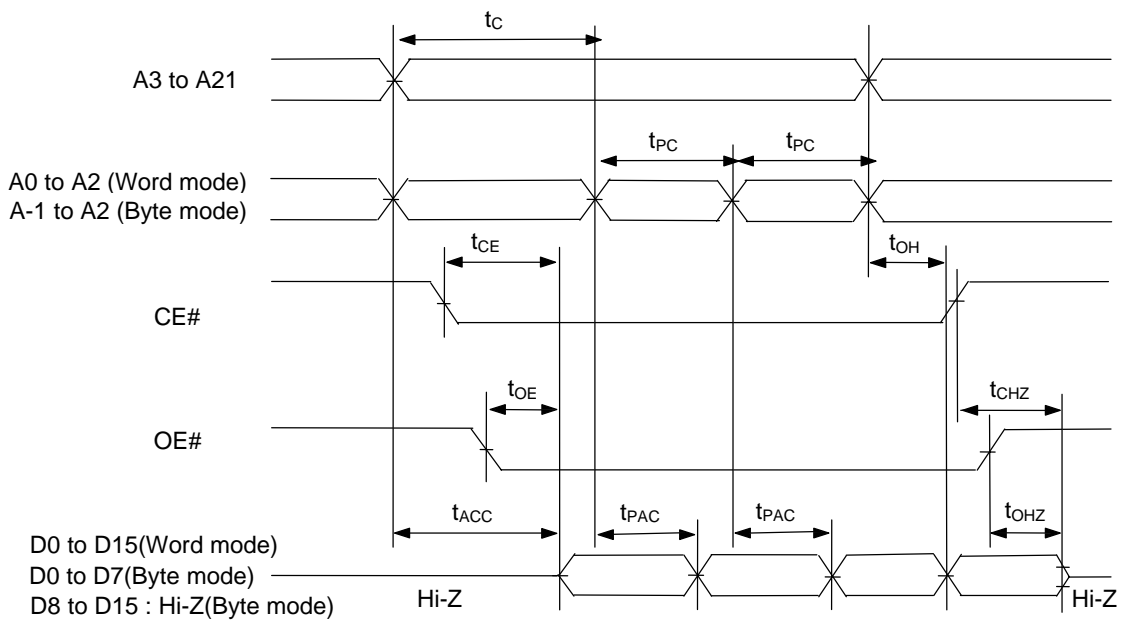


**TIMING CHART (READ CYCLE)**

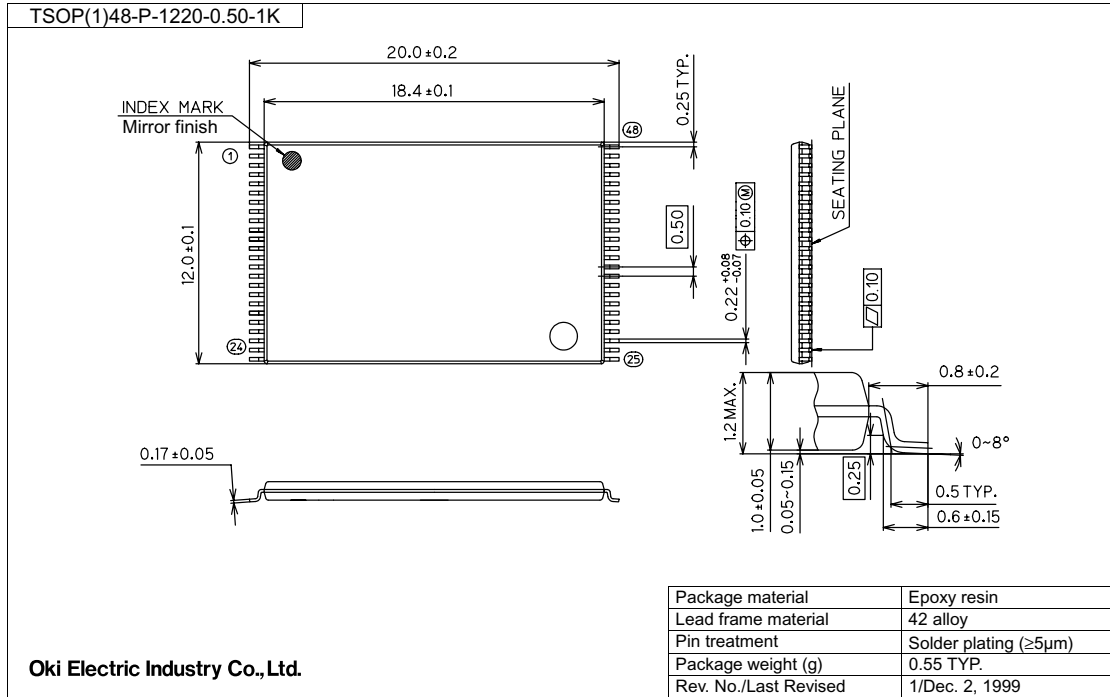
**RANDOM ACCESS MODE READ CYCLE**



**PAGE ACCESS MODE READ CYCLE**



(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

**REVISION HISTORY**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR27V12850J-02-01	Dec., 2002	–	–	Final edition 1
FEDR27V12850J-02-02	Jun. 4, 2003	1	1	Change 48TSOP(1) package code to –1K
FEDR27V12850J-02-03	Jul. 9, 2004	3	3	Add P <sub>D</sub> condition and I <sub>OS</sub> = 10mA

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