

MR27V1641L

16M-Word × 1-Bit Serial Production Programmed ROM (P2ROM)

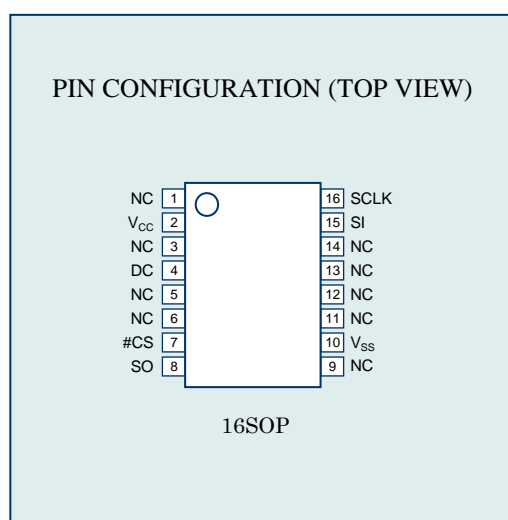
GENERAL DESCRIPTION

The MR27V1641L is a 16 Mbit Production Programmed Read-Only Memory, which is configured as 16,777,216 word × 1-bit. The MR27V1641L supports a simple read operation using a single 3.3V power supply and a Serial Peripheral Interface (SPI) compatible serial bus.

The MR27V1641L have data programmed and have functions tested at LAPIS Semiconductor factory. (Using the DC pins for the programming function is NOT allowed.)

FEATURES

- 16,777,216-word × 1-bit configuration
- +3.0 V to 3.6 V power supply
- Access time 33 MHz serial clock (FAST-READ)
 20 MHz serial clock (READ)
- Read Identification Instruction
- Active read current 25 mA MAX (FAST-READ)
 20 mA MAX (READ)
- Standby current 50 μA MAX
- Serial Clock Input and Data Input/Output
- Input Data Format
 - 1-byte command code, 3-byte address, 1-byte dummy (FAST-READ)
 - 1-byte command code, 3-byte address (READ)



PACKAGES

- MR27V1641L-xxxMP
16-pin plastic SOP (P-SOP16-375-1.27-K)

PIN DESCRIPTIONS

Pin name	Functions
#CS	Chip Select
SI	Serial Data Input
SO	Serial Data Output
SCLK	Clock Input
V _{CC}	Power supply voltage
V _{SS}	Ground
DC	Don't care (0v - V _{CC}) <for reference> Program power supply voltage V _{pp} under Programming operation
NC	No connection

READ COMMAND DEFINITION

Command	Read Array (byte)	Note
1st	03[H]	1
2nd	AD1	2
3rd	AD2	2
4th	AD3	2
Action	N byte read out until #CS goes high	3

Note:

1. The 1st command 03[H] is a Read command
2. AD1 to AD3 are address input data
3. Data output

Details of Command are shown as follows.

1-byte command code									
READ:	0	0	0	0	0	0	0	1	1
3-byte address									
AD1:	X	X	X	A20	A19	A18	A17	A16	
AD2:	A15	A14	A13	A12	A11	A10	A9	A8	
AD3:	A7	A6	A5	A4	A3	A2	A1	A0	

Note:

X: Dummy bit

FAST-READ COMMAND DEFINITION

Command	Read Array (byte)	Note
1st	0B[H]	1
2nd	AD1	2
3rd	AD2	2
4th	AD3	2
5th	X	3
Action	N byte read out until #CS goes high	4

Note:

1. The 1st command 0B[H] is a Read command
2. AD1 to AD3 are address input data
3. X is a dummy cycle
4. Data output

Details of Command are shown as follows.

1-byte command code								
FAST-READ:	0	0	0	0	1	0	1	1
3-byte address								
AD1:	X	X	X	A20	A19	A18	A17	A16
AD2:	A15	A14	A13	A12	A11	A10	A9	A8
AD3:	A7	A6	A5	A4	A3	A2	A1	A0

Note:

X: Dummy bit

READ IDENTIFICATION COMMAND DEFINITION

Command	Read Array (byte)	Note
1 st	9F[H]	1
Action	3 byte read out	2

Note:

1. The 1st command 9F[H] is a Read Identification command
2. Identification output

Details of Command are shown as follows.

1-byte command code									
RDID	1	0	0	1	1	1	1	1	1

IDENTIFICATION DEFINITION

Manufacturer Identification	Device Identification	
	Type	Capacity
AE[H]	41[H]	13[H]

DEVICE OPERATION

1. Command “03h” or “0Bh” makes this LSI become and keep active mode until next #CS High.
2. Incorrect command makes this LSI become and keep standby mode until next #CS Low. In standby mode, SO pin is High-Z.
3. At Power-up, the device must not be selected (that is #CS must follow the voltage applied on Vcc) until Vcc reaches the operating value.

COMMAND DESCRIPTION

1. Read Array

This command consists of the 4-byte code. The 1st code is a command which decides if the device becomes standby or active mode. The 1st code “03h” activates the device. The 2nd code to the 4th code are address.

2. Fast-Read Array

This command consists of the 5-byte code. The 1st code is a command which decides if the device becomes standby or active mode. The 1st code “0Bh” activates the device. The 2nd code to the 4th code are address. The 5th code is a dummy cycle.

3. Read Identification Array

This command consists of the 1-byte code. The 1st code is a command which decides if the device becomes standby or active mode. The 1st code “9Fh” activates the device.

4. Standby

When #CS is high, the device is put in standby mode at the next rising edge of SCLK. Maximum standby current is 50uA. When the above-mentioned 1st code is incorrect command, the device is put in standby mode at the next rising edge of SCLK.

DATA SEQUENCE

The data is serially sent out through SO pin, synchronized with the falling edge of SCLK. Meanwhile input data is also serially read in through SI pin, synchronized with the rising edge of SCLK. The bit sequence for both input and output data are bit7 (MSB) first, bit6, bit5, ..., and bit0(LSB).

ADDRESS SEQUENCE

The address assignment is described at the COMMAND DEFINITION on page 2 or 3.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Storage temperature	Tstg	—	-55 to 125	°C
Input voltage	V _I	relative to V _{SS}	-0.5 to V _{CC} +0.5	V
Output voltage	V _O		-0.5 to V _{CC} +0.5	V
Power supply voltage	V _{CC}		-0.5 to 5	V
Power dissipation per package	P _D	Ta = 25°C	1.0	W
Output short circuit current	I _{OS}	—	10	mA

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating temperature under bias	Ta	V _{CC} = 3.0 to 3.6 V	0	—	70	°C
V _{CC} power supply voltage	V _{CC}		3.0	—	3.6	V
Input "H" level	V _{IH}		2.4	—	V _{CC} +0.5*	V
Input "L" level	V _{IL}		-0.5**	—	0.6	V

Voltage is relative to V_{SS}.* : V_{CC}+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

PIN CAPACITANCE(V_{CC} = 3.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C _{IN1}	V _I = 0 V	—	—	10	pF
Output	C _{OUT}	V _O = 0 V	—	—	10	
DC	C _{DC}	V _I = 0 V	—	—	200	

ELECTRICAL CHARACTERISTICS**DC CHARACTERISTICS**(V_{CC} = 3.3 V ± 0.3 V, T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I _{LI}	V _I = 0 to V _{CC}	—	—	10	μA
Output leakage current	I _{LO}	V _O = 0 to V _{CC}	—	—	10	μA
V _{CC} power supply current (Standby)	I _{CCSC}	#CS = V _{CC}	—	—	50	μA
	I _{CCST}	#CS = V _{IH}	—	—	1	mA
V _{CC} power supply current (Read)	I _{CC1}	#CS = V _{IL} f=20MHz SO=open	—	—	20	mA
V _{CC} power supply current (Fast-Read)	I _{CC1F}	#CS = V _{IL} f=33MHz SO=open	—	—	25	mA
Input "H" level	V _{IH}	—	2.4	—	V _{CC} +0.5*	V
Input "L" level	V _{IL}	—	-0.5**	—	0.6	V
Output "H" level	V _{OH}	I _{OH} = -100 μA	2.4	—	—	V
Output "L" level	V _{OL}	I _{OL} = 500 μA	—	—	0.4	V

Voltage is relative to V_{SS}.* : V_{CC}+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

AC CHARACTERISTICS

FAST-READ

 $(V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, T_a = 0 \text{ to } 70^\circ\text{C})$

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock frequency	t_{CLK}	—	—	33	MHz
Clock high time	t_{SKH}	—	14	—	ns
Clock low time	t_{SKL}	—	14	—	ns
Input signal Rise time	t_{R}	—	—	3	ns
Input signal Fall time	t_{F}	—	—	3	ns
#CS lead clock time	t_{CSA}	—	10	—	ns
#CS setup time	t_{CS}	—	5	—	ns
#CS lag clock time	t_{CSB}	—	5	—	ns
#CS hold time	t_{CH}	—	5	—	ns
#CS high time	t_{CSH}	—	80	—	ns
SI setup time	t_{DS}	—	2	—	ns
SI hold time	t_{DH}	—	10	—	ns
Access time	t_{AA}	—	—	14	ns
SO hold time	t_{DOH}	—	0	—	ns
SO floating time	t_{DOZ}	—	—	15	ns

READ

 $(V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, T_a = 0 \text{ to } 70^\circ\text{C})$

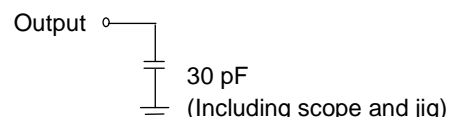
Parameter	Symbol	Condition	Min.	Max.	Unit
Clock frequency	t_{CLK}	—	—	20	MHz
Clock high time	t_{SKH}	—	20	—	ns
Clock low time	t_{SKL}	—	20	—	ns
Input signal Rise time	t_{R}	—	—	3	ns
Input signal Fall time	t_{F}	—	—	3	ns
#CS lead clock time	t_{CSA}	—	10	—	ns
#CS setup time	t_{CS}	—	5	—	ns
#CS lag clock time	t_{CSB}	—	5	—	ns
#CS hold time	t_{CH}	—	5	—	ns
#CS high time	t_{CSH}	—	80	—	ns
SI setup time	t_{DS}	—	2	—	ns
SI hold time	t_{DH}	—	10	—	ns
Access time	t_{AA}	—	—	14	ns
SO hold time	t_{DOH}	—	0	—	ns
SO floating time	t_{DOZ}	—	—	15	ns

Measurement conditions

Input signal level
 Input timing reference level
 Output load
 Output timing reference level

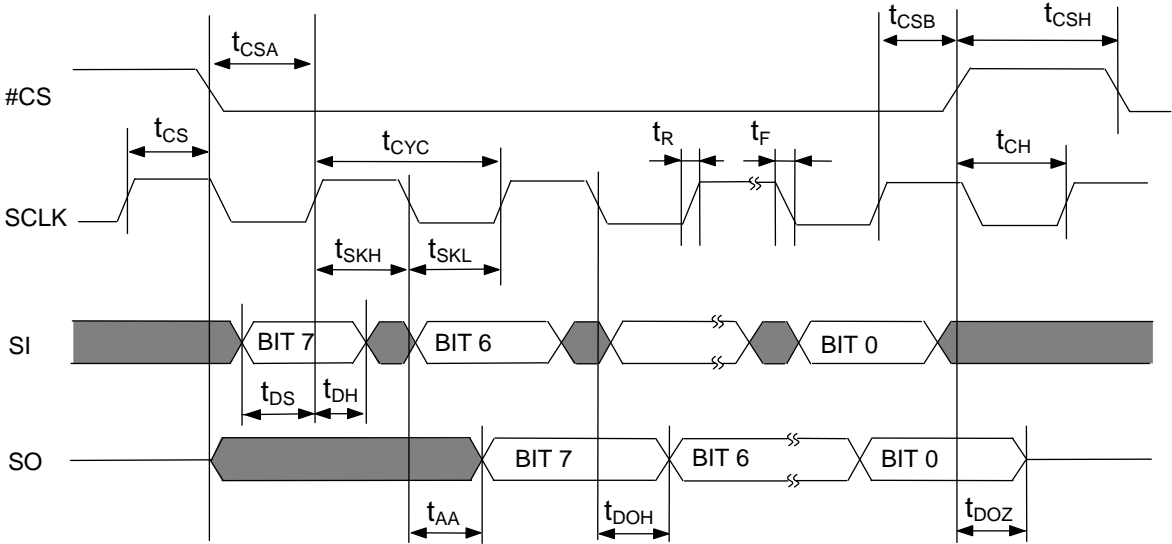
0 V/ V_{CC}
 0.3 V_{CC} /0.7 V_{CC}
 30 pF
 0.5 V_{CC}

Output load

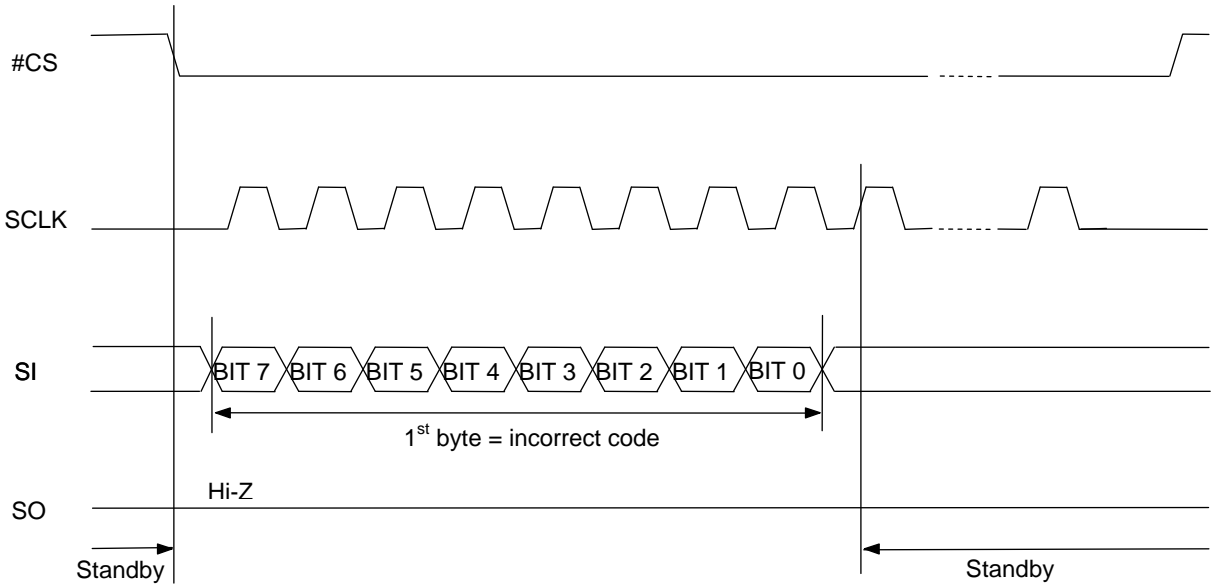


TIMING CHART (READ CYCLE)

Serial Data Input/Output Timing

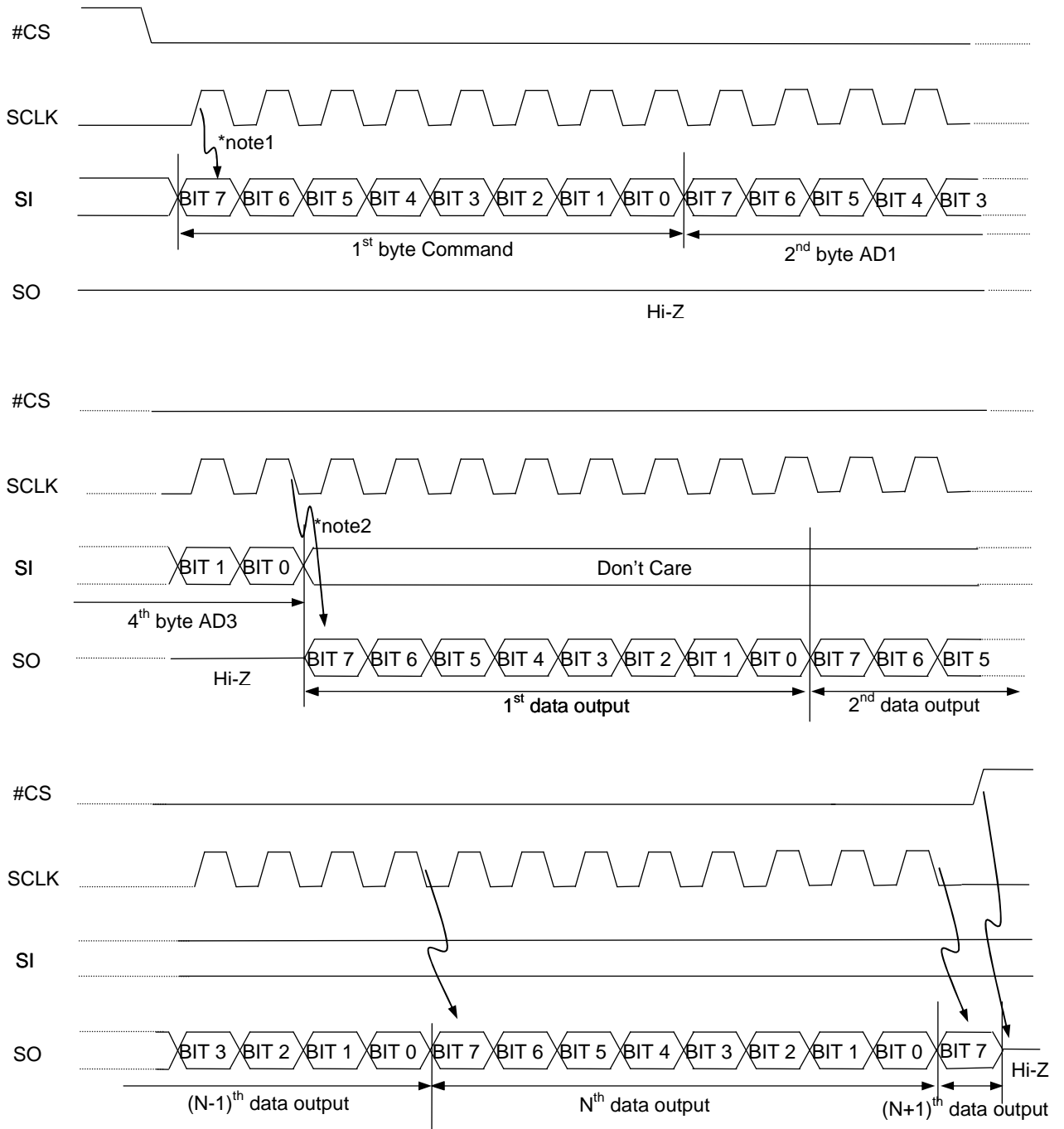


Standby Timing



Incorrect command makes this LSI become and keep standby mode until next #CS rising edge. In standby mode, SO pin is High-Z.

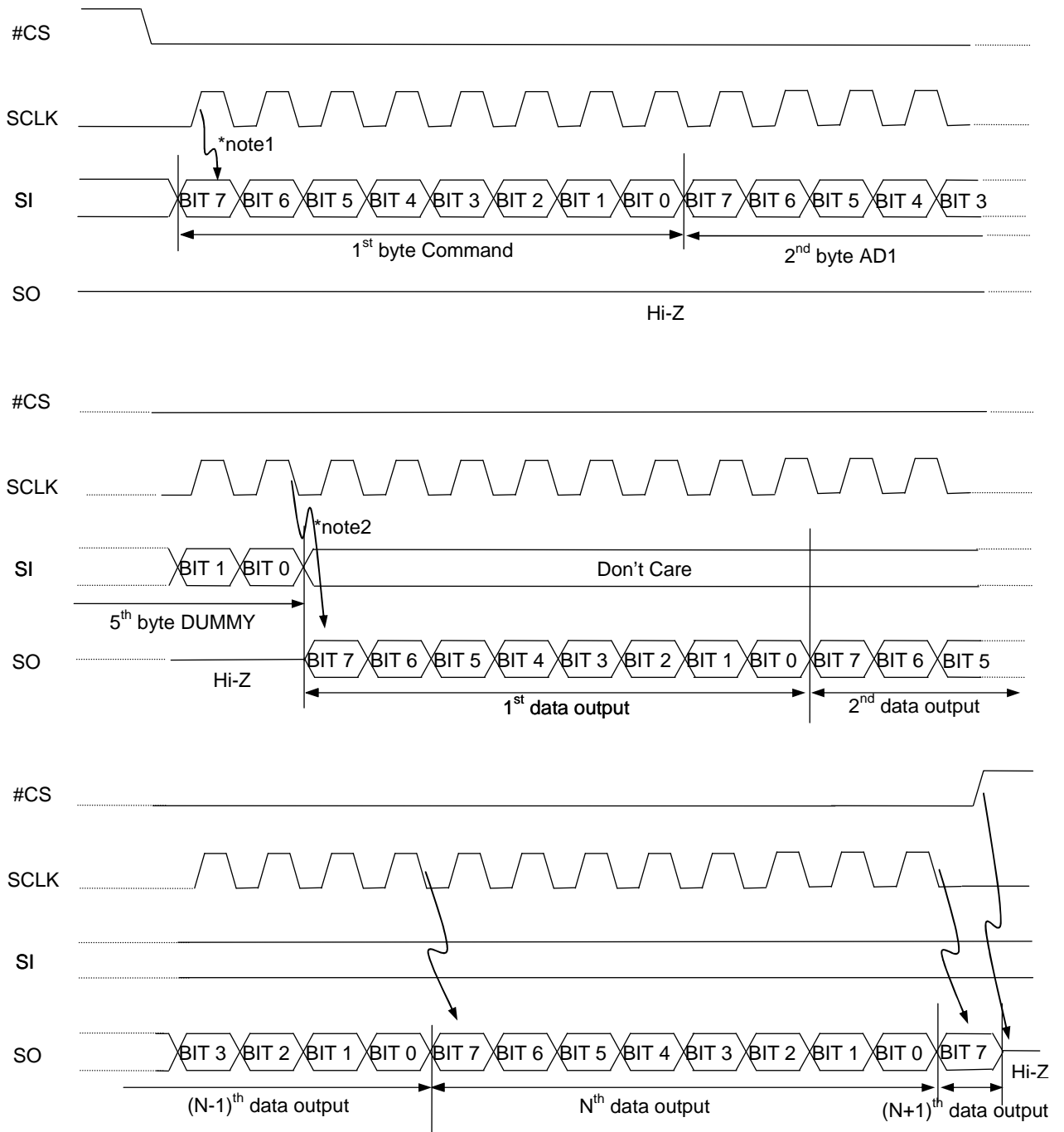
Read Array Timing Waveform



Note:

1. Input data are latched at SCLK-rising edge.
2. Data-output starts at SCLK-falling edge in bit0 of the 4th byte.

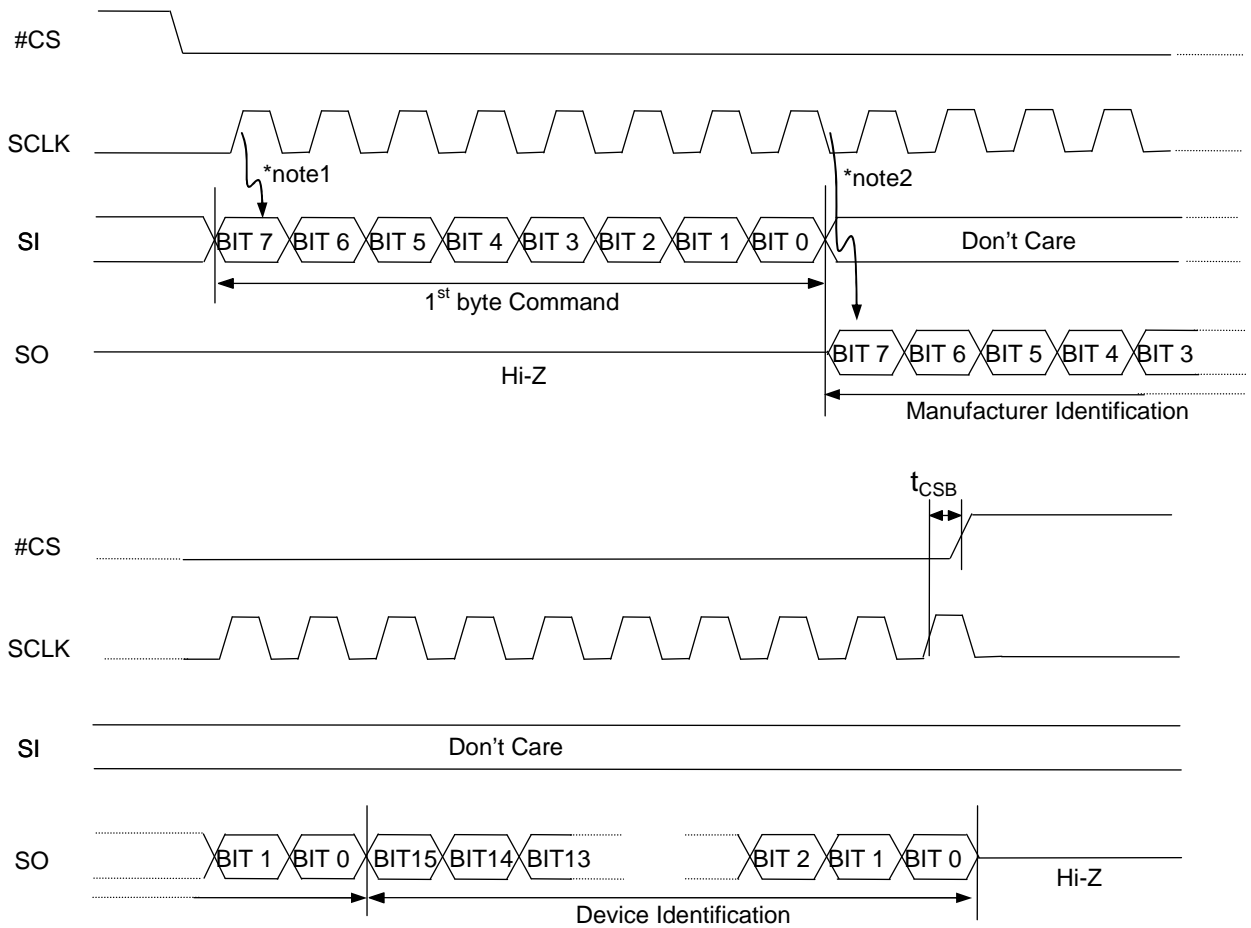
Fast Read Array Timing Waveform



Note:

1. Input data are latched at SCLK-rising edge.
2. Data-output starts at SCLK-falling edge in bit0 of the 5th byte.

Read Identification Timing Waveform

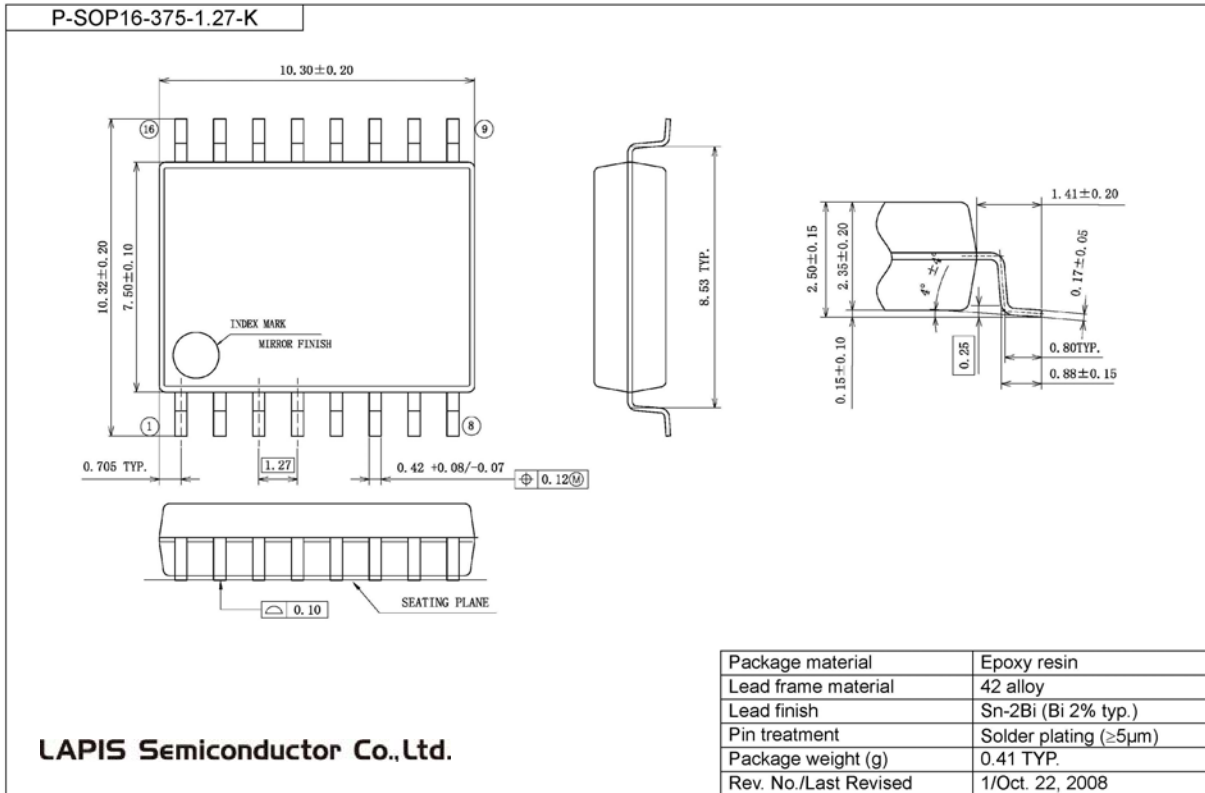


Note:

1. Input data are latched at SCLK-rising edge.
2. Data-output starts at SCLK-falling edge in bit0 of the 1st byte.

PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR27V1641L-02-01	Oct. 28, 2005	–	–	Final edition 1
FEDR27V1641L-02-02	Oct. 31, 2006	1, 7, 8	1, 7, 8	serial clock (FAST-READ) 33MHz --> 30MHz
		1	1	Don't care (H or L or Open) --> Don't care (0v - Vcc)
		5	5	device operation added 3.
		6	6	Pin Capacitance C _{IN1} Max 12pF --> 10pF C _{OUT} Max 12pF --> 10pF
		8	8	FAST-READ t _{SKH} Min. 12ns --> 14ns t _{SKL} Min. 12ns --> 14ns FAST-READ & READ t _R Min. 0.1 V/ns --> Max. 3ns t _F Min. 0.1 V/ns --> Max. 3ns t _{AA} Max. 15ns --> 14ns t _{DOZ} Max. 8ns --> 15ns
FEDR27V1641L-02-03	Mar. 16, 2007	2	2	3-byte address (0 to 3FFF[H]) --> 3-byte address
		3	3	3-byte address (0 to 3FFF[H]) --> 3-byte address
		13	13	Replaced package diagram
FEDR27V1641L-002-03	Oct. 1, 2008	–	–	Changed company logo and name to OKI SEMICONDUCTOR
FEDR27V1641L-002-04	Apr. 1, 2009	1, 7, 8	1, 7, 8	serial clock (FAST-READ) 30MHz --> 33MHz

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