MR36V04G54B

128M–Word × 32–Bit Page Mode P2ROM

FEATURES

· 128Mx32 or 256Mx16-bit
electrically switchable configuration
· Page size of 8-word x 32-Bit or 16-word x 16-Bit
· 3.0 V to 3.6 V power supply
· Random Access time..... 105 ns MAX
· Page Access time ..... 25 ns MAX
· Operating current ..... 100 mA MAX
· Standby current ..... 85 mA MAX
· Input/Output TTL compatible
· Three-state output

PACKAGES

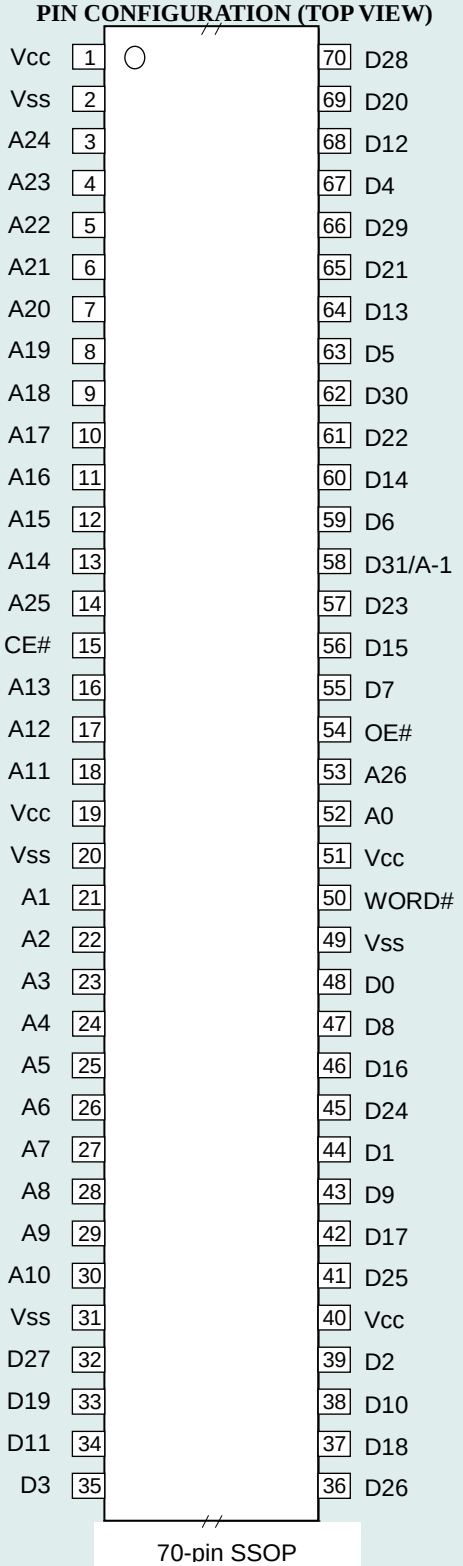
·70-pin plastic SSOP (P-SSOP70-500-0.80-EK-MC)

P2ROM ADVANCED TECHNOLOGY

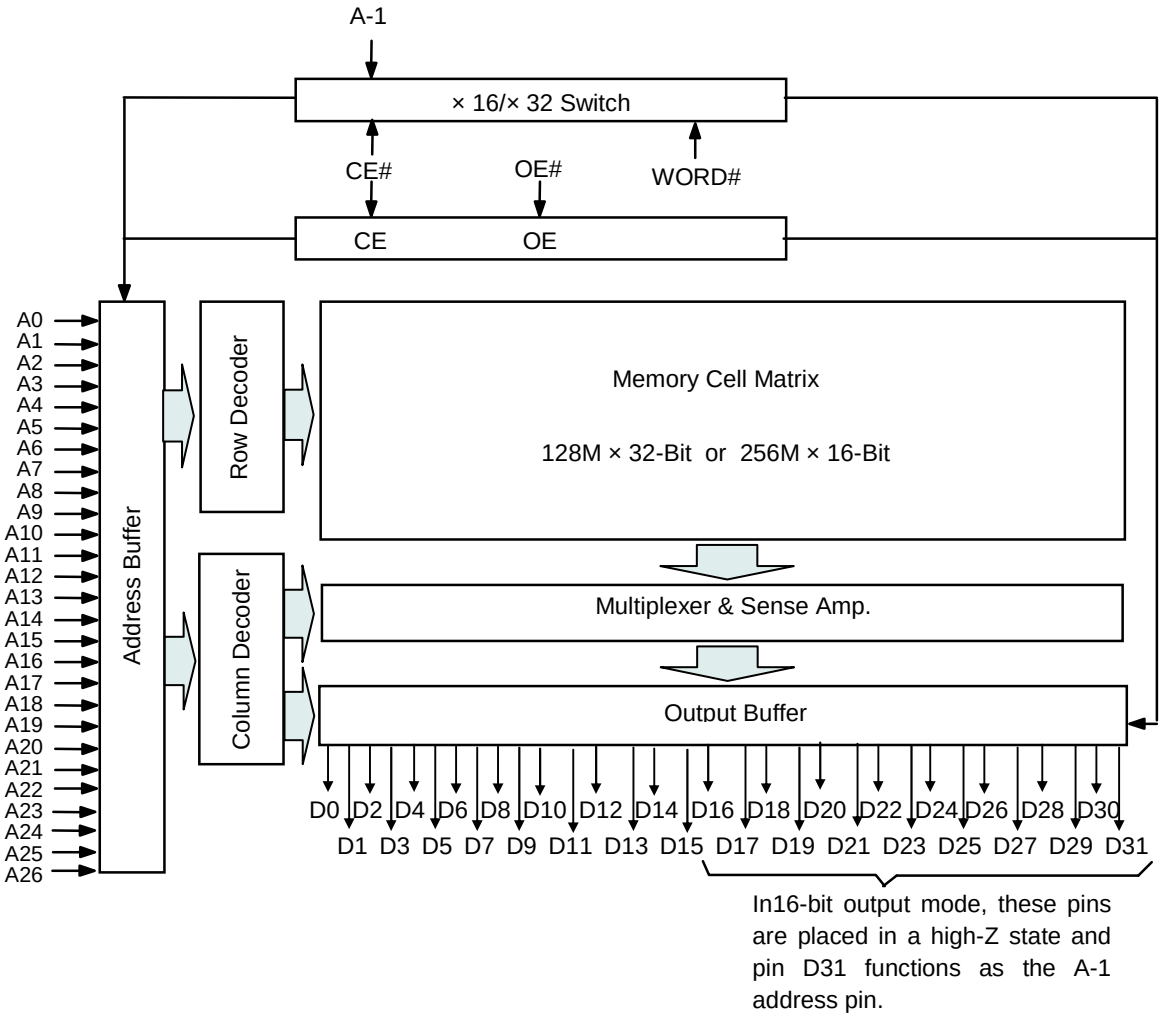
P2ROM stands for Production Programmed ROM. This exclusive LAPIS Semiconductor technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

· **Short lead time**, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
· **No mask charge**, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
· **No additional programming charge**, unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
· **Custom Marking** is available at no additional charge.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin name	Functions
A0 to A26	Address inputs
D31/ A–1	Data outputs /Address -1 input
D0 to D30	Data outputs
CE#	Chip enable input
OE#	Output enable input
WORD#	Word -Byte select input
V_{CC}	Power supply voltage
V_{SS}	Ground

FUNCTION TABLE

Mode	CE#	OE#	WORD#	V_{CC}	D0 to D15	D16 to D30	D31/A-1
Read (32-Bit)	L	L	H	3.3 V	D_{OUT}		D_{OUT}
Read (16-Bit)	L	L	L		D_{OUT}	Hi–Z	L/H
Output disable	L	H	H		Hi–Z		*
			L				
Standby	H	*	H		Hi–Z		*
			L				

*: Don't Care (H or L)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	Ta	—	0 to 70	°C
Storage temperature	Tstg		–55 to 125	°C
Input voltage	V_I	relative to V_{SS}	–0.5 to V_{CC}+0.5	V
Output voltage	V_O		–0.5 to V_{CC}+0.5	V
Power supply voltage	V_{CC}		–0.5 to 4.6	V
Output short circuit current	Ios	—	10	mA
Power dissipation per package	P_D	Ta=25°C	1.0	W

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{CC} power supply voltage	V_{CC}	V_{CC} = 3.0 to 3.6 V	3.0	—	3.6	V
Input "H" level	V_{IH}		2.2	—	V_{CC}+0.5*	V
Input "L" level	V_{IL}		–0.5**	—	0.6	V

Voltage is relative to V_{SS}.

* : V_{CC}+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

PIN CAPACITANCE

(V_{CC} = 3.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input(except Word#)	C_{IN1}	V_I = 0 V	—	—	20	pF
Output	C_{OUT}	V_O = 0 V	—	—	20	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	V_I = 0 to V_{CC}		—	—	20	μA
Output leakage current	I_{LO}	V_O = 0 to V_{CC}		—	—	20	μA
V_{CC} power supply current (Standby)	I_{CCSC}	CE# = Add.=V_{CC}	V_{CC}=3.6V	—	—	85	mA
V_{CC} power supply current (Read)	I_{CCA1}	CE# = V_{IL} OE# = V_{IH}	tc = 200 ns	—	—	100	mA
Input “H” level	V_{IH}	—		2.2	—	V_{CC}+0.5*	V
Input “L” level	V_{IL}	—		–0.5**	—	0.6	V
Output “H” level	V_{OH}	I_{OH} = –2 mA		2.4	—	—	V
Output “L” level	V_{OL}	I_{OL} = 2 mA		—	—	0.4	V

Voltage is relative to V_{SS}.

* : V_{CC}+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

AC Characteristics

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	t_C	—	105	—	ns
Address access time	t_{ACC}	—	—	105	ns
Address skew time	t_{ASK}	—	—	10	ns
CE Address skew time	T_{CSK}	—	—	10	ns
Page cycle time	t_{PC}	—	25	—	ns
Page access time	t_{PAC}	CE# = OE# = V_{IL}	—	25	ns
CE# access time	t_{CE}	OE# = V_{IL}	—	105	ns
OE# access time	t_{OE}	CE# = V_{IL}	—	25	ns
Output disable time	t_{CHZ}	OE# = V_{IL}	0	20	ns
	t_{OHZ}	CE# = V_{IL}	0	20	ns
Output hold time	t_{OH}	CE# = OE# = V_{IL}	0	—	ns

Measurement conditions

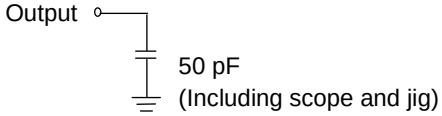
Input signal level---------- 0 V/3 V

Input timing reference level---------- 1/2Vcc

Output load ---------- 50 pF

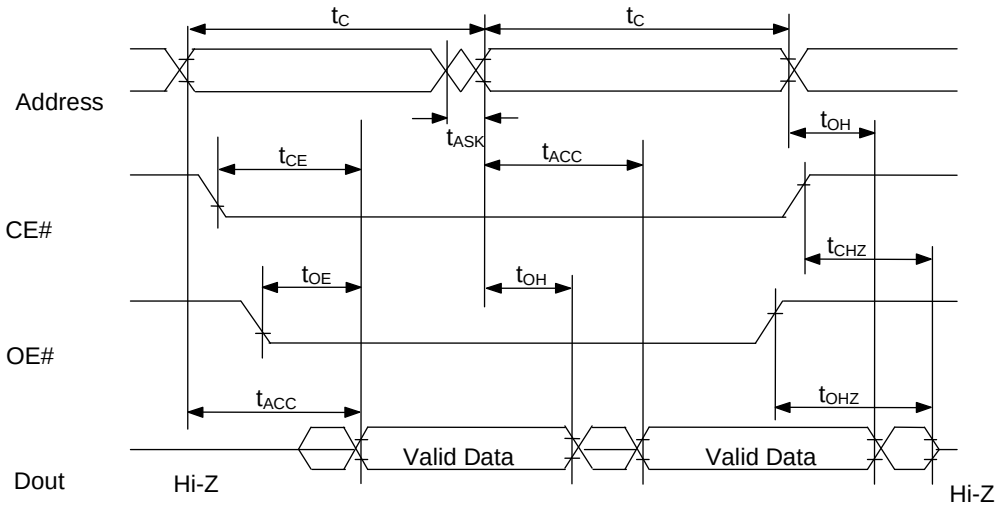
Output timing reference level---------- 1/2Vcc

Output load

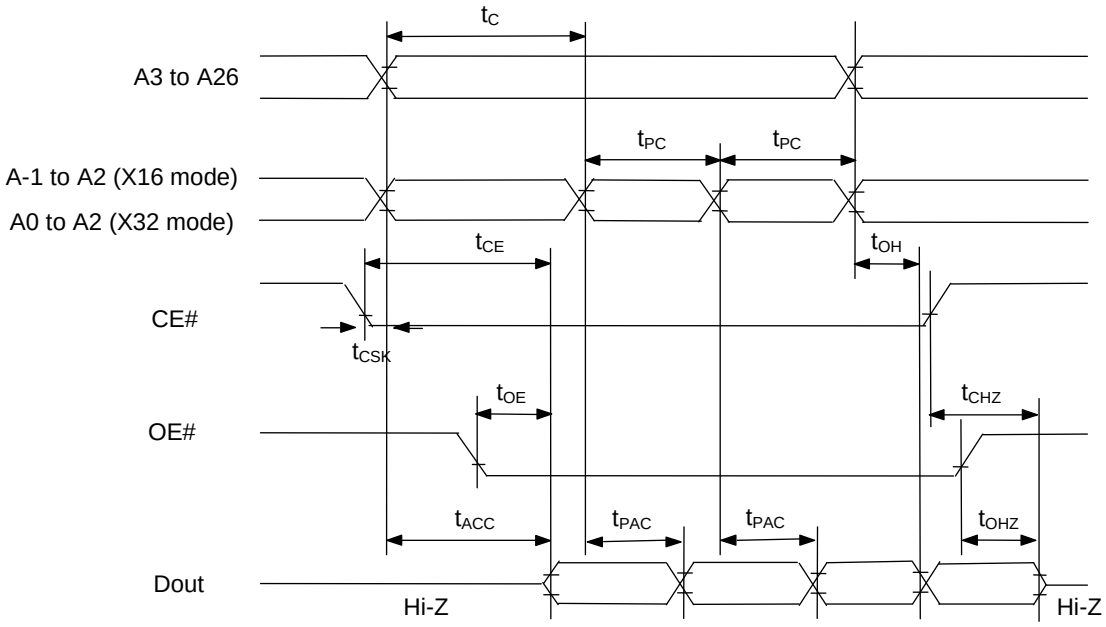


TIMING CHART (READ CYCLE)

Random Access Mode Read Cycle



Page Access Mode Read Cycle

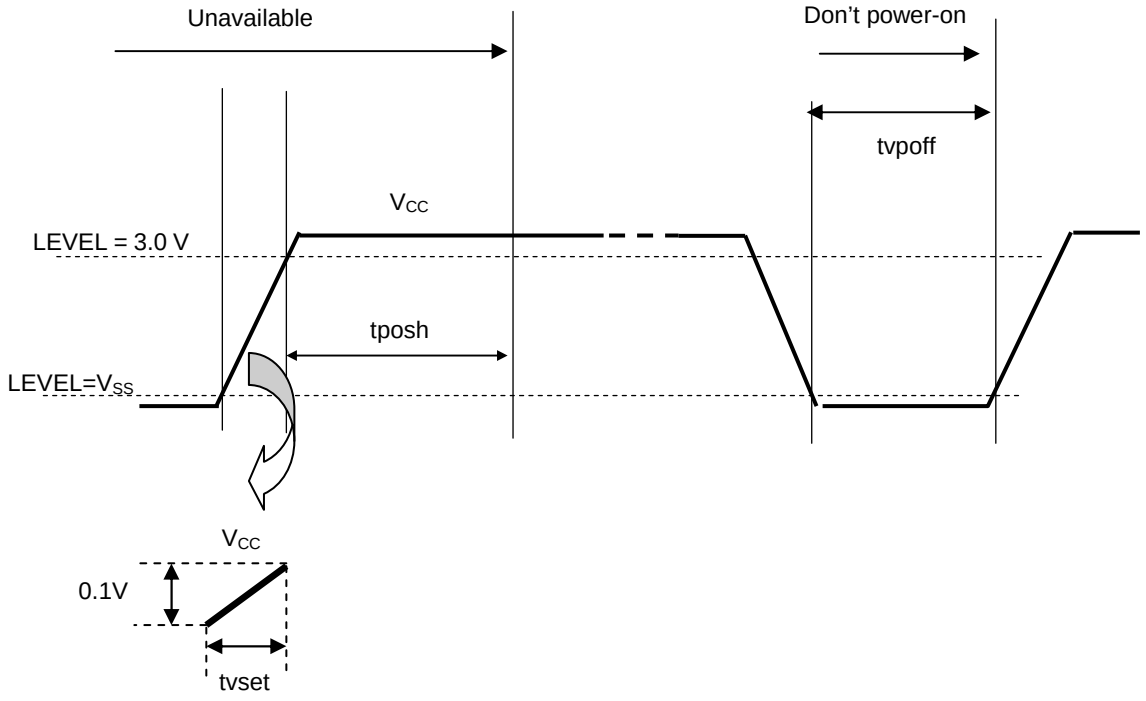


POWER ON CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
V_{CC} set up time	tvset	—	5	270	us
Power on sequence hold time	tposh	—	1	—	ms
Power off hold time	tvpoff	—	1	—	ms

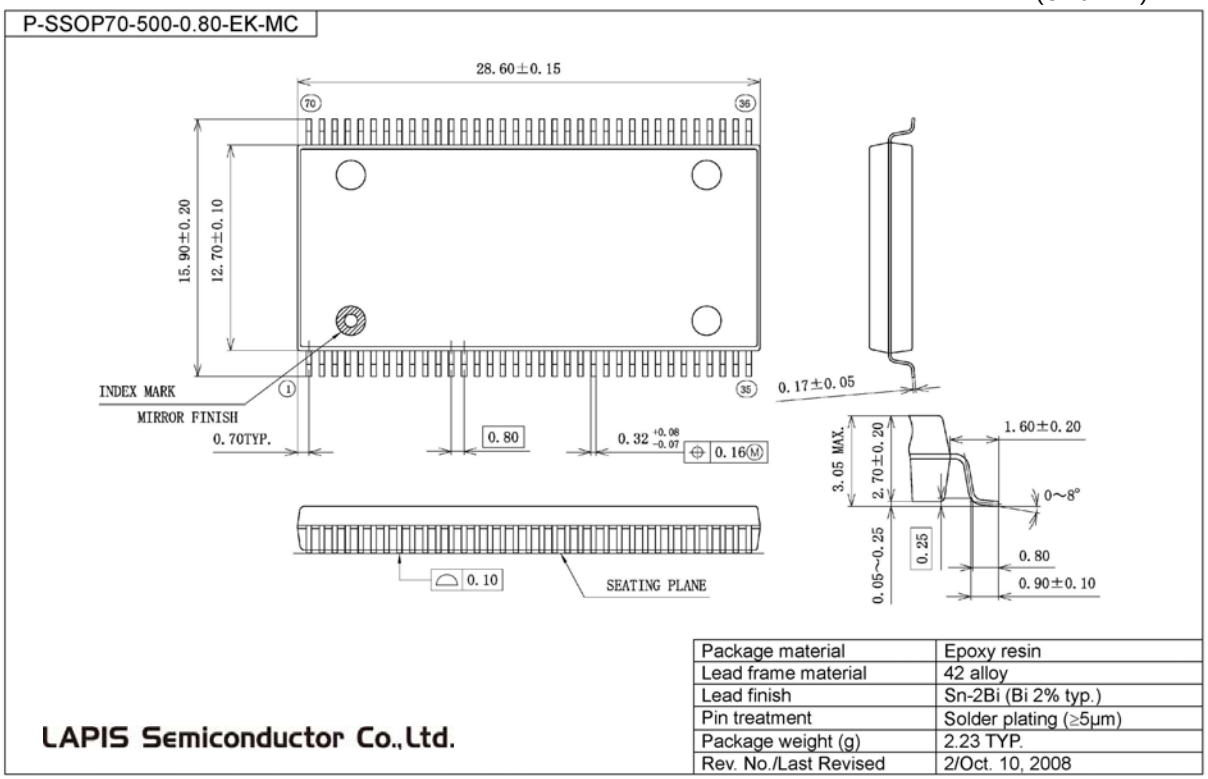
TIMING CHART (POWER ON)



Note: A start-up delay of 1ms is required after power-on.
If you power-off V_{CC}, you must wait 1ms to power-on.
CE# must be HIGH while V_{CC} power on sequence.

PACKAGE DIMENSIONS

(Unit: mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	2.23 TYP.
Rev. No./Last Revised	2/Oct. 10, 2008

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR36V04G54B-02-01	Sep. 03 2008	–	–	Final edition 1
FEDR36V04G54B-002-01	Oct. 1, 2008	–	–	Changed company logo and name to OKI SEMICONDUCTOR

NOTICE

No copying or reproduction of this document, in part or in whole, is permitted without the consent of LAPIS Semiconductor Co., Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing LAPIS Semiconductor's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from LAPIS Semiconductor upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, LAPIS Semiconductor shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. LAPIS Semiconductor does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by LAPIS Semiconductor and other parties. LAPIS Semiconductor shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While LAPIS Semiconductor always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. LAPIS Semiconductor shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). LAPIS Semiconductor shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.