

# MR37V12841A

**128M × 1-Bit Serial Production Programmed ROM (P2ROM)**

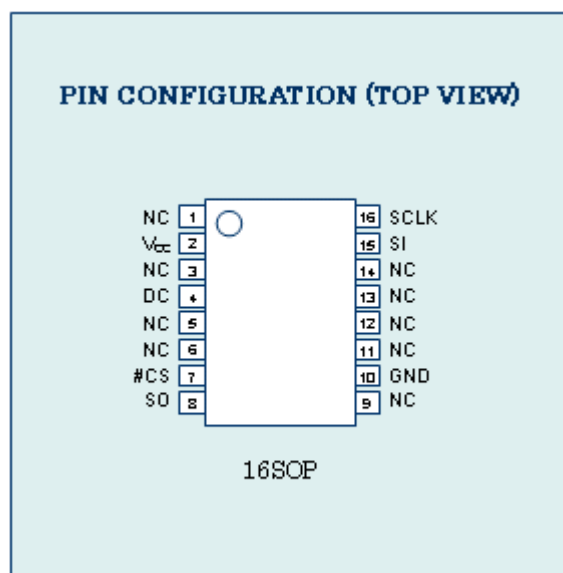
## GENERAL DESCRIPTION

The MR37V12841A is a 128Mbit Production Programmed Read-Only Memory, which is configured as 134,217,728word × 1-bit. The MR37V12841A supports a simple read operation using a single 3.3V power supply and a Serial Peripheral Interface (SPI) compatible serial bus.

The MR37V12841A have data programmed and have functions tested at LAPIS Semiconductor factory. (Using the DC pins for the programming function is NOT allowed )

## FEATURES

- Read Operation
  - +3.3 V power supply
  - 134,217,728 × 1-bit
  - Access time: 33MHz serial clock (FAST-READ)
  - 20MHz serial clock (READ)
  - Read Identification Instruction
  - Active read current: 30mA(FAST-READ)
  - 20mA(READ)
  - Standby current : 50 μA
  - Serial Clock Input and Data Input/Output
  - Input Data Format :
    - 1-byte Command code, 3-byte address, 1-byte dummy (FAST-READ)
    - 1-byte Command code, 3-byte address (READ)



## PACKAGES

- MR37V12841A-xxxMP
- 16-pin plastic SOP (P-SOP16-375-1.27-K)

## PIN DESCRIPTIONS

Pin name	Functions under Read Operation
#CS	Chip Select
SI	Serial Data Input
SO	Serial Data Output
SCLK	Clock Input
V <sub>CC</sub>	Power supply voltage
GND	Ground
DC	Don't care ( 0v - V <sub>CC</sub> ) <for reference> Program power supply voltage V <sub>pp</sub> under Programming operation
NC	Non connection

**READ COMMAND DEFINITION**

Command	Read Array (byte)	Note
1 <sup>st</sup>	03[H]	1
2 <sup>nd</sup>	AD1	2
3 <sup>rd</sup>	AD2	2
4 <sup>th</sup>	AD3	2
Action	N byte read out until #CS goes high	3

Note:

1. The 1<sup>st</sup> command 03[H] is a Read command
2. AD1 to AD3 are address input data
3. Data output

Details of command and address are shown as follows.

1-byte command code								
READ	0	0	0	0	0	0	1	1
3-byte address								
AD1:	A23	A22	A21	A20	A19	A18	A17	A16
AD2:	A15	A14	A13	A12	A11	A10	A9	A8
AD3:	A7	A6	A5	A4	A3	A2	A1	A0

**FAST READ COMMAND DEFINITION**

Command	Read Array (byte)	Note
1 <sup>st</sup>	0B[H]	1
2 <sup>nd</sup>	AD1	2
3 <sup>rd</sup>	AD2	2
4 <sup>th</sup>	AD3	2
5 <sup>th</sup>	X	3
Action	N byte read out until #CS goes high	4

Note:

1. The 1<sup>st</sup> command 0B[H] is a Read command
2. AD1 to AD3 are address input data
3. X is a dummy cycle
4. Data output

Details of command and address are shown as follows.

1-byte command code								
FAST-READ	0	0	0	0	1	0	1	1
3-byte address								
AD1:	A23	A22	A21	A20	A19	A18	A17	A16
AD2:	A15	A14	A13	A12	A11	A10	A9	A8
AD3:	A7	A6	A5	A4	A3	A2	A1	A0

**READ IDENTIFICATION COMMAND DEFINITION**

Command	Read Array (byte)	Note
1 <sup>st</sup>	9F[H]	1
Action	3 byte read out	2

Note:

1. The 1<sup>st</sup> command 9F[H] is a Read Identification command
2. Identification output

Details of command and address are shown as follows.

1-byte command code								
RDID	1	0	0	1	1	1	1	1

**IDENTIFICATION DEFINITION**

Manufacturer Identification	Device Identification	
	Type	Capacity
AE[H]	41[H]	16[H]

## DEVICE OPERATION

1. Command “03h” or “0Bh” makes this LSI become and keep active mode until next #CS High.
2. Incorrect command makes this LSI become and keep standby mode until next #CS Low. In standby mode, SO pin is High-Z.

## COMMAND DESCRIPTION

1. Read Array  
This command consists of the 4-byte code. The 1<sup>st</sup> code is a command which decides if the device becomes standby or active mode. The 1<sup>st</sup> code “03h” activates the device. The 2<sup>nd</sup> code to the 4<sup>th</sup> code are address inputs.
2. Fast Read Array  
This command consists of the 5-byte code. The 1<sup>st</sup> code is a command which decides if the device becomes standby or active mode. The 1<sup>st</sup> code “0Bh” activates the device. The 2<sup>nd</sup> code to the 4<sup>th</sup> code are address. The 5<sup>th</sup> code is a dummy cycle.
3. Identification Read Array  
This command consists of the 1-byte code. The 1<sup>st</sup> code is a command which decides if the device becomes standby or active mode. The 1<sup>st</sup> code “9Fh” activates the device.
4. Standby  
When #CS is high, the device is put in standby mode at the next rising edge of SCLK. Maximum standby current is 10uA. When the above-mentioned 1<sup>st</sup> code is incorrect command, the device is put in standby mode at the next rising edge of SCLK.

## DATA SEQUENCE

The data is serially sent out through SO pin, synchronized with the falling edge of SCLK. Meanwhile input data is also serially read in through SI pin, synchronized with the rising edge of SCLK. The bit sequence for both input and output data are bit7 (MSB) first, bit6, bit 5, ..., and bit0(LSB).

## ADDRESS SEQUENCE

The address assignment is described at the COMMAND DEFINITION on page 2, 3.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Value	Unit
Storage temperature	Tstg	—	–55 to 125	°C
Input voltage	V <sub>I</sub>	relative to V <sub>SS</sub>	–0.5 to V <sub>CC</sub> +0.5	V
Output voltage	V <sub>O</sub>		–0.5 to V <sub>CC</sub> +0.5	V
Power supply voltage	V <sub>CC</sub>		–0.5 to 5	V
Power dissipation per package	P <sub>D</sub>	Ta = 25°C	1.0	W
Output short circuit current	I <sub>OS</sub>	—	10	mA

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating temperature under bias	Ta	V <sub>CC</sub> = 3.0 to 3.6 V	0	—	70	°C
V <sub>CC</sub> power supply voltage	V <sub>CC</sub>		3.0	—	3.6	V
Input “H” level	V <sub>IH</sub>		2.4	—	V <sub>CC</sub> +0.5*	V
Input “L” level	V <sub>IL</sub>		–0.5**	—	0.6	V

Voltage is relative to V<sub>SS</sub>.

\* : V<sub>CC</sub>+1.5V(Max.) when pulse width of positive overshoot is less than 10ns.

\*\* : –1.5V(Min.) when pulse width of negative overshoot is less than 10ns.

**PIN CAPACITANCE**

(V<sub>CC</sub> = 3.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C <sub>IN1</sub>	V <sub>I</sub> = 0 V	—	—	8	pF
Output	C <sub>OUT</sub>	V <sub>O</sub> = 0 V	—	—	10	
DC	C <sub>DC</sub>	V <sub>I</sub> = 0 V	—	—	200	

**ELECTRICAL CHARACTERISTICS****DC Characteristics**(V<sub>CC</sub> = 3.0V-3.6V, Ta = 0 to 70°C)

parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I <sub>LI</sub>	V <sub>I</sub> = 0 to V <sub>CC</sub>	—	—	10	μA
Output leakage current	I <sub>LO</sub>	V <sub>O</sub> = 0 to V <sub>CC</sub>	—	—	10	μA
V <sub>CC</sub> power supply current (Standby)	I <sub>SB1</sub>	#CS = V <sub>CC</sub>	—	—	50	μA
	I <sub>SB2</sub>	#CS = V <sub>IH</sub>	—	—	1	mA
V <sub>CC</sub> power supply current (Read)	I <sub>CC1</sub>	#CS = V <sub>IL</sub> , f = 20MHz SO= open	—	—	20	mA
V <sub>CC</sub> power supply current (Fast Read)	I <sub>CC1F</sub>	#CS = V <sub>IL</sub> , f = 33Hz SO= open	—	—	30	mA
Input “H” level	V <sub>IH</sub>	—	2.4	—	V <sub>CC</sub> +0.5*	V
Input “L” level	V <sub>IL</sub>	—	−0.5**	—	0.6	V
Output “H” level	V <sub>OH</sub>	I <sub>OH</sub> = −100 μA	V <sub>CC</sub> -0.2	—	—	V
Output “L” level	V <sub>OL</sub>	I <sub>OL</sub> = 500 μA	—	—	0.4	V

Voltage is relative to V<sub>SS</sub>.\* : V<sub>CC</sub>+1.5V(Max.) when pulse width of positive overshoot is less than 10ns.

\*\* : −1.5V(Min.) when pulse width of negative overshoot is less than 10ns.

## AC Characteristics

( t<sub>sclk</sub>=33MHz, V<sub>CC</sub> = 3.0V-3.6V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock frequency	t <sub>SCLK</sub>	—	—	33 *	MHz
Clock High time	t <sub>SKH</sub>	—	11	—	ns
Clock Low time	t <sub>SKL</sub>	—	11	—	ns
Clock Rise time	t <sub>R</sub>	—	—	4	ns
Clock Fall time	t <sub>F</sub>	—	—	4	ns
#CS Lead Clock Time	t <sub>CSA</sub>	—	5	—	ns
#CS Setup Time	t <sub>CS</sub>	—	5	—	ns
#CS Lag Clock Time	t <sub>CSB</sub>	—	5	—	ns
#CS Hold Time	t <sub>CH</sub>	—	5	—	ns
#CS High Time	t <sub>CSH</sub>	—	100	—	ns
SI Setup Time	t <sub>DS</sub>	—	2	—	ns
SI Hold Time	t <sub>DH</sub>	—	10	—	ns
Access time	t <sub>AA</sub>	—	—	8	ns
SO Hold Time	t <sub>DOH</sub>	—	0	—	ns
SO Floating Time	t <sub>DOZ</sub>	—	—	8	ns

( t<sub>sclk</sub>=20MHz V<sub>CC</sub> = 3.0V-3.6V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock frequency	t <sub>SCLK</sub>	—	—	20 **	MHz
Clock High time	t <sub>SKH</sub>	—	20	—	ns
Clock Low time	t <sub>SKL</sub>	—	20	—	ns
Clock Rise time	t <sub>R</sub>	—	—	5	ns
Clock Fall time	t <sub>F</sub>	—	—	5	ns
#CS Lead Clock Time	t <sub>CSA</sub>	—	10	—	ns
#CS Setup Time	t <sub>CS</sub>	—	10	—	ns
#CS Lag Clock Time	t <sub>CSB</sub>	—	5	—	ns
#CS Hold Time	t <sub>CH</sub>	—	5	—	ns
#CS High Time	t <sub>CSH</sub>	—	100	—	ns
SI Setup Time	t <sub>DS</sub>	—	5	—	ns
SI Hold Time	t <sub>DH</sub>	—	10	—	ns
Access time	t <sub>AA</sub>	—	—	15	ns
SO Hold Time	t <sub>DOH</sub>	—	0	—	ns
SO Floating Time	t <sub>DOZ</sub>	—	—	10	ns

\*: FAST-READ instructions

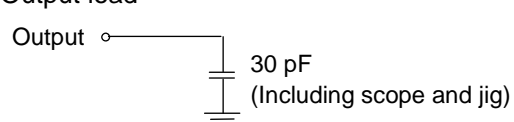
\*\*: READ instructions

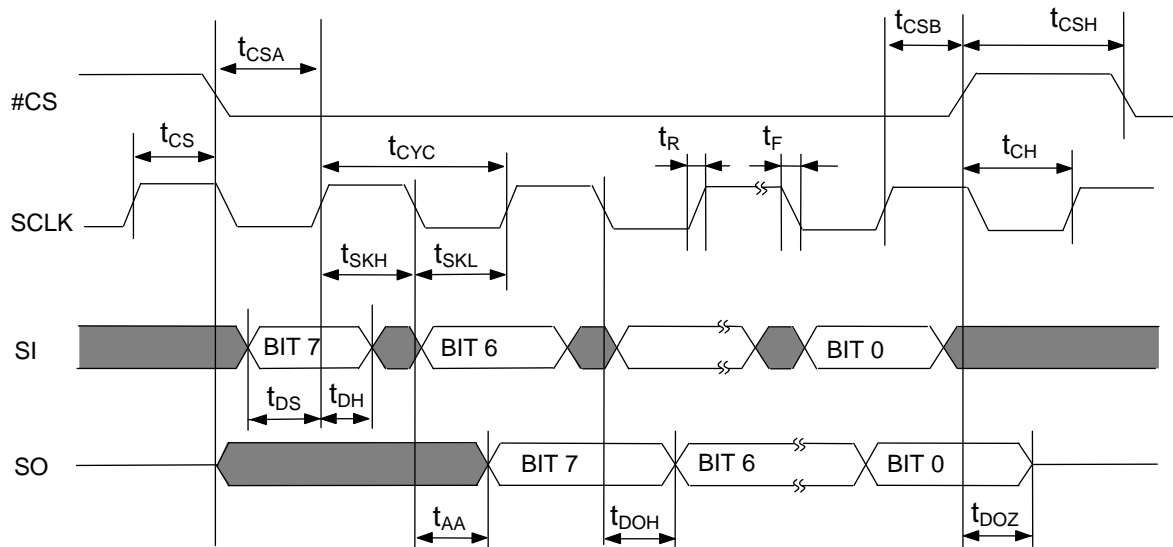
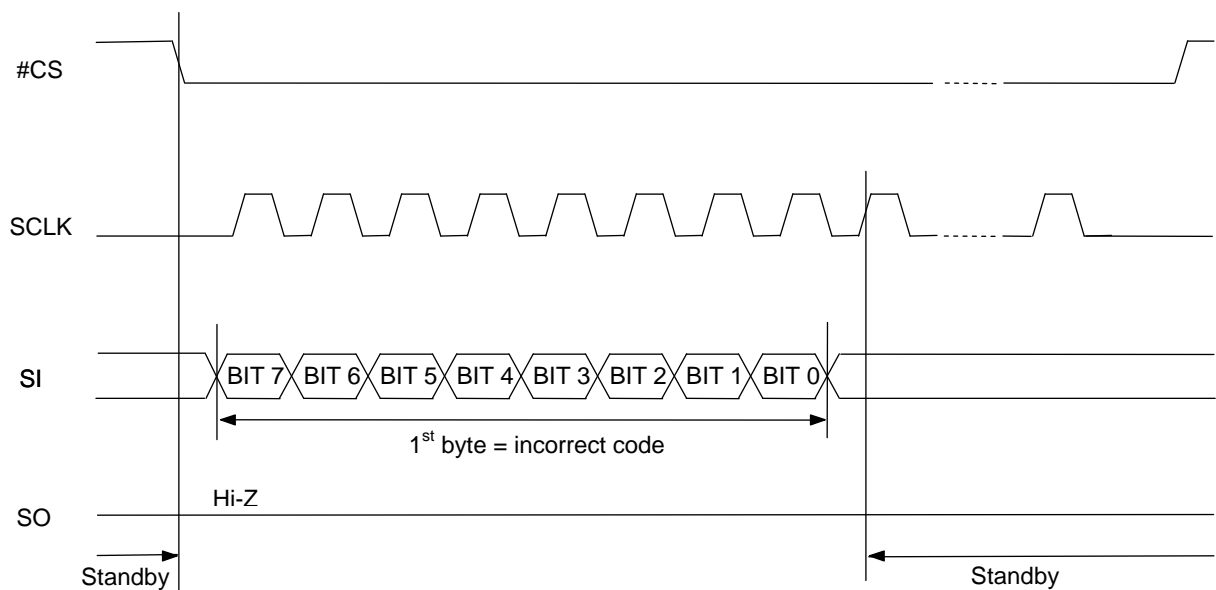
## Measurement conditions

Input signal level  
 Input timing reference level  
 Output load  
 Output timing reference level

V<sub>CC</sub>/0v  
 2.4V/ 0.6V  
 30 pF  
 0.5 V<sub>CC</sub>

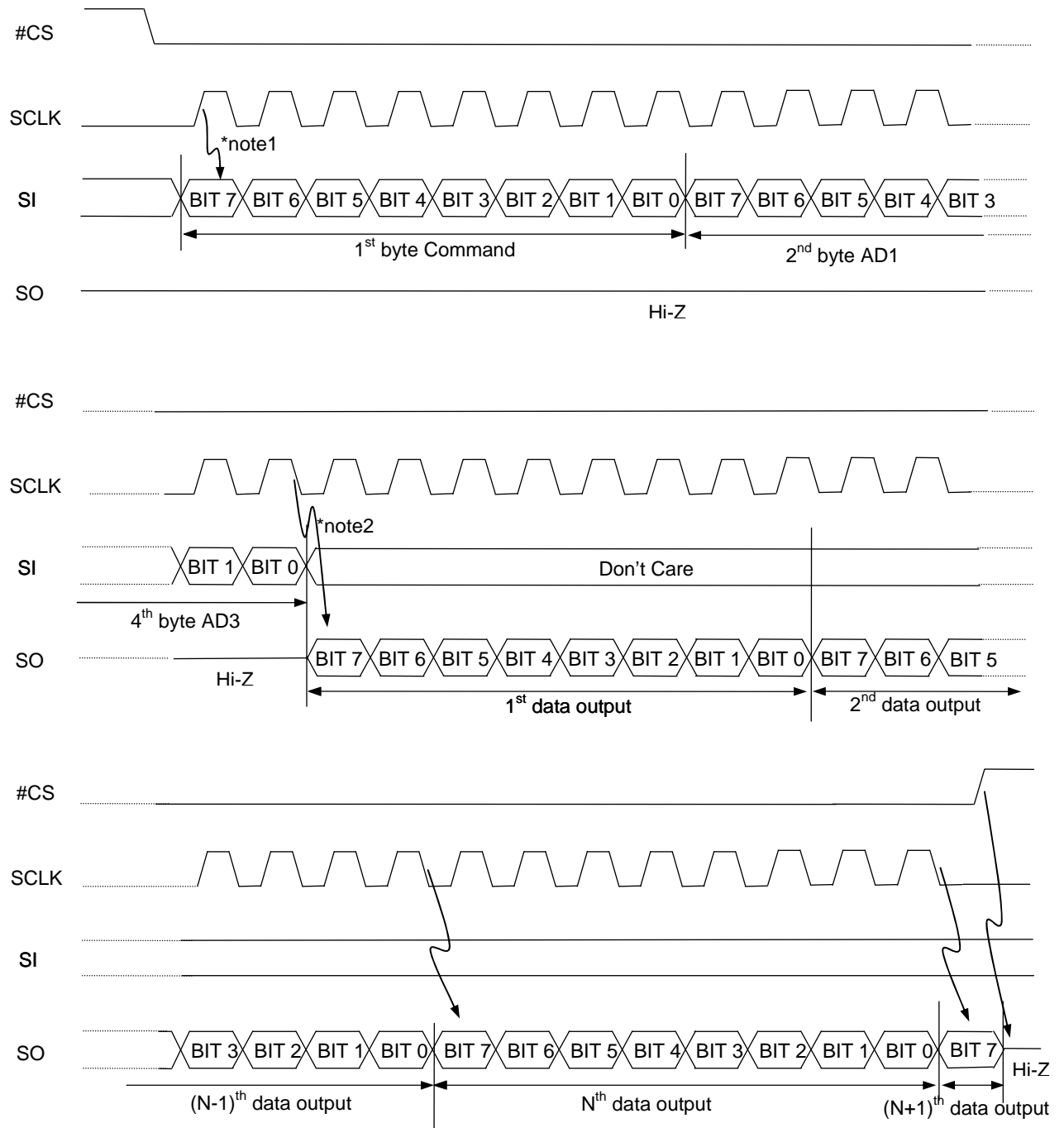
## Output load



**TIMING CHART (READ CYCLE)****Serial Data Input/Output Timing****Standby Timing**

Incorrect command makes this LSI become and keep standby mode until next  $\#CS$  rising edge. In standby mode, SO pin is High-Z.

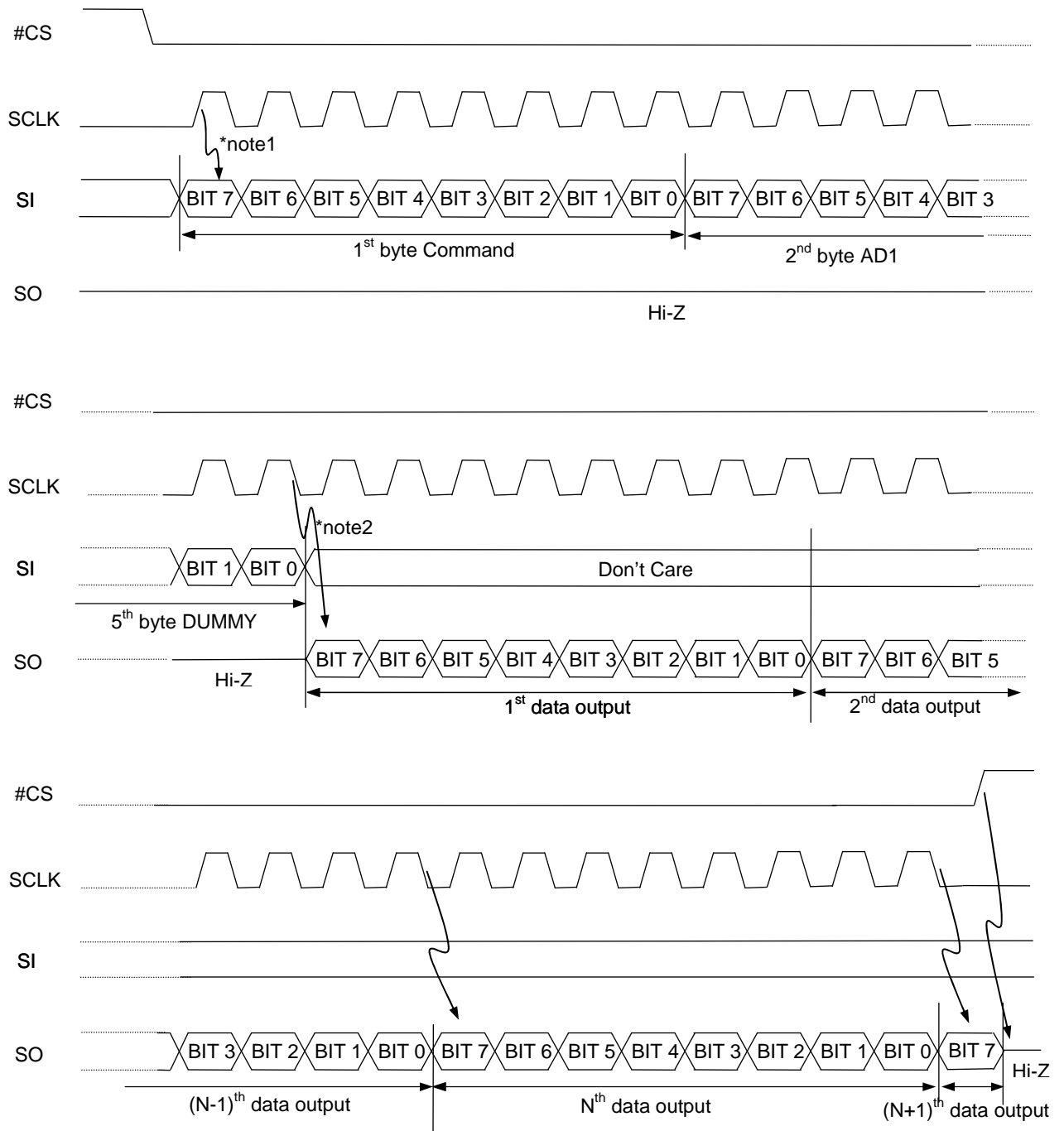
## Read Array Timing Waveform



## Note:

1. Input data are latched at SCLK-rising edge.
2. Data-output starts at SCLK-falling edge in bit0 of the 4th byte.

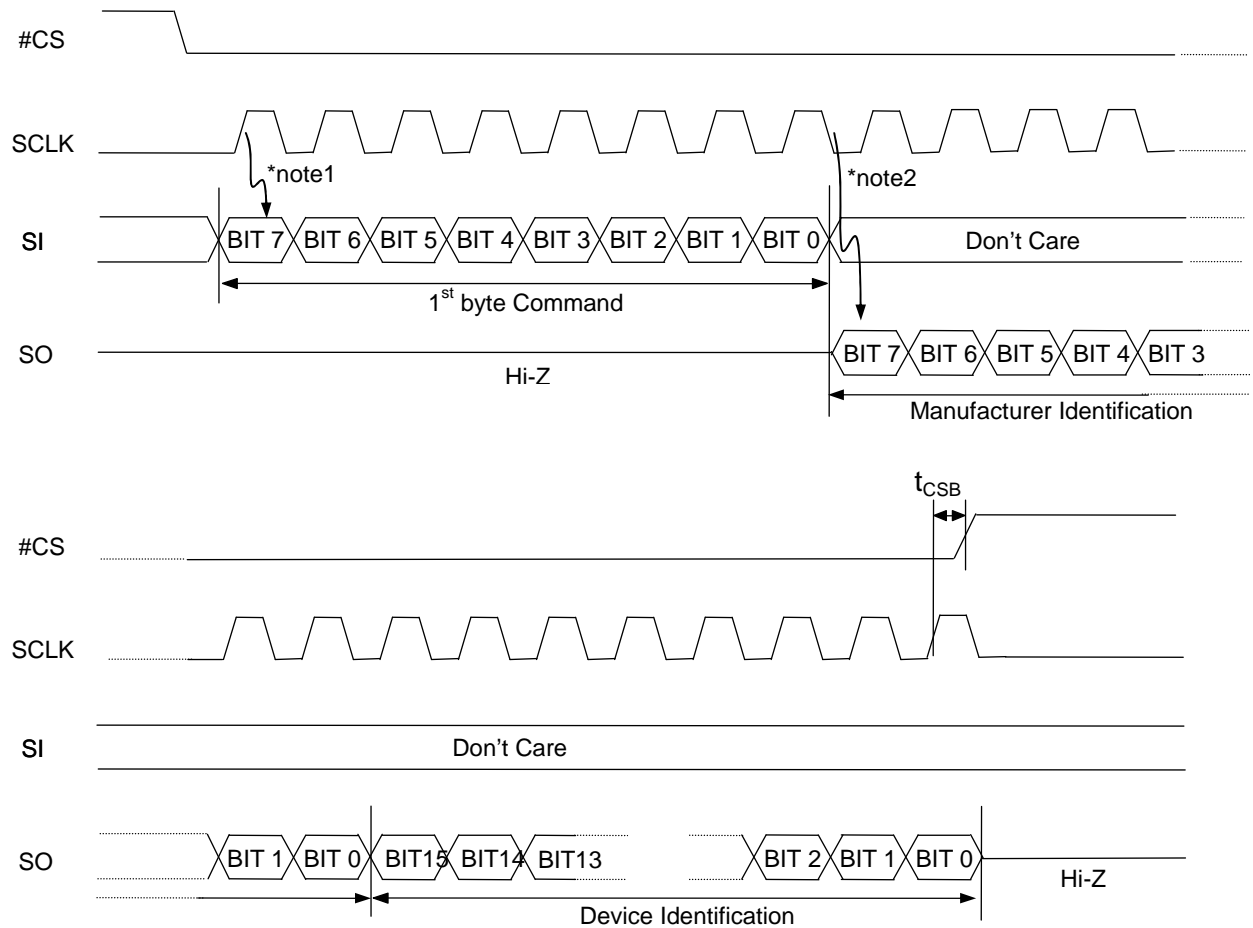
## Fast Read Array Timing Waveform



## Note:

1. Input data are latched at SCLK-rising edge.
2. Data-output starts at SCLK-falling edge in bit0 of the 5<sup>th</sup> byte.

## Read Identification Timing Waveform

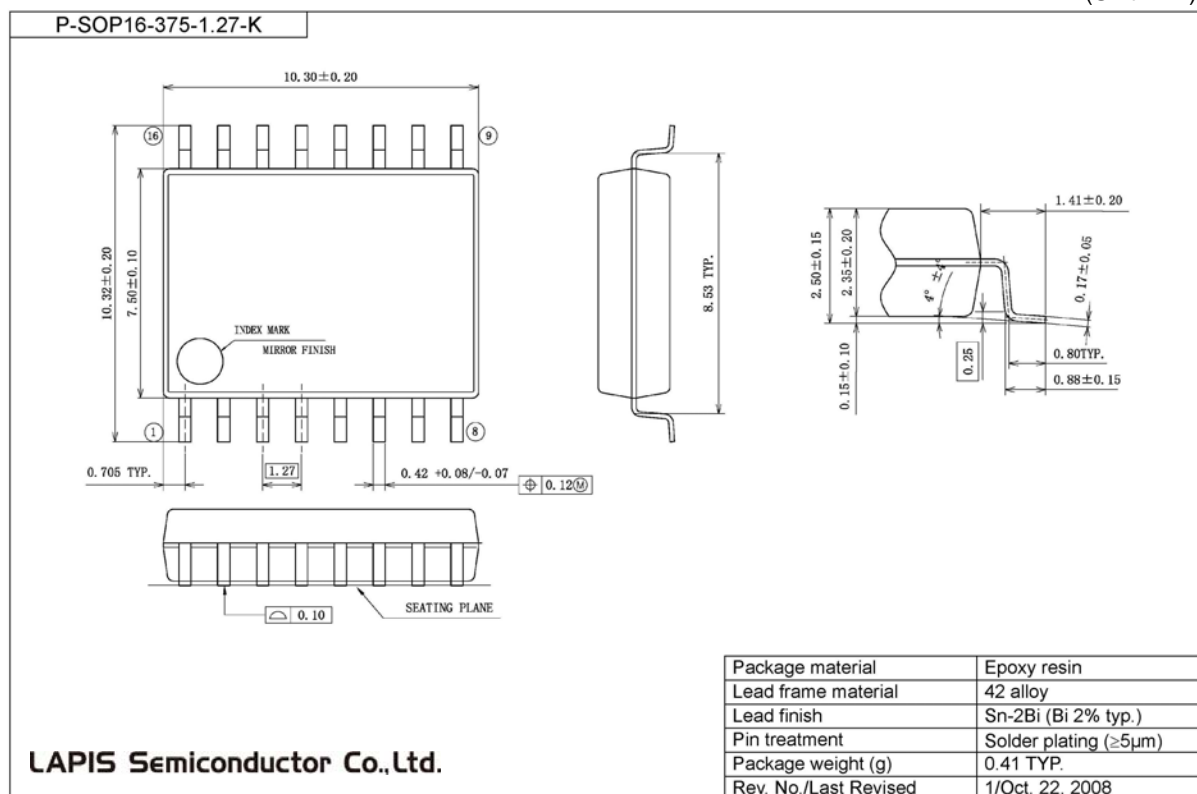


Note:

1. Input data are latched at SCLK-rising edge.
2. Data-output starts at SCLK-falling edge in bit0 of the 1<sup>st</sup> byte.

## PACKAGE DIMENSIONS

(Unit: mm)



## Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

**REVISION HISTORY**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR37V12841A-02-01	Nov. 9, 2006	–	–	Final edition 1
FEDR37V12841A-02-02	Mar. 16, 2007	13	13	Replaced package diagram
FEDR37V12841A-002-02	Oct. 1, 2008	–	–	Changed company logo and name to OKI SEMICONDUCTOR

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