FEDR44V100A-02
Issue Date: Oct. 25, 2018

MR44V100A

1M Bit(131,072-Word -Word × 8-Bit) FeRAM (Ferroelectric Random Access Memory) I2C

GENERAL DESCRIPTION

The MR44V100A is a nonvolatile 131,072-word x 8-bit ferroelectric random access memory (FeRAM) developed in the ferroelectric process and silicon-gate CMOS technology. The MR44V100A is accessed using Two-wire Serial Interface (I2C BUS).Unlike SRAMs, this device, whose cells are nonvolatile, eliminates battery backup required to hold data. This device has no mechanisms of erasing and programming memory cells and blocks, such as those used for various EEPROMs. Therefore, the write cycle time can be equal to the read cycle time and the power consumption during a write can be reduced significantly.
The MR44V100A can be used in various applications, because the device is guaranteed for the write/read tolerance of 10^{13} cycles per bit and the rewrite count can be extended significantly.

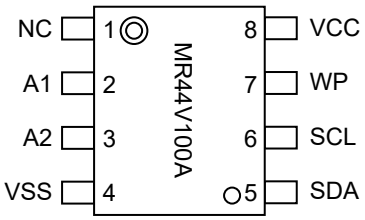
FEATURES

- 131,072-word × 8-bit configuration I2C BUS Interface
- A single 3.3 V typ. (1.8V to 3.6V) power supply
- Operating frequency: 3.4MHz(Max) HS-mode
  1MHz(Max) F/S-mode Plus
- Read/write tolerance 10^{13} cycles/bit
- Data retention 10 years
- Guaranteed operating temperature range –40 to 85°C
- Low power consumption
  Power supply current (@3.4MHz) 1.1mA(Max.)
  Standby mode supply current 10µA(Typ.), 50µA(Max.)
  Sleep mode supply current 0.1µA(Typ.), 2µA(Max.)

- Package options:
  8-pin plastic SOP (P-SOP8-200-1.27-T2K)
- RoHS (Restriction of hazardous substances) compliant

PIN CONFIGURATION

8-pin plastic SOP



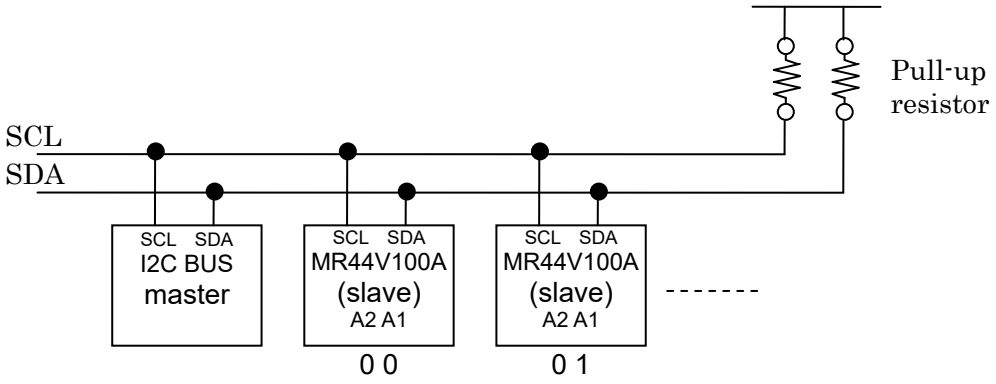
PIN DESCRIPTIONS

Pin Name	Description
NC	Not Connected Pin (open) It should always be left open or connected to any potential (ground, power supply)
A1 – A2	Address (input) Address pin indicates device address. When Address value is match the device address code from SDA, the device will be selected. The address pins are pulled down internally.
SDA	Serial data input serial data output (input / output) SDA is a bi-directional line for I2C interface. The output driver is open-drain. A pull-up resistor is required.
SCL	Serial Clock (input) Serial Clock is the clock input pin for setting for serial data timing. Inputs are latched on the rising edge and outputs occur on the falling edge.
WP	Write protect (input) Write Protect pin controls write-operation to the memory. When WP is high, all address in the memory will be protected. When WP is low, all address in the memory will be written. WP pin is pulled down internally.
V_{CC}, V_{SS}	Power supply Apply the specified voltage to V_{CC}. Connect V_{SS} to ground.

I2C BUS

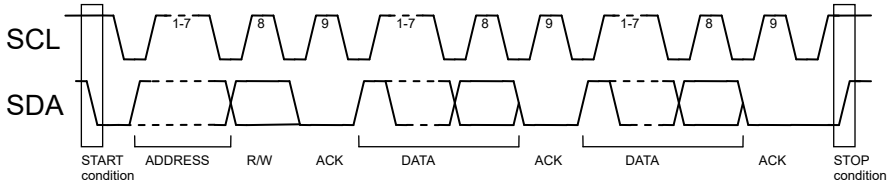
The MR44V100A employs a bi-directional two-wire I2C BUS interface, works as a slave device.

An example of I2C interface system with MR44V100A



I2C BUS COMUNICATION

I2C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, acknowledge is always required after each byte. I2C BUS carries out data transmission with plural devices connected by 2 communication lines of serial data (SDA) and serial clock (SCL).



START CONDITION

Before executing each command, start condition (start bit) where SDA goes from “HIGH” down to “LOW” when SCL is “HIGH” is necessary. MR44V100A always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this condition is satisfied, any command is not executed.

STOP CONDITION

Each command can be ended by SDA rising from “LOW” to “HIGH” when stop condition (stop bit), namely, SCL is “HIGH”.

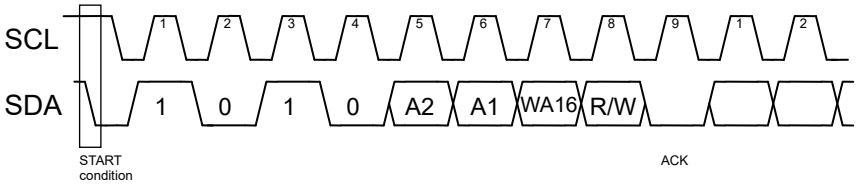
ACKNOWLEDGE (ACK) SIGNAL

This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master and slave, the device (μ-COM at slave address input of write command, read command, and this IC at data output of read command) at the transmitter (sending) side releases the bus after output of 8bit data.
The device (this IC at slave address input of write command, read command, and μ-COM at data output of read command) at the receiver (receiving) side sets SDA "LOW" during 9 clock cycles, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) "LOW".
Each write action outputs acknowledge signal (ACK signal) "LOW", at receiving 8bit data (word address and write data).
Each read action outputs 8bit data (read data), and detects acknowledge signal (ACK signal) "LOW".
When acknowledge signal (ACK signal) is detect, and stop condition is not sent from the master (μ-COM) side, this IC continues data output. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, and recognizes stop condition (stop bit), and ends read action. And this IC gets in status.

SLAVE ADDRESS

Output a slave address after start condition from master.
The significant 4 bits of slave address are used for recognizing a device type. The device code of this IC is fixed to "1010".
Next slave addresses (A2 A1 … device address) are for selecting devices, and plural ones can be used on a same bus according to the number of device addresses, and next comes most significant bit (WA16).
The most insignificant bit (R/W…READ/WRITE) of slave address is used for designating write or read action, and is as shown below.

Setting R/W to 0	write (setting 0 to word address setting of random read)
Setting R/W to 1	read



WRITE PROTECT

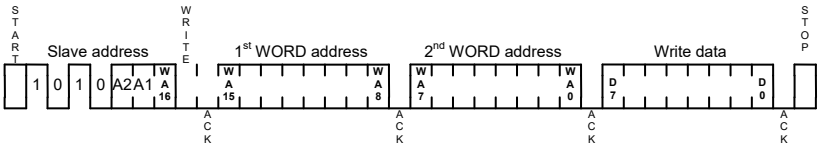
When WP terminal is set Vcc(H level), data rewrite of all addresses is prohibited. When it is set Vss(L level), data rewrite of all address is enabled. Be sure to connect this terminal to Vcc or Vss, or control it to H level or L level. Because this terminal is pulled down internally, in the case of Open the terminal will be recognized as L level
During write cycle WP terminal must be always "L" level. WP terminal must be fixed from start condition to stop condition.

COMMAND

BYTE WRITE CYCLE

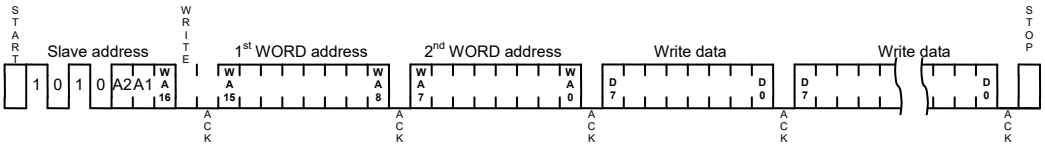
Arbitrary data is written to FeRAM. When to write only 1 byte, byte write is normally used.

start condition
slave address with LSB is 0 (write)
1st and 2nd word address
byte of write data.
stop condition



PAGE WRITE CYCLE

When to write continuous data of 2 bytes or more, simultaneous write is possible by page write cycle. The address reaches the final address, the address will be rolled over to the first address. By page write cycle, up to 128K bytes data can be written. When data above the maximum bytes are sent, data from the first byte will be overwritten.

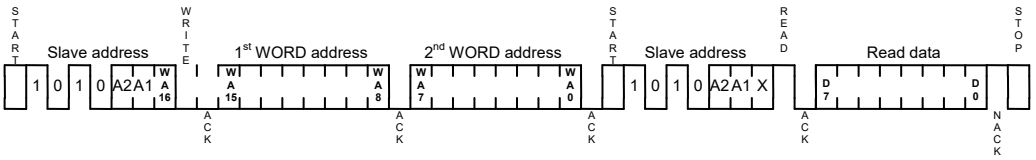


RANDOM READ CYCLE

Random read cycle is a command to read data by designating address.

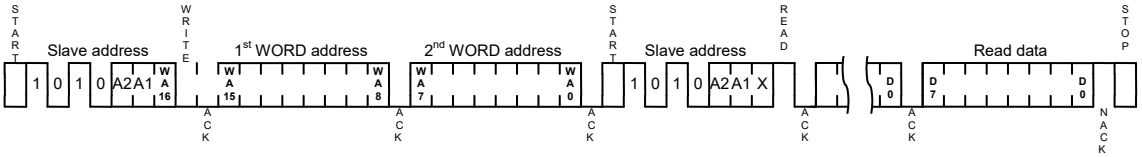
Random read sequence

1. Next to Start condition,
   slave address with LSB is 0 (write)
2. 1st and 2nd word address
3. Next to Start condition,
   slave address with LSB is 1 (read)
   The bit of equivalent to WA16 is ignored.
4. read out byte of data.
5. ACK to “H”
6. Send Stop condition and finish the sequence.



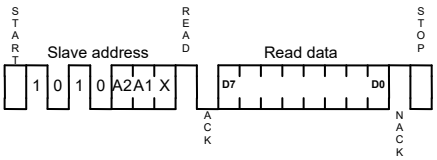
SEQUENTIAL READ CYCLE

When ACK signal “L” after D0 is detected, and stop condition is not sent from master side, the next address data can be read in succession. The address reaches the final address, the address will be rolled over to the first address.



CURRENT ADDRESS READ CYCLE

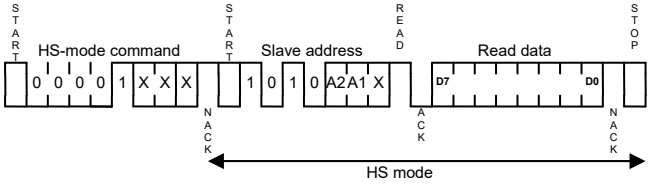
Current address read cycle is a command to read data of internal address register without designating address. When the last read or write address is (n)-th address just before current read cycle, the current address read command outputs data of (n+1)-th address. The previous read or write sequence should be complete up to stop condition. Just after POWER ON or after recovering from SLEEP mode, the internal address resister is unstable.



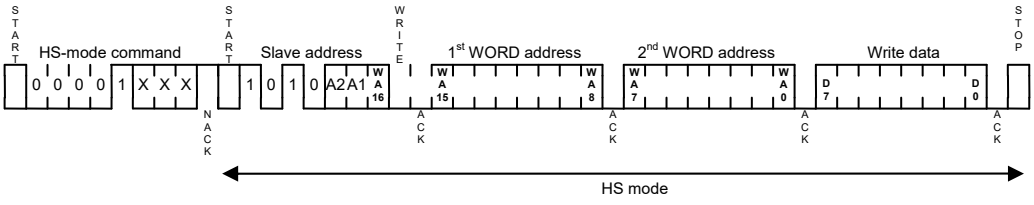
HS-MODE

The MR44V100A support a maximum 3.4MHz high speed mode. When HS-mode operation is needed, the HS-mode command is required before any command. After the HS-mode command is issued, MR44V100A will be the HS-mode, until stop condition is issued.

CURRENT ADDRESS READ CYCLE (HS-MODE)



BYTE WRITE CYCLE (HS-MODE)



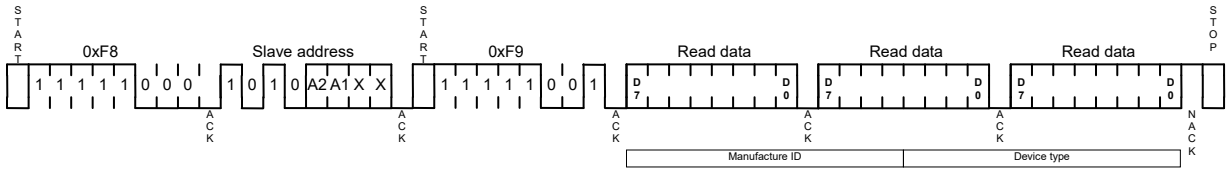
DEVICE ID

The device ID can be read out.
The ID is constructed with 12bit Manufacture ID and 12bit Device type.

Device ID Read Sequence

1. Next to Start condition, send 0xF8. MR44V100A responds ACK signal.
2. Send the Slave address (WA16 and R/W are “Don’t care”). MR44V100A responds ACK signal.
3. Again next to Start condition, send 0xF9.
   MR44V100A responds ACK signal, then outputs 3 bytes of Device ID.
4. Send Stop condition and finish the sequence.

1st Byte	2nd Byte	3rd Byte
0x01	0xb0	0x00
Manufacture ID (LAPIS)		Device Type (MR44V100A)

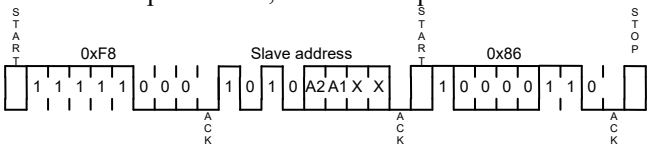


SLEEP

MR44V100A can provide SLEEP Mode which suppresses the current consumption more than Standby status. Transition to SLEEP Mode and Return from SLEEP mode are the following sequences.

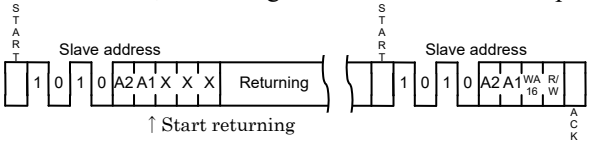
Transition to SLEEP Mode

1. Next to Start condition, send 0xF8. MR44V100A responds ACK signal.
2. Send the Slave address (WA16 and R/W are ”Don’t care”). MR44V100A responds ACK signal.
3. Again Next to Start condition, send 0xF8.
   MR44V100A responds ACK signal and transits to SLEEP Mode.
4. Send Stop condition, finish the sequence.



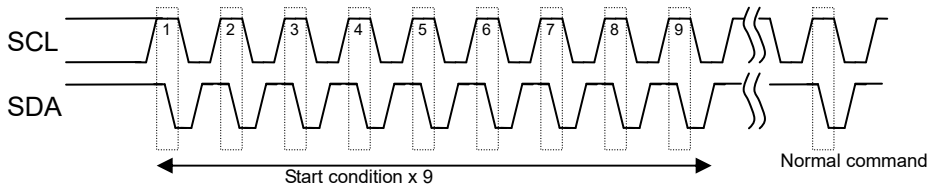
Return from SLEEP Mode

1. Next to Start condition, send the Slave address (WA16 and R/W are “Don’t care”）.
2. When the device address is matched, Start the operation of returning from SLEEP Mode at the falling edge of 6th clocks of SCL after Start condition. When the device address is not matched, SLEEP mode will continue. .
3. Return to standby after the Returning time from SLEEP.
   After that, as sending the Slave address and responding ACK signal, MR44V100A is returning from SLEEP.



Caution : When to input Slave address for returning from SLEEP mode, Stop condition is not recognized.

Software Reset
Software reset is executed to avoid malfunction after power ON, and during command input.



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

The application of stress (voltage, current, or temperature) that exceeds the absolute maximum rating may damage the device. Therefore, do not allow actual characteristics to exceed any one parameter ratings

PIN VOLTAGES

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Pin Voltage (Input Signal)	V_{IN}	–0.5	V_{CC} + 0.5	V	
Pin Voltage (Input/Output Voltage)	V_{INQ}, V_{OUTQ}	–0.5	V_{CC} + 0.5	V	
Power Supply Voltage	V_{CC}	–0.5	4.0	V	

TEMPERATURE RANGE

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Storage Temperature	Tstg	–55	125	°C	
Operating Temperature	Topr	–40	85	°C	

OTHERS

Parameter	Symbol	Rating	Note
Power Dissipation	P_D	1,000mW	Ta=25°C

RECOMMENDED OPERATING CONDITIONS

POWER SUPPLY VOLTAGE

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	V_{CC}	1.8	3.3	3.6	V	
Ground Voltage	V_{SS}	0	0	0	V	

DC INPUT VOLTAGE

Parameter	Symbol	Min.	Max.	Unit	Note
Input High Voltage	V_{IH}	V_{CC} x 0.7	V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	–0.3	V_{CC} x 0.3	V	

DC CHARACTERISTICS

DC INPUT/OUTPUT CHARACTERISTICS

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
Output Low Voltage	V_{OL}	I_{OL} =3mA	—	0.4	V	
Input Leakage Current	I_{LI}	—	–10	10	μA	
Output Leakage Current	I_{LO}	—	–10	10	μA	

POWER SUPPLY CURRENT

V_{CC}=Max.to Min, Ta=Topr

Parameter	Symbol	Condition	Typ.*	Max.	Unit	Note
Power Supply Current (Standby)	I_{CCS}	SCL,SDA= V_{CC}, A2,A1= V_{CC} or V_{SS}	10	50	μA	
Power Supply Current (Sleep)	I_{ZZ}	SCL,SDA= V_{CC}, A2,A1,WP= V_{CC} or V_{SS}	0.1	2	μA	
Power Supply Current (Operating)	I_{CCA}	fSCL=3.4MHz fSCL=1MHz	0.7 350	1.1 450	mA μA	

Note: Typical condition Vcc=3.3V, Ta=Room temperature.

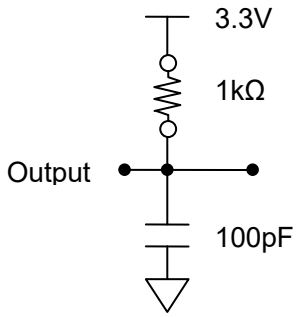
AC CHARACTERISTICS

V_{CC}=Max. to Min., Ta=Topr.

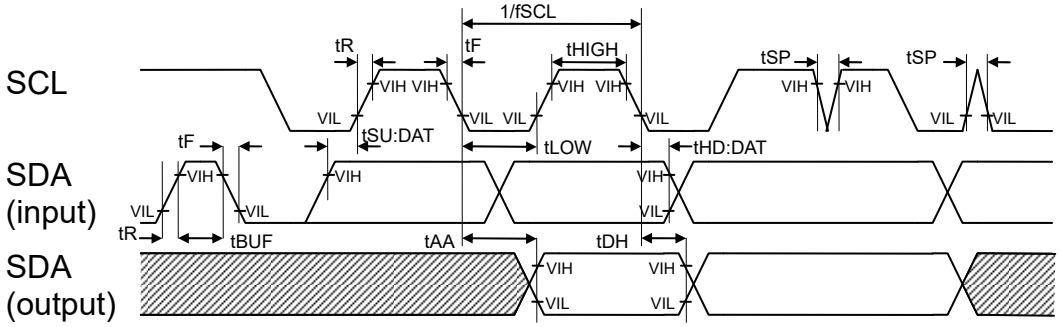
Parameter	Symbol	F/S-mode		F/S-mode Plus		HS-mode		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Clock frequency	f_{SCL}	D.C.	400	D.C.	1000	DC	3400	KHz	
Clock Low time	tLOW	1300	—	500	—	160	—	ns	
Clock High time	tHIGH	600	—	300	—	60	—	ns	
Output Data delay time	tAA	—	900	—	450	—	130	ns	
BUS release time before transfer start	tBUF	1300	—	500	—	300	—	ns	
Start condition hold time	tHD:STA	600	—	250	—	160	—	ns	
Start condition setup time	tSU:STA	600	—	250	—	160	—	ns	
Input data hold time	tHD:DAT	0	—	0	—	0	—	ns	
Input data setup time	tSU:DAT	100	—	100	—	10	—	ns	
SDA, SCL rise time	tR	—	300	—	300	—	80	ns	1
SDA, SCL fall time	tF	—	300	—	120	—	80	ns	1
Stop condition setup time	tSU:STO	600	—	250	—	160	—	ns	
Output data hold time	tDH	0	—	0	—	0	—	ns	
Noise removal time (SDA, SCL)	tSP	—	50	—	50	—	5	ns	
Sleep mode recovery time	tREC	—	100	—	100	—	100	μs	

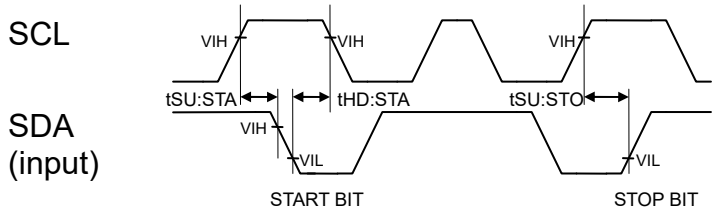
Note: 1. Not 100% tested

Equivalent AC Load Circuit



TIMING


SCL
SDA
(input)
SDA
(output)
1/fSCL
tR
tF
tHIGH
tSP
tSP
tF
tSU:DAT
tLOW
tHD:DAT
tR
tBUF
tAA
tDH
VIH
VIL


SCL
SDA
(input)
VIH
tSU:STA
tHD:STA
tSU:STO
VIL
START BIT
STOP BIT

•POWER-ON AND POWER-OFF CHARACTERISTICS

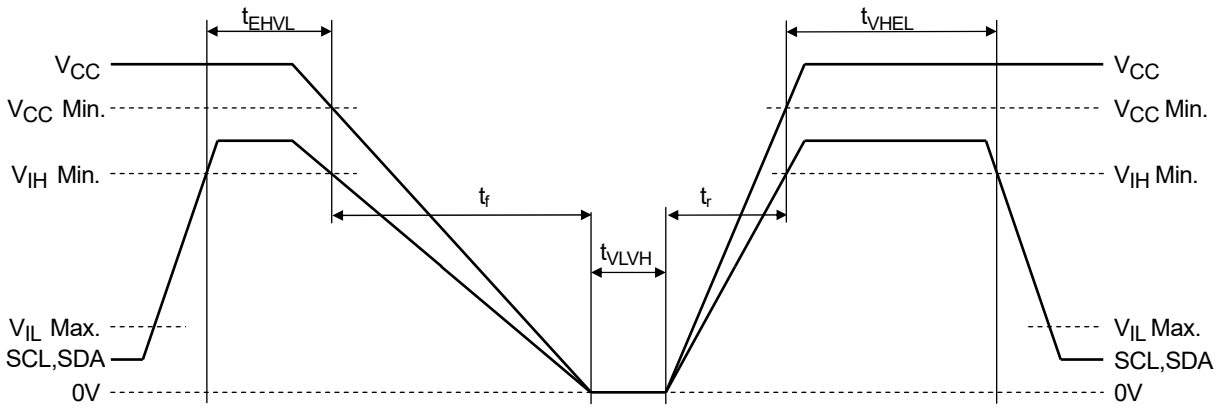
(Under recommended operating conditions)

Parameter	Symbol	Min.	Max.	Unit	Note
Power-On SCL,SDA High Hold Time	t_{VHEL}	100	—	ns	1, 2
Power-Off SCL, SDA High Hold Time	t_{EHVL}	0	—	ns	1
Power-On Interval Time	t_{VLVH}	0	—	μs	2
V_{CC} Power-On ramp rate	tr	30		μs/V	
V_{CC} Power-Off ramp rate	tf	30		μs/V	

Notes:

1. To prevent an erroneous operation, be sure to maintain SCL=SDA="H", and set the FeRAM in an inactive state (standby mode) before and after power-on and power-off.
2. Powering on at the intermediate voltage level will cause an erroneous operation; thus, be sure to power up from 0 V.
3. Enter all signals at the same time as power-on or enter all signals after power-on.

•Power-On and Power-Off Sequences



▪ After Power-Off, terminal state

When MR44V100A only goes power-off while the other IC's on I2C bus are active, all the input pins including I/O pin of MR44V100A must be GND level.

(When to reduce stand-by current while SCL or SDA bus are active, recommend the use of SLEEP mode.)

READ/WRITE CYCLES AND DATA RETENTION

Ta=Topr (Under recommended operating conditions)

Parameter	Min.	Max.	Unit	Note
Read/Write Cycle	10^{13}	—	Cycle	1
Data Retention	10	—	Year	

Note:
1. Total power on time ≤ 10 years

CAPACITANCE

V_{CC} =3.3V, V_{IN} = V_{OUT} = GND, f = 1MHz, and Ta = 25°C

Signal	Symbol	Min.	Max.	Unit	Note
Input Capacitance	C_{IN}	—	10	pF	1
Input/Output Capacitance	C_{OUT}	—	10	pF	1

Note1:
Sampling value.

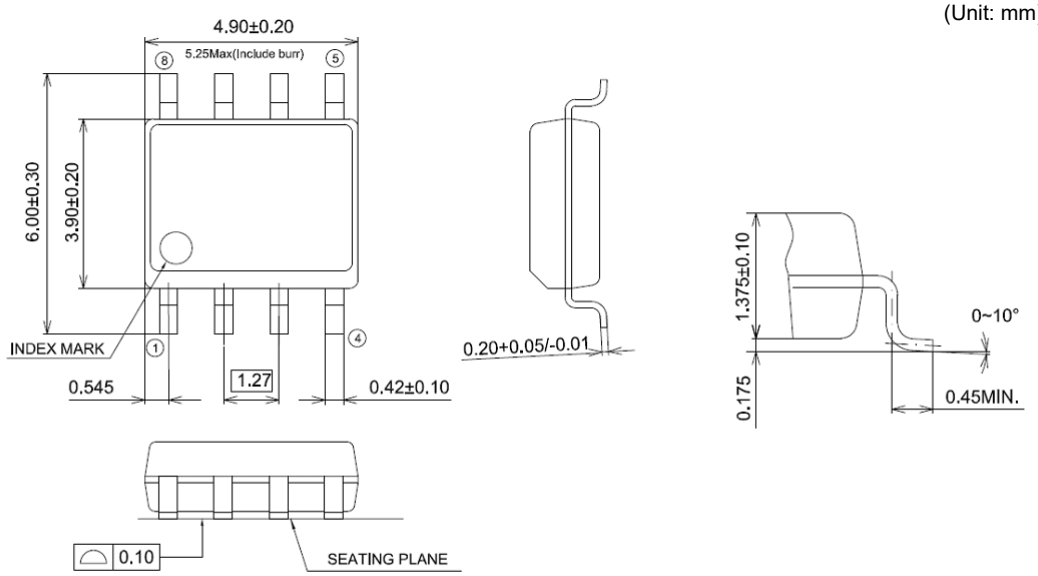
ORDERING INFORMATION

Product No.	Package Type (Package Code)	Packing	Temp. Range
MR44V100AMAZAATL	8-pin plastic SOP (P-SOP8-200-1.27-T2K)	Tape and Reel	−40 to 85°C

PACKAGE DIMENSIONS

P-SOP8-200-1.27-T2K

(Unit: mm)



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Semiconductor Co.,Ltd.

Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Sn (100%)
Solder thickness	10μm Typ.
Package weight (g)	0.077 TYP.
Rev. No./Last Revised	5 / Oct. 19, 2011

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR44V100A-01	Sep. 04, 2017	–	–	Final edition 1
FEDR44V100A-02	Oct. 25, 2018	1, 15 15 – 11	1, 15 15 16 11	Changed Read/write tolerance : 10^{12} cycles →10^{13} cycles Added Note1 Added ordering information Fixed condition of I_{CCA}

Notes

1) The information contained herein is subject to change without notice.
2) Although LAPIS Semiconductor is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury or fire arising from failure, please take safety measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. LAPIS Semiconductor shall have no responsibility for any damages arising out of the use of our Products beyond the rating specified by LAPIS Semiconductor.
3) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.
4) The technical information specified herein is intended only to show the typical functions of the Products and examples of application circuits for the Products. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Semiconductor or any third party with respect to the information contained in this document; therefore LAPIS Semiconductor shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.
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6) The Products specified in this document are not designed to be radiation tolerant.
7) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a LAPIS Semiconductor representative: transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.
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