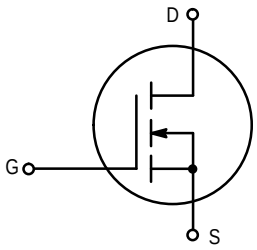
The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode MOSFET

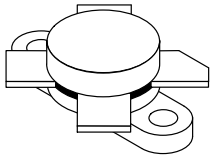
MRF141

150 W, 28 V, 175 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET

Designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 30 MHz, 28 V:
  Output Power — 150 W
  Gain — 18 dB (22 dB Typ)
  Efficiency — 40%
- Typical Performance at 175 MHz, 50 V:
  Output Power — 150 W
  Gain — 13 dB
- Low Thermal Resistance
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability





CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage	V_{DGO}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.71	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

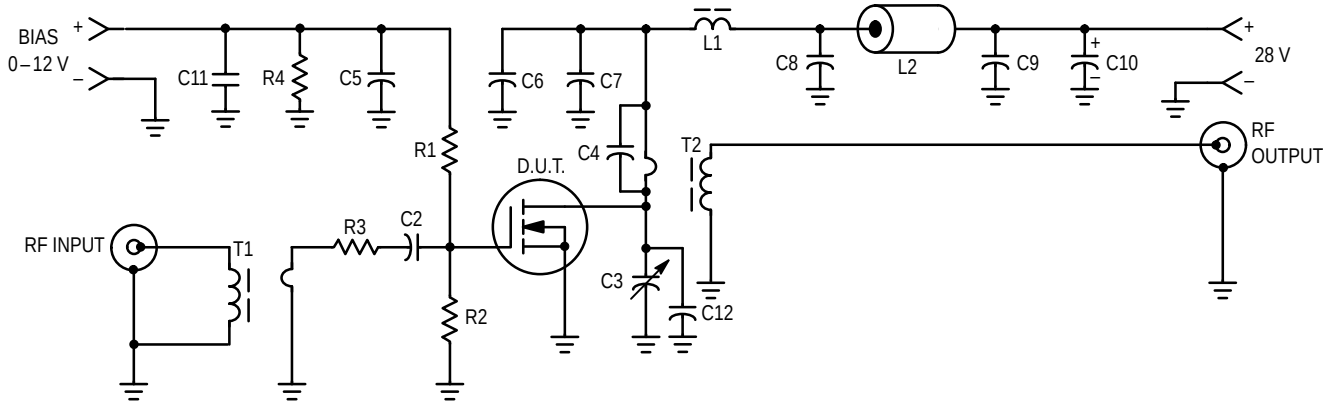
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	0.1	0.9	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	5.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	350	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	420	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	35	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain, f = 30; 30.001 MHz (V_{DD} = 28 V, P_{out} = 150 W (PEP), I_{DQ} = 250 mA) f = 175 MHz	G_{ps}	16 —	20 10	— —	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 250 mA, I_D (Max) = 5.95 A)	η	40	45	—	%
Intermodulation Distortion (1) (V_{DD} = 28 V, P_{out} = 150 W (PEP), f = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 250 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	−30 −60	−28 —	dB
Load Mismatch (V_{DD} = 28 V, P_{out} = 150 W (PEP), f1 = 30; 30.001 MHz, I_{DQ} = 250 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 28 V, P_{out} = 50 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 4.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9-13)}$	— — —	23 −50 −75	— — —	dB

NOTE:
1. To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C2, C5, C6, C7, C8, C9 — 0.1 μF Ceramic Chip or Monolythic with Short Leads
C3 — Arco 469
C4 — 820 pF Unencapsulated Mica or Dipped Mica with Short Leads
C10 — 10 μF/100 V Electrolytic
C11 — 1 μF, 50 V, Tantalum
C12 — 330 pF, Dipped Mica (Short leads)
L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 μH
L2 — Ferrite Bead(s), 2.0 μH
R1, R2 — 51 Ω/1.0 W Carbon
R3 — 1.0 Ω/1.0 W Carbon or Parallel Two 2 Ω, 1/2 W Resistors
R4 — 1 kΩ/1/2 W Carbon
T1 — 16:1 Broadband Transformer
T2 — 1:25 Broadband Transformer
Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, ε_r = 5

Figure 1. 30 MHz Test Circuit (Class AB)

TYPICAL CHARACTERISTICS

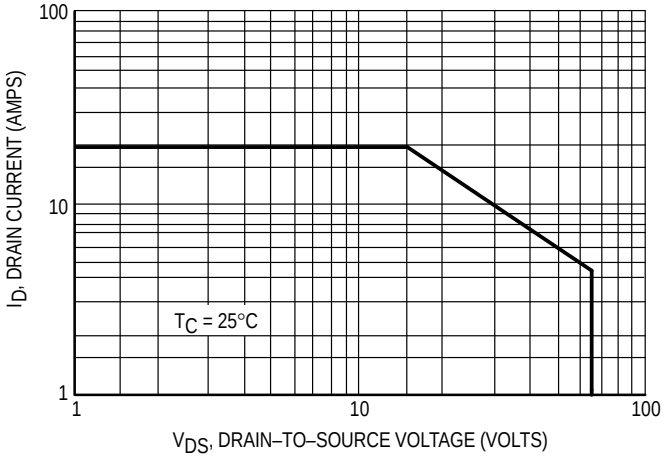


Figure 2. DC Safe Operating Area

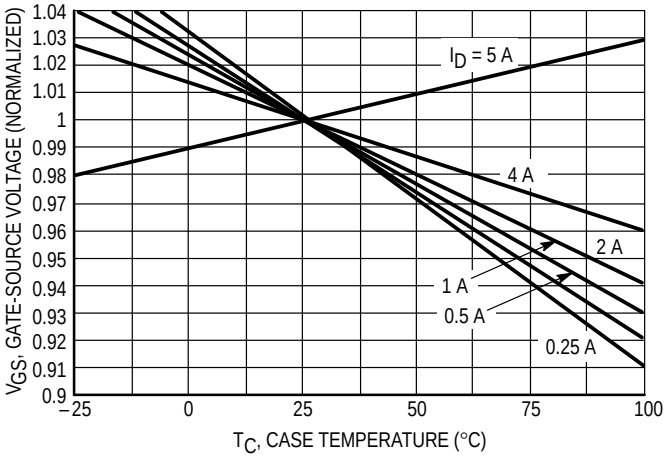


Figure 3. Gate–Source Voltage versus Case Temperature

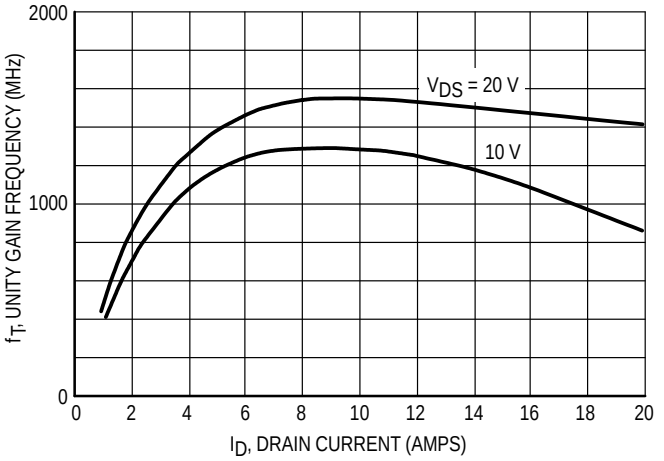


Figure 4. Common Source Unity Gain Frequency versus Drain Current

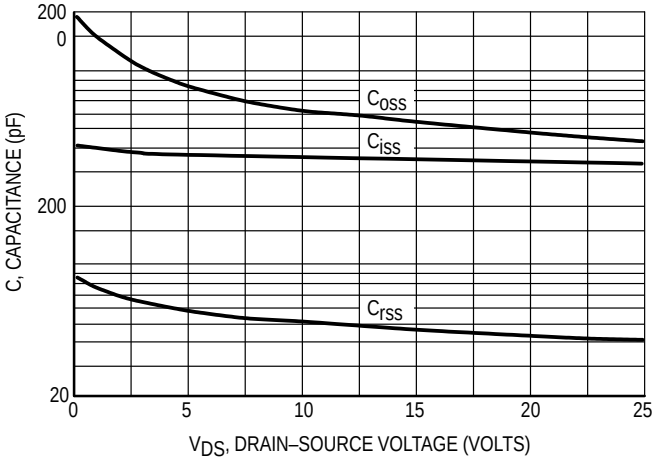


Figure 5. Capacitance versus Drain–Source Voltage

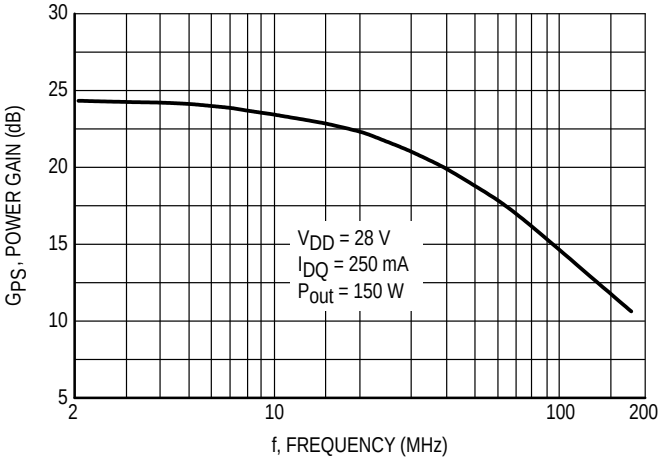


Figure 6. Power Gain versus Frequency

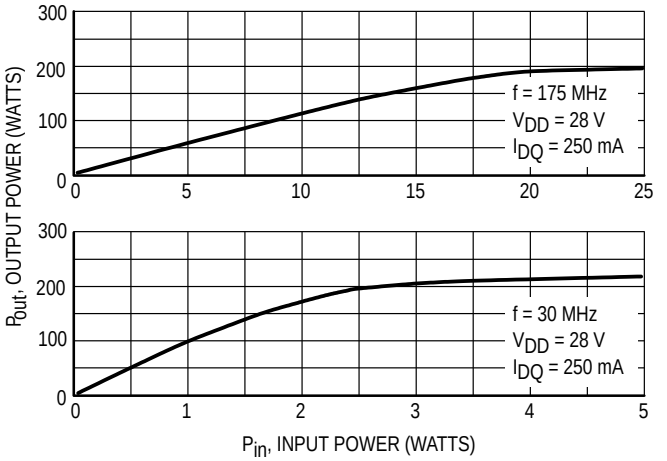


Figure 7. Output Power versus Input Power

TYPICAL CHARACTERISTICS

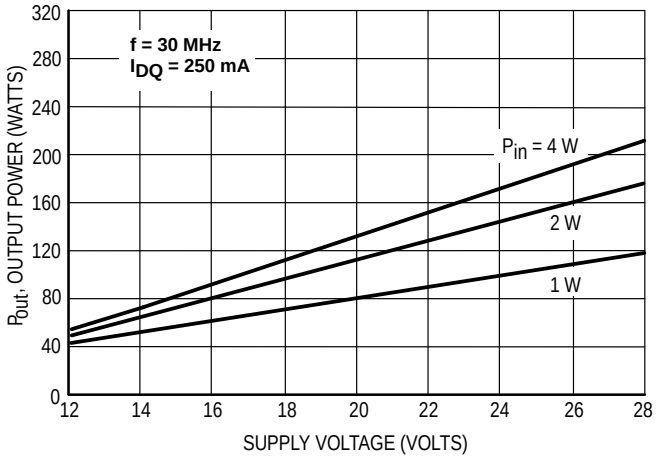


Figure 8. Output Power versus Supply Voltage

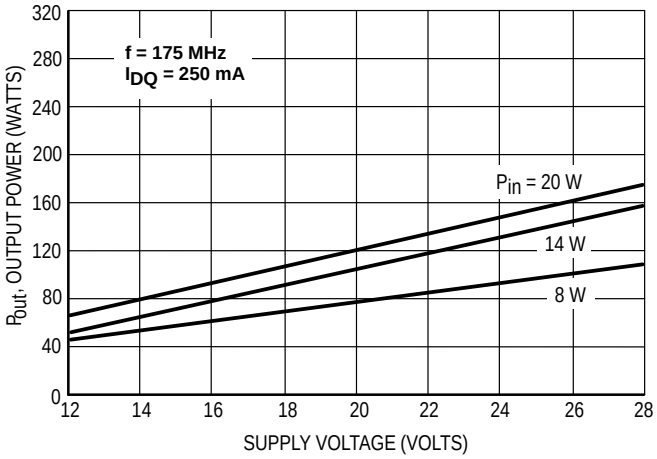


Figure 9. Output Power versus Supply Voltage

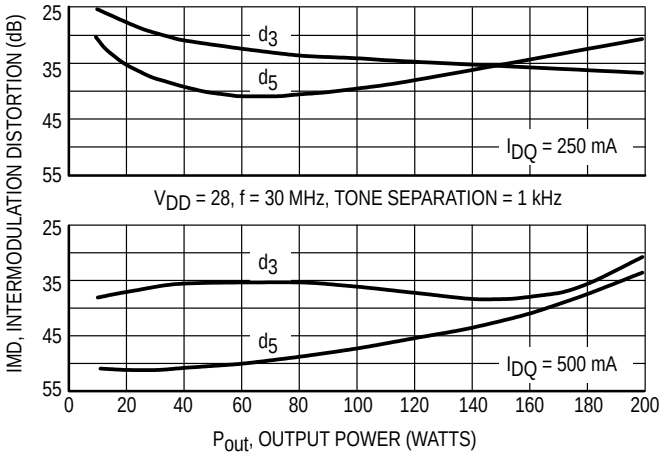


Figure 10. IMD versus P_{out} (PEP)

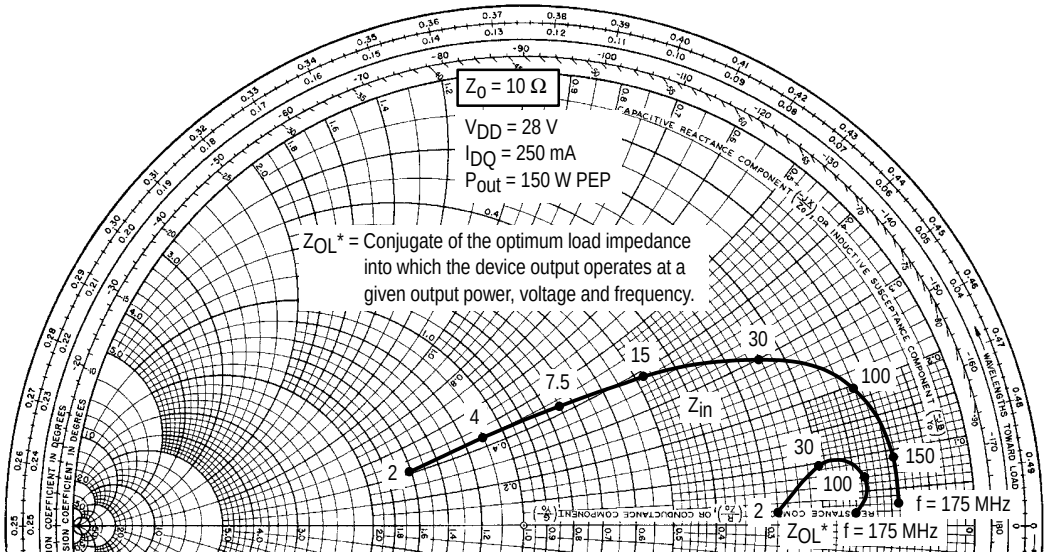
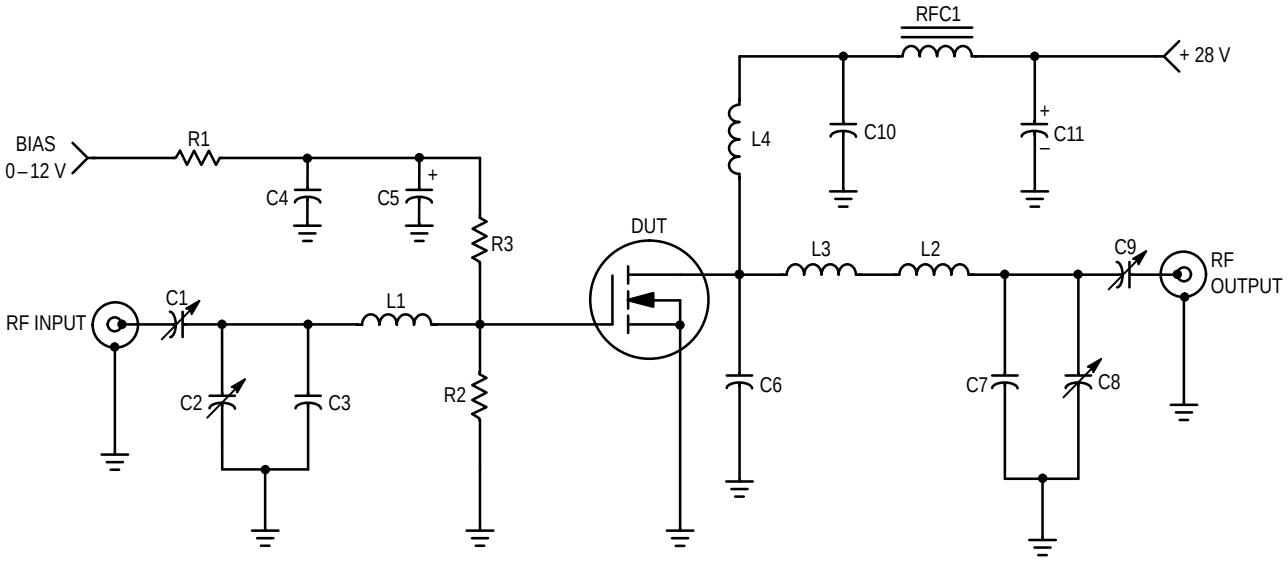


Figure 11. Input and Output Impedances



C1, C2, C8 — Arco 463 or equivalent
C3 — 25 pF, Unelco
C4 — 0.1 μF, Ceramic
C5 — 1.0 μF, 15 WV Tantalum
C6 — 25 pF, Unelco J101
C7 — 25 pF, Unelco J101
C9 — Arco 262 or equivalent
C10 — 0.05 μF, Ceramic
C11 — 15 μF, 35 WV Electrolytic
L1 — 3/4″, #18 AWG into Hairpin
L2 — Printed Line, 0.200″ x 0.500″
L3 — 7/8″, #16 AWG into Hairpin
L4 — 2 Turns, #16 AWG, 5/16 ID
RFC1 — 5.6 μH, Molded Choke
RFC2 — VK200–4B
R1 — 150 Ω, 1.0 W Carbon
R2 — 10 kΩ, 1/2 W Carbon
R3 — 120 Ω, 1/2 W Carbon

Figure 12. 175 MHz Test Circuit (Class AB)

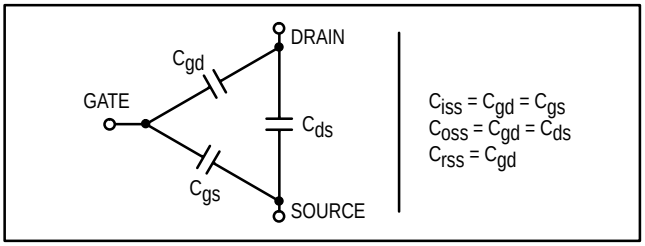
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 4 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of this device is essentially capacitor. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the device due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — This device does not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

DESIGN CONSIDERATIONS

The MRF141 is an RF Power, MOS, N–channel enhancement mode field–effect transistor (FET) designed for HF and VHF power amplifier applications.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

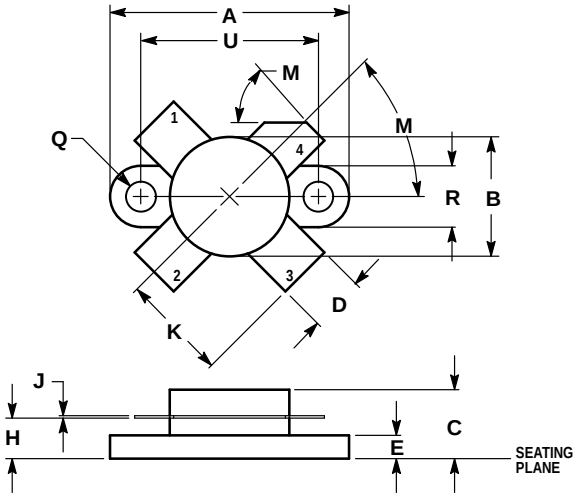
The MRF141 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF141 was characterized at I_{DQ} = 250 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

GAIN CONTROL

Power output of the MRF141 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.960	0.990	24.39	25.14
B	0.465	0.510	11.82	12.95
C	0.229	0.275	5.82	6.98
D	0.216	0.235	5.49	5.96
E	0.084	0.110	2.14	2.79
H	0.144	0.178	3.66	4.52
J	0.003	0.007	0.08	0.17
K	0.435	—	11.05	—
M	45° NOM		45° NOM	
Q	0.115	0.130	2.93	3.30
R	0.246	0.255	6.25	6.47
U	0.720	0.730	18.29	18.54

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 211–11
ISSUE N

How to reach us:

USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
– US & Canada ONLY 1–800–774–1848

INTERNET: http://motorola.com/sps

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 4–32–1,
Nishi–Gotanda, Shinagawa–ku, Tokyo 141, Japan. 81–3–5487–8488

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298