The RF MOSFET Line

RF Power Field-Effect Transistor

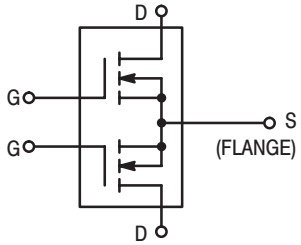
N–Channel Enhancement–Mode MOSFET

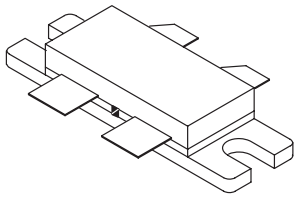
MRF151G

300 W, 50 V, 175 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET

Designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 175 MHz, 50 V:
  Output Power — 300 W
  Gain — 14 dB (16 dB Typ)
  Efficiency — 50%
- Low Thermal Resistance — 0.35°C/W
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- S–Parameters Available for Download into Frequency Domain Simulators. See http://motorola.com/sps/rf/designtds/





CASE 375–04, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Drain–Gate Voltage	V_{DGO}	125	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	40	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	500 2.85	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

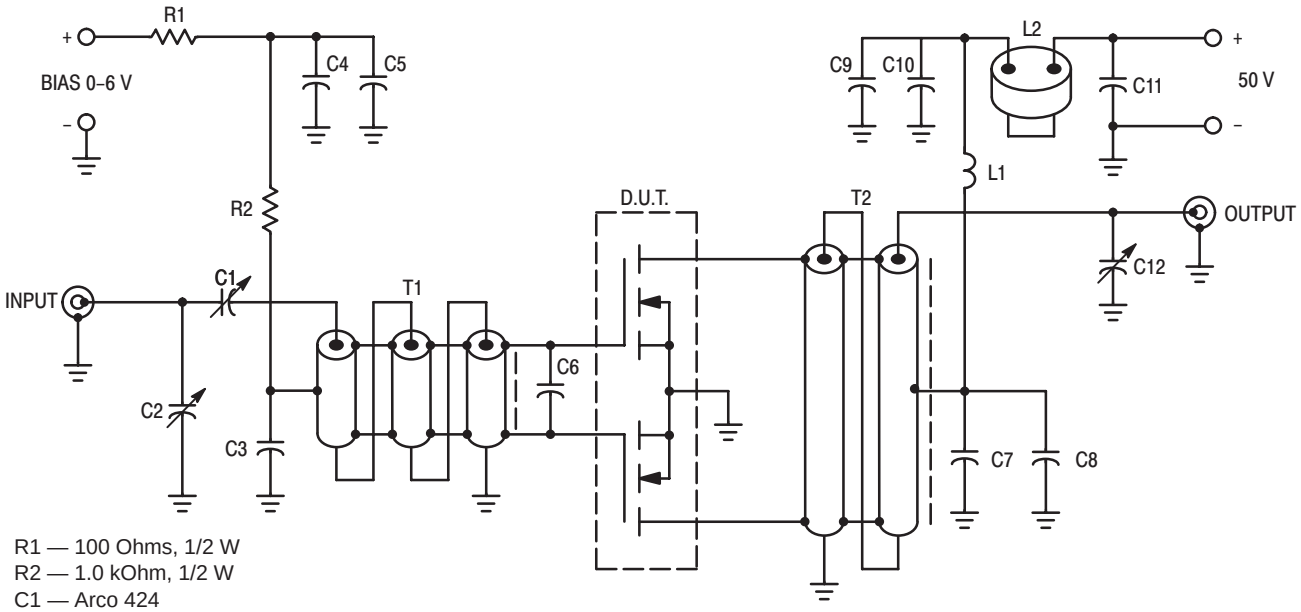
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.35	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Each Side)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (Each Side)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	5.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS (Each Side)					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	350	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	220	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	15	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 300 W, I_{DQ} = 500 mA, f = 175 MHz)	G_{ps}	14	16	—	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 300 W, f = 175 MHz, I_D (Max) = 11 A)	η	50	55	—	%
Load Mismatch (V_{DD} = 50 V, P_{out} = 300 W, I_{DQ} = 500 mA, VSWR 5:1 at all Phase Angles)	ψ	No Degradation in Output Power			



R1 — 100 Ohms, 1/2 W
R2 — 1.0 kOhm, 1/2 W
C1 — Arco 424
C2 — Arco 404
C3, C4, C7, C8, C9 — 1000 pF Chip
C5, C10 — 0.1 μF Chip
C6 — 330 pF Chip
C11 — 0.47 μF Ceramic Chip, Kemet 1215 or Equivalent (100 V)
C12 — Arco 422
L1 — 10 Turns AWG #18 Enameled Wire, Close Wound, 1/4″ I.D.
L2 — Ferrite Beads of Suitable Material for 1.5–2.0 μH Total Inductance

Unless Otherwise Noted, All Chip Capacitors are ATC Type 100 or Equivalent.

T1 — 9:1 RF Transformer. Can be made of 15–18 Ohms Semirigid Co–Ax, 62–90 Mils O.D.
T2 — 1:4 RF Transformer. Can be made of 16–18 Ohms Semirigid Co–Ax, 70–90 Mils O.D.
Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, ε_r = 5.0

NOTE: For stability, the input transformer T1 must be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

See Figure 6 for construction details of T1 and T2.

Figure 1. 175 MHz Test Circuit

TYPICAL CHARACTERISTICS

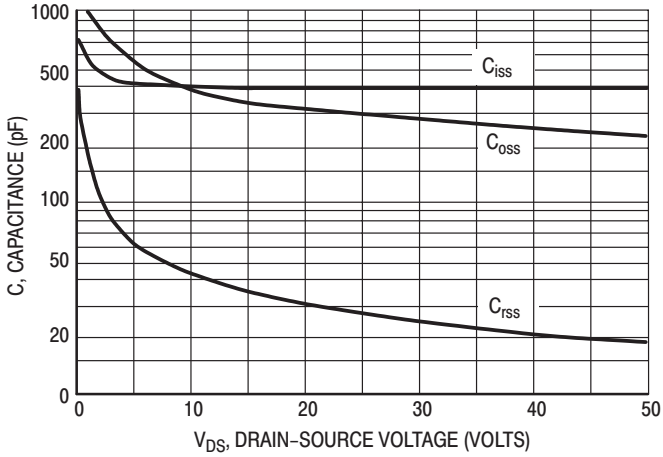


Figure 2. Capacitance versus Drain–Source Voltage*

*Data shown applies to each half of MRF151G.

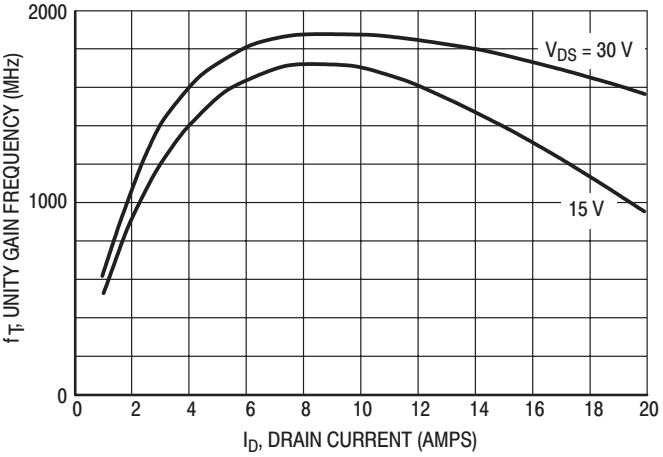


Figure 3. Common Source Unity Gain Frequency versus Drain Current*

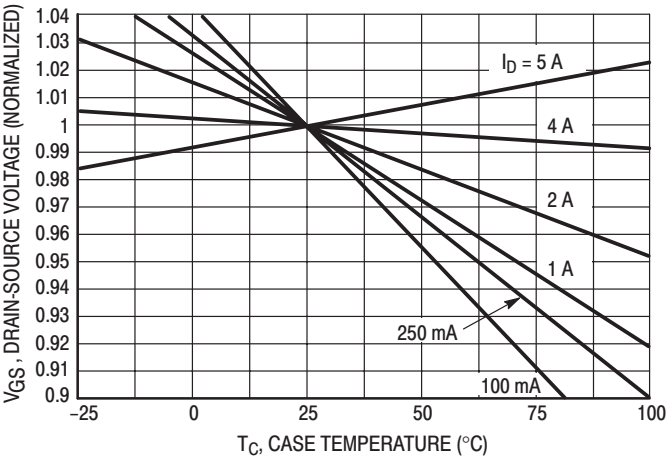


Figure 4. Gate–Source Voltage versus Case Temperature*

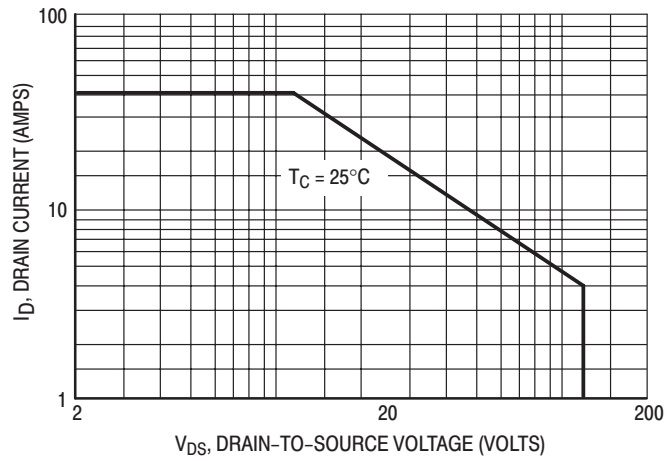


Figure 5. DC Safe Operating Area

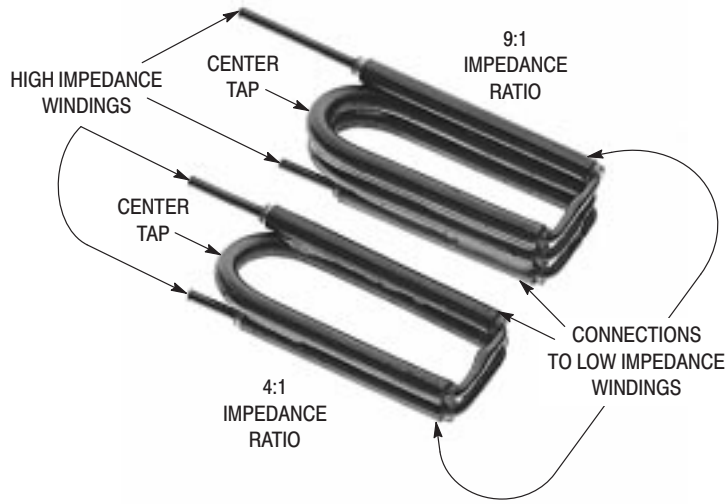


Figure 6. RF Transformer

TYPICAL CHARACTERISTICS

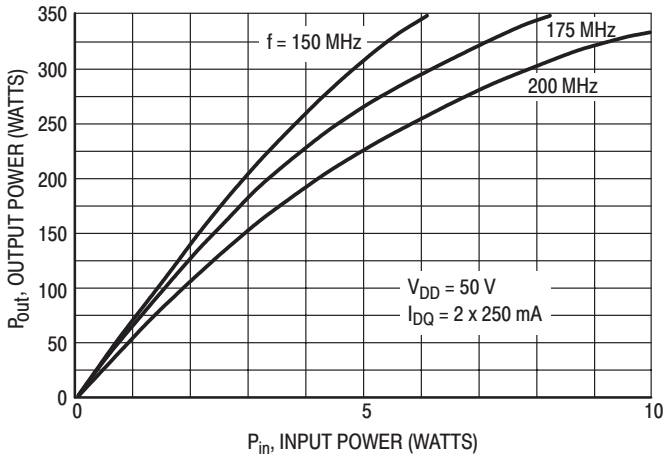


Figure 7. Output Power versus Input Power

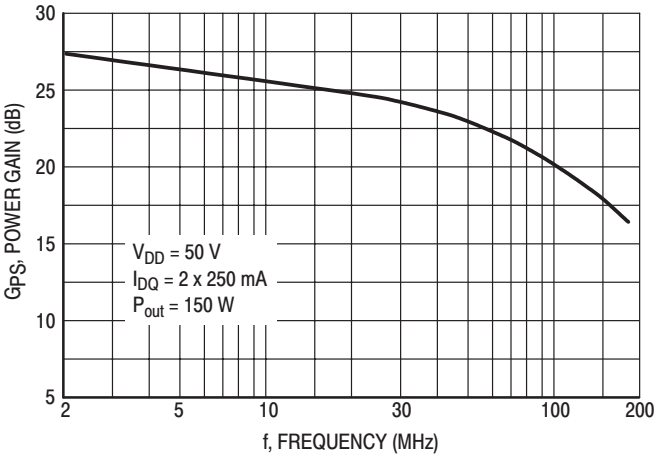
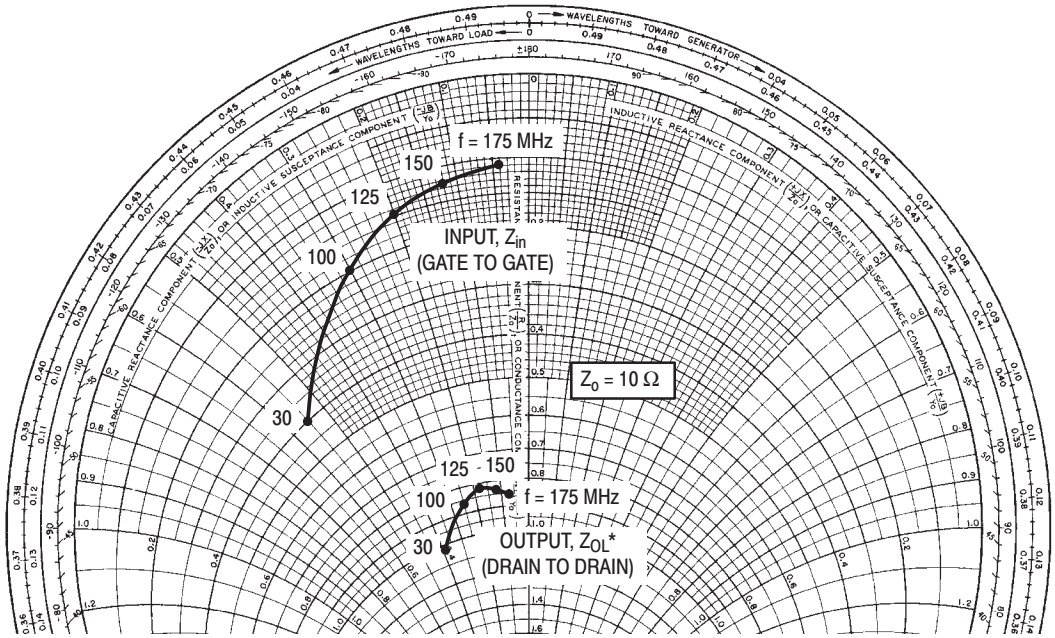


Figure 8. Power Gain versus Frequency



Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 9. Input and Output Impedance

NOTE: S–Parameter data represents measurements taken from one chip only.

Table 1. Common Source S–Parameters (V_{DS} = 50 V, I_D = 2 A)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
30	0.877	–174	10.10	77	0.008	19	0.707	–169
40	0.886	–175	7.47	69	0.009	24	0.715	–172
50	0.895	–175	5.76	63	0.008	33	0.756	–171
60	0.902	–176	4.73	58	0.009	39	0.764	–171
70	0.912	–176	3.86	52	0.009	46	0.784	–172
80	0.918	–177	3.19	48	0.010	54	0.802	–171
90	0.925	–177	2.69	45	0.011	62	0.808	–171
100	0.932	–177	2.34	40	0.013	67	0.850	–173
110	0.936	–178	2.06	37	0.014	72	0.865	–175
120	0.942	–178	1.77	35	0.015	76	0.875	–173
130	0.946	–179	1.55	32	0.017	77	0.874	–172
140	0.950	–179	1.39	30	0.019	77	0.884	–174
150	0.954	–180	1.23	27	0.021	78	0.909	–175
160	0.957	–180	1.13	24	0.023	79	0.911	–176
170	0.960	180	1.01	22	0.024	82	0.904	–177
180	0.962	179	0.90	20	0.026	82	0.931	–176
190	0.964	179	0.84	19	0.028	80	0.929	–178
200	0.967	179	0.75	18	0.030	79	0.922	–179
210	0.967	178	0.71	16	0.032	80	0.937	–180
220	0.969	178	0.67	14	0.035	82	0.949	180
230	0.971	178	0.60	12	0.038	81	0.950	179
240	0.970	177	0.57	12	0.037	80	0.950	179
250	0.972	177	0.51	12	0.039	80	0.935	179
260	0.973	177	0.47	11	0.041	79	0.954	178
270	0.972	176	0.45	9	0.044	80	0.953	176
280	0.974	176	0.41	9	0.046	80	0.965	175
290	0.974	176	0.40	6	0.046	79	0.944	175
300	0.975	176	0.39	10	0.048	82	0.929	176
310	0.976	175	0.36	9	0.049	82	0.943	176
320	0.974	175	0.33	7	0.053	78	0.954	173
330	0.975	174	0.31	4	0.056	78	0.935	172
340	0.976	174	0.30	10	0.056	77	0.948	172
350	0.975	174	0.29	7	0.058	80	0.950	174
360	0.977	174	0.28	8	0.059	79	0.978	172
370	0.976	173	0.26	8	0.061	76	0.981	170
380	0.976	173	0.26	7	0.065	75	0.944	171
390	0.977	173	0.24	10	0.066	76	0.960	171
400	0.976	172	0.23	7	0.068	80	0.955	173
410	0.976	172	0.22	9	0.071	77	0.999	170
420	0.977	172	0.21	9	0.071	76	0.962	168
430	0.976	171	0.19	10	0.073	76	0.950	168

Table 1. Common Source S–Parameters (V_{DS} = 50 V, I_D = 2 A) (continued)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
440	0.976	171	0.20	12	0.075	75	0.953	168
450	0.978	171	0.19	10	0.080	77	0.982	168
460	0.978	170	0.18	13	0.082	74	0.990	165
470	0.978	170	0.18	10	0.081	77	0.953	168
480	0.974	170	0.18	13	0.085	78	0.944	167
490	0.973	169	0.17	13	0.086	75	0.966	165
500	0.972	169	0.17	14	0.089	73	0.980	165

Table 2. Common Source S–Parameters (V_{DS} = 50 V, I_D = 0.38 A)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
30	0.834	–168	9.70	74	0.014	–10	0.747	–162
40	0.869	–169	6.47	62	0.013	–19	0.731	–159
50	0.883	–170	5.13	55	0.012	–24	0.754	–161
60	0.892	–171	4.03	51	0.011	–24	0.823	–164
70	0.901	–172	3.39	50	0.010	–20	0.912	–167
80	0.911	–173	2.80	47	0.009	–16	0.996	–168
90	0.924	–173	2.39	42	0.008	–14	1.100	–167
100	0.935	–174	1.99	35	0.006	–15	1.100	–167
110	0.945	–174	1.67	29	0.005	–17	1.070	–169
120	0.953	–175	1.36	25	0.004	–10	0.988	–167
130	0.958	–175	1.14	23	0.004	4	0.934	–169
140	0.962	–176	1.01	23	0.004	26	0.935	–170
150	0.964	–177	0.93	24	0.004	45	0.983	–172
160	0.966	–177	0.85	24	0.004	58	1.080	–173
170	0.969	–178	0.79	21	0.005	61	1.170	–173
180	0.972	–178	0.74	17	0.006	57	1.250	–173
190	0.975	–178	0.65	10	0.007	56	1.210	–174
200	0.977	–179	0.56	8	0.008	63	1.110	–174
210	0.979	–179	0.50	7	0.008	72	1.010	–174
220	0.980	–179	0.44	9	0.008	81	0.958	–172
230	0.980	–180	0.41	9	0.009	79	1.020	–175
240	0.981	180	0.38	12	0.009	74	1.020	–178
250	0.982	180	0.38	11	0.011	74	1.060	–176
260	0.983	179	0.34	8	0.014	76	1.180	–179
270	0.984	179	0.34	4	0.014	80	1.220	–180
280	0.984	179	0.30	3	0.013	79	1.180	–179
290	0.984	178	0.27	–4	0.012	73	1.040	–177
300	0.984	178	0.25	0	0.014	69	0.996	–178
310	0.984	178	0.24	4	0.017	74	0.951	–178
320	0.985	177	0.23	7	0.019	83	0.964	179
330	0.985	177	0.20	3	0.019	90	1.060	180
340	0.986	177	0.22	7	0.017	87	1.100	179

Table 2. Common Source S–Parameters (V_{DS} = 50 V, I_D = 0.38 A) (continued)

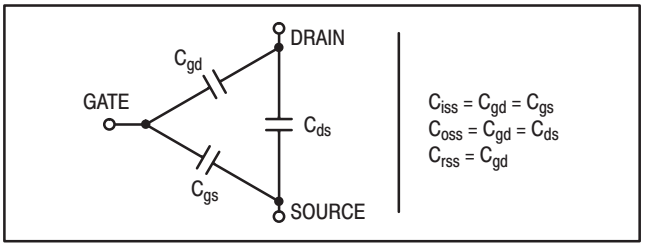
f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
350	0.986	177	0.20	5	0.017	76	1.140	–180
360	0.986	176	0.19	–2	0.021	67	1.160	180
370	0.985	176	0.17	–3	0.024	69	1.100	180
380	0.985	176	0.16	–3	0.024	77	1.070	–180
390	0.985	176	0.15	0	0.021	85	0.993	–180
400	0.985	175	0.14	3	0.018	85	0.962	–180
410	0.985	175	0.14	2	0.021	72	1.040	179
420	0.986	175	0.13	5	0.027	68	1.060	177
430	0.986	174	0.13	4	0.031	73	1.100	177
440	0.986	174	0.13	0	0.030	81	1.140	177
450	0.985	174	0.13	–1	0.025	87	1.110	178
460	0.984	174	0.11	–2	0.022	68	1.090	176
470	0.984	174	0.10	–1	0.025	59	1.020	177
480	0.985	173	0.10	3	0.034	66	0.993	179
490	0.986	173	0.10	1	0.038	79	1.020	178
500	0.986	173	0.10	6	0.035	93	1.010	177

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 3 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

DESIGN CONSIDERATIONS

The MRF151G is an RF Power, MOS, N–channel enhancement mode field–effect transistor (FET) designed for HF and VHF power amplifier applications.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

The MRF151G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF151G was characterized at I_{DQ} = 250 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

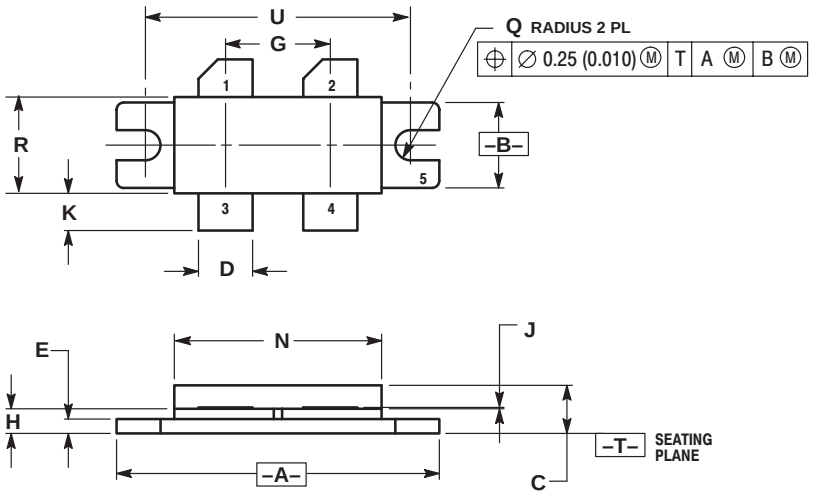
The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF151G may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

NOTES

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.330	1.350	33.79	34.29
B	0.370	0.410	9.40	10.41
C	0.190	0.230	4.83	5.84
D	0.215	0.235	5.47	5.96
E	0.050	0.070	1.27	1.77
G	0.430	0.440	10.92	11.18
H	0.102	0.112	2.59	2.84
J	0.004	0.006	0.11	0.15
K	0.185	0.215	4.83	5.33
N	0.845	0.875	21.46	22.23
Q	0.060	0.070	1.52	1.78
R	0.390	0.410	9.91	10.41
U	1.100 BSC		27.94 BSC	

STYLE 2:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

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