Freescale Semiconductor
Technical Data

Document Number: MRF1570N
Rev. 9, 6/2008

RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies up to 470 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 12.5 volt mobile FM equipment.

- Specified Performance @ 470 MHz, 12.5 Volts
  Output Power — 70 Watts
  Power Gain — 11.5 dB
  Efficiency — 60%
- Capable of Handling 20:1 VSWR, @ 15.6 Vdc, 470 MHz, 2 dB Overdrive

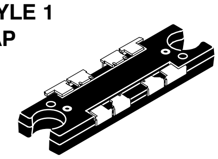
Features

- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Broadband-Full Power Across the Band: 135-175 MHz
  400-470 MHz
- Broadband Demonstration Amplifier Information Available Upon Request
- 200°C Capable Plastic Package
- N Suffix Indicates Lead-Free Terminations. RoHS Compliant.
- In Tape and Reel. T1 Suffix = 500 Units per 44 mm, 13 inch Reel.

MRF1570NT1
MRF1570FNT1

470 MHz, 70 W, 12.5 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs

CASE 1366-05, STYLE 1
TO-272-8 WRAP
PLASTIC
MRF1570NT1



CASE 1366A-03, STYLE 1
TO-272-8
PLASTIC
MRF1570FNT1

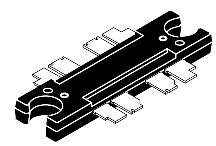


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	+0.5, +40	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	165 0.5	W W/°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.29	°C/W

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)
Charge Device Model	C2 (Minimum)

Table 4. Moisture Sensitivity Level

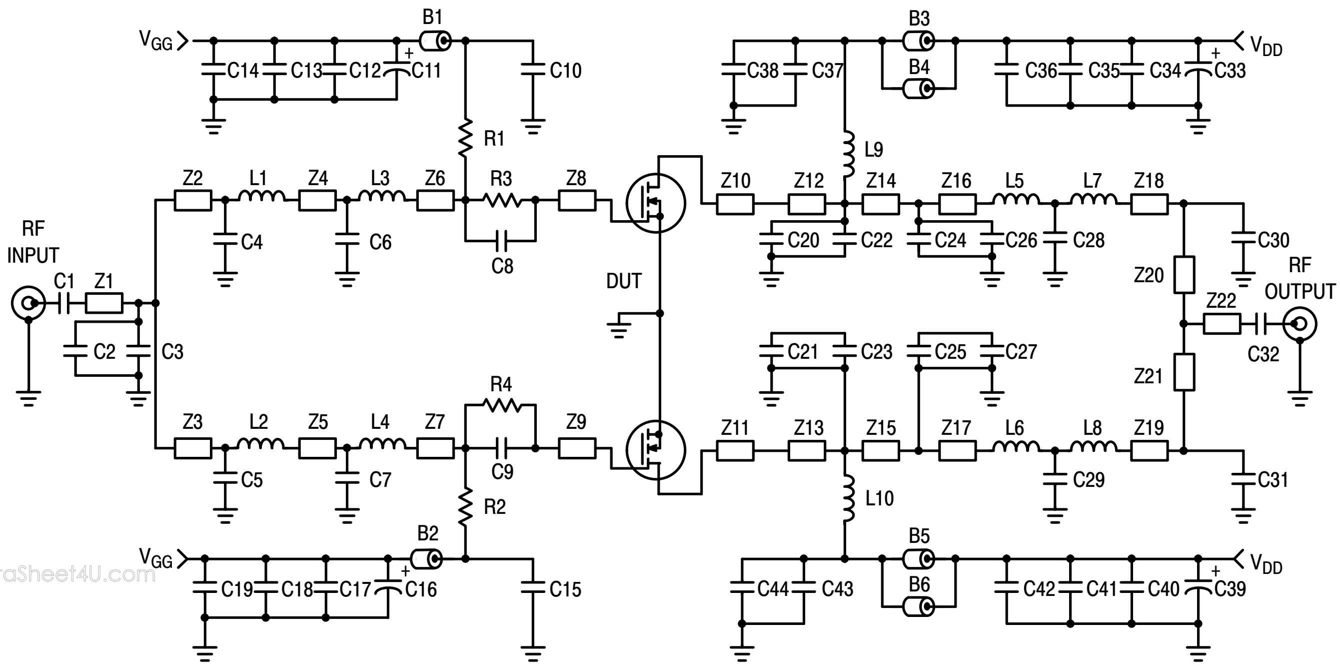
Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	1	260	°C

1. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

freescale™

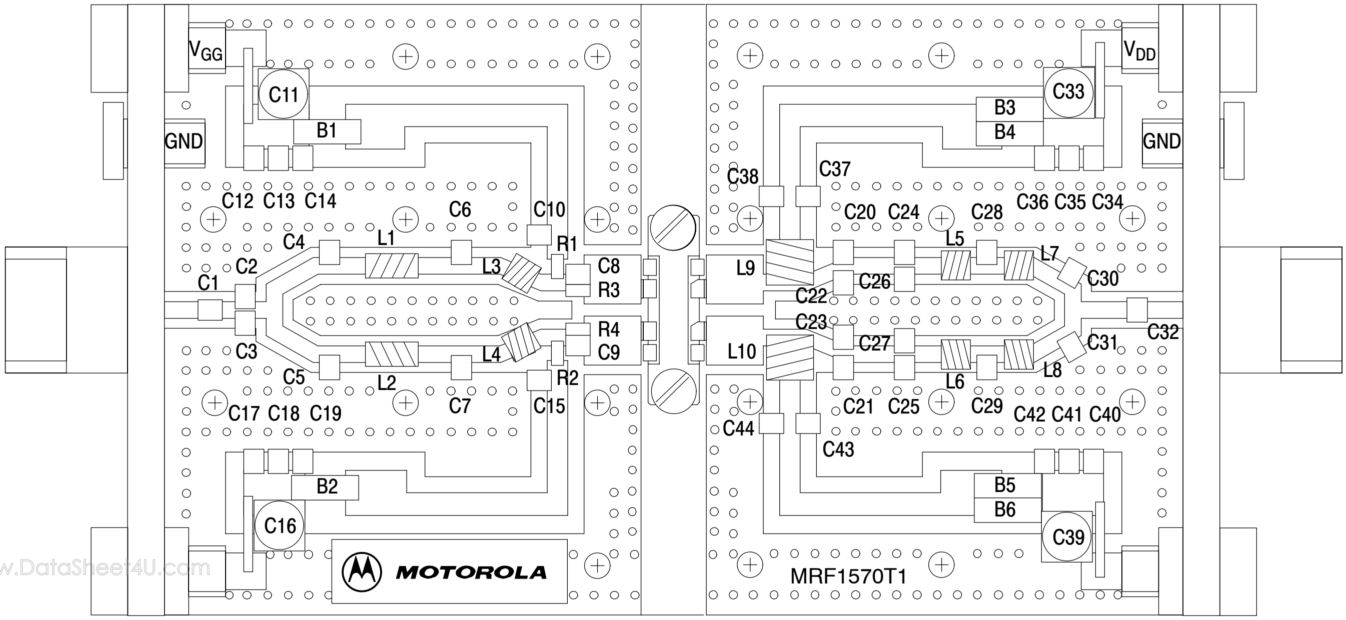
Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μA
On Characteristics					
Gate Threshold Voltage (V_{DS} = 12.5 Vdc, I_D = 0.8 mAdc)	$V_{GS(th)}$	1	—	3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.0 Adc)	$V_{DS(on)}$	—	—	1	Vdc
Dynamic Characteristics					
Input Capacitance (Includes Input Matching Capacitance) (V_{DS} = 12.5 Vdc, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	—	—	500	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0 V, f = 1 MHz)	C_{oss}	—	—	250	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0 V, f = 1 MHz)	C_{rss}	—	—	35	pF
RF Characteristics (In Freescale Test Fixture)					
Common-Source Amplifier Power Gain (V_{DD} = 12.5 Vdc, P_{out} = 70 W, I_{DQ} = 800 mA) f = 470 MHz	G_{ps}	—	11.5	—	dB
Drain Efficiency (V_{DD} = 12.5 Vdc, P_{out} = 70 W, I_{DQ} = 800 mA) f = 470 MHz	η	—	60	—	%



B1, B2, B3, B4, B5, B6	Long Ferrite Beads, Fair Rite Products	L3, L4	5 nH, 2 Turn Inductors, Coilcraft
C1, C32, C37, C43	270 pF, 100 mil Chip Capacitors	L5, L6, L7, L8	1 Turn, #18 AWG, 0.33″ ID Inductors
C2, C20, C21	33 pF, 100 mil Chip Capacitors	L9, L10	3 Turn, #16 AWG, 0.165″ ID Inductors
C3	18 pF, 100 mil Chip Capacitor	N1, N2	Type N Flange Mounts
C4, C5	30 pF, 100 mil Chip Capacitors	R1, R2	25.5 Ω Chip Resistors (1206)
C6, C7	180 pF, 100 mil Chip Capacitors	R3, R4	9.3 Ω Chip Resistors (1206)
C8, C9	150 pF, 100 mil Chip Capacitors	Z1	0.32″ x 0.080″ Microstrip
C10, C15	300 pF, 100 mil Chip Capacitors	Z2, Z3	0.46″ x 0.080″ Microstrip
C11, C16, C33, C39	10 μF, 50 V Electrolytic Capacitors	Z4, Z5	0.34″ x 0.080″ Microstrip
C12, C17, C34, C40	0.1 μF, 100 mil Chip Capacitors	Z6, Z7	0.45″ x 0.080″ Microstrip
C13, C18, C35, C41	1000 pF, 100 mil Chip Capacitors	Z8, Z9, Z10, Z11	0.28″ x 0.240″ Microstrip
C14, C19, C36, C42	470 pF, 100 mil Chip Capacitors	Z12, Z13	0.39″ x 0.080″ Microstrip
C22, C23	110 pF, 100 mil Chip Capacitors	Z14, Z15	0.27″ x 0.080″ Microstrip
C24, C25	68 pF, 100 mil Chip Capacitors	Z16, Z17	0.25″ x 0.080″ Microstrip
C26, C27	120 pF, 100 mil Chip Capacitors	Z18, Z19	0.29″ x 0.080″ Microstrip
C28, C29	24 pF, 100 mil Chip Capacitors	Z20, Z21	0.14″ x 0.080″ Microstrip
C30, C31	27 pF, 100 mil Chip Capacitors	Z22	0.32″ x 0.080″ Microstrip
C38, C44	240 pF, 100 mil Chip Capacitors	Board	31 mil Glass Teflon®
L1, L2	17.5 nH, 6 Turn Inductors, Coilcraft		

Figure 1. 135 - 175 MHz Broadband Test Circuit Schematic



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. 135 - 175 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS, 135 - 175 MHz

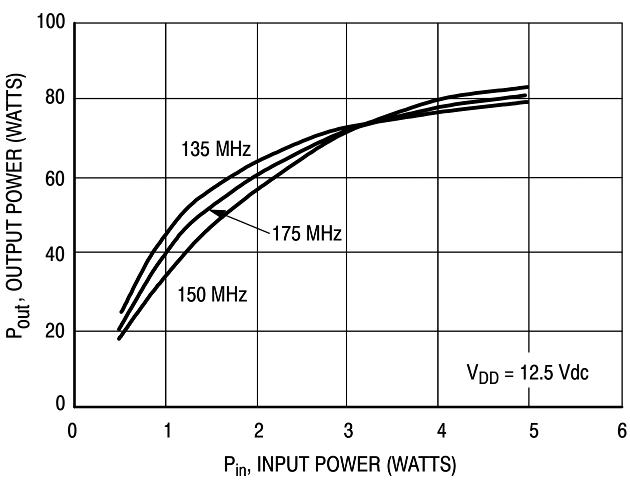


Figure 3. Output Power versus Input Power

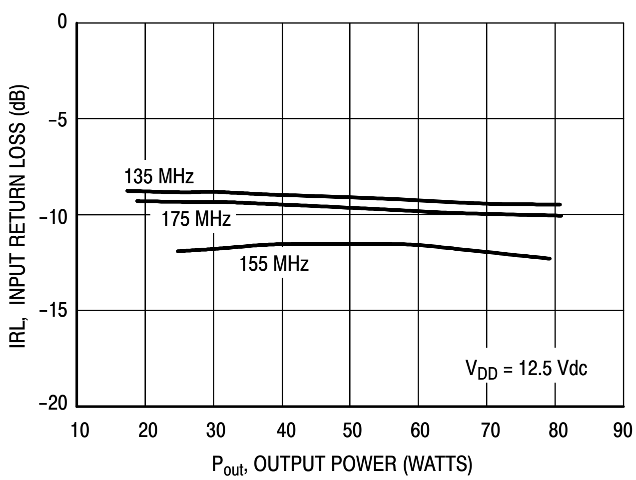


Figure 4. Input Return Loss versus Output Power

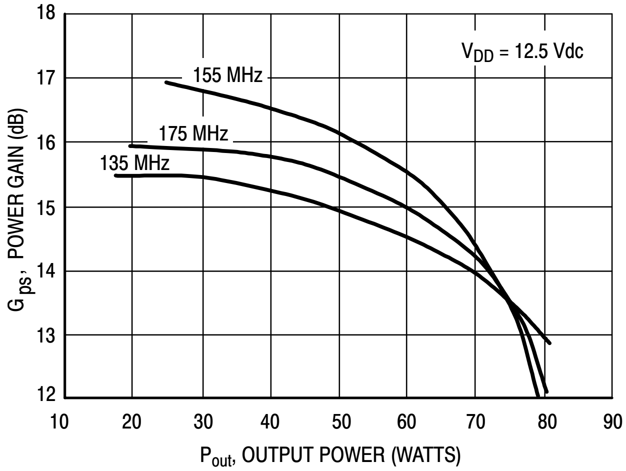


Figure 5. Gain versus Output Power

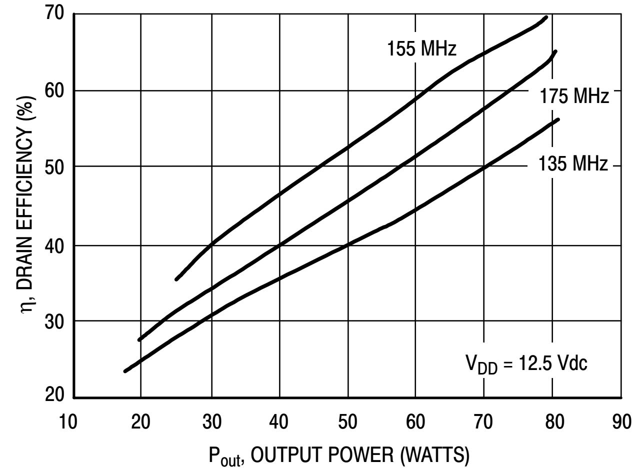


Figure 6. Drain Efficiency versus Output Power

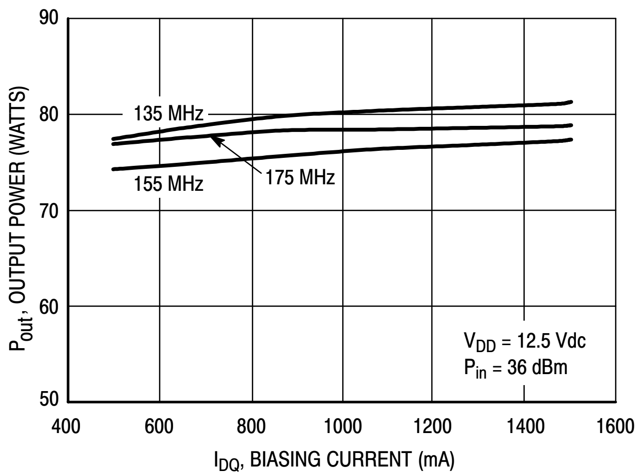


Figure 7. Output Power versus Biasing Current

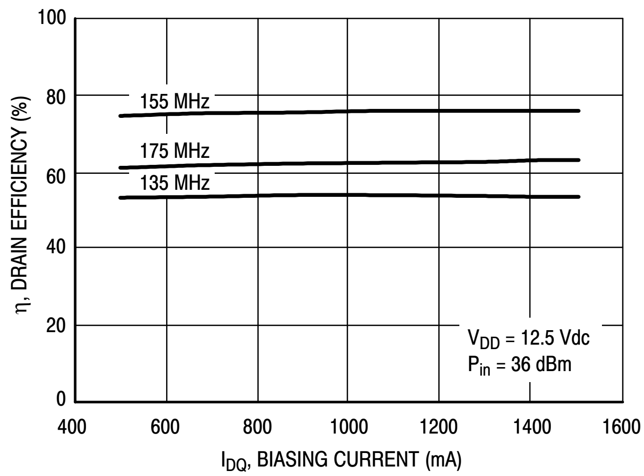


Figure 8. Drain Efficiency versus Biasing Current

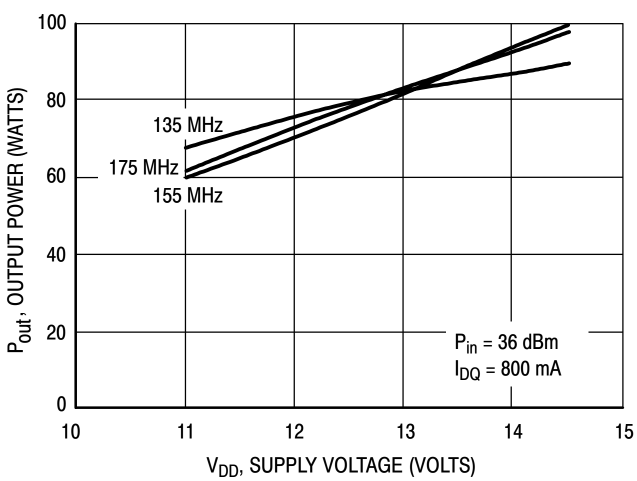


Figure 9. Output Power versus Supply Voltage

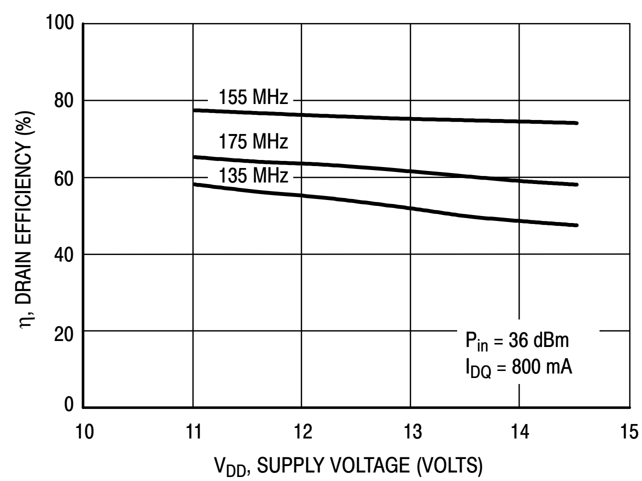
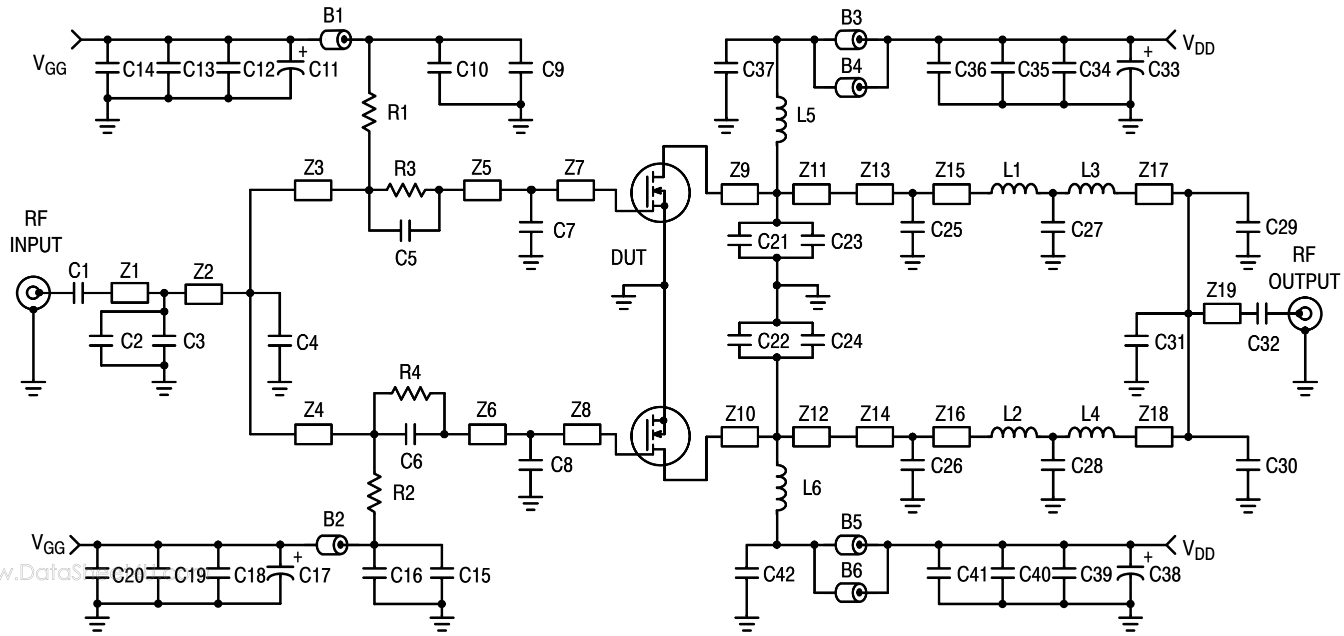


Figure 10. Drain Efficiency versus Supply Voltage



B1, B2, B3, B4, B5, B6	Long Ferrite Beads, Fair Rite Products	L1, L2, L3, L4	1 Turn, #18 AWG, 0.085″ ID Inductors
C1, C9, C15, C32	270 pF, 100 mil Chip Capacitors	L5, L6	2 Turn, #16 AWG, 0.165″ ID Inductors
C2, C3	7.5 pF, 100 mil Chip Capacitors	N1, N2	Type N Flange Mounts
C4	5.1 pF, 100 mil Chip Capacitor	R1, R2	25.5 Ω Chip Resistors (1206)
C5, C6	180 pF, 100 mil Chip Capacitors	R3, R4	10 Ω Chip Resistors (1206)
C7, C8	47 pF, 100 mil Chip Capacitors	Z1	0.240″ x 0.080″ Microstrip
C10, C16, C37, C42	120 pF, 100 mil Chip Capacitors	Z2	0.185″ x 0.080″ Microstrip
C11, C17, C33, C38	10 μF, 50 V Electrolytic Capacitors	Z3, Z4	1.500″ x 0.080″ Microstrip
C12, C18, C34, C39	470 pF, 100 mil Chip Capacitors	Z5, Z6	0.150″ x 0.240″ Microstrip
C13, C19, C35, C40	1200 pF, 100 mil Chip Capacitors	Z7, Z8	0.140″ x 0.240″ Microstrip
C14, C20, C36, C41	0.1 μF, 100 mil Chip Capacitors	Z9, Z10	0.140″ x 0.240″ Microstrip
C21, C22	33 pF, 100 mil Chip Capacitors	Z11, Z12	0.150″ x 0.240″ Microstrip
C23, C24	27 pF, 100 mil Chip Capacitors	Z13, Z14	0.270″ x 0.080″ Microstrip
C25, C26	15 pF, 100 mil Chip Capacitors	Z15, Z16	0.680″ x 0.080″ Microstrip
C27, C28	2.2 pF, 100 mil Chip Capacitors	Z17, Z18	0.320″ x 0.080″ Microstrip
C29, C30	6.2 pF, 100 mil Chip Capacitors	Z19	0.380″ x 0.080″ Microstrip
C31	1.0 pF, 100 mil Chip Capacitor	Board	31 mil Glass Teflon®

Figure 11. 400 - 470 MHz Broadband Test Circuit Schematic

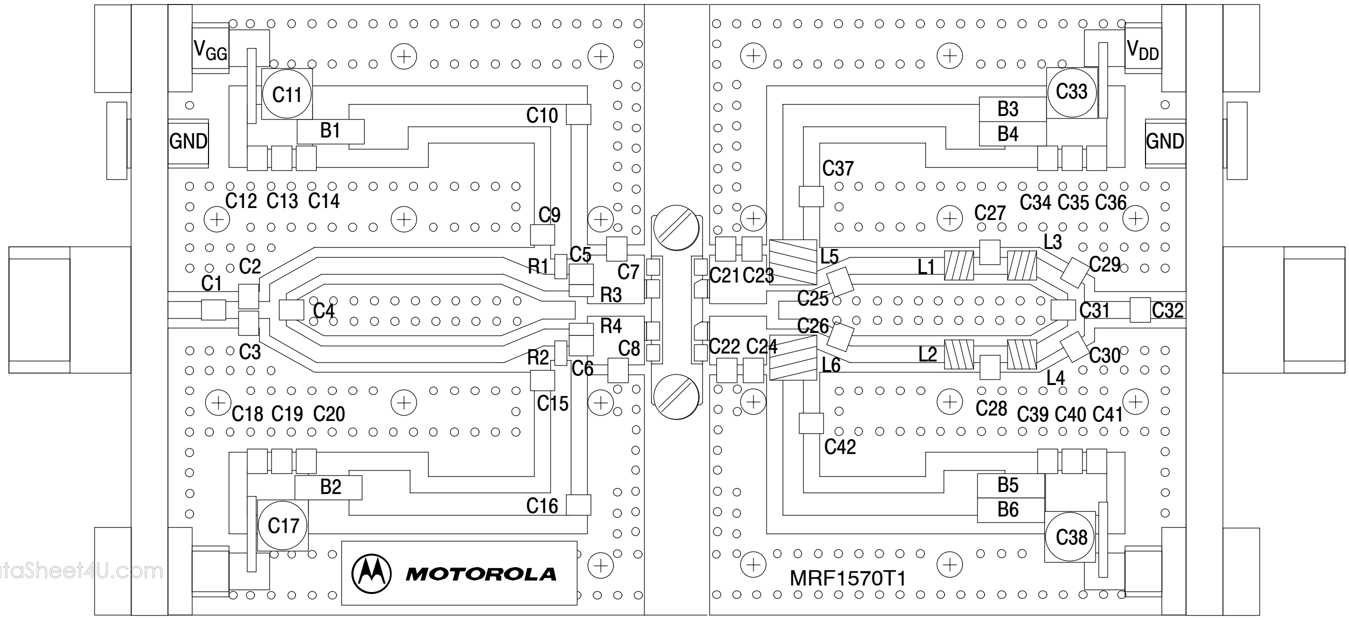


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Figure 12. 400 - 470 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS, 400 - 470 MHz

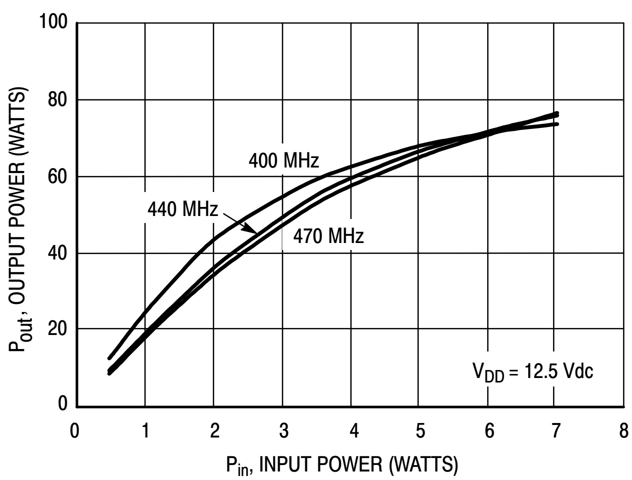


Figure 13. Output Power versus Input Power

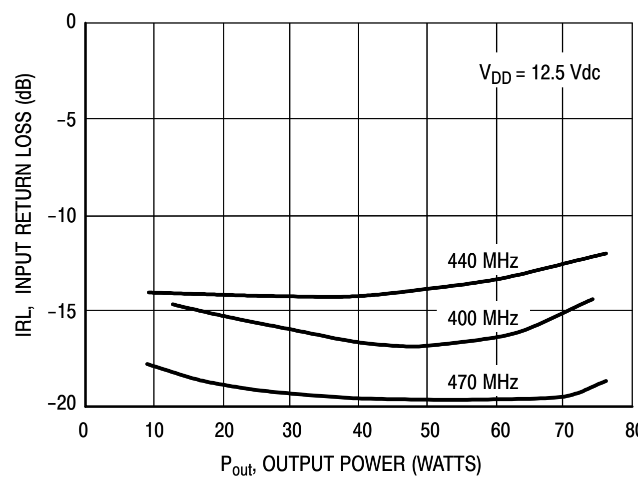


Figure 14. Input Return Loss versus Output Power

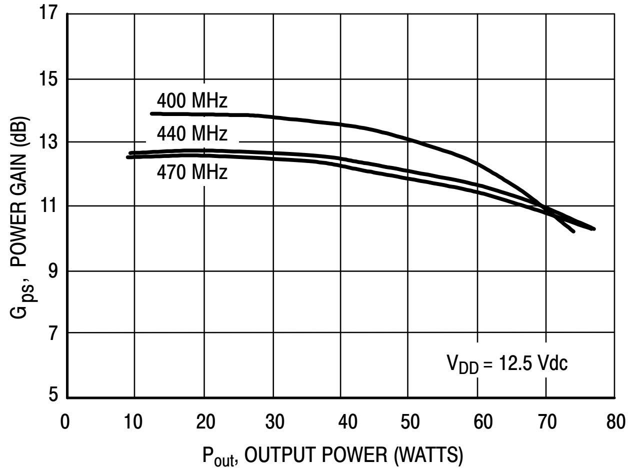


Figure 15. Gain versus Output Power

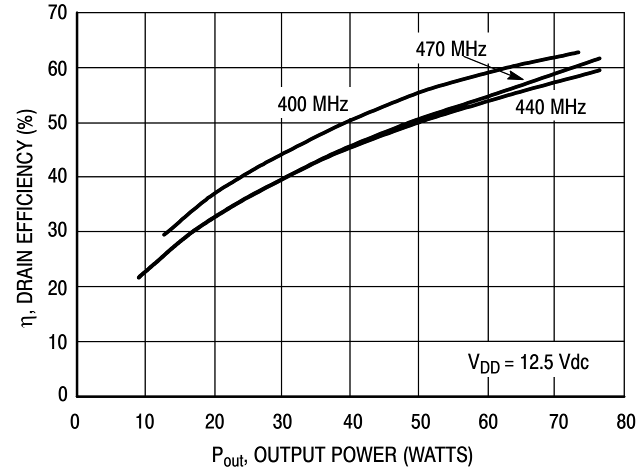


Figure 16. Drain Efficiency versus Output Power

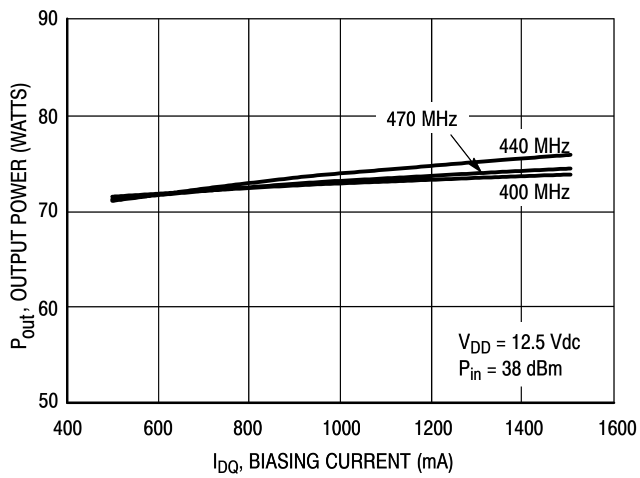


Figure 17. Output Power versus Biasing Current

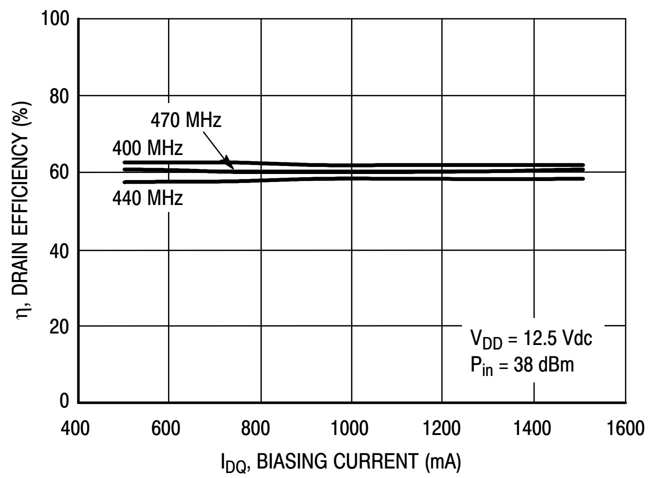


Figure 18. Drain Efficiency versus Biasing Current

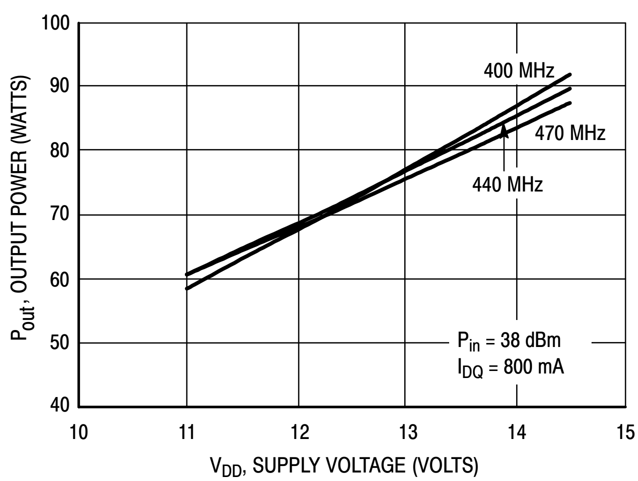


Figure 19. Output Power versus Supply Voltage

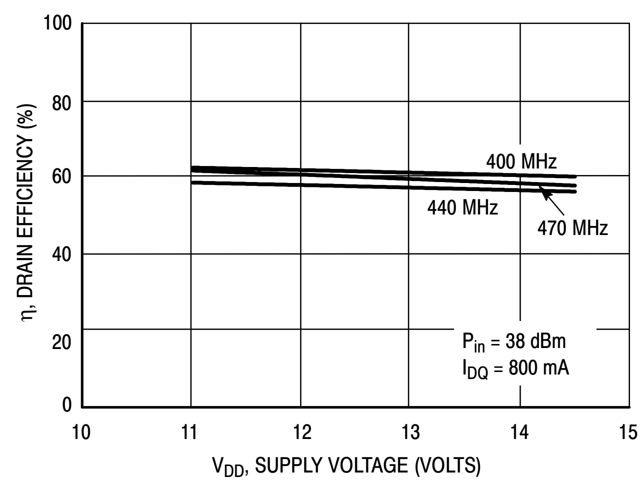
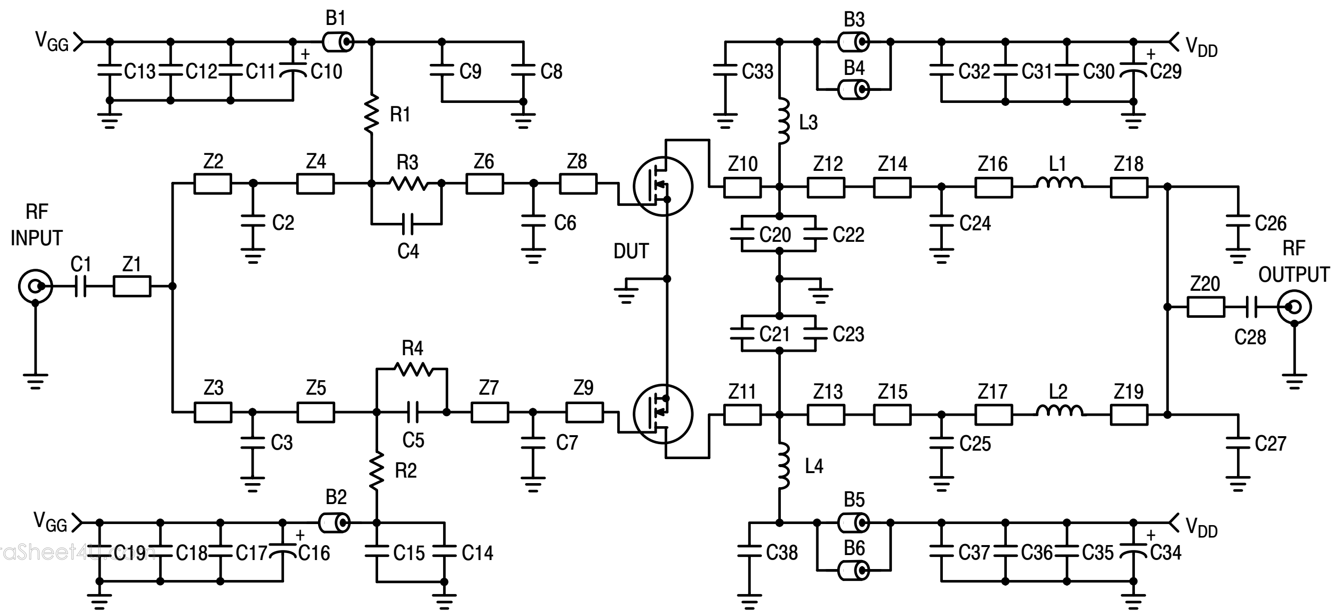


Figure 20. Drain Efficiency versus Supply Voltage



B1, B2, B3, B4, B5, B6	Long Ferrite Beads, Fair Rite Products	N1, N2	Type N Flange Mounts
C1, C8, C14, C28	270 pF, 100 mil Chip Capacitors	R1, R2	1.0 kΩ Chip Resistors (1206)
C2, C3	10 pF, 100 mil Chip Capacitors	R3, R4	10 Ω Chip Resistors (1206)
C4, C5	180 pF, 100 mil Chip Capacitors	Z1	0.40″ x 0.080″ Microstrip
C6, C7	47 pF, 100 mil Chip Capacitors	Z2, Z3	0.26″ x 0.080″ Microstrip
C9, C15, C33, C38	120 pF, 100 mil Chip Capacitors	Z4, Z5	1.35″ x 0.080″ Microstrip
C10, C16, C29, C34	10 μF, 50 V Electrolytic Capacitors	Z6, Z7	0.17″ x 0.240″ Microstrip
C11, C17, C30, C35	470 pF, 100 mil Chip Capacitors	Z8, Z9	0.12″ x 0.240″ Microstrip
C12, C18, C31, C36	1200 pF, 100 mil Chip Capacitors	Z10, Z11	0.14″ x 0.240″ Microstrip
C13, C19, C32, C37	0.1 μF, 100 mil Chip Capacitors	Z12, Z13	0.15″ x 0.240″ Microstrip
C20, C21	22 pF, 100 mil Chip Capacitors	Z14, Z15	0.18″ x 0.172″ Microstrip
C22, C23	20 pF, 100 mil Chip Capacitors	Z16, Z17	1.23″ x 0.080″ Microstrip
C24, C25, C26, C27	5.1 pF, 100 mil Chip Capacitors	Z18, Z19	0.12″ x 0.080″ Microstrip
L1, L2	1 Turn, #18 AWG, 0.115″ ID Inductors	Z20	0.40″ x 0.080″ Microstrip
L3, L4	2 Turn, #16 AWG, 0.165″ ID Inductors	Board	31 mil Glass Teflon®

Figure 21. 450 - 520 MHz Broadband Test Circuit Schematic

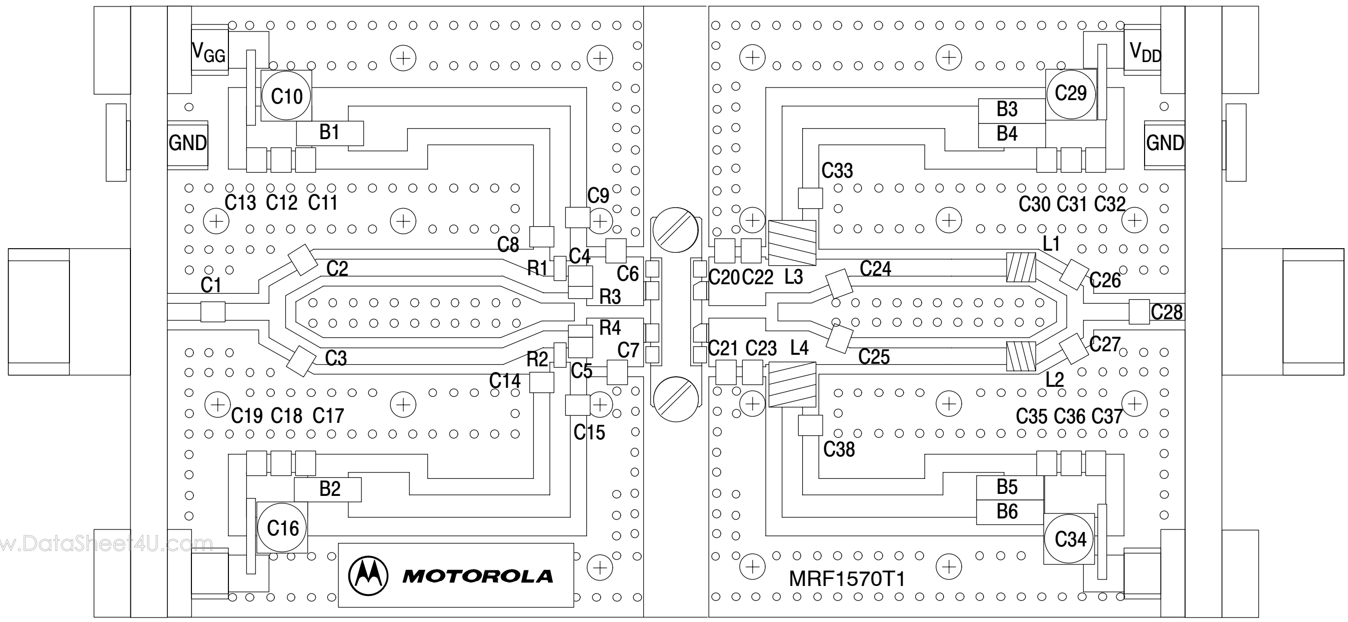


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Figure 22. 450 - 520 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS, 450 - 520 MHz

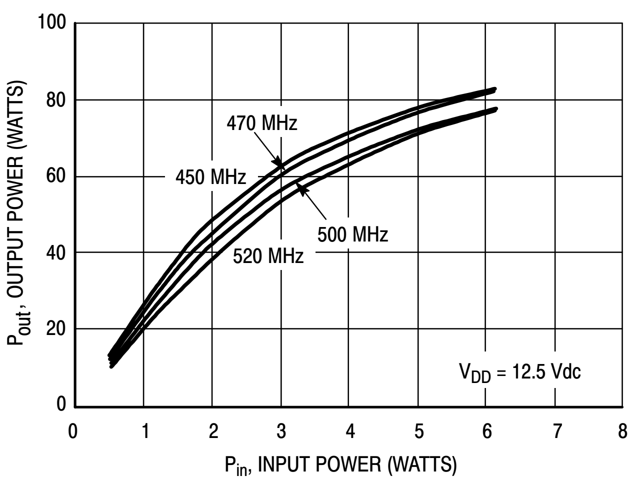


Figure 23. Output Power versus Input Power

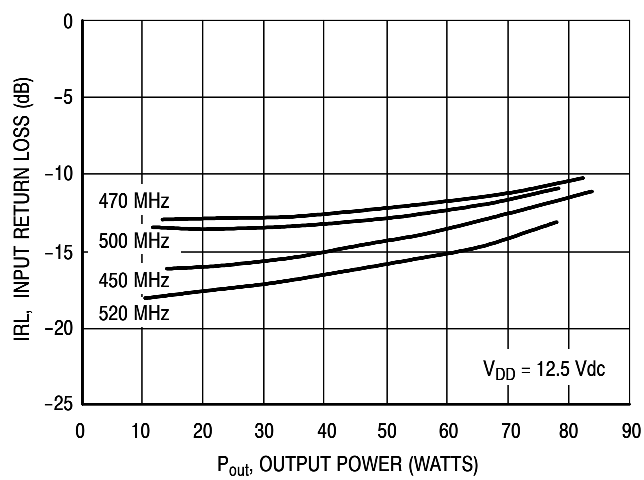


Figure 24. Input Return Loss versus Output Power

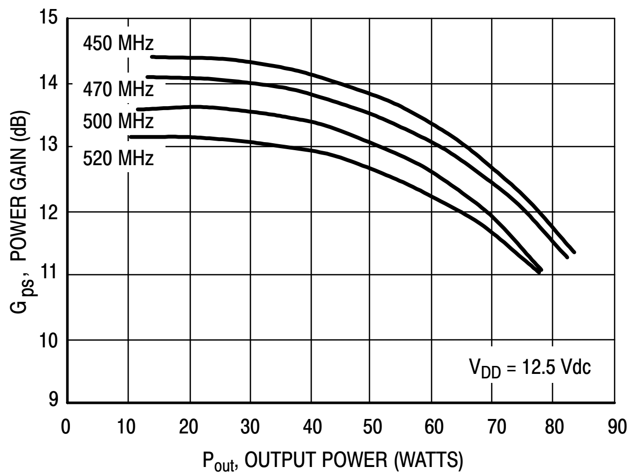


Figure 25. Gain versus Output Power

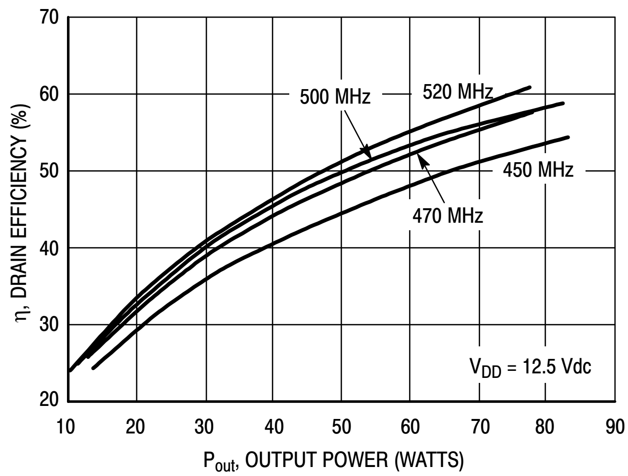


Figure 26. Drain Efficiency versus Output Power

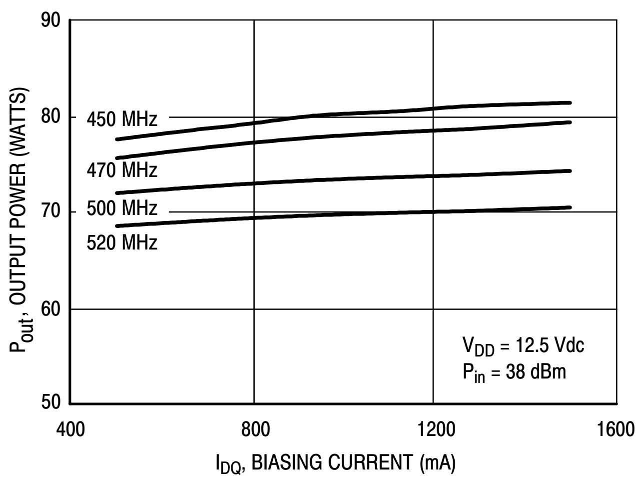


Figure 27. Output Power versus Biasing Current

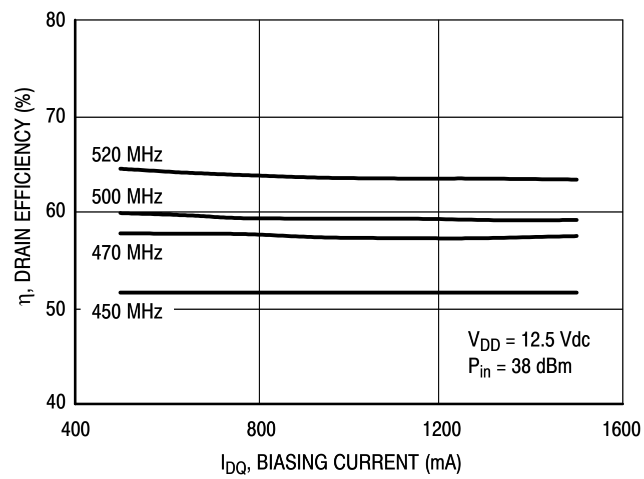


Figure 28. Drain Efficiency versus Biasing Current

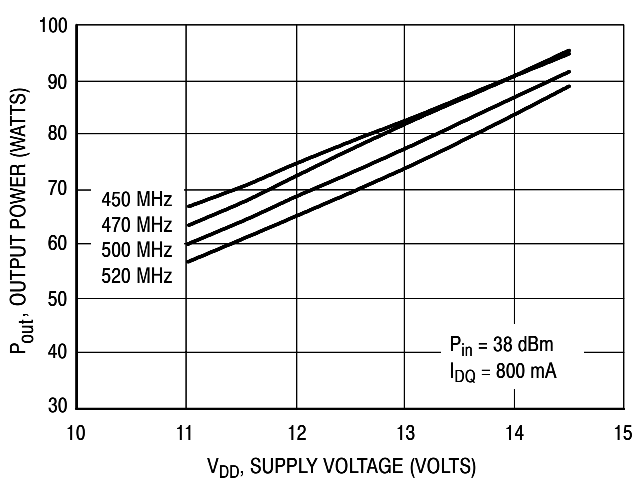


Figure 29. Output Power versus Supply Voltage

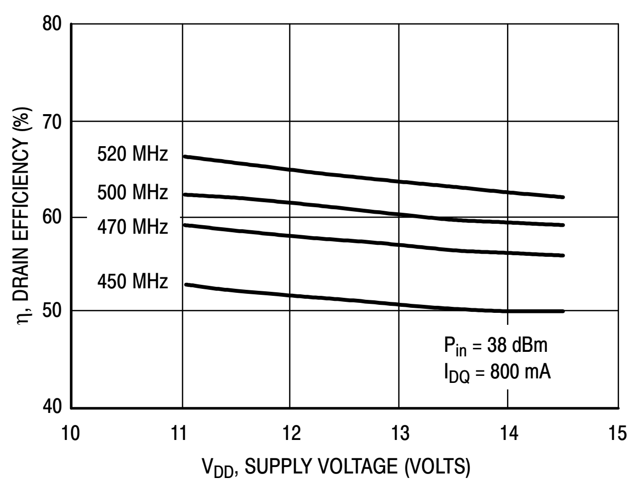
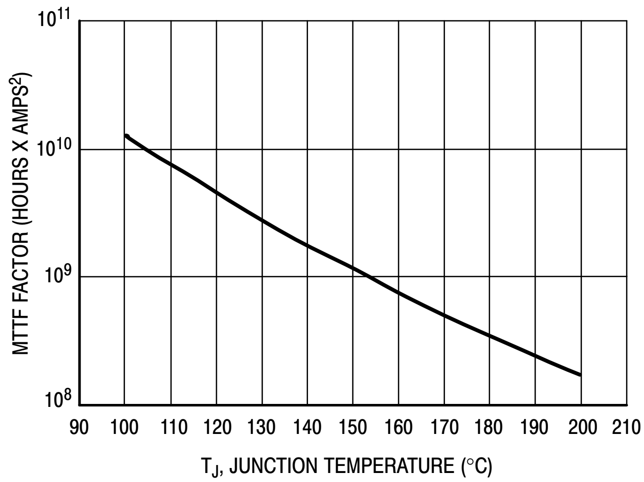


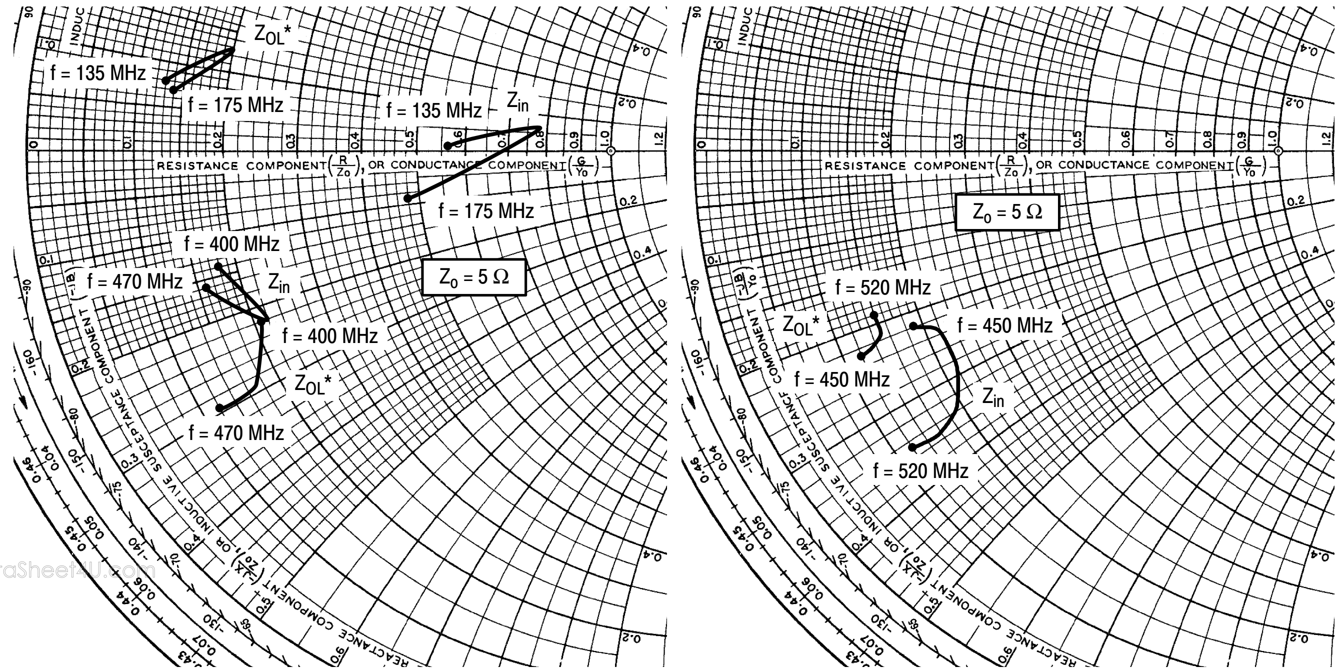
Figure 30. Drain Efficiency versus Supply Voltage

TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours x ampere^2 drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 31. MTTF Factor versus Junction Temperature



V_{DD} = 12.5 V, I_{DQ} = 0.8 A, P_{out} = 70 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
135	2.8 +j0.05	0.65 +j0.42
155	3.9 +j0.34	1.01 +j0.63
175	2.4 -j0.47	0.71 +j0.37

V_{DD} = 12.5 V, I_{DQ} = 0.8 A, P_{out} = 70 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
400	0.92 -j0.71	1.05 -j1.10
440	1.12 -j1.11	0.83 -j1.45
470	0.82 -j0.79	0.59 -j1.43

V_{DD} = 12.5 V, I_{DQ} = 0.8 A, P_{out} = 70 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
450	0.94 -j1.12	0.61 -j1.14
470	1.03 -j1.17	0.62 -j1.12
500	0.95 -j1.71	0.75 -j1.03
520	0.62 -j1.74	0.77 -j0.97

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Notes: Impedance Z_{in} was measured with input terminated at 50 Ω.
Impedance Z_{OL} was measured with output terminated at 50 Ω.

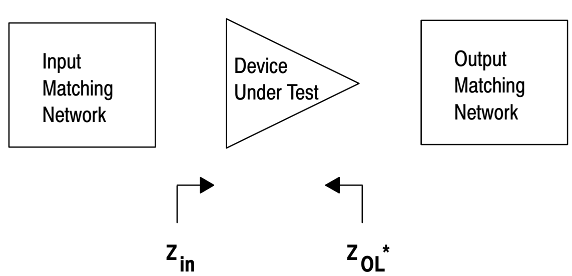


Figure 32. Series Equivalent Input and Output Impedance

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

This device is a common-source, RF power, N-Channel enhancement mode, Lateral Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Freescale Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF mobile power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

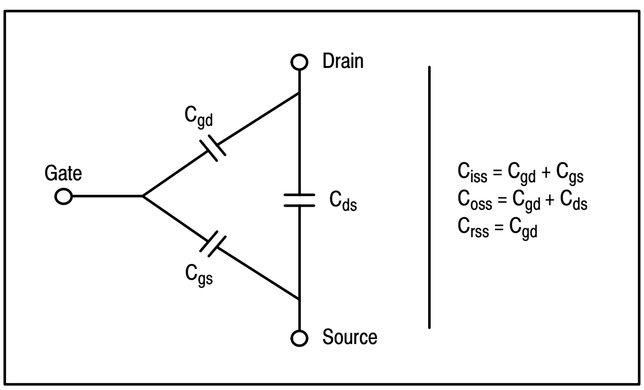
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The drain-source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high - on the order of $10^9\ \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at I_{DQ} = 800 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

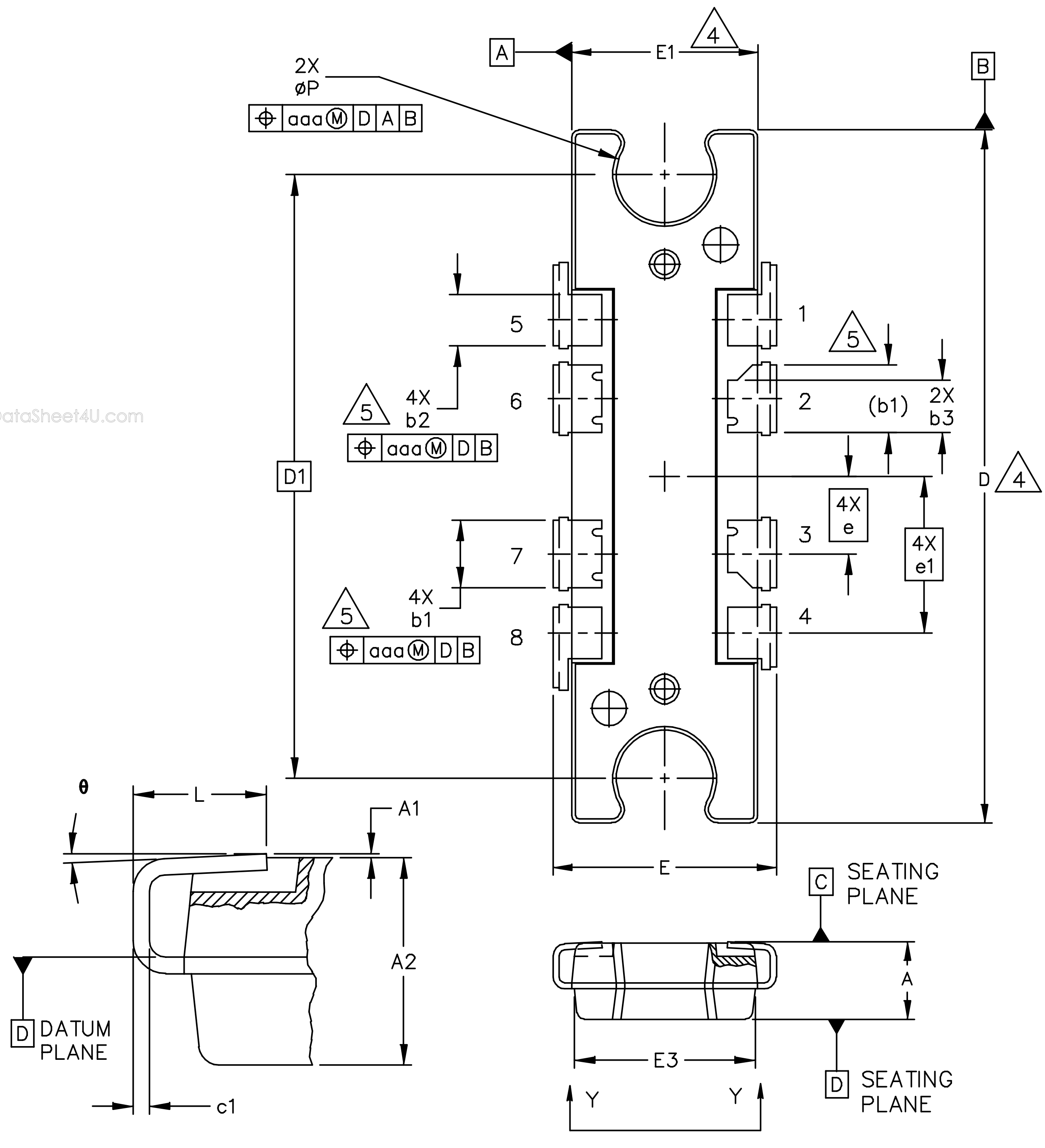
Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Freescale Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large-signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region. See Freescale Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters" for a discussion of two port network theory and stability.

PACKAGE DIMENSIONS



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TITLE: TO-272, SPLIT LEAD	DOCUMENT NO: 98ASA99295D		REV: E
	CASE NUMBER: 1366-05		03 AUG 2007
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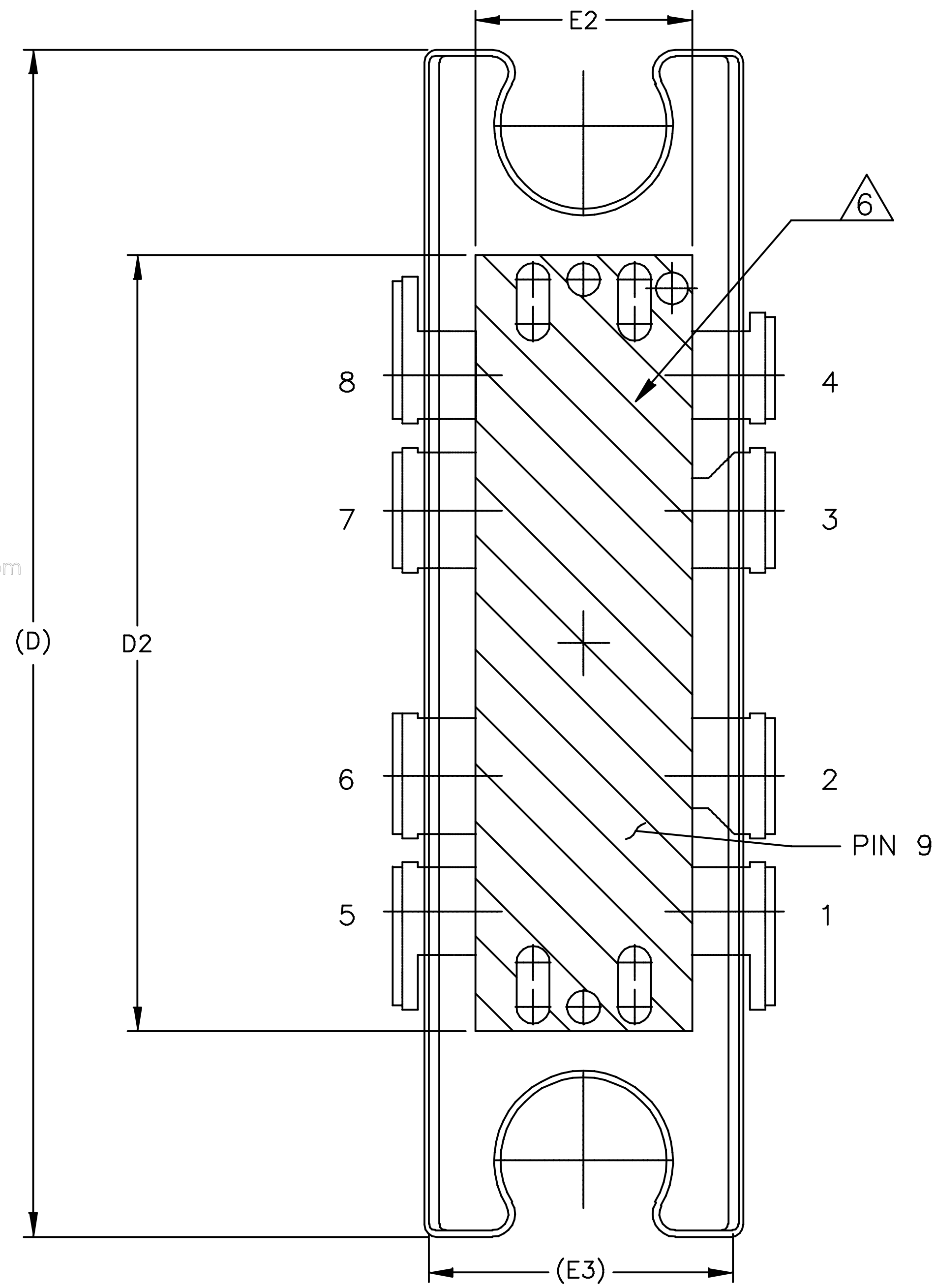

VIEW Y–Y

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	CASE NUMBER: 1366–05	03 AUG 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. DATUM PLANE −H− IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.

5. DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:

PIN 1 − SOURCE (COMMON)
PIN 2 − DRAIN
PIN 3 − DRAIN
PIN 4 − SOURCE (COMMON)
PIN 5 − SOURCE (COMMON)
PIN 6 − GATE
PIN 7 − GATE
PIN 8 − SOURCE (COMMON)
PIN 9 − SOURCE (COMMON)

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.098	.108	2.49	2.74	b1	.088	.094	2.24	2.39
A1	.000	.004	0.000	0.10	b2	.066	.072	1.68	1.83
A2	.100	.104	2.54	2.64	b3	.067	.073	1.70	1.85
D	.928	.932	23.57	23.67	c1	.007	.011	0.178	0.279
D1	.810 BSC		20.57 BSC		e	.104 BSC		2.64 BSC	
D2	.604	----	15.34	----	e1	.210 BSC		5.33 BSC	
E	.296	.304	7.52	7.72	θ	0°	6°	0°	6°
E1	.248	.252	6.30	6.40	aaa	.004		0.1	
E2	.162	----	4.11	----					
E3	.241	.245	6.12	6.22					
L	.060	.070	1.52	1.78					
P	.126	.134	3.20	3.40					

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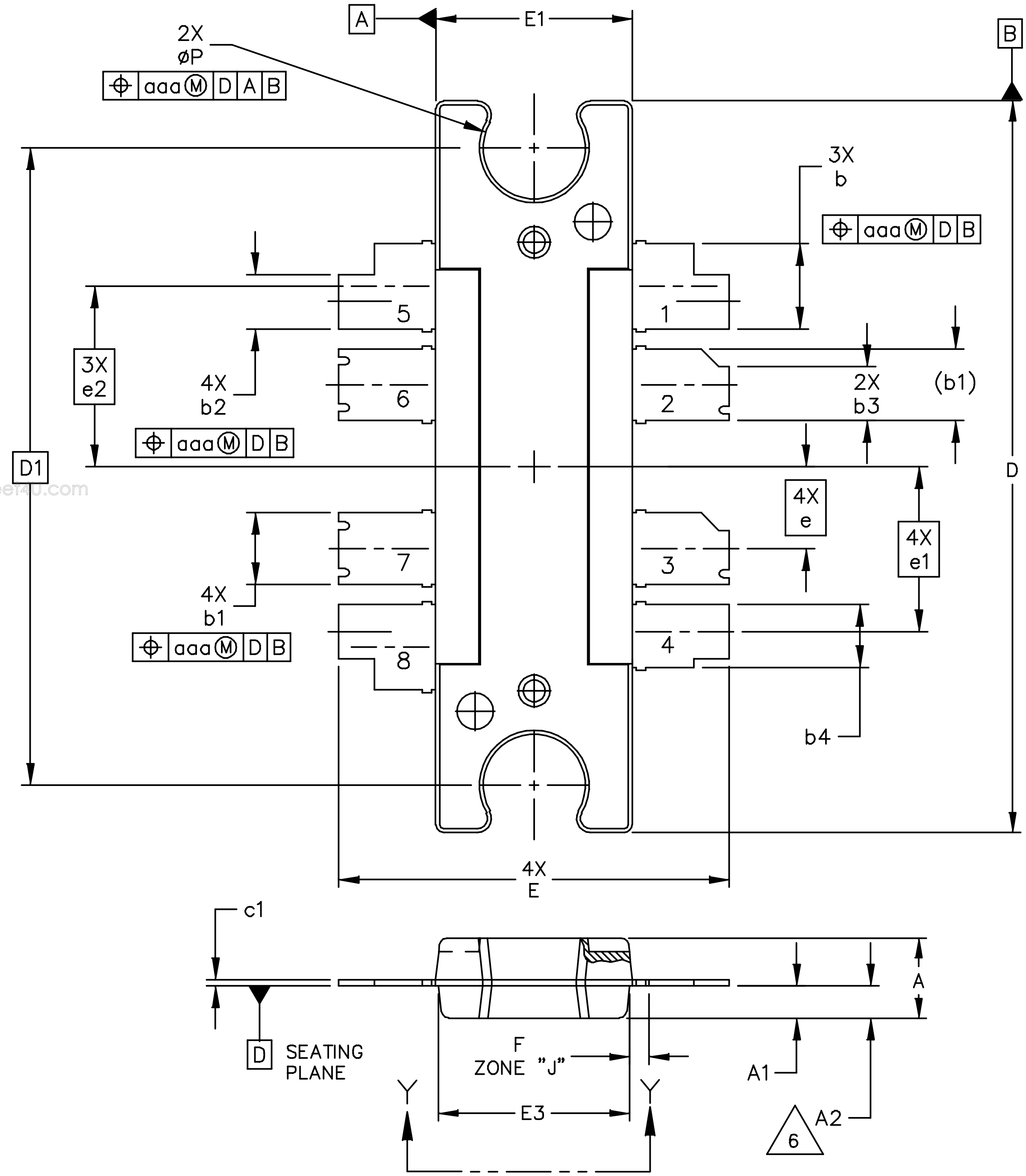

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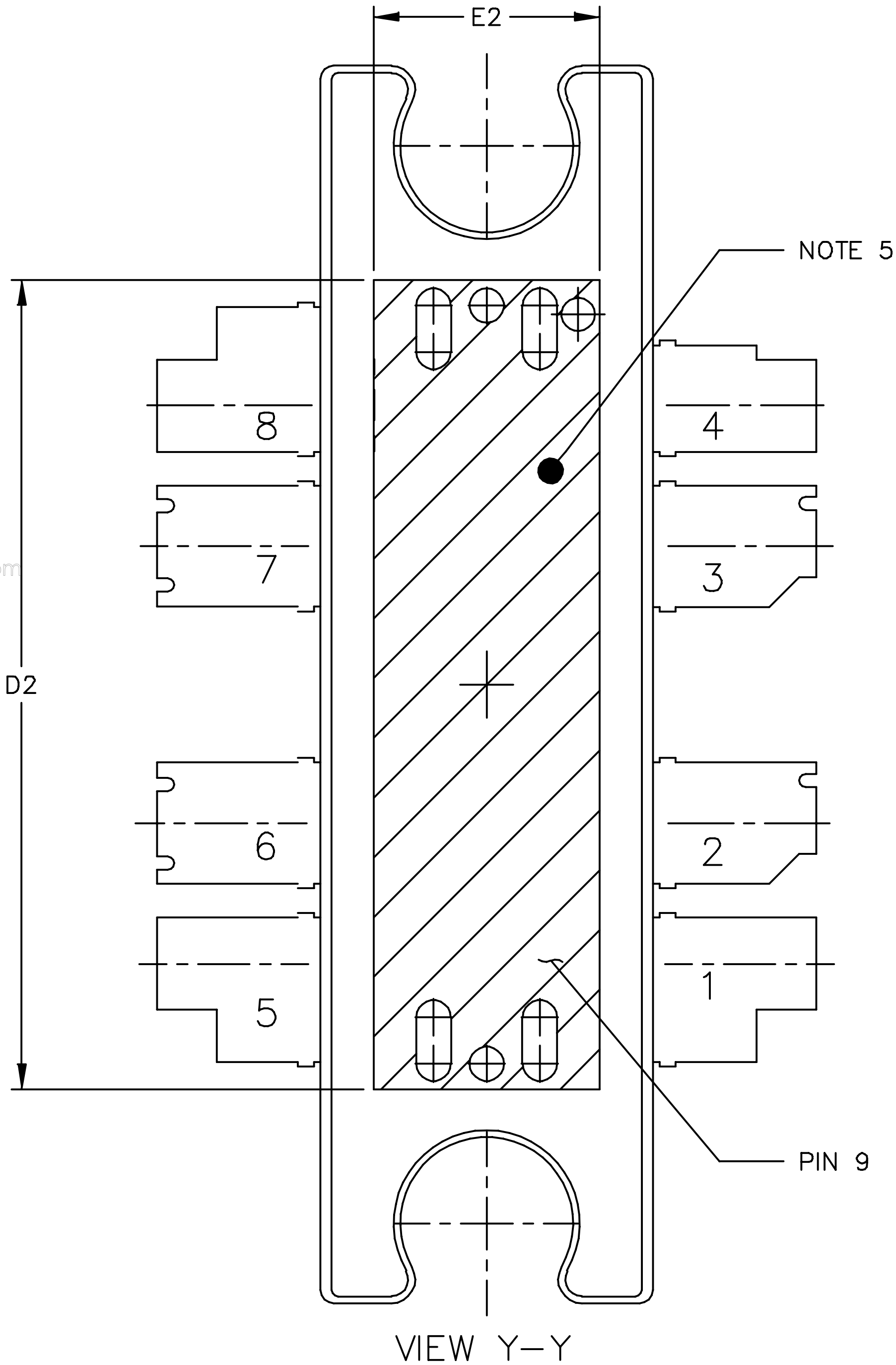
	CASE NUMBER: 1366A–03	03 AUG 2007
	STANDARD: NON–JEDEC	



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	CASE NUMBER: 1366A-03	03 AUG 2007
	STANDARD: NON-JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.

4. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" AND "b2" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

5. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

6. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

STYLE 1:

PIN 1 - SOURCE (COMMON)
PIN 2 - DRAIN
PIN 3 - DRAIN
PIN 4 - SOURCE (COMMON)
PIN 5 - SOURCE (COMMON)
PIN 6 - GATE
PIN 7 - GATE
PIN 8 - SOURCE (COMMON)
PIN 9 - SOURCE (COMMON)

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.098	.106	2.49	2.69	b	.105	.111	2.67	2.82
A1	.038	.044	0.96	1.12	b1	.088	.094	2.24	2.39
A2	.040	.042	1.02	1.07	b2	.066	.072	1.68	1.83
D	.926	.934	23.52	23.72	b3	.067	.073	1.70	1.85
D1	.810 BSC		20.57 BSC		b4	.077	.083	1.96	2.11
D2	.604	----	15.34	----	c1	.007	.011	.178	.279
E	.492	.500	12.50	12.70	e	.104 BSC		2.64 BSC	
E1	.246	.254	6.25	6.45	e1	.210 BSC		5.33 BSC	
E2	.162	----	4.11	----	e2	.229 BSC		5.82 BSC	
E3	.241	.245	6.12	6.22					
F	.025 BSC		0.64 BSC		aaa	.004		0.1	
P	.126	.134	3.20	3.40	bbb	.008		0.2	

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PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN211A: Field Effect Transistors in Theory and Practice
- AN215A: RF Small-Signal Design Using Two-Port Parameters
- AN721: Impedance Matching Networks Applied to RF Power Transistors
- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN4005: Thermal Management and Mounting Method for the PLD 1.5 RF Power Surface Mount Package

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
9	June 2008	• Corrected specified performance values for power gain and efficiency on p. 1 to match typical performance values in the functional test table on p. 2 • Replaced Case Outline 1366-04 with 1366-05, Issue E, p. 1, 16-18. Removed Drain-ID label from View Y-Y. Added Pin 9 designation. Changed dimensions D2 and E2 from basic to .604 Min and .162 Min, respectively. • Replaced Case Outline 1366A-02 with 1366A-03, Issue D, p. 1, 19-21. Removed Drain-ID label from View Y-Y. Removed Surface Alignment tolerance label for cross hatched section on View Y-Y. Added Pin 9 designation. Changed dimensions D2 and E2 from basic to .604 Min and .162 Min, respectively. Added dimension E3. Restored dimensions F and P designators to DIM column on Sheet 3. • Added Product Documentation and Revision History, p. 22

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