

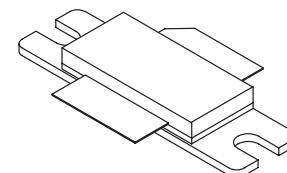
The RF MOSFET Line RF Power Field Effect Transistors N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for CDMA, TDMA, GSM and multicarrier amplifier applications.

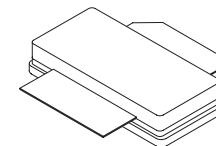
- Typical CDMA Performance: 1960 MHz, 26 Volts
IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
Output Power — 7.5 Watts
Power Gain — 12.5 dB
Adjacent Channel Power —
 885 kHz: -47 dBc @ 30 kHz BW
 1.25 MHz: -55 dBc @ 12.5 kHz BW
 2.25 MHz: -55 dBc @ 1 MHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 60 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.

MRF19060
MRF19060R3
MRF19060SR3

1990 MHz, 60 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF19060R3



CASE 465A-06, STYLE 1
NI-780S
MRF19060SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	65	Vdc
Gate-Source Voltage	V _{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T _C ≥ = 25°C Derate above 25°C	P _D	180 1.03	Watts W/°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Operating Junction Temperature	T _J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	0.97	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage ($V_{GS} = 0 \text{ Vdc}$, $I_D = 10 \mu\text{A}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 26 \text{ Vdc}$, $V_{GS} = 0 \text{ Vdc}$)	I_{DSS}	—	—	6	μA
Gate–Source Leakage Current ($V_{GS} = 5 \text{ Vdc}$, $V_{DS} = 0 \text{ Vdc}$)	I_{GSS}	—	—	1	μA
ON CHARACTERISTICS					
Forward Transconductance ($V_{DS} = 10 \text{ Vdc}$, $I_D = 2 \text{ Adc}$)	g_{fs}	—	4.7	—	S
Gate Threshold Voltage ($V_{DS} = 10 \text{ Vdc}$, $I_D = 300 \mu\text{Adc}$)	$V_{GS(th)}$	2	—	4	V
Gate Quiescent Voltage ($V_{DS} = 26 \text{ Vdc}$, $I_D = 500 \text{ mA}$)	$V_{GS(Q)}$	2.5	3.9	4.5	V
Drain–Source On–Voltage ($V_{GS} = 10 \text{ Vdc}$, $I_D = 2 \text{ Adc}$)	$V_{DS(on)}$	—	0.27	—	V

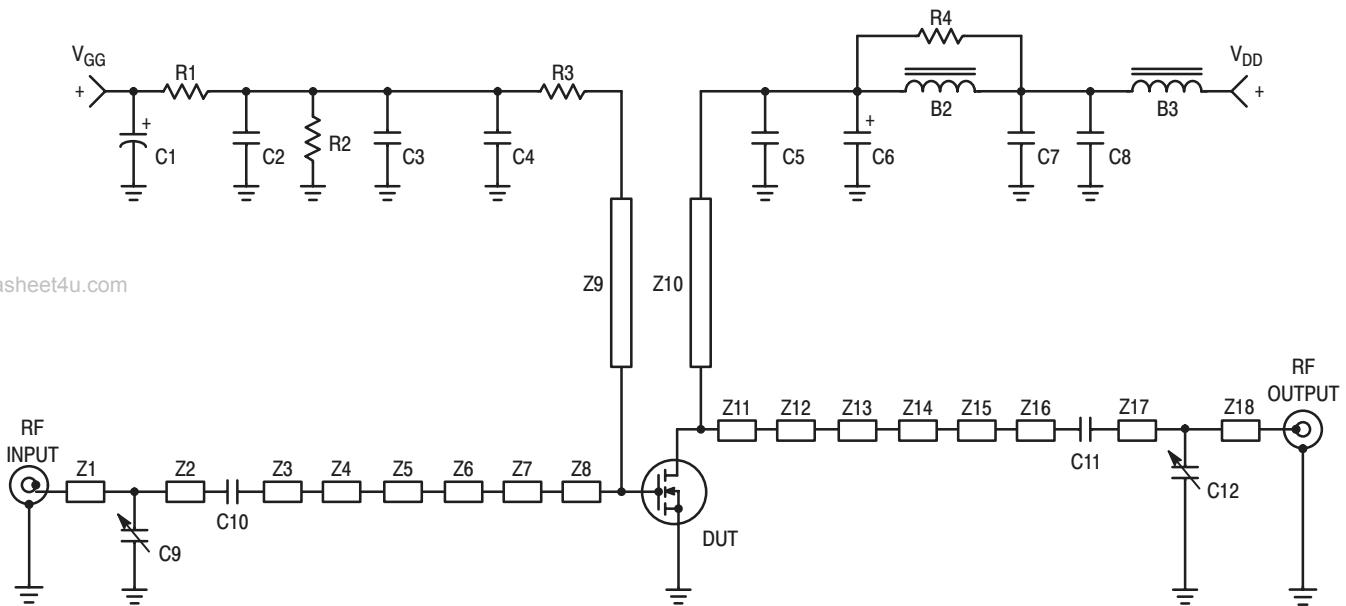
DYNAMIC CHARACTERISTICS

Reverse Transfer Capacitance (1) ($V_{DS} = 26 \text{ Vdc}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$)	C_{rss}	—	2.7	—	pF
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FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)

Two-Tone Common–Source Amplifier Power Gain ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 60 \text{ W PEP}$, $I_{DQ} = 500 \text{ mA}$, $f = 1930 \text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	Gps	11	12.5	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 60 \text{ W PEP}$, $I_{DQ} = 500 \text{ mA}$, $f = 1930 \text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	n	33	36	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 60 \text{ W PEP}$, $I_{DQ} = 500 \text{ mA}$, $f = 1930 \text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	IMD	—	-31	-28	dBc
Input Return Loss ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 60 \text{ W PEP}$, $I_{DQ} = 500 \text{ mA}$, $f = 1930 \text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	IRL	—	-12	—	dB
P_{out} , 1 dB Compression Point ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 60 \text{ W CW}$, $f = 1990 \text{ MHz}$)	P1dB	—	60	—	W
Output Mismatch Stress ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 60 \text{ W CW}$, $I_{DQ} = 500 \text{ mA}$, $f = 1930 \text{ MHz}$, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B2 – B3	Ferrite Beads, Fair Rite, 2743019447	Z4	0.152" x 0.140" Microstrip
C1	10 μ F, 50 V Electrolytic Capacitor, Panasonic #ECEV1HV100R	Z5	0.090" x 0.102" Microstrip
C2, C7	1000 pF Chip Capacitors, B Case, ATC #100B102JCA500X	Z6	0.245" x 0.217" Microstrip
C3, C8	0.10 μ F Chip Capacitors, B Case, Kemet #CDR33BX104AKWS	Z7	0.090" x 0.737" Microstrip
C4	5.1 pF Chip Capacitor, B Case, ATC #100B5R1JCA500X	Z8	0.530" x 0.941" Microstrip
C5	6.2 pF Chip Capacitor, B Case, ATC #100B6R2JCA500X	Z9	1.010" x 0.050" Microstrip
C6	22 μ F, 35 V Tantalum Capacitor, SMT, Sprague	Z10	1.060" x 0.050" Microstrip
C9	0.8 pF – 8.0 pF Variable Capacitor, Johanson Gigatrim	Z11	0.446" x 1.137" Microstrip
C10, C11	10 pF Chip Capacitors, B Case, ATC #100B100JCA500X	Z12	0.152" x 0.567" Microstrip
C12	0.4 pF – 2.5 pF Variable Capacitor, Johanson Gigatrim	Z13	0.183" x 0.220" Microstrip
R1	1 k Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z14	0.100" x 0.338" Microstrip
R2	560 k Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z15	0.480" x 0.142" Microstrip
R3	15 Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z16	0.140" x 0.080" Microstrip
R4	10 Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z17	0.173" x 0.080" Microstrip
Z1	0.580" x 0.074" Microstrip	Z18	0.420" x 0.080" Microstrip
Z2	0.100" x 0.074" Microstrip	Board	0.030" Glass Teflon [®] Arlon GX-0300-55-22, 2 oz Cu
Z3	0.384" x 0.074" Microstrip		

Figure 1. MRF19060 Test Circuit Schematic

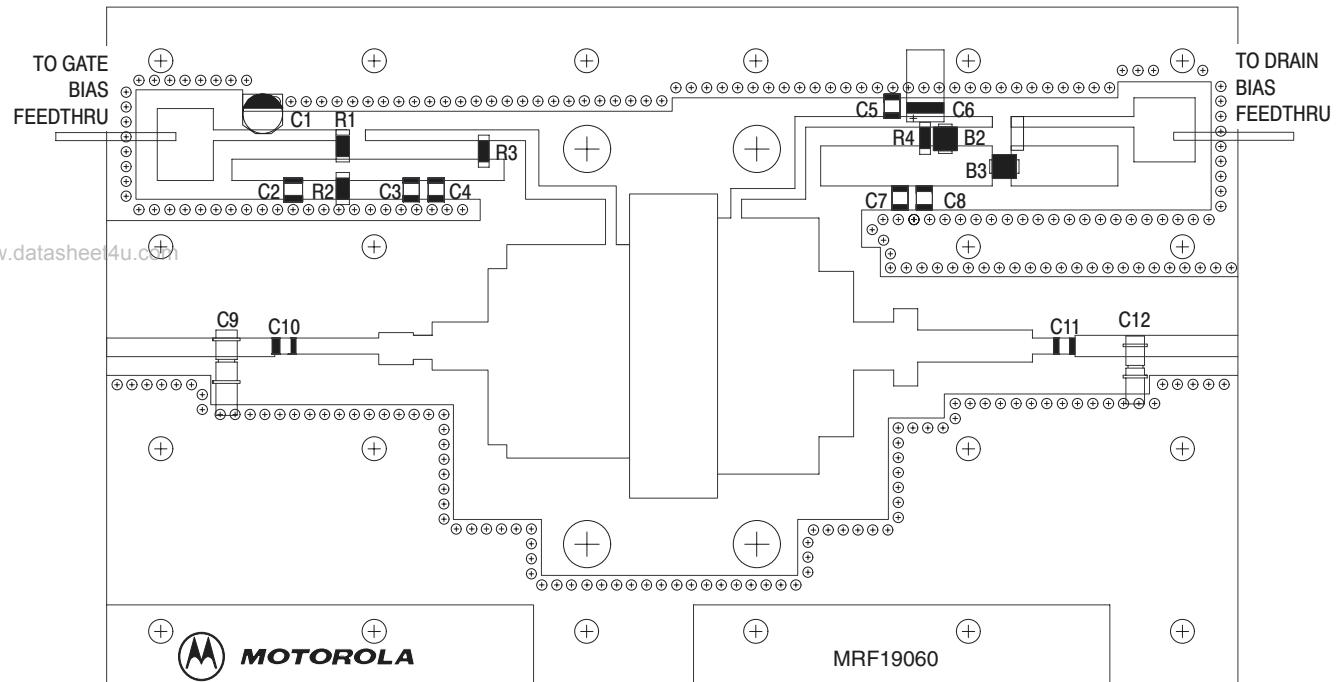
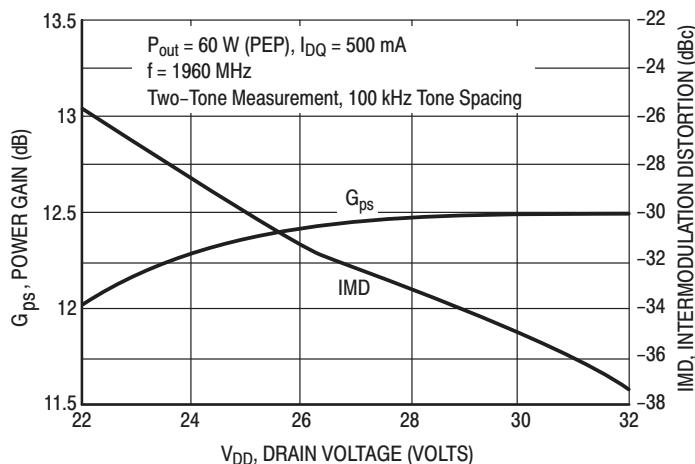
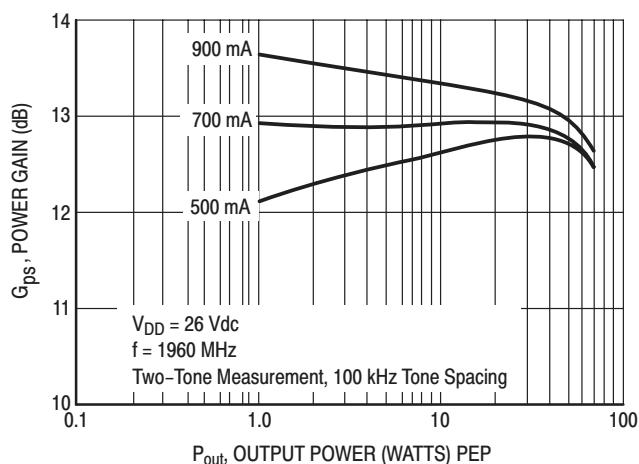
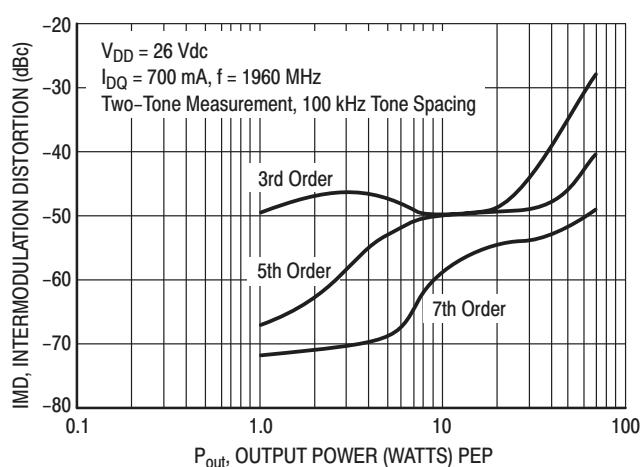
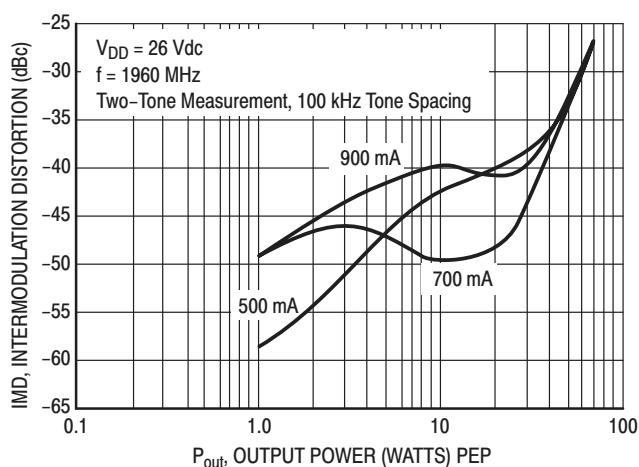
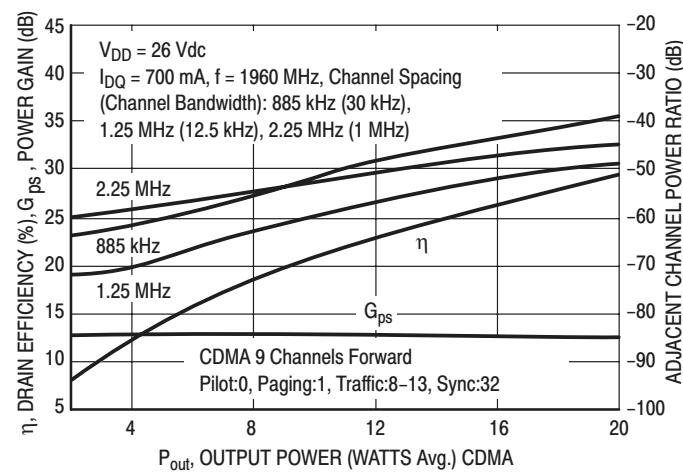
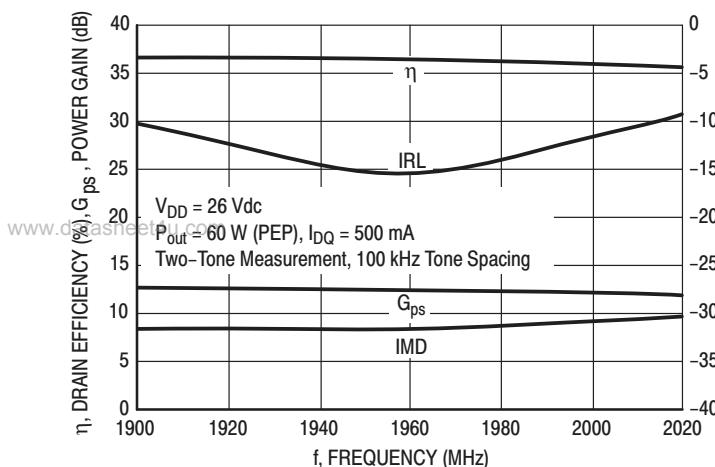
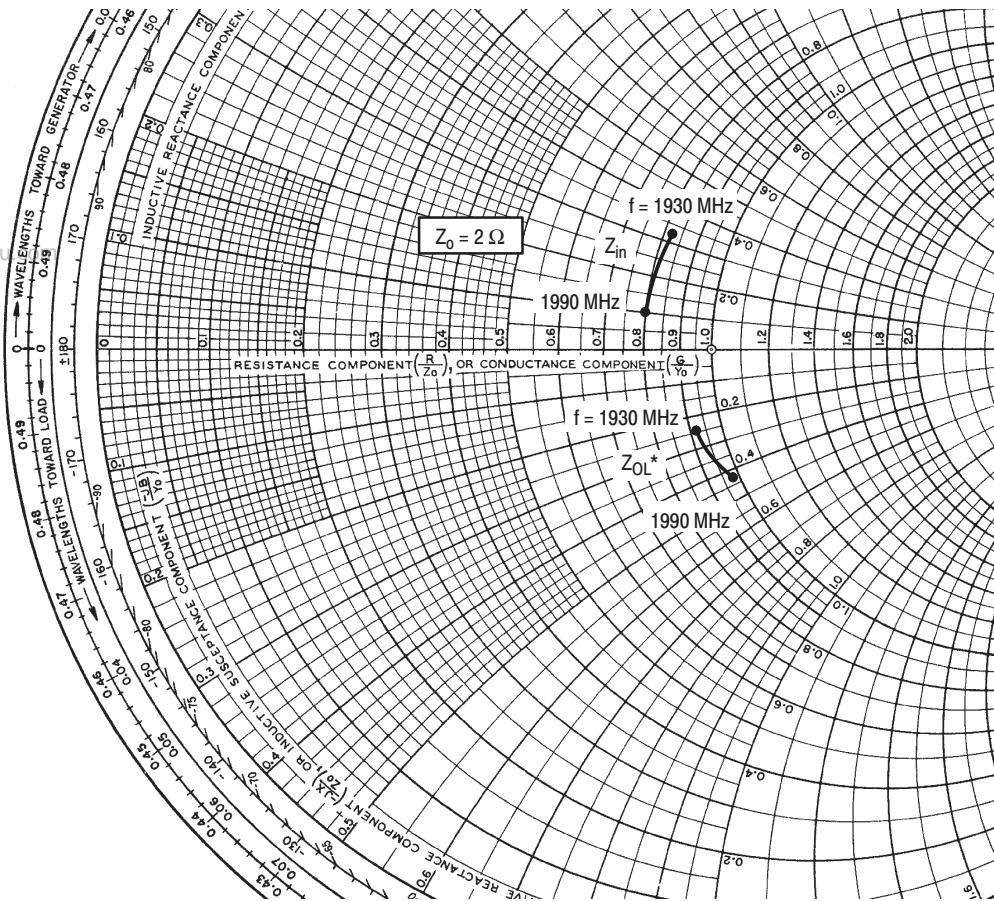


Figure 2. MRF19060 Test Circuit Component Layout

TYPICAL CHARACTERISTICS





$V_{DD} = 26 \text{ V}$, $I_{DQ} = 500 \text{ mA}$, $P_{out} = 60 \text{ W PEP}$

f MHz	Z_{in} Ω	Z_{OL^*} Ω
1930	$1.65 + j0.67$	$1.85 - j0.50$
1960	$1.64 + j0.45$	$1.89 - j0.74$
1990	$1.60 + j0.20$	$1.96 - j0.94$

Z_{in} = Complex conjugate of source impedance.

Z_{OL^*} = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL^*} was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

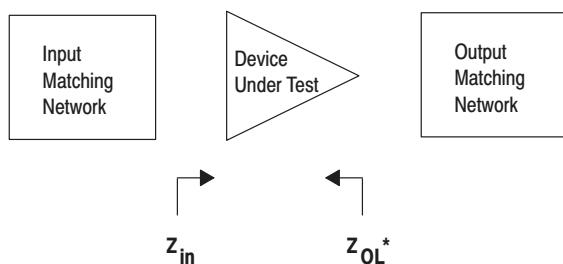
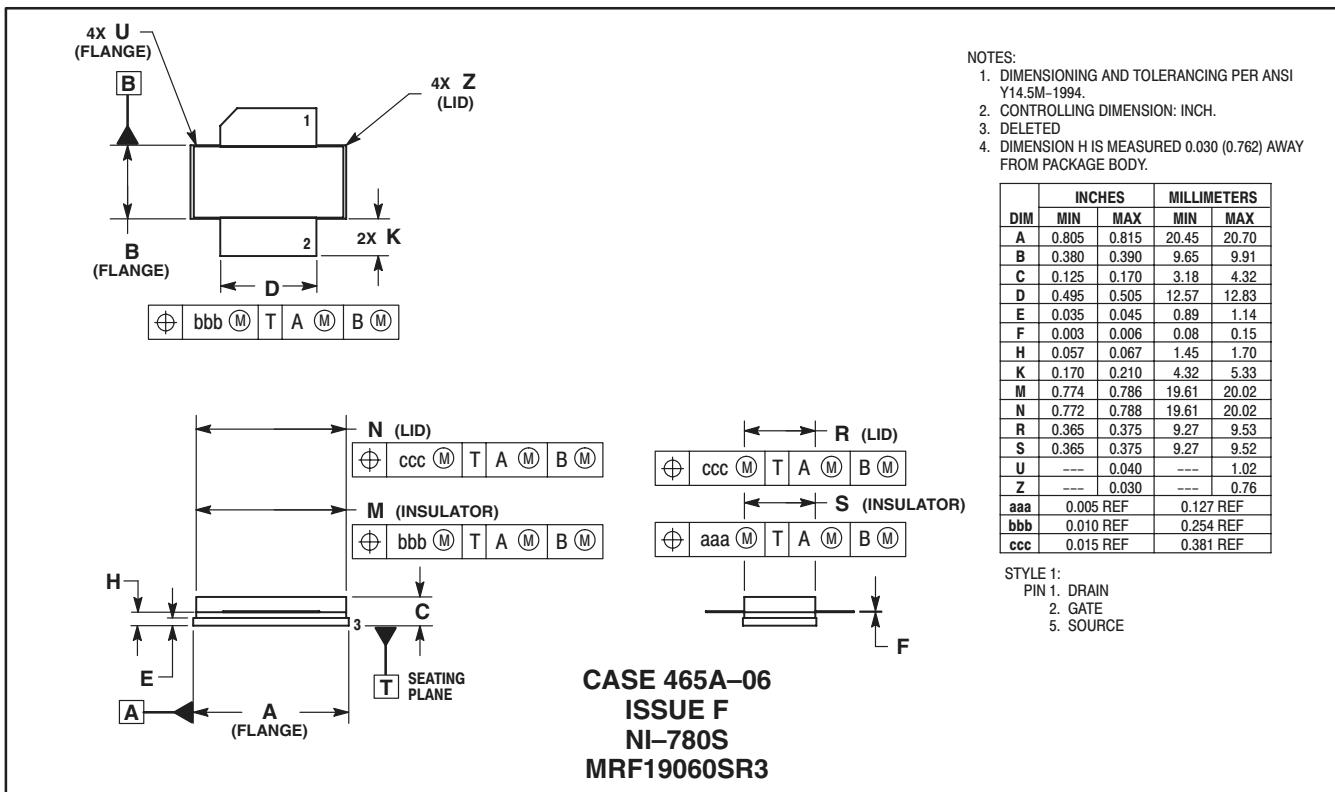
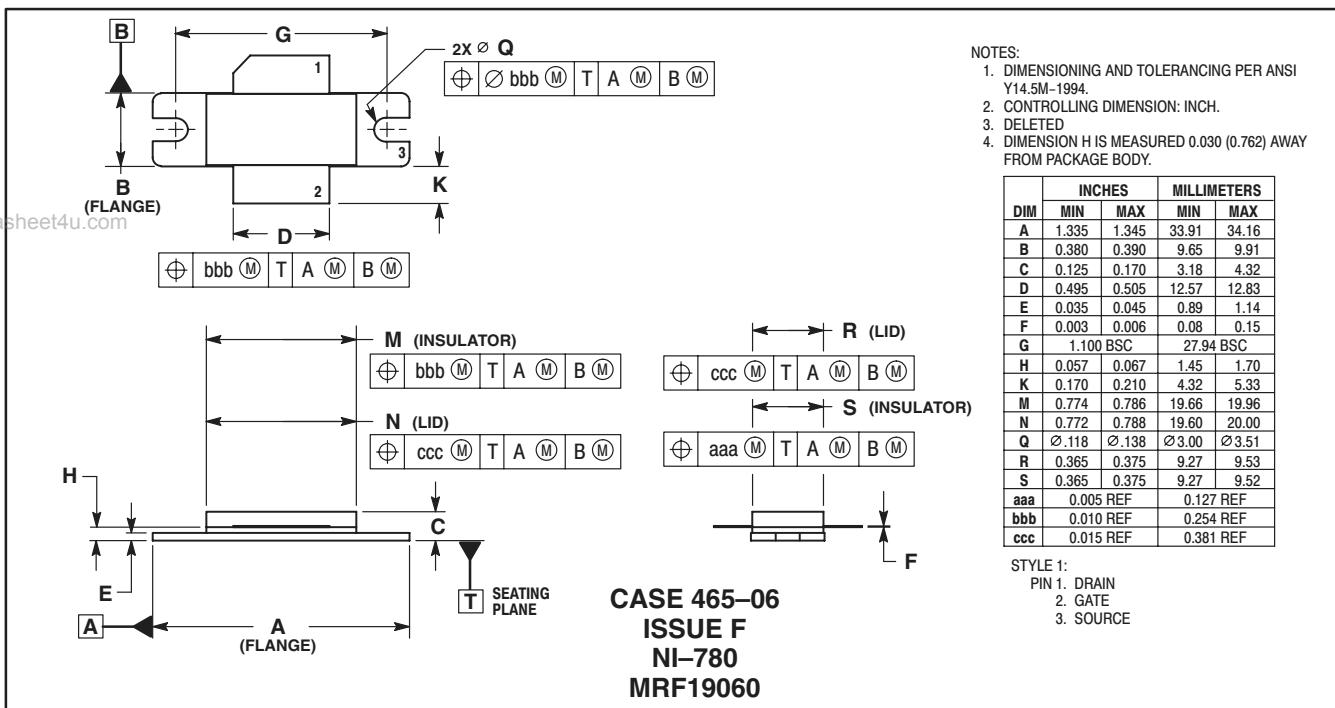


Figure 9. Series Equivalent Input and Output Impedance

PACKAGE DIMENSIONS

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